XDPE132G5D Digital Multi-phase Controller

16-phase Dual Loop PWM Voltage Regulator

Quality Requirement Category: Industrial

Features

- 16-phase single or up to 8+8 dual loop configurable PWM Controller
- I2C and PMBus Rev 1.3 with AVSBus for output voltage control and telemetry
- 0.625 mV VID step via PMBUS VOUT_COMMAND
- AMD SVI2 Rev 1.09 compliant with Peak Current Control (PCC) and IOUT telemetry support up to 1023 A
- nVIDIA PWMVID compliant
- Phase Fault Protection and Flag with auto-compensation
- Digitally Progammable Load Line – No external components
- Min/Max Telemetry registers and real-time monitoring via PMBus and AVSBus (I_{OUT}, V_{OUT}, Temp)
- Phase current sense gain and offset calibration
- Cycle-by-cycle phase current limit
- Analog “IMON” for output current reporting
- Two IOUT_WARN pins to flag an output OC condition on both loops
- Input Over Power flag
- Catastophic Fault Output (CAT_FLT) pin
- Dual Enable Pins
- Adaptive Transient Algorithm (ATA) minimizes output bulk capacitors and system cost
- Efficiency Shaping Features using Dynamic Phase Control and Diode Emulation
- Protections: OVP, UVP, OC Warn, OCP, OT Warn, OTP, cycle-by-cycle per phase current limit
- Multiple Time Programming (MTP) with up to 25 writes for USER Section
- Compatible with 3.3 V tri-state Drivers
- 200 kHz to 2 MHz switching frequency per phase
- +3.3 V supply voltage; -40 °C to 120 °C Ambient
- Pb-Free, Halogen Free, RoHS, 7x7 mm, 56-pin, 0.4 mm pitch QFN

Applications

- AMD SVI2 GPU and CPU Processors
- nVIDIA GPU Processors
- High Performance ASIC Processors with AVSBus.
- High performance Ethernet Switching and Routing ASSPs

Description

The XDPE132G5D is a digital multi-phase buck controller that can be configured in either a single loop or dual loop mode with a feature set optimized to support high performance processors that require AVSBus, AMD SVI2, or nVIDIA PWMVID. It can support up to 16 phases and allows flexible phase assignment between the two loops. The controller allows system voltage set point programming and margining through PMBus or dynamic voltage

scaling through AVSBus. The output voltage set point can also be controlled through the SVI2 bus or the nVIDIA PWM_VID.

The XDPE132G5D includes Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. Dynamic Phase Control adds/drops phases based upon load current. The XDPE132G5D can be configured to enter 1- or 2-phase operation and active diode emulation mode automatically or by command (through PMBus, AVSBus, or SVI2 commands).

The XDPE132G5D offers digitally programmable load line thereby eliminating the need for any external load line setting components. The controller is designed to work with internal current sense OptiMOS™ Power Stages and provides accurate input and output current reporting.

A unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear control algorithms provides excellent transient response with reduced output capacitance. The controller also supports programmable cycle-by-cycle per phase current limit for superior dynamic current limiting.

The I2C/PMBus interface can communicate with up to 127 XDPE132G5D-based controllers. Device configuration and fault parameters are easily defined using the OpenPower GUI and stored in on-chip memory.

The XDPE132G5D's extensive fault protection includes output OV, UV and OC protection, with 2 OT protection inputs with an OT Warning VRHOT signal output, and two output over-current warning flags.

Note: "Infineon strongly recommends pairing Infineon's OptiMOS™ Power Stages with our Digital XDP™ family of controllers to ensure correct interoperability. Interoperability when pairing with other vendor power stages/ discrete power components cannot be guaranteed by Infineon and requires thorough evaluation and characterization by the power stage/ discrete power component vendor."

Table of Contents

1 Ordering Information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
XDPE132G5D	QFN 7 mm x 7 mm	Tape and Reel	3000	XDPE132G5D-Gxxx[1]
XDPE132G5D	QFN 7 mm x 7 mm	Tape and Reel	3000	XDPE132G5D-G000

Note: 1) Customer Specific Configuration File, where xxx = Customer Configuration File (Codes assigned by IFX Marketing).

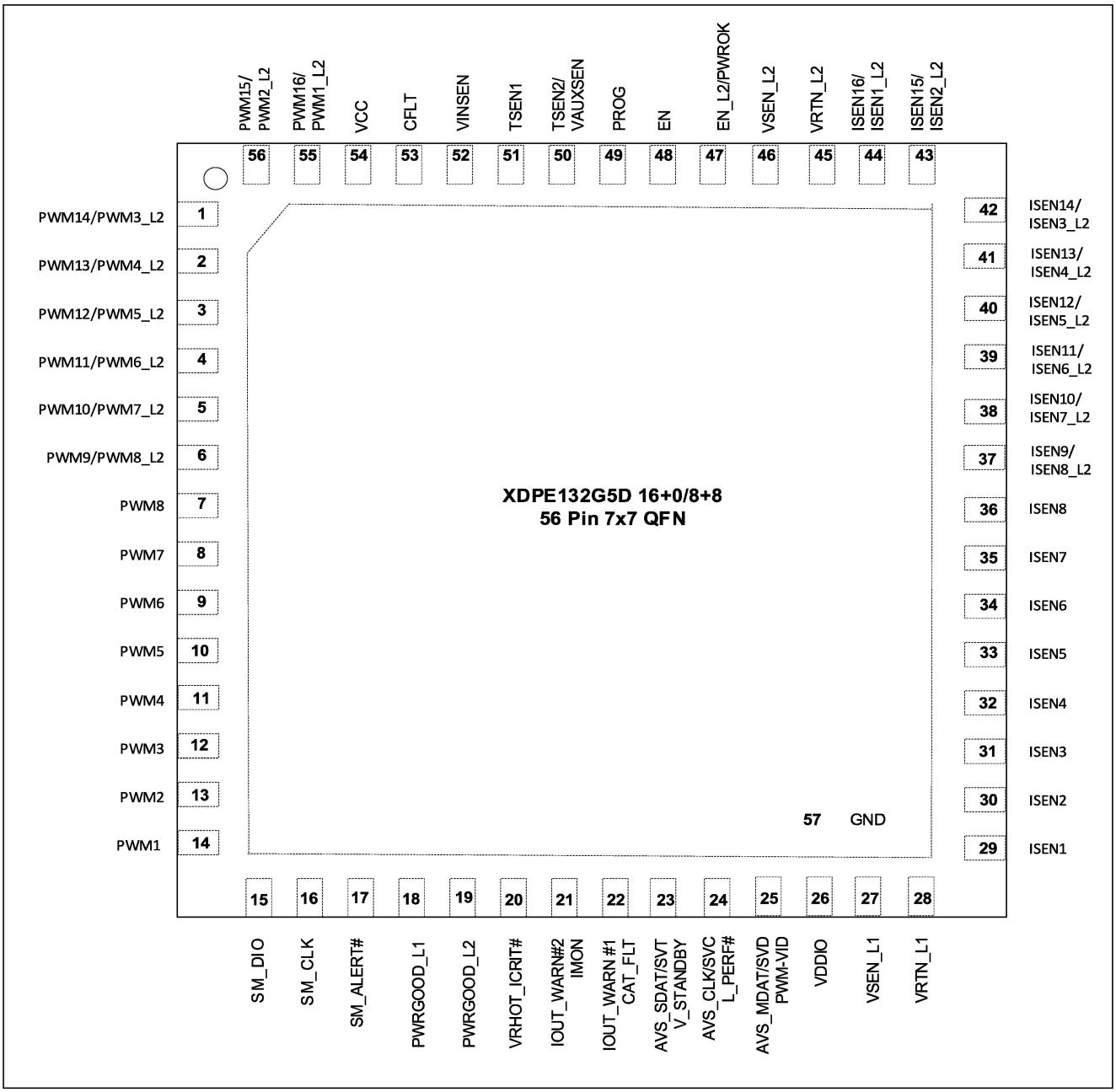

Figure 1 Package Top View

2 Functional Block Diagram

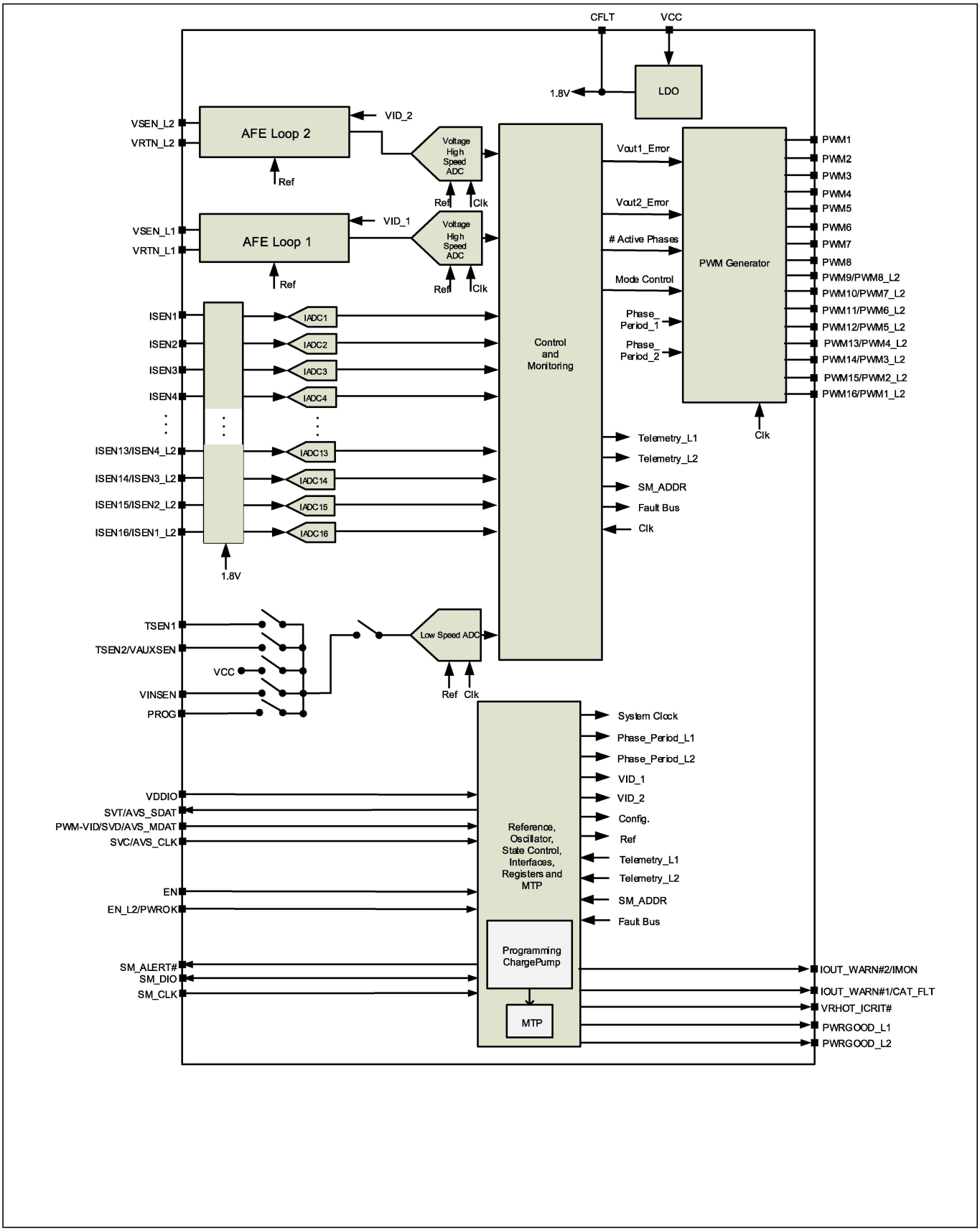

Figure 2 Block Diagram

3 Typical Application Diagram

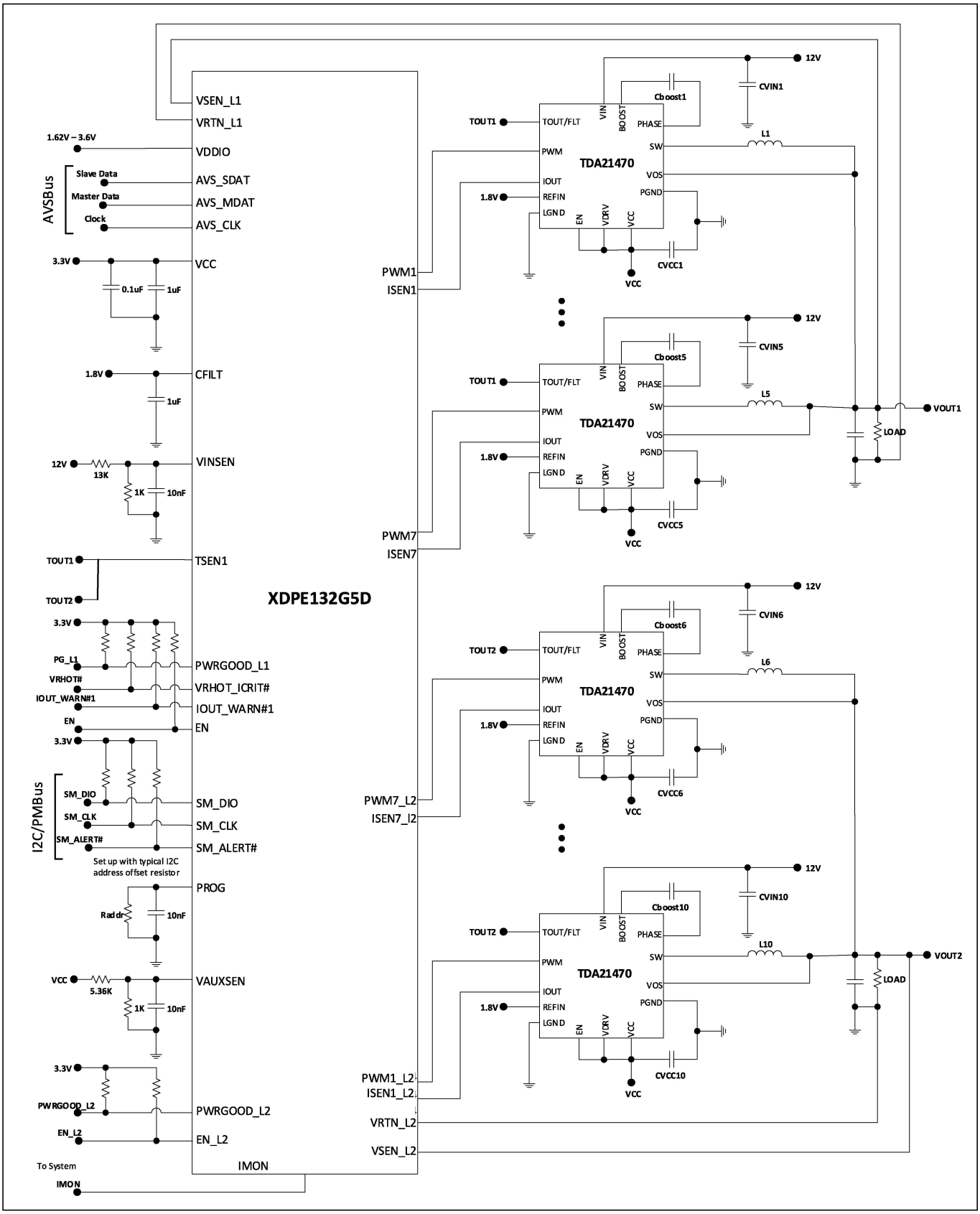

Figure 3 Dual Loop VR using XDPE132G5D Controller and TDA21470 Power Stage in 7+7 Phase Configuration

4 Pin Descriptions

Table 1 Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	PWM14/ PWM3_L2	D [O]	**Loop1 PWM14/Loop2 PWM3 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 14 or Phase 3 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
2	PWM13/ PWM4_L2	D [O]	**Loop1 PWM13/Loop2 PWM4 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 13 or Phase 4 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
3	PWM12/ PWM5_L2	D [O]	**Loop1 PWM12/Loop2 PWM5 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 12 or Phase 5 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
4	PWM11/ PWM6_L2	D [O]	**Loop1 PWM11/Loop2 PWM6 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 11 or Phase 6 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
5	PWM10/ PWM7_L2	D [O]	**Loop1 PWM10/Loop2 PWM7 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 10 or Phase 7 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
6	PWM9/ PWM8_L2	D [O]	**Loop1 PWM9/Loop2 PWM8 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 9 or Phase 8 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
7	PWM8	D [O]	**Loop1 PWM8.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 8. The power-up state is high-impedance until ENABLE goes active. Float if not used.
8	PWM7	D [O]	**Loop1 PWM7 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 7. The power-up state is high-impedance until ENABLE goes active. Float if not used.
9	PWM6	D [O]	**Loop1 PWM6 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 6. The power-up state is high-impedance until ENABLE goes active. Float if not used.
10	PWM5	D [O]	**Loop1 PWM5 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 5. The power-up state is high-impedance until ENABLE goes active. Float if not used.
11	PWM4	D [O]	**Loop1 PWM4 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 4. The power-up state is high-impedance until ENABLE goes active. Float if not used.
12	PWM3	D [O]	**Loop1 PWM3 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 3. The power-up state is high-impedance until ENABLE goes active. Float if not used.
13	PWM2	D [O]	**Loop1 PWM2 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 2. The power-up state is high-

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
			impedance until ENABLE goes active. Float if not used.
14	PWM1	D [O]	**Loop1 PWM1 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 1. The power-up state is high-impedance until ENABLE goes active.
15	SM_DIO	D [IO]	**Serial Data Line I/O.** I2C/SMBus/PMBus bi-directional serial data line. Requires a pull-up resistor.
16	SM_CLK	D [I]	**Serial Clock Line Input.** I2C/SMBus/PMBus clock input. The interface is rated to 3.4 MHz. Requires a pull-up resistor.
17	SM_ALERT#	D [O]	**SMBus/PMBus Alert Line.** Open-drain active low alert pin to indicate that the regulator status has changed. Requires a pull-up. Float if not used.
18	PWRGOOD_L1	D [O]	**Voltage Regulator Ready Output (Loop #1**). Open-drain output that asserts high when the VR has completed soft-start to Loop #1 boot voltage. Pull up to an external voltage through a resistor.
19	PWRGOOD_L2	D [O]	**Voltage Regulator Ready Output (Loop #2).** Open-drain output that asserts high when the VR has completed soft-start to Loop #2 boot voltage. Pull up to an external voltage through a resistor.
20	VRHOT_ICRIT#	D [O]	**VRHOT# and ICRIT# Output.** Active low alert pin that can be programmed to assert if temperature exceeds a user-definable threshold or if the output current exceeds a user-definable theshold. Pull up to an external voltage through a resistor.
21	IMON	A [O]	**Current Monitor Output for Loop#1.** This pin outputs an analog voltage corresponding to the average output current of Loop #1.The IMON output can be scaled to accommodate the maximum output current. The IMON output will be 0 V = 0 A to 2.55 V = 1024 A or 512 A based on the set IMON scale factor. The maximum current on this pin is +/-100 µA. No output capacitor on this pin is required, but should be limited to 1 nF maximum if one is used.
	IOUT_WARN#2	D [O]	**Warning Output 2.** Open-drain active low alert pin that can be configured to indicate an; 1) Output Over-current Warning for Loop 1, 2) Output Over-current Warning for Loop 2, 3) Output Over-current Warning for Loop 1 and Loop2, or 4) Loop2 input over-power warning
22	CAT_FLT	D [O]	**Catastrophic Fault Output Pin.** This pin may be used as a Catastrophic Fault CMOS Output Pin that is driven to VCC under output OVP, NVM CRC errors or a TSENx fault input.
	IOUT_WARN#1	D [O]	**Warning Output 1.** Open-drain active low alert pin that can be configured to indicate an; 1) Output Over-current Warning for Loop 1, 2) Output Over-current Warning for Loop 2, 3) Output Over-current Warning for Loop 1 and Loop2, or 4) Loop 1 input over-power warning
23	AVS_SDAT	D [O]	**AVS Slave Data.** Bus line that is driven by an AVSBus Slave (VR Controller) and carries data to the master (ASIC, FPGA, or Processor). Float if not used.
	SVT	D [O]	**SVI Telemetry Output (AMD).** Telemetry and VOTF information output. Float if not used.
	V_STANDBY	D [I]	**nVIDIA PWM standby control input.** Digital control input of nVIDIA standby voltage. High = V _STANDBY
24	AVS_CLK	D [I]	**AVS Bus Clock.** Bus clock that is driven by the master and clocks data for both the AVS_MDAT and AVS_SDAT lines. Float if not used.

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
	SVC	D [I]	**SVI Clock Input (AMD).** Clock input driven by the CPU/GPU Master. Float if not used.
	L_PERF#	D [I]	**nVIDIA low performance indicator.** Digital control input; low indicates one or more 12 V sources are not connected. The VR will operate with only one phase in low performance mode.
25	AVS_MDAT	D [I]	**AVS Master Data.** A serial data bus line that is driven by the AVSBus Master (ASIC, FPGA, or Processor) and carries data to the slave (VR Controller). Float if not used.
	SVD	D [I]	**SVI Data In (AMD).** A serial data bus line over which the CPU/GPU Master issues commands to the slave (VR Controller). Float if not used.
	PWM-VID	D [I]	**PWMVID Input.** VID control input for nVIDIA PWMVID. Connect to ground with 10 kΩ resistor
26	VDDIO	A [I]	**IO Voltage for AVS Bus.** Common voltage for the master and slave I/O circuitry. Float if not used.
27	VSEN_L1	A [I]	**Remote Voltage Sense Input Loop 1.** This pin is connected directly to the VR output voltage of Loop 1 at the load and should be routed differentially with VRTN_L1.
28	VRTN_L1	A [I]	**Remote Voltage Sense Return Input Loop 1.** This pin is connected directly to Loop 1 ground at the load and should be routed differentially with VSEN_L1.
29	ISEN1	A [I]	**Loop 1 Phase 1 Current Sense Input.** Phase 1 sensed current input. Float or connect to CFLT if not used.
30	ISEN2	A [I]	**Loop 1 Phase 2 Current Sense Input.** Phase 2 sensed current input. Float or connect to CFLT if not used.
31	ISEN3	A [I]	**Loop 1 Phase 3 Current Sense Input.** Phase 3 sensed current input. Float or connect to CFLT if not used.
32	ISEN4	A [I]	**Loop 1 Phase 4 Current Sense Input.** Phase 4 sensed current input. Float or connect to CFLT if not used.
33	ISEN5	A [I]	**Loop 1 Phase 5 Current Sense Input.** Phase 5 sensed current input. Float or connect to CFLT if not used.
34	ISEN6	A [I]	**Loop 1 Phase 6 Current Sense Input.** Phase 6 sensed current input. Float or connect to CFLT if not used.
35	ISEN7	A [I]	**Loop 1 Phase 7 Current Sense Input.** Phase 7 sensed current input. Float or connect to CFLT if not used.
36	ISEN8	A [I]	**Loop 1 Phase 8 Current Sense Input.** Phase 8 sensed current input. Float or connect to CFLT if not used.
37	ISEN9/ ISEN8_L2	A [I]	**Loop 1 Phase 9/ Loop 2 Phase 8 Current Sense Input.** Phase 9 or Phase 8 of Loop 2 sensed current input. Float or connect to CFLT if not used.
38	ISEN10/ ISEN7_L2	A [I]	**Loop 1 Phase 10/ Loop 2 Phase 7 Current Sense Input.** Phase 10 or Phase 7 of Loop 2 sensed current input. Float or connect to CFLT if not used.
39	ISEN11/ ISEN6_L2	A [I]	**Loop 1 Phase 11/ Loop 2 Phase 6 Current Sense Input.** Phase 11 or Phase 6 of Loop 2 sensed current input. Float or connect to CFLT if not used.
40	ISEN12/ ISEN5_L2	A [I]	**Loop 1 Phase 12/ Loop 2 Phase 5 Current Sense Input.** Phase 12 or Phase 5 of Loop 2 sensed current input. Float or connect to CFLT if not used.

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
41	ISEN13/ ISEN4_L2	A [I]	**Loop 1 Phase 13/ Loop 2 Phase 4 Current Sense Input.** Phase 13 or Phase 4 of Loop 2 sensed current input. Float or connect to CFLT if not used.
42	ISEN14/ ISEN3_L2	A [I]	**Loop 1 Phase 14/ Loop 2 Phase 3 Current Sense Input.** Phase 14 or Phase 3 of Loop 2 sensed current input. Float or connect to CFLT if not used.
43	ISEN15/ ISEN2_L2	A [I]	**Loop 1 Phase 15/ Loop 2 Phase 2 Current Sense Input.** Phase 15 or Phase 2 of Loop 2 sensed current input. Float or connect to CFLT if not used.
44	ISEN16/ ISEN1_L2	A [I]	**Loop 1 Phase 16/ Loop 2 Phase 1 Current Sense Input.** Phase 16 or Phase 1 of Loop 2 sensed current input. Float or connect to CFLT if not used.
45	VRTN_L2	A [I]	**Remote Voltage Sense Return Input Loop 2.** This pin is connected directly to Loop 2 ground at the load and should be routed differentially with VSEN_L2. Ground is not used.
46	VSEN_L2	A [I]	**Remote Voltage Sense Input Loop 2.** This pin is connected directly to the VR output voltage of Loop 2 at the load and should be routed differentially with VRTN_L2. It is also used to switch in the local voltage into the feedback path during an OV event and as a monitoring point for telemetry reporting of the local voltage. Ground if not used.
47	EN_L2	D [I]	**VR Enable Input (Loop 2).** ENABLE is used to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up inside the controller. When the controller is disabled, the controller de-asserts PWRGOOD_L2 and shuts down the regulator. ENABLE pin cannot be left floating and must be pulled high or low.
	PWROK	D [I]	**Power OK Input (AMD).** An input that when low indicates to return to the Boot voltage and when high indicates to use the SVI2 bus VID for VOUT**.**
48	EN	D [I]	**VR Enable Input** (Loop 1 or loop1 and 2 if EN_L2 is disabled)**.** ENABLE is used to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up inside the controller. When the controller is disabled, the controller de-asserts PWRGOOD_Lx and shuts down the regulator. ENABLE pin cannot be left floating and must be pulled high or low.
49	PROG	A [I]	**Bus Address Offset.** A resistor to ground on this pin sets an offset to the register value I2C/PMBus address if configured to do so. **Configuration Selection.** A resistor to ground on this pin selects one of multiple configurations saved in MTP if configured to do so.
50	VAUXSEN	A [I]	**Auxiliary Voltage Sense Input.** This pin can be used to sense an auxiliary input voltage. It is typically used to monitor the 5V driver voltage and inhibit startup if the driver voltage is not above, or drops below, the programmed voltage thresholds. In this mode the sense point controls operation of both Loop #1 and Loop #2. Ground if not used.
	TSEN2	A [I]	**Temperature Sense Input Loop 2.** The temperature reporting output from an IFX OptiMOS™ Power Stage (TOUT) can be connected to this pin to measure temperature for VRHOT and OTP shutdown for Loop 2. Ground if not used.
51	TSEN1	A [I]	**Temperature Sense Input Loop 1.** The temperature reporting output from an IFX OptiMOS™ Power Stage (TOUT) can be connected to this pin to measure temperature for VRHOT and OTP shutdown loor Loop 1. If TSEN2 is disabled, connect TOUT from Loop 1 and Loop 2 to this input.
52	VINSEN	A [I]	**Voltage Sense Input.** This is used to detect and measure a valid input

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
			supply voltage (typically 4.5 V-13.2 V) to the VR.
53	CFLT	A [O]	**1.8V Decoupling.** A 1 µF capacitor on this pin provides decoupling for the internal 1.8 V supply.
54	VCC	A [P]	**Input Supply Voltage.** 3.3 V supply to power the device.
55	PWM16/ PWM1_L2	D [O]	**Loop1 PWM16/Loop2 PWM1 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 16 or Phase 1 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
56	PWM15/ PWM2_L2	D [O]	**Loop1 PWM15/Loop2 PWM2 Output.** PWM signal pin which is connected to the input of an external MOSFET gate driver for Phase 15 or Phase 2 of Loop 2. The power-up state is high-impedance until ENABLE goes active. Float if not used.
57	GND	A [P]	**Ground.** Ground reference for the IC. The large metal pad on the bottom must be connected to Ground.

A-Analog; D – Digital; [I] – Input; [O] – Output; [P] - Power

5 Absolute Maximum Ratings

Subjecting the controller to stresses above those listed in Table 2 may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational section of this specification. Exposure to the absolute maximum ratings for extended periods may adversely affect the operation and reliability of the device.

Table 2 Absolute Maximum Ratings

Supply Voltage (VCC)	GND-0.3 V to 4.0 V
CFLT, VINSEN	GND-0.2 V to 2.2 V
ISENx, VSENx, VRTNx, VDDIO	GND-0.3 V to VCC+0.3 V
AVS_MDAT/SVD, AVS_SDAT/SVT, AVS_CLK/SVC, PWRGOOD_Lx, VRHOT_ICRIT#, IOUT_WARN#x, EN, EN_L2/PWROK, TSEN1, TSEN2/VAUXSEN, PROG, PWMx	GND-0.3 V to VCC
SM_DIO, SM_CLK, SM_ALERT#	GND-0.3 V to 5.5 V
Maximum Operating Junction Temperature	-40 °C & 125 °C
Maximum Storage Temperature Range	-65 °C & 150 °C
Maximum Lead Temperature (Soldering 10s)	300 °C

Attention: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

6 Electrical Characteristics

Table 3 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{cc}		2.90	3.3	3.6	V
Ambient Temperature[1]	T_a		-40	25	120	°C

Note: [1] assumes the PCB temperature at the XDPE132G5D is no higher than 124 °C

Table 4 Temperature Information

Symbol	Description	7mm x 7mm QFN
$\theta_{JA(0)}$[1]	Junction-to-ambient thermal resistance at 0 lfm	27.1 °C/W
$\theta_{JA(200)}$[1]	Junction-to-ambient thermal resistance at 200 lfm	23.1 °C/W
$\theta_{JA(500)}$[1]	Junction-to-ambient thermal resistance at 500 lfm	21.7 °C/W
θ_{JC}	Junction-to-case thermal resistance	2.8 °C/W

Note: [1] θ_{JA} is measured with the component mounted on a highly effective thermal conductivity test board in free air.

Unless otherwise specified, the Electrical Characteristics table lists the spread of values that can occur within the recommended operating conditions. Typical values represent the median values, which are related to 25 °C.

Table 5 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply	**VCC, CFLT, GND**					
Supply Voltage	V_{cc}		2.90	3.3	3.6	V
Supply Current	I_{vcc}	no PWMx activity	-	67	-	mA
3.3V UVLO Turn-on Threshold			-	2.80	2.9	V
3.3V UVLO Turn-off Threshold	Vcc_{uvlo}		2.6	2.65	-	V
3.3V Rise Time[1]	T_{rise}		1			msec
1.8V Supply	CFLT		-	1.8	-	
1.8V Supply Current[1]	I_{CFLT}		20	50	80	mA
Input voltage Sense Input	**VINSEN**					
Input Impedance			-	1	-	MΩ
Input Range[1]			0	0.857	1.1	V
UVLO Turn-on Programmable Range[1]		With 14:1 divider	-	0 –15.25	-	V
UVLO Turn-off Programmable Range[1]	Vin_{uvlo}		-	0 – 15.25	-	V
OVP Threshold (if enabled) [1]	Vin_{ov}		-	0 – 15.25	-	V
UVLO Turn-on Programmable Range[1]		With 22:1 divider	-	0 –24.25	-	V

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
UVLO Turn-off Programmable Range[1]	Vin_{uvlo}		-	0 –24.25	-	V
OVP Threshold (if enabled) [1]	Vin_{ov}		-	0 –24.25	-	V
Auxiliary Voltage Sense Input	**VAUXSEN**					
Input Impedance			-	1	-	MΩ
Input Range[1]	Vaux	Vaux = 0-7 V with external 6.4:1 divider	0	0.781	1.1	V
Turn-on Threshold[1]		VAUX Voltage	-	3.3-7.0	-	V
UVLO Threshold[1]		With external 6.4:1 divider	-	3.3-7.0	-	V
Reference Voltage and DAC						
DAC Resolution	DAC		-	0.625	-	mV
Vboot and PMBus/AVSBus Voltage Range[1]	V_{OUT}		-	0.20 – 2.55	-	V
Voltage Accuracy[1] AVS/PMBus/nVIDIA PWM	V_{OUT}	0 °C to 85 °C Temp Range				
		DAC = 2.005 V–2.55 V	-1.1	-	1.1	%VID
		DAC = 1.805 V–2.00 V	-0.75		0.75	%VID
		DAC = 1.600 V-1.800 V	-0.6		0.6	%VID
		DAC= 1.0 V–1.595 V	-0.5	-	0.5	%VID
		DAC = 0.8 V–0.995 V	-5	-	5	mV
		DAC= 0.25 V–0.795 V	-8	-	8	mV
		-40 °C to 0 °C, 85 °C to 125 °C Temp Range				
		DAC = 2.005 V–2.55 V	-1.65	-	1.65	%VID
		DAC = 1.655 V–2.0 V	-1.0	-	1.0	%VID
		DAC = 1.0 V–1.65 V	-0.75	-	0.75	%VID
		DAC = 0.8 V – 0.995 V	-7.5	-	7.5	mV
		DAC = 0.25 V – 0.795 V	-12	-	12	mV
Voltage Accuracy[1] AMD	V_{OUT}	0 °C to 85 °C Temp Range				
		DAC = 1.20625 V–1.55 V	-0.75	-	0.75	%VID
		DAC= 0.8 V–1.2 V	-0.5	-	0.5	%VID
		DAC = 0.55 V–0.79375 V	-4	-	4	mV
		DAC= 0.25 V–0.54375 V	-8	-	8	mV
		-40 °C to 0 °C, 85 °C to 125 °C Temp Range				
		DAC = 1.20625 V–1.55 V	-1	-	1	%VID
		DAC = 0.8 V–1.2 V	-0.75	-	0.75	%VID
		DAC = 0.55 V–0.79375 V	-6	-	6	mV
		DAC = 0.25 V– 0.54375 V	-12	-	12	mV
DAC Slew Rate[1]		0.25 mV/µs resolution		0.25 – 127.75		mV/µs
Oscillator and PWM Generator						
Internal Oscillator			-	48	-	MHz

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Accuracy		0 °C to 85 °C Temp Range	-3	-	3	%
		-40 °C - 0 °C, 85 °C - 125 °C Temp Range	-5	-	5	%
PWM Frequency Range[1]			-	200 to 2000	-	kHz
PWM Resolution[1]			-	163	-	ps
Temperature Sense Input - TOUT	**TSENx**					
Input Voltage		For TSENx = 0 to 1.8 V	-	8	-	mV/°C
Offset Voltage			-	0.6	-	V
Digital Inputs – Low Vth Type 1	**EN, EN_L2 , SM_CLK, SM_DIO**					
Input High Voltage		EN, EN_L2	0.725	-	-	V
Input Low Voltage		EN, EN_L2	-	-	0.35	V
Input High Voltage		SM_CLK, SM_DIO	1.1	-	-	V
Input Low Voltage		SM_CLK, SM_DIO	-	-	0.6	V
Input Leakage		Vpad = 0 to 3.6 V	-	-	±5	µA
Digital Inputs – LVTTL	**EN, EN_L2, SM_CLK, SM_DIO**					
Input High Voltage			2.1	-	-	V
Input Low Voltage			-	-	0.8	V
Input Leakage		Vpad = 0 to 3.6 V	-	-	±1	µA
Digital Inputs – VDDIO	**AVS_MDAT/SVD, AVS_CLK/SVC**					
Period			40	-	200	ns
Input High Voltage		User programmable, AVS application	-	0.55, 0.65, 0.80, 0.90	-	V
		AMD SVI2		0.78		V
Input Low Voltage		User programmable, AVS application	-	0.45, 0.55, 0.70, 0.80	-	V
		AMD SVI2		0.63		V
Input Leakage Current		Vpad = 0 to 3.6 V	-	-	±5	µA
Remote Voltage Sense Inputs	**VSEN_Lx, VRTN_Lx**					
VSEN Input Current		VSEN = 0.5 V to 2.55 V	-	-25 to +100	-	µA
VRTN Input Current			-	-50	-	µA
Differential Input Voltage Range[1]		VRTN = ±100 mV	-	0 to 2.55	-	V
VRTN Input CM Voltage[1]			-	-100 to 100	-	mV
Phase Current Sense Inputs	**ISENx**					
Voltage Range[1]			-	CFLT-0.15 to CFLT+0.6	-	V
High Current Range Input		ISNSx to CFLT	10	15	20	KΩ

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resistance						
High Current Range Input Attenuation Factor			65.5	66.25	67.0	%
Output Current Monitor	**IMON**					
Voltage Range			-	0 to 2.55	-	V
Voltage Accuracy[1]		0 °C to 85 °C Temp Range				
		IMON = 1.1 V–2.56 V	-0.8	-	0.8	%
		IMON = 0.8 V–1.095 V	-8.5	-	8.5	mV
		IMON = 0.5 V–0.795 V	-10	-	10	mV
		IMON = 0.005 V–0.495 V	-12.5	-	12.5	mV
		-40 °C - 0 °C, 85°C - 125 °C Temp Range				
		IMON = 1.0 V–2.56 V	-1.75	-	1.75	%
		IMON = 0.5 V–0.995 V	-20	-	20	mV
		IMON = 0.005 V– 0.495 V	-25	-	25	mV
Resolution			-	5	-	mV
Output Impedance			-	210	-	Ω
Open-drain Outputs – 4mA Drive	**PWRGOOD_Lx, SM_DIO[1], SM_ALERT#**					
Output Low Voltage		4 mA	-	-	0.3	V
Output Leakage		Vpad = 0 to 3.6 V	-	-	±5	µA
Open-drain Outputs – 20mA Drive	**VRHOT_ICRIT#, IOUT_ WARN#x**					
Output Low Voltage		I = 20 mA	-	-	0.26	V
On Resistance		I = 20 mA	4	9	13	Ω
Output Leakage		Vpad = 0 to 3.6 V	-	-	±5	µA
CMOS Output - VDDIO	**AVS_SDAT/SVT**					
Period[1]			40	-	200	ns
Output Low Voltage		Iol = +20 mA	-	20% VDDIO	-	V
Output High Voltage		Ioh= -10 mA, VDDIO ≤ 1.2 V	-	80% VDDIO	-	V
Output Leakage		Vpad = 0 to 3.6 V	-	-	±5	µA
CMOS Output - VCC	**CAT_FLT**					
Output Low Voltage		Iol = +4mA	-	-	0.4	V
Output High Voltage		Ioh= -4 mA	VCC-0.4	-	-	V
PWM Outputs	**PWMx**					
Output Low Voltage		I = +4 mA	-	-	0.4	V
Output High Voltage		I = -4 mA	2.9	-	-	V
Tri-State Leakage		Vpad = 0 to Vcc	-	-	±2	µA

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AMD SVI2 BUS	**SVC**					
Tperiod (SVC Period)[1]			47.6		10,000	ns
SVI2 SVC Frequency[1]			0.1	20.0	21.0	MHz
Address Offset/ Config Selection	**PROG**					
Output Current		Vpad = 0 to 1.2 V	97	100	103	µA
I2C/PMBus & Telemetry						
Bus Speed[1]		Normal	-	100	-	kHz
		Fast	-	400	-	kHz
		Maximum	-	3400	-	kHz
Iout, Iin, Pout, and Pin Update Rate[1]			-	12	-	MHz
Iout, Vout, Temp, and Vin Filter Rate[1]		Selectable (Selected Frequency applies to all parameters)		2.106 to 269.5		Hz
Temperature Filter Rate[1]				4.6		kHz
Iin, Pin and Pout Filter Rate[1]				2		kHz
Iout, Iin, Pout, and Pin Update Rate[1]			-	12	-	MHz
Vout Update Rate[1]			-	48	-	MHz
Vin, Vaux and Temperature Update Rate[1]			-	100	-	kHz
Vin Range Reporting[1]		With 14:1 divider	-	0 to 16.8	-	V
Vin Accuracy Reporting		With 1% resistors	-3	-	+3	%
Vin Resolution Reporting[1]			-	31.25	-	mV
Vout Range Reporting[1]			-	-	2.55	V
Vout Accuracy Reporting[1]		No load-line		±0.5		%
Vout Resolution Reporting[1]			-	2	-	mV
Iout Per Phase Range Reporting[1]	Low	1 A Resolution	-	-20 to +80	-	A
Iout Per Phase Range Reporting[1]	High	1.5 A Resolution	-	-30 to +120	-	A
Iout Accuracy Reporting[1]		Maximum load, all phases active (based on R_{DSon} current sense and # active phases)	-	±3	-	%
Loop1 Iout Resolution Reporting[1]		Iout < 255.75 A 256 < Iout < 511.5 A Iout > 512 A	-	0.25 0.5 1	-	A
Loop2 Iout Resolution Reporting[1]		Iout < 255.75 A Iout > 256 A	-	0.25 0.5	-	A
Loop1 Iin Resolution Reporting[1]			-	62.5	-	mA

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Loop2 Iin Resolution Reporting[1]			-	31.25	-	mA
P_in Resolution Reporting-PMBUS[1]			-	0.5	-	W
P_out Resolution Reporting-PMBUS[1]			-	0.5	-	W
Temperature Range Reporting[1]			-256	-	255	°C
Temperature Accuracy Reporting[1]		With TOUT signal	-5	-	5	°C
Temperature Resolution Reporting[1]			-	1	-	°C
AVSBus & Telemetry						
Bus Speed[1]				5 to 25		MHz
Iout Update Rate[1]			-	12	-	MHz
Iout Filter Rate[1]		Selectable	-	2.5, 5, 7.5, 60	-	kHz
Temperature Update Rate[1]			-	100	-	kHz
Temperature Filter Rate[1]			-	4.6	-	kHz
Fault Protections						
Fixed OVP Threshold		Selectable	-	1.2, 1.275, 1.35, 2.5	-	V
OVP Operating Threshold[1] (programmable)		Relative to VID	-	50 - 400	-	mV
OVP/UVP Filter Delay[1]			-	160	-	ns
Output UVP Threshold[1] (programmable)		Relative to VID	-	50 - 400	-	mV
Fast OCP Range[1]			-	4 – 1023	-	A
Fast OCP Filter Bandwidth[1]				LL_BW		kHz
VRHOT# range[1]				64 to 255		°C
OTP range[1]				64 to 255		°C
IOUT_WARN#x delay[1]	Delay from summed inductor current exceeding threshold				1	µs
Dynamic Phase Control						
Current Filter Bandwidth[1]		For Phase Add		60		kHz
Current Filter Bandwidth[1]		For Phase drop	-	7.5	-	kHz
Timing Information (See Figure 8)						
Automatic Configuration from MTP[1]	t_3-t_2	3.3 V ready to end of trim configuration	-	-	1	ms
Automatic Trim Time[1]	T_4-t_3		-	-	4	ms
Configure USER Registers[1]	T_5-t_4				1	ms

Note: *[1] Verified and approved by design community.*

7 General Description

The XDPE132G5D is a flexible, dual loop, digital, multiphase PWM buck controller optimized to convert a 12 V or 20 V input supply to a voltage level required by high performance microprocessors and DDR memory. It is easily configurable for 1 to 16 phases of operation on Loop 1 and 0 to 8 phase operation on Loop 2 provided that the total number of phases is limited to 16. The unique partitioning of analog and digital circuits within the XDPE132G5D provides the user with easy configuration capability while maintaining the required accuracy and performance. Access to on-chip Multiple Time Programming memory (MTP) to store the XDPE132G5D configuration parameters enables power supply designers to optimize their designs without changing external components.

7.1 Operating Modes

The XDPE132G5D can be used for AVSBus Processor designs, AMD SVI2 CPU and GPU designs, nVIDIA PWM-VID designs, DDR Memory, and stand-alone voltage rails without significant changes to the Bill of Materials (BOM). The required mode is selected in MTP and the pin-out, output voltage, and other relevant functions are automatically configured. This greatly reduces time-to-market and eliminates the need to manage and inventory different PWM controllers.

7.2 Digital Controller and PWM

A linear Proportional-Integral-Derivative (PID) digital controller provides the loop compensation for system regulation. The digitized error voltage from the high-speed voltage error ADC is processed by the digital compensator. The digital PWM generator uses the outputs of the PID and the phase current balance control signals to determine the pulse width for each phase on each loop. The PWM generator has enough resolution to ensure that there are no limit cycles. The compensator coefficients are user-configurable to optimize the system response. The compensation algorithm uses a PID with two additional programmable poles. This provides the digital equivalent of a Type III analog compensator.

7.3 Adaptive Transient Algorithm (ATA)

Dynamic load step-up and load step-down transients require fast system response to maintain the output voltage within specification limits. This is achieved by a unique adaptive non-linear digital transient control loop based on a proprietary algorithm.

7.4 Multiple Time Programming Memory

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by Cyclic Redundancy Code (CRC) checking on each power up. The controller will not start up in the event of a CRC error.

The XDPE132G5D offers up to 25 writes to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. In addition to this, the XDPE132G5D also allows loading of multiple user configuration files (up to 16, based on the resistor on-board at the PROG pin. See Table 39) and allows loading of a specific configuration file corresponding to a specific application automatically (this is especially valuable in mother-boards with multiple XDPE132G5D controllers).

7.5 Internal Oscillator

The XDPE132G5D has a single 48 MHz internal oscillator that generates all the internal system clock frequencies required for proper device function. The oscillator frequency is factory-trimmed for precision, and has extremely low jitter (Figure 4) even in light-load mode (Figure 5). The single internal oscillator is used to set the same switching frequency on each loop.

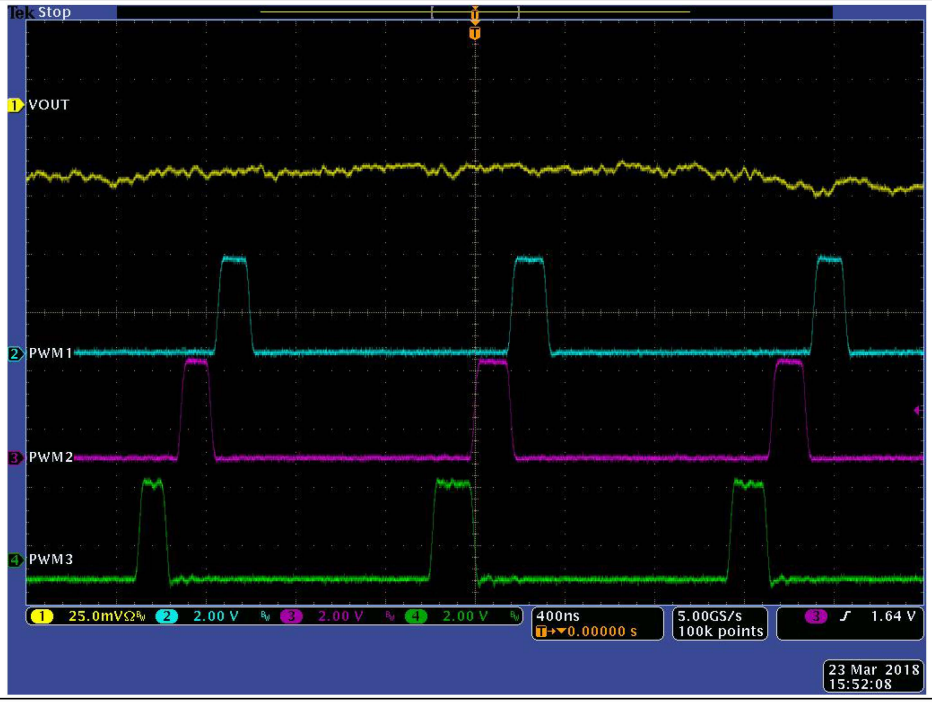

Figure 4 Persistence plot of a 5Φ, 100 A system

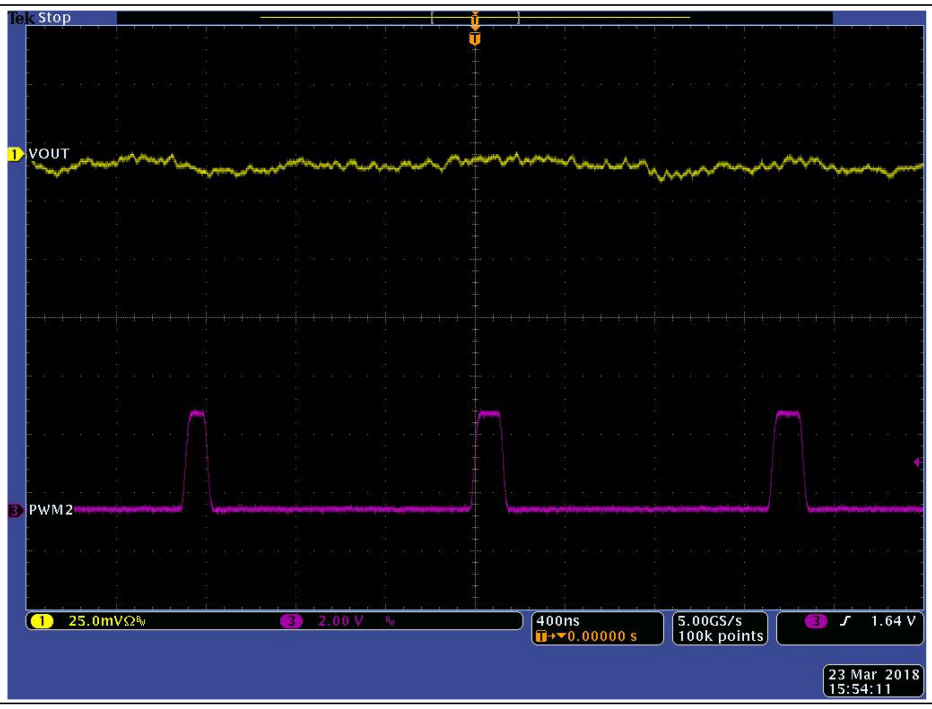

Figure 5 Persistence plot in 1Φ, No Load

7.6 High-precision Voltage Reference

The internal high-precision voltage reference supplies the required reference voltages to the VID DACs, ADCs and other analog circuits. This factory-trimmed reference is guaranteed over temperature and manufacturing variations.

7.7 Output Voltage Sense

An error voltage is generated from the difference between the target voltage, defined by the VID and the differentially sensed output voltage (remote sense). For each loop, the error voltage is digitized by a high-speed, high-precision ADC. An anti-alias filter provides the necessary high frequency noise rejection. The gain and offset of the voltage sense circuitry for each loop is factory-trimmed to deliver the required accuracy.

7.8 Output Current Sense

The XDPE132G5D supports R_{DS}on current sensing OptiMOS™ Power Stages. In case of R_{DS}on based current sensing, the controller is designed to handle a signal with fixed gain of 5 mV/A. No external component is required for thermal compensation as it is implemented inside the R_{DS}on sensing OptiMOS™ Power Stage, thus reducing the component count.

The controller is designed to handle phase currents from -20 A to 80 A with configuration option for extended high current range of -30 A to +120 A.

7.9 MOSFET Driver and Power Stage Compatibility

The output PWM signals of the XDPE132G5D are designed for compatibility with industry standard +3.3 V Tri-State MOSFET drivers.

7.10 I2C and PMBus Interface

An I2C or PMBus interface is used to communicate with the XDPE132G5D. This two-wire serial interface consists of clock and data signals, and operates as fast as 3.4 MHz. The bus provides read & write access to the internal registers for configuration, and for monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, an exclusive address for the XDPE132G5D is programmed into MTP.

To protect customer configuration and information, the I2C interface can be configured for either limited access or locked with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers.

The XDPE132G5D supports the Packet Error Checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents. Refer to the PMBus Command Codes in Table 44 for more information.

7.11 IFX OpenPower GUI

The OPENPOWER GUI provides the designer with a comprehensive design environment that includes interactive tools to calculate VR efficiency and DC error budget, design thermal compensation & feedback loop networks, generate system loop response (Bode plots) and output impedance plots. The GUI environment is a key utility for design optimization, debug, and validation of designs that saves the designer significant time and allowing faster time-to-market (TTM).

The OPENPOWER GUI allows real-time design optimization and monitoring of key parameters such as output current and power, input current and power, phase currents, temperature, and faults.

The OPENPOWER GUI also allows access to the system configuration settings for switching frequency, soft start rate, output voltage setting, power savings settings, loop compensation, transient control system parameters, input under-voltage, output over-voltage, output under-voltage, output over-current and over-temperature.

7.12 Programming

Once a design is complete, the OPENPOWER GUI produces a complete configuration file.

The configuration file can be re-coded into an I2C/PMBus master (e.g. a Test System) and loaded into the XDPE132G5D using the bus protocols described on Page 78. The XDPE132G5D has a special in-circuit programming mode that allows the MTP to be loaded at board test in mass production without powering on the entire board.

7.13 Real-time Monitoring

The XDPE132G5D can be accessed through the use of PMBus Command codes (described in Table 44), to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power, and temperature. Additionally, output voltage, output current, and temperature can be accessed through AVSBus commands.

In addition, the IMON pin provides an analog output voltage corresponding to the total average output current according to Figure 6. This internally generated signal provides the user with additional flexibility in making decisions based on the reported output current. Care needs to be taken to ensure that this pin is not loaded, as the source capability of this pin is limited to 100 µA. An output capacitor on this pin is not required but if a capacitor is used, its value must be limited to a maximum of 1 nF.

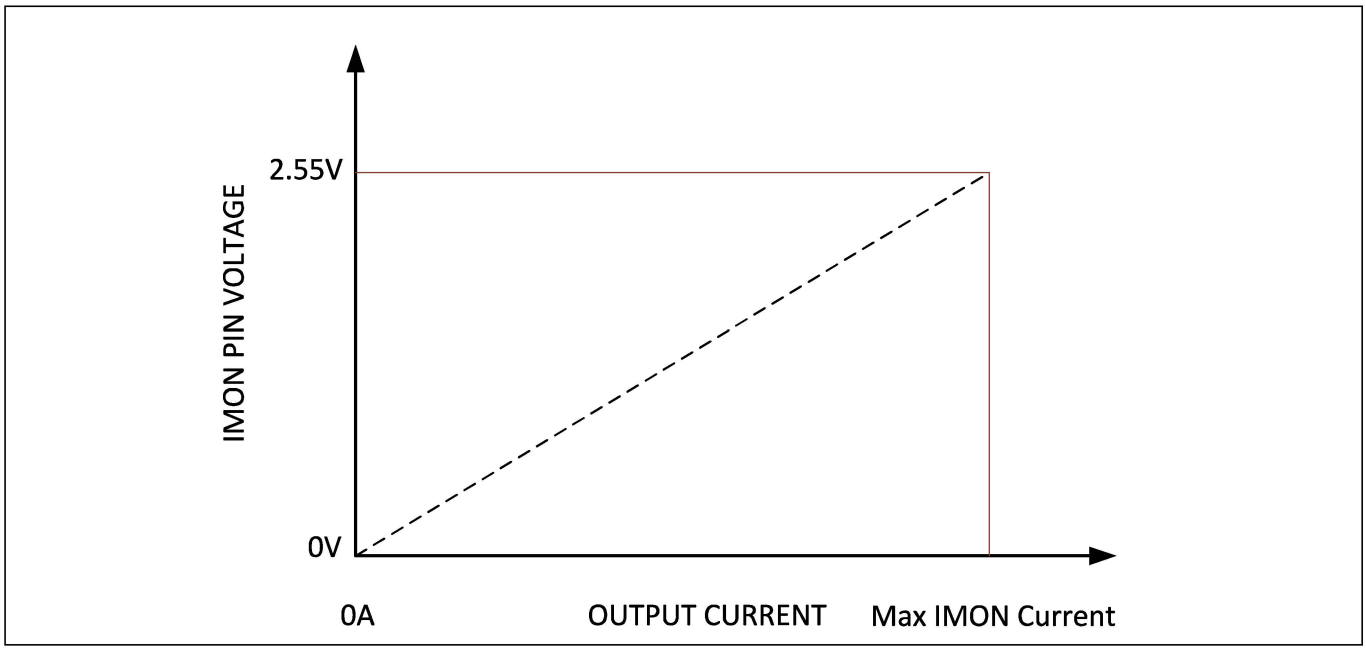

Figure 6 IMON Voltage (V) versus Output Current (A)

Figure 7 Response time IMON Voltage (V) versus Output Current (A)

The Maximum IMON Current can be set based on the maximum current of the system. Imon_max_code can be set to 1024 A or 512 A to use the full-scale of the IMON output.

8 Theory of Operation

8.1 Operating Mode

The XDPE132G5D changes its functionality based on the user-selected operating mode, allowing one device to be used for multiple applications without significant BOM changes. This greatly reduces the user's design cycles and time-to-market (TTM).

The functionality for each operating mode is completely configurable by simple selections in MTP. The mode configuration is shown in Table 6.

Table 6 Mode Selection

Mode	Description
PMBus	Vboot and Dynamic Voltage controlled through VOUT_COMMAND
AVSBus	Vboot controlled by AVS Voltage Setting (register), dynamic Voltage controlled by AVSBus Voltage Command.
AMD SVI2	VBOOT set by SVC/SVD pin state, dynamic voltage controlled by SVI2 command VID code
PWM-VID	VBOOT set with NVM register value, dynamic voltage controlled by PWM-VID duty cycle

8.2 Device Power-on and Initialization

The XDPE132G5D is powered from a 3.3 V DC supply. Figure 8 shows the timing diagram during device initialization. An internal regulator generates a 1.8 V rail to power the control logic within the device. During initial startup, the 1.8 V rail follows the rising 3.3 V supply voltage, proportional to an internal resistor tree. The internal oscillator becomes active at t_1 as the 1.8 V rail is ramping up. Until soft-start begins, the XDPE132G5D PWM outputs are disabled in a high impedance state to ensure that the system comes up in a known state.

The controller comes out of power-on reset (POR) at t_2 (see Figure 8) when the 3.3 V supply is high enough for the internal bias control to generate 1.8 V. After a delay of (t_3-t_2), the trims are read and the automatic trim routines are complete by time t_4. Upon completing the loading of trim registers, the user configuration registers will be initiated at t_4 and complete by t_5. At this time; if enabled in MTP and when the VINSEN voltage is valid, the controller will initiate soft-start if there is no fault in the system.

Note: The minimum rise time for the 3.3V supply is 1ms.

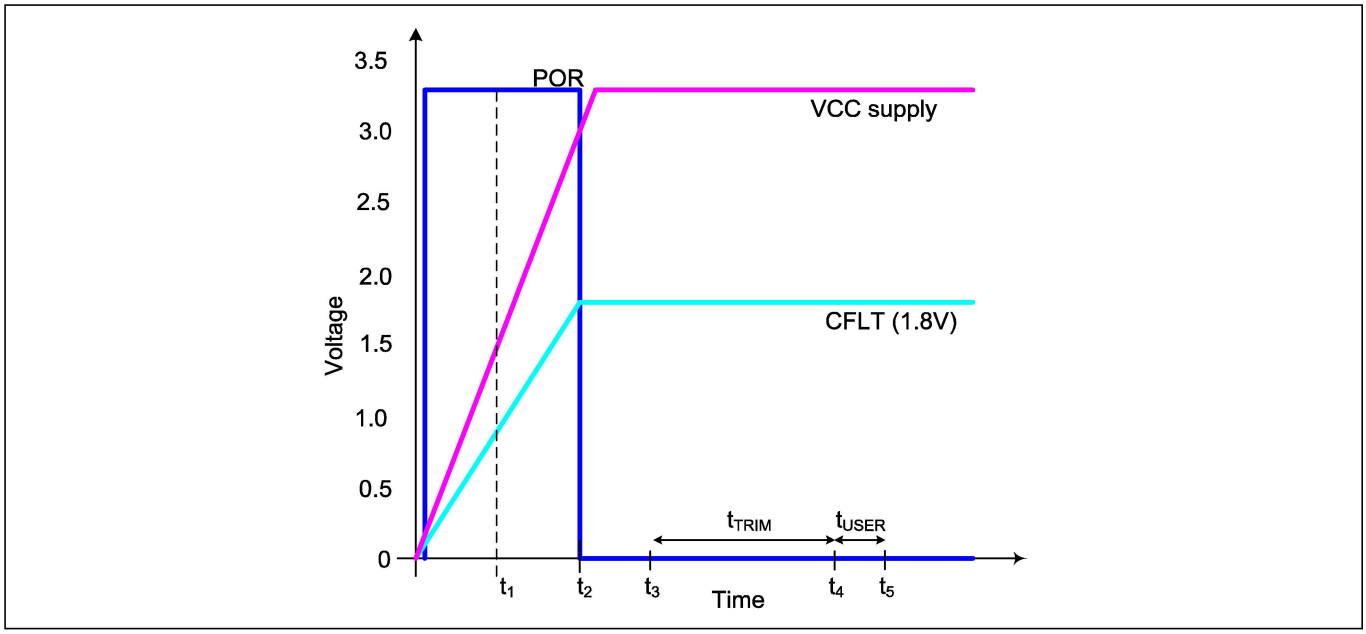

Figure 8 Controller Startup and Initialization

8.3 Test Mode

Driving the PROG pin high (+3.3 V) engages a special test mode in which the I2C address changes to 0Ah. This allows individual in-circuit programming of the controller. This is specifically useful in multi-controller systems that use a single I2C bus. Note that MTP will not load to the working registers while in test mode.

8.4 Supply Voltages

The controller is powered by a 3.3 V supply rail VCC, and has an internal 1.8 V LDO (CFLT) that is used to power internal circuitry. The power phases in the voltage regulator are powered by VIN while the Power Stages/MOSFET Drivers that control the VR are supplied by a lower voltage VAUX supply, typically 5 V.

The recommended decoupling for the 3.3 V is shown in Figure 9. The Vcc pin should have a 0.1 µF and 1 µF X5R-type ceramic capacitors placed as close as possible to the package.

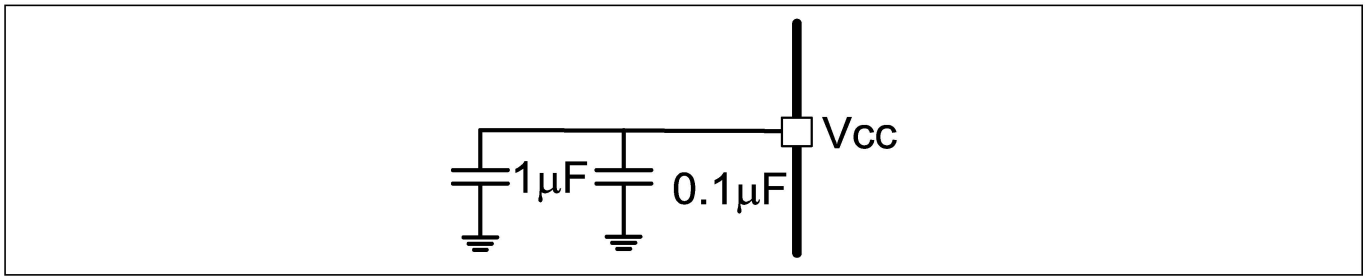

Figure 9 VCC 3.3V Decoupling

8.4.1 CFLT

The CFLT pin must have a 1 µF, X5R (or better) type decoupling capacitor connected close to the package as shown in Figure 10.

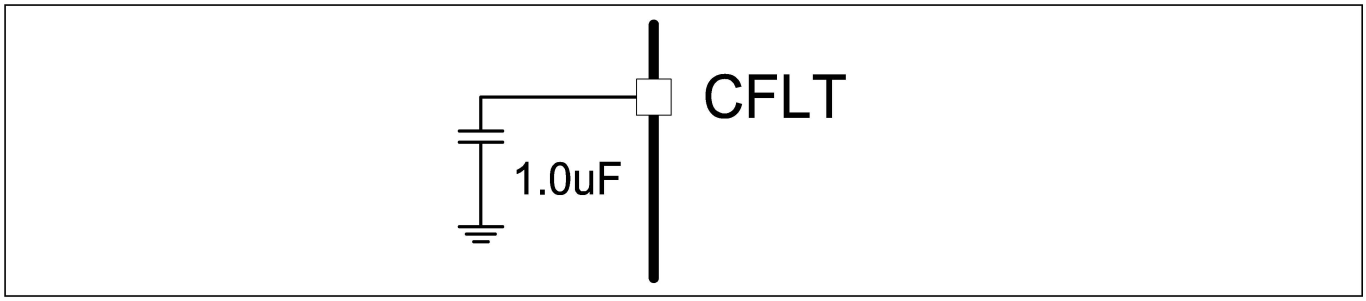

Figure 10 CFLT 1.8 V Decoupling

8.4.2 VIN

The XDPE132G5D is designed to accommodate a wide variety of input power supplies and applications. It allows the user to program the VINSEN turn-on/off voltages.

Table 7 VINSEN Turn-on/off Voltage Range

Threshold	Range
Turn-on	0 V to 15.25 V in ¼ V steps[1]
Turn-off	0 V to 15.25 V in ¼ V steps[1]

Note: [1] Must not be programmed below 4.5 V

The VIN supply voltage on the VINSEN pin is compared against a programmable threshold. Once the rising VINSEN voltage crosses the turn-on threshold and ENx is asserted, all PWM outputs become active. The VINSEN supply voltage is valid until it falls below the programmed turn-off level.

A 14:1 attenuation network is connected to the VINSEN pin as shown in Figure 11. Recommended values for a 12 V system are RVIN_1 = 13 kΩ and RVIN2 = 1 kΩ, with a 1% tolerance or better. CVINSEN is required to have a minimum 1 nF for noise suppression, with a maximum value of 10 nF.

Alternatively, a 22:1 attenuation network can be used for VR that require operation up to 22V.

A configuration bit specifies the 22:1 or 14:1 attenuation network

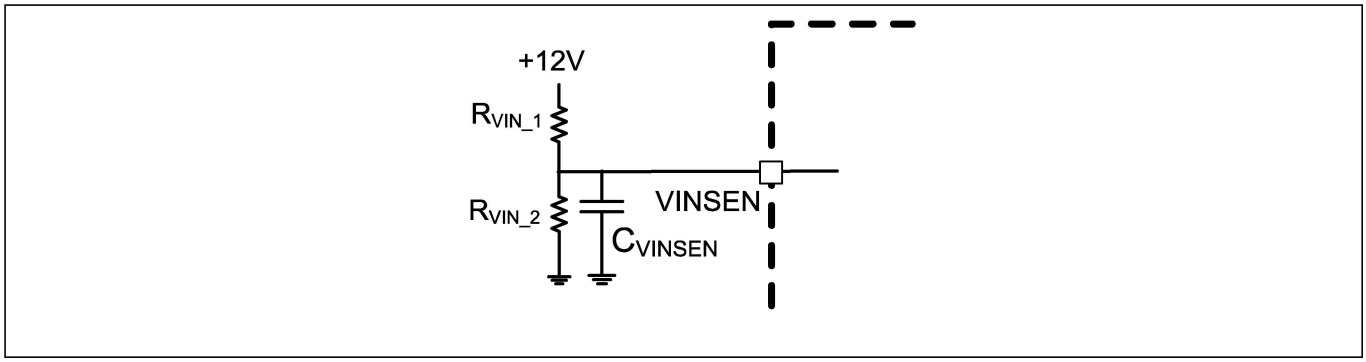

Figure 11 VINSEN Resistor Divider Network

8.4.3 VAUX

The XDPE132G5D also supports monitoring of an auxiliary supply rail (typically used to monitor Power Stage VCC to control sequencing). The supply voltage on the VAUXSEN pin is compared against a programmable threshold. Once the rising VAUXSEN voltage crosses the turn-on threshold and ENx is asserted, all PWM outputs become

active when there are no faults in the VR. The VAUXSEN supply voltage is valid until it falls below the programmed turn-off level.

Table 8 VAUXSEN Turn-on/off Voltage Range

Threshold	Range
Turn-on	0 V to 7 V in 1/32 V steps
Turn-off	0 V to 7 V in 1/32 V steps

A 6.4:1 attenuation network is connected to the VAUXSEN pin as shown in Figure 12. Recommended values for a 5 V system are R1=5.36 kΩ and R2=1 kΩ, with a 1% tolerance or better. C1 is required to have a minimum 1 nF for noise suppression, with a maximum value of 10 nF.

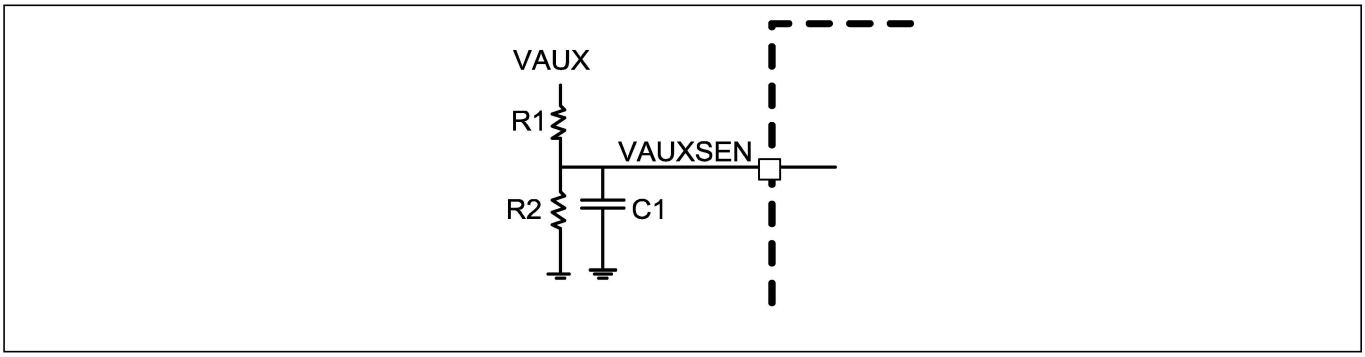

Figure 12 VAUXSEN Resistor Divider Network

The VAUX UV function can be disabled so that the VAUXSEN input can be used purely as a voltage monitor without shutting down the voltage regulator. This is beneficial in some redundant VR applications for monitoring the local voltage (output voltage before the ORing FET) on a phase.

8.5 Power-on Sequence

Once initialization of the device is complete, the ENx signal is used to begin the soft start sequence by enabling the PWM outputs once the 3.3 V and Input Supply rails (VIN and VAUX) are within the defined operating bands. The soft-start time is controlled by the PMBus command TON_RISE.

The VR power-on sequence is initiated when all of the following conditions are satisfied:

- XDPE132G5D Vcc (+3.3 V rail) > VCC Start Threshold (2.8 V)
- Input Voltage (VINSEN rail) > Vin Start Threshold
- Vaux Voltage (if enabled) > VAUX_ON
- ENABLE is HIGH
- The VR has no Over-current, Over-voltage, Over-temperature, Under-voltage, TSEN high or VAUX UVLO faults (when monitored)
- MTP transfer to configuration registers occurred without parity error

Once the above conditions are cleared, start-up behavior is controlled by the operating mode.

Note: STATUS_MFR_SPECIFIC bit 2 (VAUX UV Fault) will be asserted after a controller 3.3V POR if VAUX is below the VAUX_ON threshold. Ensure that VAUX is above the VAUX_ON threshold prior to a 3.3V POR event to avoid asserting VAUX_UV Fault .

8.5.1 Loop Start-up Sequence and Delay

The XDPE132G5D has two Enable pins that can control the startup of each loop. Each loop has independent soft-start times and delay times controlled by TON_RISE and TON_DELAY.

The XDPE132G5D can be configured to enable both loops with a single Enable pin in the following sequence:

- Both loops start together.
- Loop 2 follows Loop 1.
- Loop1 follows Loop 2.

If the XDPE132G5D is configured with a shared enable pin, the delay between the two loops or from Enable can be adjusted for the following pre-defined en_delay_time intervals:

- 0 ms, 0.25 ms, 0.5 ms, 1 ms, 2.5 ms, 5 ms, 10 ms

Table 9 Enable Delay Mode

Mode	Description	Loop1 Start	Loop2 Start
0	Independent Enables	After Loop1 Enable	After Loop2 Enable
1	Shared Enable	After EN1 + Enable Delay Time	
2	Loop1 EN -> Loop2	After EN1	After EN1 + Enable Delay Time
3	Loop2 EN -> Loop1	After EN2 + Enable Delay Time	After EN2
4	Loop1 PG -> Loop2	After EN1	After Loop1 PG + Enable Delay Time
5	Loop2 PG -> Loop1	After Loop2 PG + Enable Delay Time	After EN2

Alternatively, the turn on delay can be more finely controlled by the PMBus command TON_DELAY. Range of this delay is 0 – 63.5 ms in 0.5 ms increments and can be controlled via the PMBus interface or the PMBus register location.

Note: In AMD SVI2 mode, LOOP2 EN function is not available. The multi function Loop2 EN/PWROK pin is dedicated to the AMD SVI2 PWROK function.

Note: In AMD SVI2 mode, either the PWROK or the VR_EN pin (or both) must be low during 3.3V POR

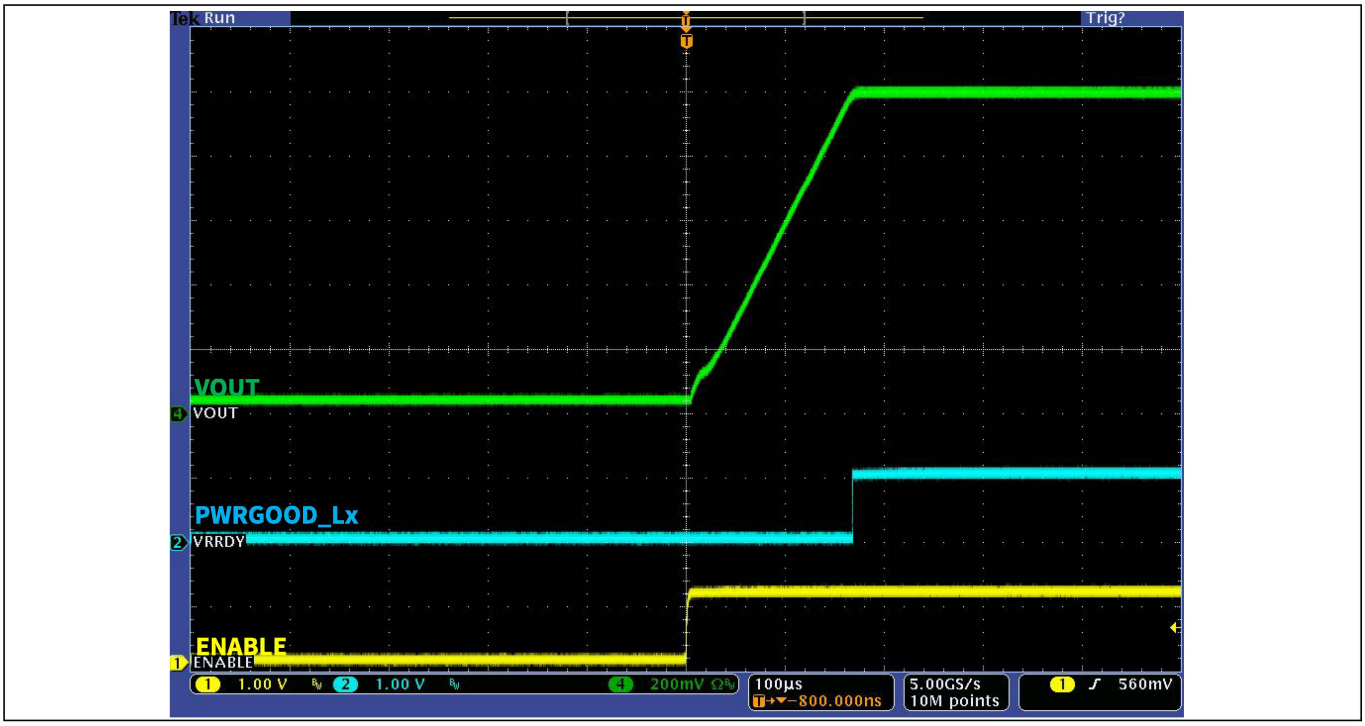

Figure 13 Enable-based Startup

8.6 Power-off Sequence

When the controller is disabled by deactivating the ENx signal, it de-asserts PWRGOOD_LX and shuts down the regulator. The output voltage ramps down to 0 V using the slew rate configured by the PMBus TOFF_FALL command, or decays to 0 V if the PMBus ON_OFF_CONFIG is configured to do so.

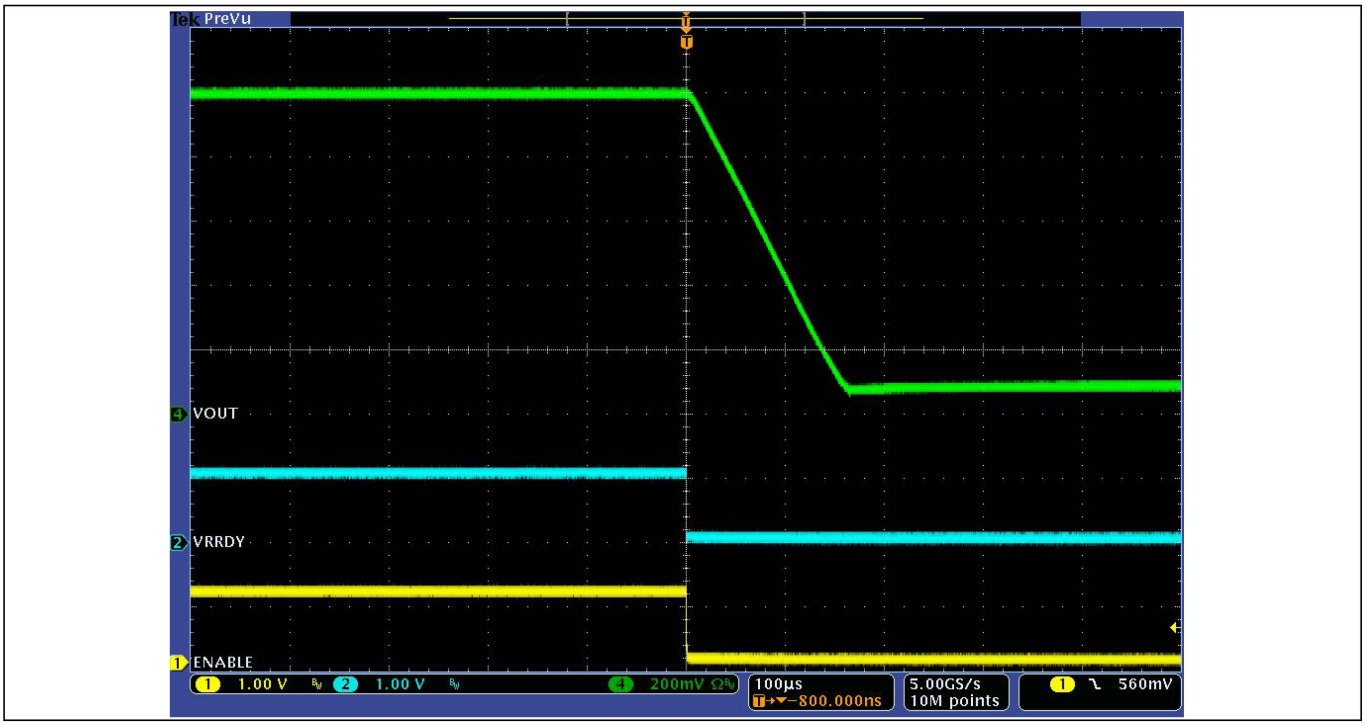

Figure 14 Enabled-based Shutdown (Ramping)

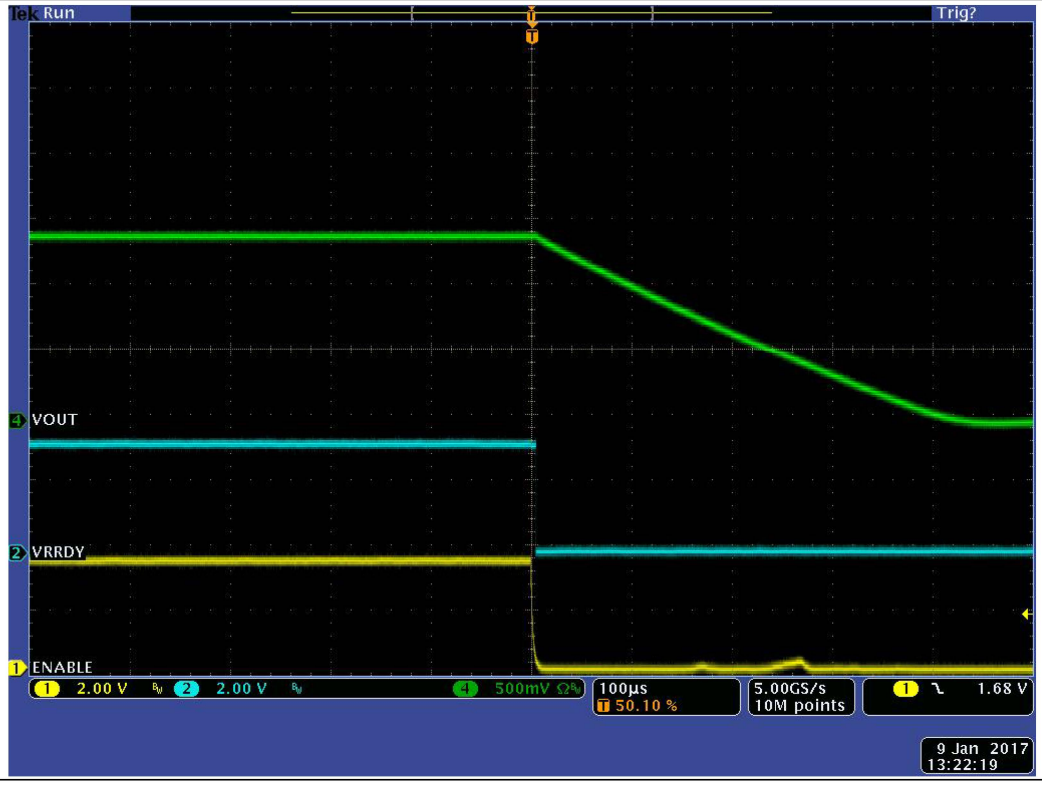

Figure 15 Enabled-based Shutdown (Decay)

8.6.1 Loop Shutdown Sequence and Delay

In the XDPE132G5D, the turn-off sequence of the two output voltages can be controlled by the PMBus command TOFF_DELAY (0-63.5 ms, 0.5 ms increments). This is useful if there is only one enable pin used to control both outputs.

Figure 16 Shutdown Delay of Vout1 Versus Vout2

8.7 PMBus/AVSBus Mode

When the power-on sequence is initiated, and if VBOOT is set to > 0 V, the output voltage will ramp to its configured boot voltage and assert PWRGOOD_Lx. The Vboot voltage is programmed via the VOUT_COMMAND registers or the AVS Voltage register. The slew rate to VBOOT is programmed via the TON_RISE register.

If Vboot = 0 V, the VR will stay at 0 V and will not soft-start until the Power Management System or CPU issues a non-0 V Voltage command through either VOUT_COMMAND or AVSBus to the loop.

The voltage control depends on the configuration of the OPERATION Command as shown in Table 10 .

Table 10 Vout Control

OPERATION Command	Vout Control
80h, 82h	PMBus VOUT_COMMAND
B0h	AVSBus Target Voltage

Whenever Vout Control is transferred from PMBus to AVSBus (OPERATION transitions from 80h or 82h to B0h) the AVSBus Target Voltage is updated with the VOUT_COMMAND value. Alternatively, whenever Vout Control is transferred from AVSBus to PMBus, the AVSBus Target Voltage can either update the VOUT_COMMAND (OPERATION = 82h) or not update VOUT_COMMAND (OPERATION = 80h).

Both values of the PMBus VOUT_COMMAND and the AVSBus Target Voltage can be stored in memory and be available upon device initialization. The output voltage will boot to these voltages based on the stored value of the OPERATION Command. The VOUT_COMMAND value is based on the VOUT_MODE setting (see the XDPE132G5D PMBus Command Set for more information). The AVSBus value is based on the register setting (avs_vout_voltage) shown in Table 11. See the XDPE132G5D Reg Map Document for more detail.

Table 11 AVSBus Boot Voltage

Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)
09F6	2.55	0780	1.92	05FF	1.535	047E	1.15	02FD	0.765	017C	0.38
09EC	2.54	077B	1.915	05FA	1.53	0479	1.145	02F8	0.76	0177	0.375
09E2	2.53	0776	1.91	05F5	1.525	0474	1.14	02F3	0.755	0172	0.37
09D8	2.52	0771	1.905	05F0	1.52	046F	1.135	02EE	0.75	016D	0.365
09CE	2.51	076C	1.9	05EB	1.515	046A	1.13	02E9	0.745	0168	0.36
09C4	2.5	0767	1.895	05E6	1.51	0465	1.125	02E4	0.74	0163	0.355
09BA	2.49	0762	1.89	05E1	1.505	0460	1.12	02DF	0.735	015E	0.35
09B0	2.48	075D	1.885	05DC	1.5	045B	1.115	02DA	0.73	0159	0.345
09A6	2.47	0758	1.88	05D7	1.495	0456	1.11	02D5	0.725	0154	0.34
099C	2.46	0753	1.875	05D2	1.49	0451	1.105	02D0	0.72	014F	0.335
0992	2.45	074E	1.87	05CD	1.485	044C	1.1	02CB	0.715	014A	0.33
0988	2.44	0749	1.865	05C8	1.48	0447	1.095	02C6	0.71	0145	0.325
097E	2.43	0744	1.86	05C3	1.475	0442	1.09	02C1	0.705	0140	0.32
0974	2.42	073F	1.855	05BE	1.47	043D	1.085	02BC	0.7	013B	0.315
096A	2.41	073A	1.85	05B9	1.465	0438	1.08	02B7	0.695	0136	0.31
0960	2.4	0735	1.845	05B4	1.46	0433	1.075	02B2	0.69	0131	0.305
0956	2.39	0730	1.84	05AF	1.455	042E	1.07	02AD	0.685	012C	0.3
094C	2.38	072B	1.835	05AA	1.45	0429	1.065	02A8	0.68	0127	0.295
0942	2.37	0726	1.83	05A5	1.445	0424	1.06	02A3	0.675	0122	0.29
0938	2.36	0721	1.825	05A0	1.44	041F	1.055	029E	0.67	011D	0.285

Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)
092E	2.35	071C	1.82	059B	1.435	041A	1.05	0299	0.665	0118	0.28
0924	2.34	0717	1.815	0596	1.43	0415	1.045	0294	0.66	0113	0.275
091A	2.33	0712	1.81	0591	1.425	0410	1.04	028F	0.655	010E	0.27
0910	2.32	070D	1.805	058C	1.42	040B	1.035	028A	0.65	0109	0.265
0906	2.31	0708	1.8	0587	1.415	0406	1.03	0285	0.645	0104	0.26
08FC	2.3	0703	1.795	0582	1.41	0401	1.025	0280	0.64	00FF	0.255
08F2	2.29	06FE	1.79	057D	1.405	03FC	1.02	027B	0.635	00FA	0.25
08E8	2.28	06F9	1.785	0578	1.4	03F7	1.015	0276	0.63	00F5	0
08DE	2.27	06F4	1.78	0573	1.395	03F2	1.01	0271	0.625	00F0	0
08D4	2.26	06EF	1.775	056E	1.39	03ED	1.005	026C	0.62	00EB	0
08CA	2.25	06EA	1.77	0569	1.385	03E8	1	0267	0.615	00E6	0
08C0	2.24	06E5	1.765	0564	1.38	03E3	0.995	0262	0.61	00E1	0
08B6	2.23	06E0	1.76	055F	1.375	03DE	0.99	025D	0.605	00DC	0
08AC	2.22	06DB	1.755	055A	1.37	03D9	0.985	0258	0.6	00D7	0
08A2	2.21	06D6	1.75	0555	1.365	03D4	0.98	0253	0.595	00D2	0
0898	2.2	06D1	1.745	0550	1.36	03CF	0.975	024E	0.59	00CD	0
088E	2.19	06CC	1.74	054B	1.355	03CA	0.97	0249	0.585	00C8	0
0884	2.18	06C7	1.735	0546	1.35	03C5	0.965	0244	0.58	00C3	0
087A	2.17	06C2	1.73	0541	1.345	03C0	0.96	023F	0.575	00BE	0
0870	2.16	06BD	1.725	053C	1.34	03BB	0.955	023A	0.57	00B9	0
0866	2.15	06B8	1.72	0537	1.335	03B6	0.95	0235	0.565	00B4	0
085C	2.14	06B3	1.715	0532	1.33	03B1	0.945	0230	0.56	00AF	0
0852	2.13	06AE	1.71	052D	1.325	03AC	0.94	022B	0.555	00AA	0
0848	2.12	06A9	1.705	0528	1.32	03A7	0.935	0226	0.55	00A5	0
083E	2.11	06A4	1.7	0523	1.315	03A2	0.93	0221	0.545	00A0	0
0834	2.1	069F	1.695	051E	1.31	039D	0.925	021C	0.54	009B	0
082A	2.09	069A	1.69	0519	1.305	0398	0.92	0217	0.535	0096	0
0820	2.08	0695	1.685	0514	1.3	0393	0.915	0212	0.53	0091	0
0816	2.07	0690	1.68	050F	1.295	038E	0.91	020D	0.525	008C	0
080C	2.06	068B	1.675	050A	1.29	0389	0.905	0208	0.52	0087	0
0807	2.055	0686	1.67	0505	1.285	0384	0.9	0203	0.515	0082	0
0802	2.05	0681	1.665	0500	1.28	037F	0.895	01FE	0.51	007D	0
07FD	2.045	067C	1.66	04FB	1.275	037A	0.89	01F9	0.505	0078	0
07F8	2.04	0677	1.655	04F6	1.27	0375	0.885	01F4	0.5	0073	0
07F3	2.035	0672	1.65	04F1	1.265	0370	0.88	01EF	0.495	006E	0
07EE	2.03	066D	1.645	04EC	1.26	036B	0.875	01EA	0.49	0069	0
07E9	2.025	0668	1.64	04E7	1.255	0366	0.87	01E5	0.485	0064	0
07E4	2.02	0663	1.635	04E2	1.25	0361	0.865	01E0	0.48	005F	0
07DF	2.015	065E	1.63	04DD	1.245	035C	0.86	01DB	0.475	005A	0
07DA	2.01	0659	1.625	04D8	1.24	0357	0.855	01D6	0.47	0055	0
07D5	2.005	0654	1.62	04D3	1.235	0352	0.85	01D1	0.465	0050	0
07D0	2	064F	1.615	04CE	1.23	034D	0.845	01CC	0.46	004B	0
07CB	1.995	064A	1.61	04C9	1.225	0348	0.84	01C7	0.455	0046	0
07C6	1.99	0645	1.605	04C4	1.22	0343	0.835	01C2	0.45	0041	0
07C1	1.985	0640	1.6	04BF	1.215	033E	0.83	01BD	0.445	003C	0
07BC	1.98	063B	1.595	04BA	1.21	0339	0.825	01B8	0.44	0037	0
07B7	1.975	0636	1.59	04B5	1.205	0334	0.82	01B3	0.435	0032	0
07B2	1.97	0631	1.585	04B0	1.2	032F	0.815	01AE	0.43	002D	0
07AD	1.965	062C	1.58	04AB	1.195	032A	0.81	01A9	0.425	0028	0
07A8	1.96	0627	1.575	04A6	1.19	0325	0.805	01A4	0.42	0023	0
07A3	1.955	0622	1.57	04A1	1.185	0320	0.8	019F	0.415	001E	0
079E	1.95	061D	1.565	049C	1.18	031B	0.795	019A	0.41	0019	0
0799	1.945	0618	1.56	0497	1.175	0316	0.79	0195	0.405	0014	0

Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)	Reg Value (hex)	Vboot (V)
0794	1.94	0613	1.555	0492	1.17	0311	0.785	0190	0.4	000F	0
078F	1.935	060E	1.55	048D	1.165	030C	0.78	018B	0.395	000A	0
078A	1.93	0609	1.545	0488	1.16	0307	0.775	0186	0.39	0005	0
0785	1.925	0604	1.54	0483	1.155	0302	0.77	0181	0.385	0000	0

Note: Any output voltage set to less than 250mV will go to 0V (Gray Section)

8.8 Phasing

The XDPE132G5D offers flexible phase assignment between the two loops. Loop1 can support up to 16 phases and loop2 can support up to 8 phases provided the sum of loop1 & loop2 phases is less than or equal to 16. The phase of the PWM outputs is automatically adjusted to optimize phase interleaving for minimum output ripple. Phase interleaving results in a ripple frequency that is the product of the switching frequency and the number of phases. A high ripple frequency results in reduced ripple voltage thereby minimizing the output filter capacitance requirements, resulting in significant total BOM cost reduction.

Phases are disabled based upon the configuration used. Disabled PWM outputs should be left floating. Typical PWM pulse phase relationships are shown in Table 12, and Figure 17 and Figure 18.

Table 12 Phase Relationship

Phases	Phase Angle
1	-
2	180°
3	120°
4	90°
5	72°
6	60°
7	51.43°
8	45°
9	40°
10	36°
11	32.73°
12	30°
13	27.69°
14	25.7°
15	24°
16	22.5°

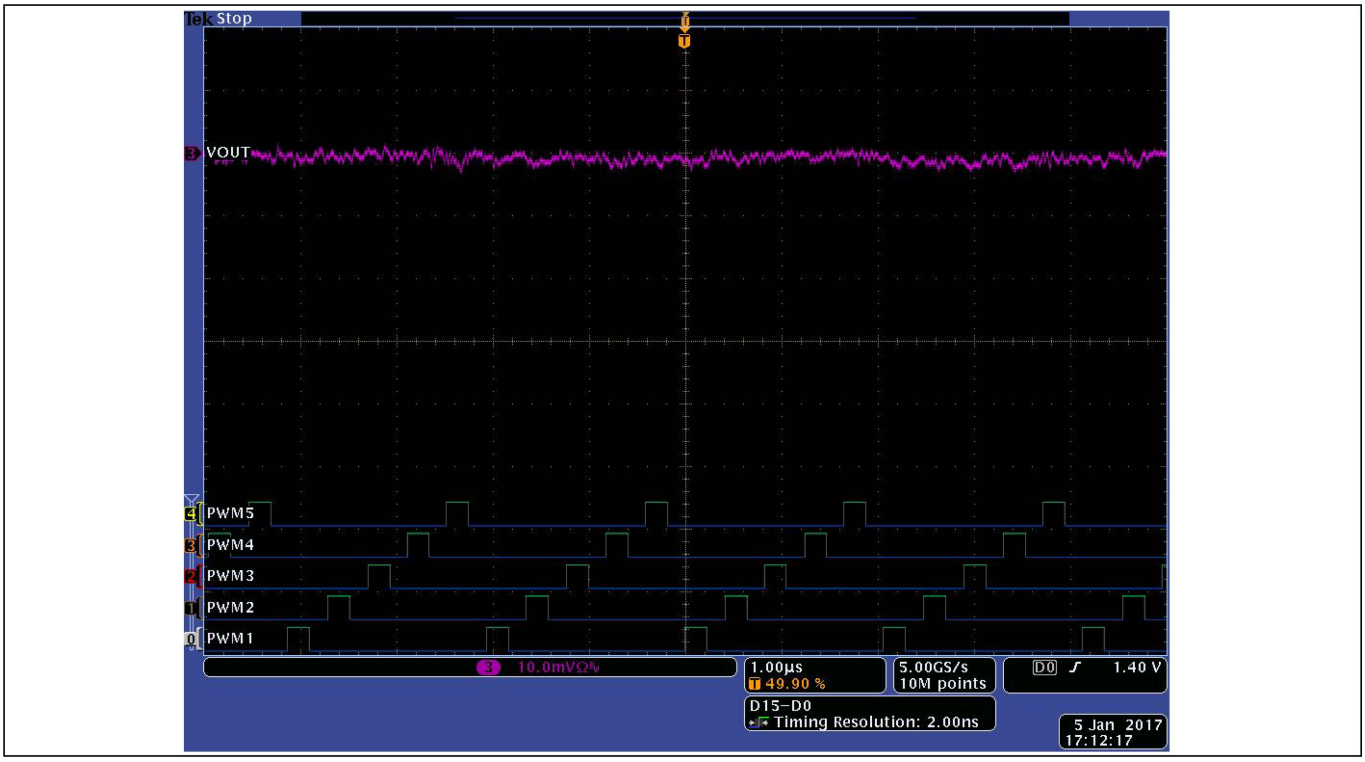

Figure 17 PWM Interleaving for 5 phases

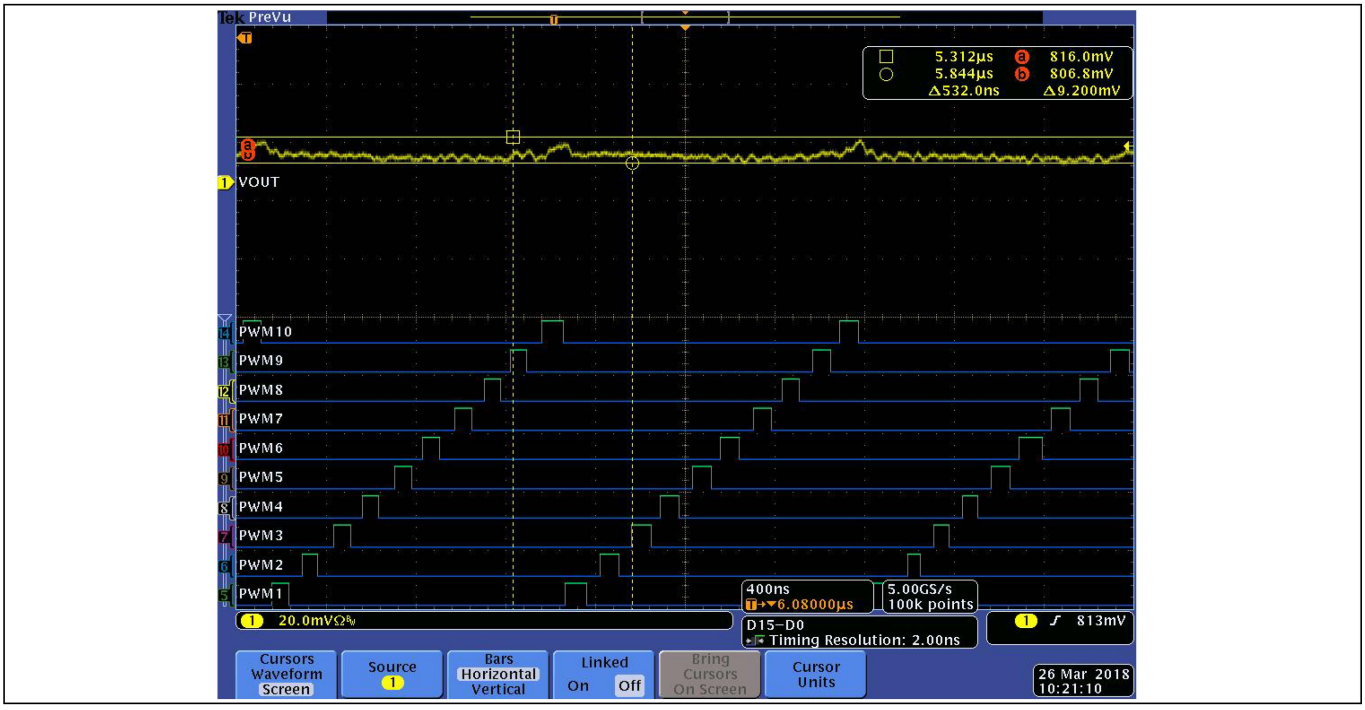

Figure 18 PWM Interleaving for 10 phases

8.9 Switching Frequency

The phase switching frequency (Fsw) of the XDPE132G5D is set by a user-configurable register. The switching frequency variation with register setting has been plotted in Figure 19.

The XDPE132G5D oscillator is factory-trimmed to guarantee high accuracy and very low jitter compared to analog controllers.

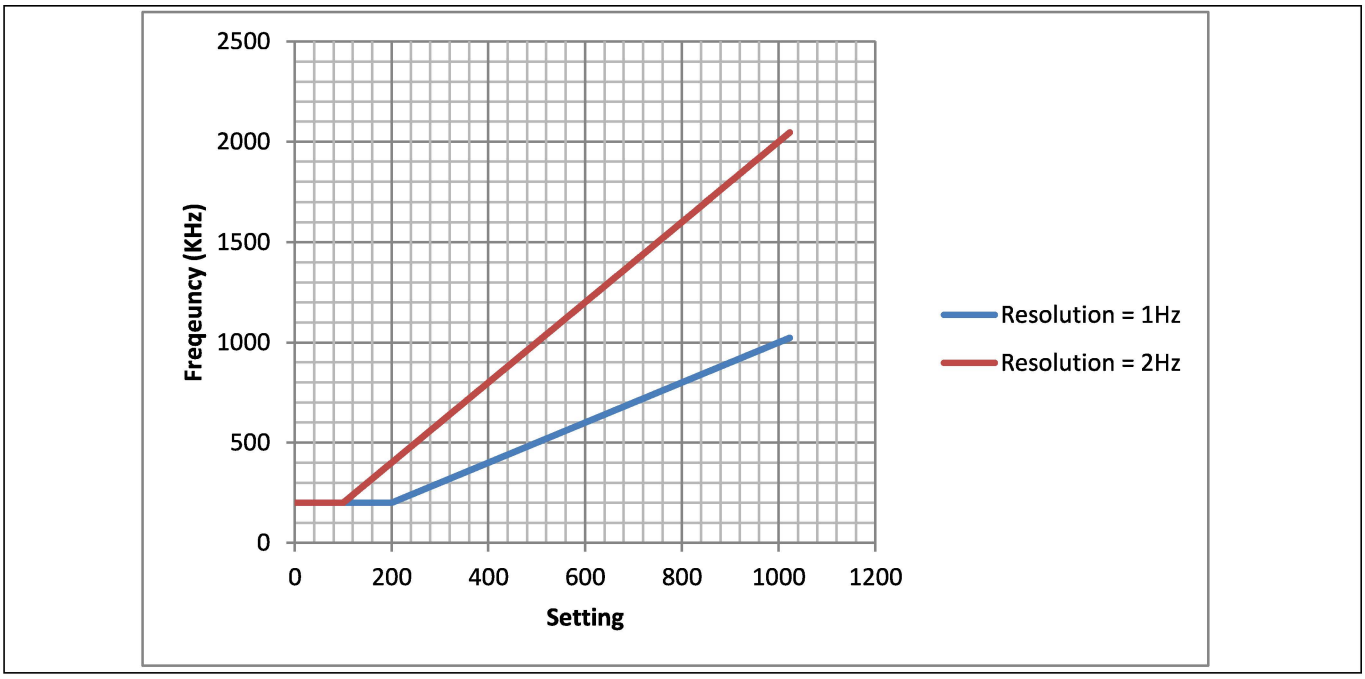

Figure 19 Switching Frequency versus register setting

8.10 MOSFET Driver and Power Stage Selection

The PWM signals from the active phases of The XDPE132G5D are designed to operate with industry standard tri-state type drivers or OptiMOS™ Power Stage devices. The logic operation for these types of tri-state drivers is depicted in Figure 20.

When in tri-state, The XDPE132G5D floats the outputs so that the voltage level is determined by an external voltage divider which is typically inside the MOSFET driver.

Note that the PWM outputs are tri-stated whenever the controller is disabled (EN = low), the shut-down ramp has completed or prior to soft-start.

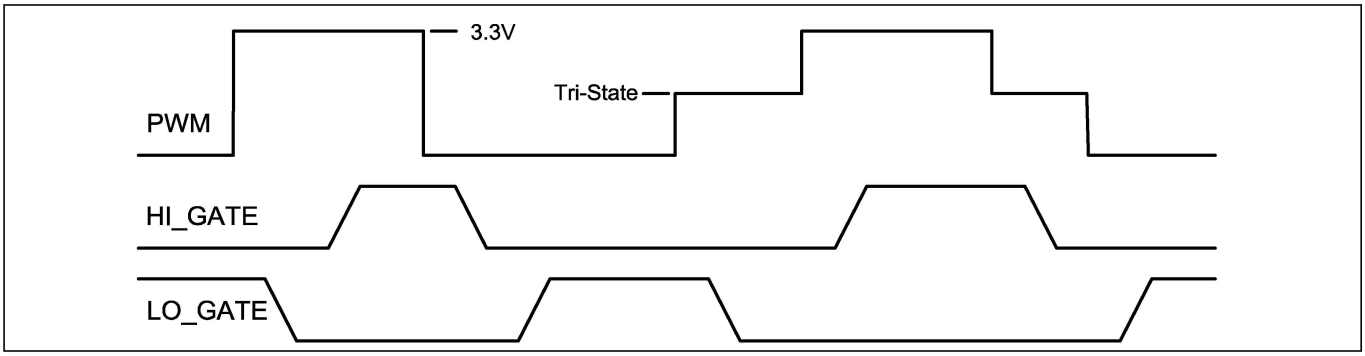

Figure 20 3.3 V Tri-state Driver Logic Levels

8.11 Output Voltage Differential Sensing

The XDPE132G5D's VSEN and VRTN pins for each loop are connected to the load sense pins of the output voltage to provide true differential remote voltage sensing with high common-mode rejection. Each loop has a high bandwidth error amplifier that generates the error voltage between this remote sense voltage and the target voltage. The error voltage is digitized by a fast, high-precision ADC.

As shown in Figure 21, the Vsen and Vrtn inputs have a 20 kΩ pull up to an internal 1 V rail. This causes some current flow in the VSEN and VRTN lines. To minimize the offset created by this current flow, the external series impedance on these lines needs to be kept to a minimum.

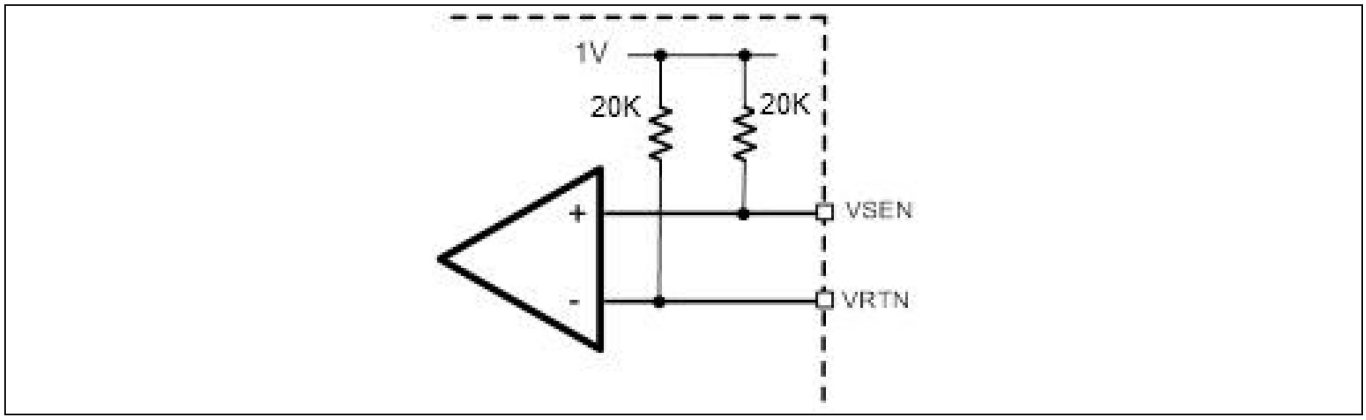

Figure 21 Output Voltage Sensing Impedance

8.12 Input Current Sensing

The XDPE132G5D supports a proprietary lossless input current sensing scheme. The controller can accurately estimate the actual input current on a per loop basis, as it knows the value of output current, output voltage, and pulse width of each phase. This eliminates the need for a dedicated IINSEN pin and also simplifies the board layout by eliminating the external amplifier and shunt.

8.13 Output Current Sensing

The XDPE132G5D supports individual output current sensing for each phase to support accurate Adaptive Voltage Positioning (AVP), current balancing, and over-current protection. The XDPE132G5D also supports RDSon current sensing techniques.

The RDSon current sense Power Stages provide temperature compensated phase current information (gain = 5 mV/A) based on sensing the voltage across the RDSon of the low-side MOSFET. The XDPE132G5D can accept the Power Stage's current output directly without any external component in the interface. This allows a clean, tight layout of the current sense signals and also reduces the overall solution size and BOM cost. Figure 22 shows the direct connect between the Power Stage and the XDPE132G5D at the current sense interface.

The individual phase currents are summed to get the total output current which is used for AVP and OCP.

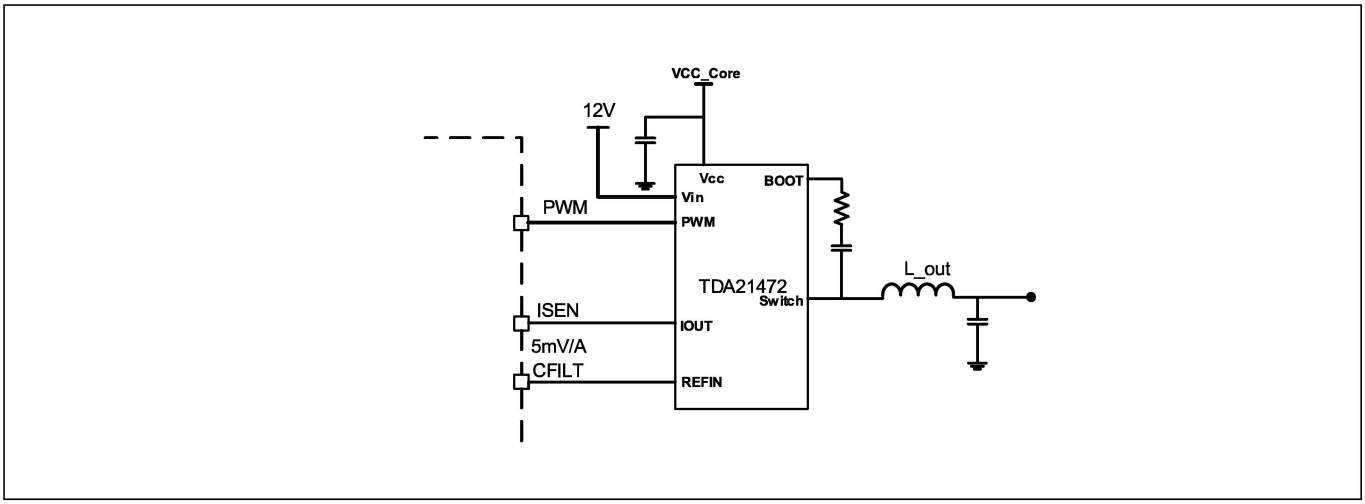

Figure 22 RDson Current Sense

8.13.1 Output Current Balance

The XDPE132G5D provides accurate digital phase current balancing in any phase configuration. Current balancing equalizes the current across all the phases. This improves efficiency, prevents hotspots and reduces the possibility of inductor saturation.

The sensed current information is digitized by a high-speed A/D converter. The digitized currents are low-pass filtered and passed through a proprietary current balance algorithm to enable the equalization of the phase currents as shown in Figure 23.

The proprietary high-speed active phase current balance operates during load transients to eliminate current imbalance that can result from a load current oscillating near the switching frequency. The order in which the phases output PWM pulses is decided based on an adaptive High Speed Phase Balance (HSPB) to ensure that the phases remain balanced during high frequency load transients.

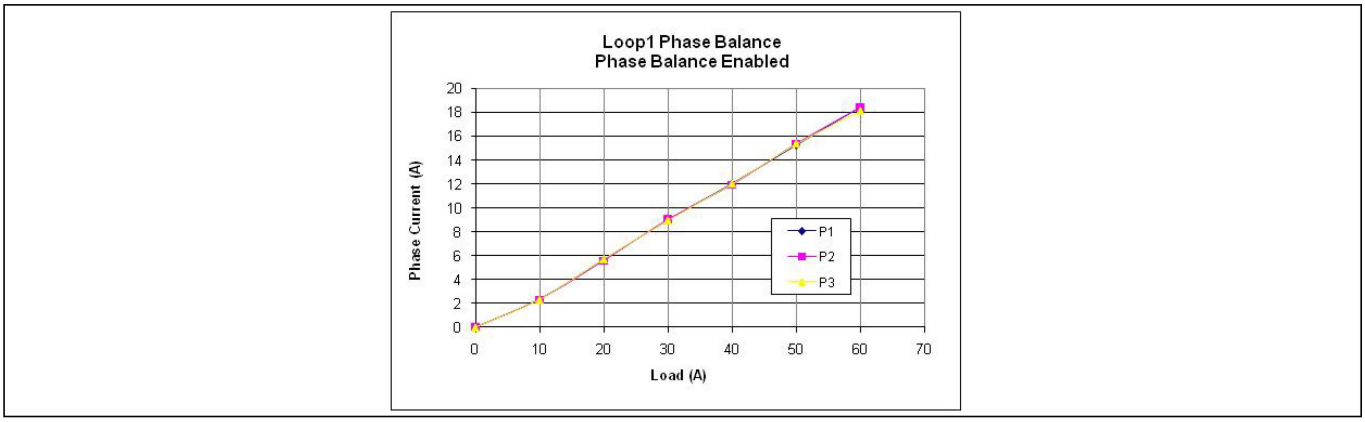

Figure 23 Typical Phase Current Balance (3-Phases enabled)

8.13.2 Output Current Calibration

XDPE132G5D allows calibration of individual phase currents as well as the total output current. Each phase can be turned on individually and its corresponding gain and offset can be adjusted for superior output current

accuracy. In addition to this, the gain and offset of the total output current can also be calibrated. The table below summarizes the gain and offset adjustment options for the phase current and total output current.

Table 13 Phase and Total Output Current Calibration

		Range	Resolution
Individual Phase Current	Gain	-25% to +24.2%	0.78%
	Offset	-8 A to +7.75 A	0.25 A
Total Output Current	Gain	-25% to +24.2%	0.78%
	Offset	-16 A to +15.75 A	0.25 A

8.14 Load Line for Active Voltage Positioning

The XDPE132G5D offers a digital load line which can be set via a configuration register or PMBus VOUT_DROOP command without a need for any external components. The digitized individual phase currents are summed and utilized for setting the digital load line. The load line can be programmed from 0 to 19.98 mΩ at a resolution of 19.53 µΩ. In addition to this, the bandwidth of the digital load line is also programmable from 30 kHz up to 1 MHz.

8.15 Digital Feedback Loop and PWM Control

The XDPE132G5D uses a digital feedback loop to minimize the requirement for output decoupling, and to maintain a tightly regulated output voltage. The error between the target and the output voltage is digitized and passed through a low-pass filter. This filtered signal is then passed through an initial single-pole filter stage, followed by the PID (Proportional Integral Derivative) compensator, and an additional single-pole filter stage. The loop compensation parameters Kp (proportional coefficient), Ki (integral coefficient), and Kd (derivative coefficient), as well as the low-pass filter pole locations are user-configurable to optimize the VR design for the chosen external components.

The adaptive PID control used in the XDPE132G5D intelligently scales the coefficients and the low-pass filters in real-time, to maintain optimum stability, as phases are added and dropped dynamically in the application. This auto-scaling feature significantly reduces design time by virtue of having to design the PID coefficients design only for one loop combination (Figure 24).

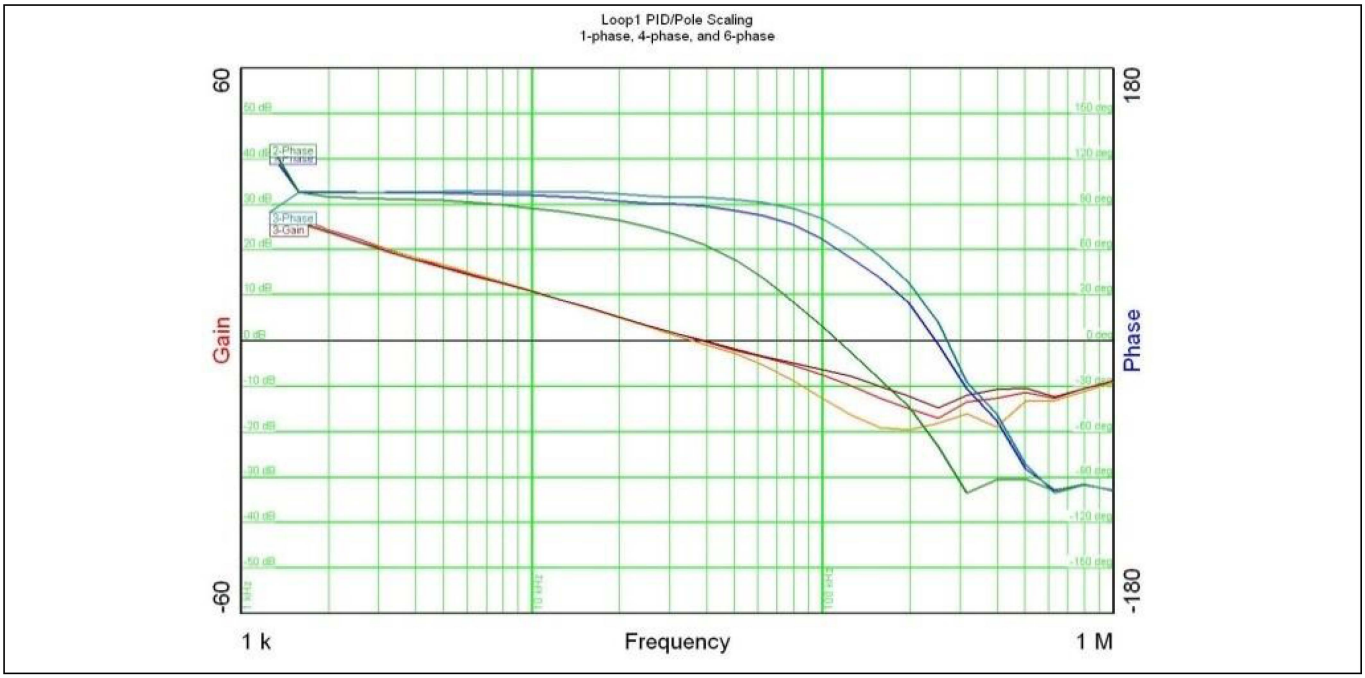

Figure 24 Stability With Phase Add/Drop

Each of the proportional, integral and derivative terms is a 7-bit value stored in MTP that is decoded by the IC's digital core. This allows the designer to set the converter bandwidth and phase margin to the desired values.

The compensator's transfer function is defined as:

$$\left(Kp + \frac{Ki}{s} + Kd \bullet s\right) \bullet \left(\frac{1}{1 + s/\omega p_1}\right) \bullet \left(\frac{1}{1 + s/\omega p_2}\right)$$

where ωp1 and ωp2 are the two configurable poles, typically positioned to filter noise, and to roll off the high-frequency gain that the Kd term creates.

The outputs of the compensator and the phase current balance block are fed into a digital circuit to generate the PWM pulses for the active phases. The digital PWM generator has a native time resolution of 1.3 ns which is combined with digital dithering to provide an effective PWM resolution of 163 ps. This ensures that there is no limit cycling when operating at the highest switching frequency.

8.16 Adaptive Transient Algorithm (ATA)

The XDPE132G5D Adaptive Transient Algorithm (ATA) is a high speed non-linear control technique that allows compliance with CPU voltage transient load regulation requirements, with minimum output bulk capacitance for reduced system cost.

A high-speed digitizer measures both the magnitude and slope of the error signal to predict the load current transient. This prediction is used to control the phase relationships of the PWM pulses. The ATA is a wide-band non-linear control loop which can react faster to load transients and ensures that the output voltage is within the regulation limits even during fast dynamic load and voltage change events. Figure 25 illustrates the transient performance improvement provided by the ATA showing the clear reduction in undershoot and overshoot. Figure 26 is a zoomed-in scope capture of a load step, illustrating the fast reaction time of the ATA, and how the algorithm changes the pulse phase relationships. XDPE132G5D provides the option to enable or disable this feature, using a digitally programmable bit.

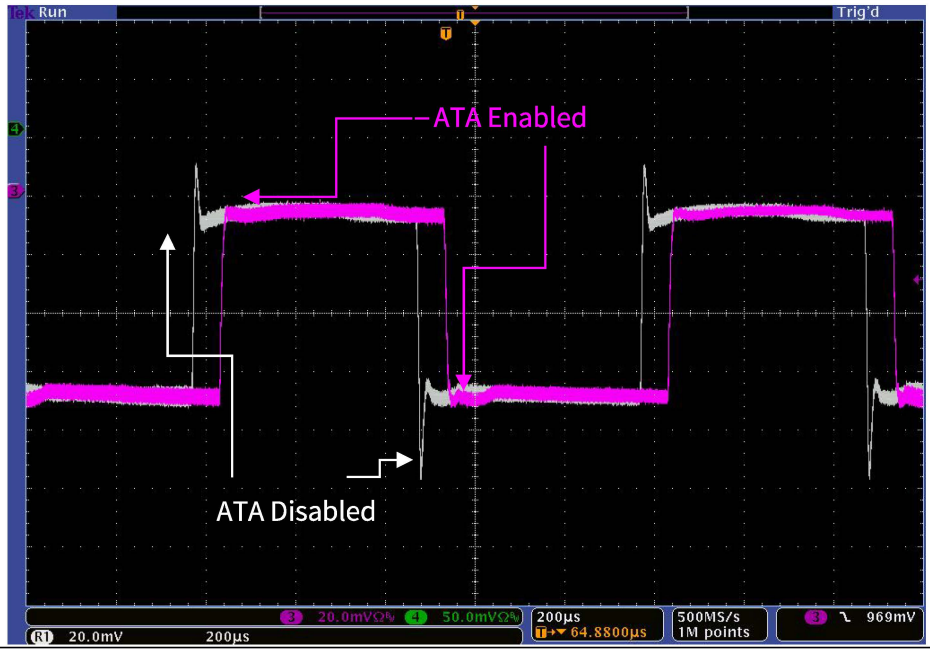

Figure 25 ATA Enable/Disable Comparison

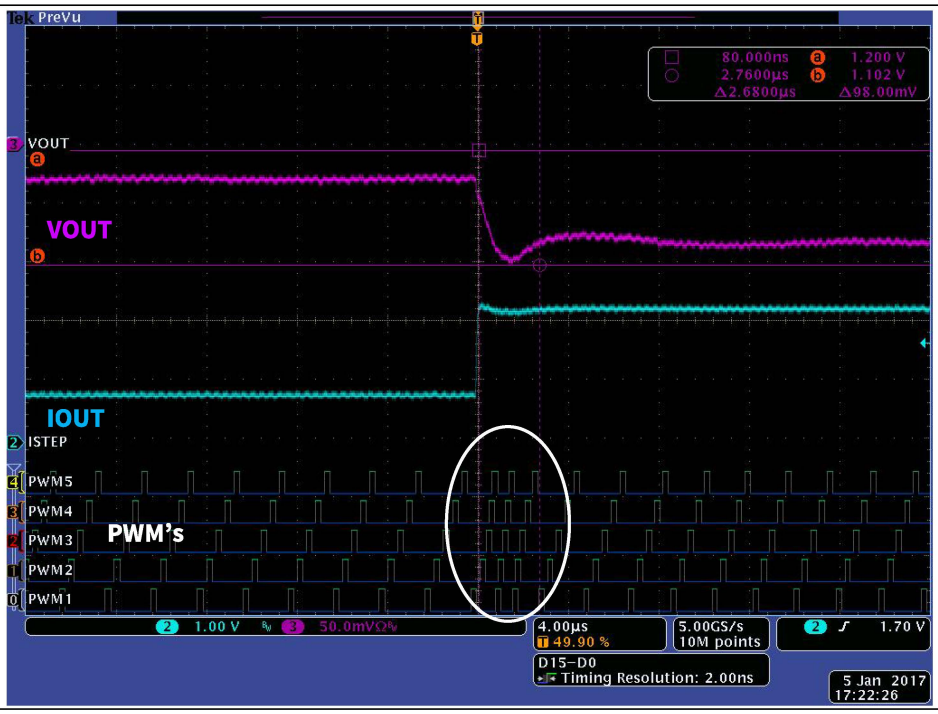

Figure 26 ATA Feature – Zoomed In

In addition, during load release events, the ATA may also be programmed to turn off the low-side MOSFETS instead of leaving them on. This forces the load current to flow through the larger FET body diode, and helps to reduce the overshoot created during a load release, as shown in Figure 27 below.

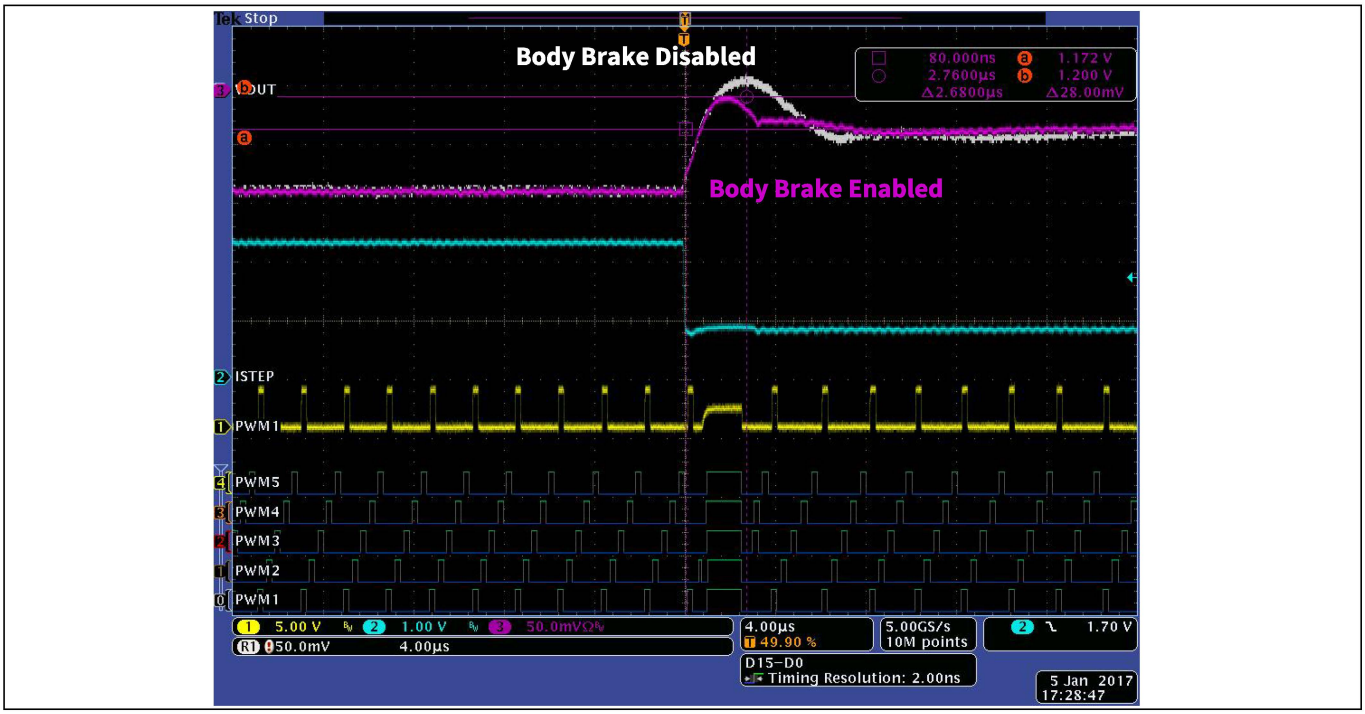

Figure 27 Body Braking during Load Release

8.17 Dynamic Output Voltage Control

8.17.1 Slew Rate

The XDPE132G5D provides the VR designer with a slew rate range from 0.25 mV/µs to 127 mV/µs , which can be configured in 0.25 mV/µs steps through the VOUT_TRANSITION_RATE Register for each loop.

8.17.2 Dynamic Output Voltage Compensation

The XDPE132G5D can compensate for the error produced by the current feedback in a system with AVP (Active Voltage Positioning) when the output voltage is ramping to a higher voltage. An output capacitance term is provided in the MTP registers to help model the effects of variation in output voltage during a voltage ramp, due to the inrush current into the output bulk capacitors. Once properly modeled, the output voltage will follow the DAC more closely during a positive dynamic output voltage change, and provide better dynamic response. Figure 28 shows the effects that Dynamic Output Voltage Compensation has on the output voltage.

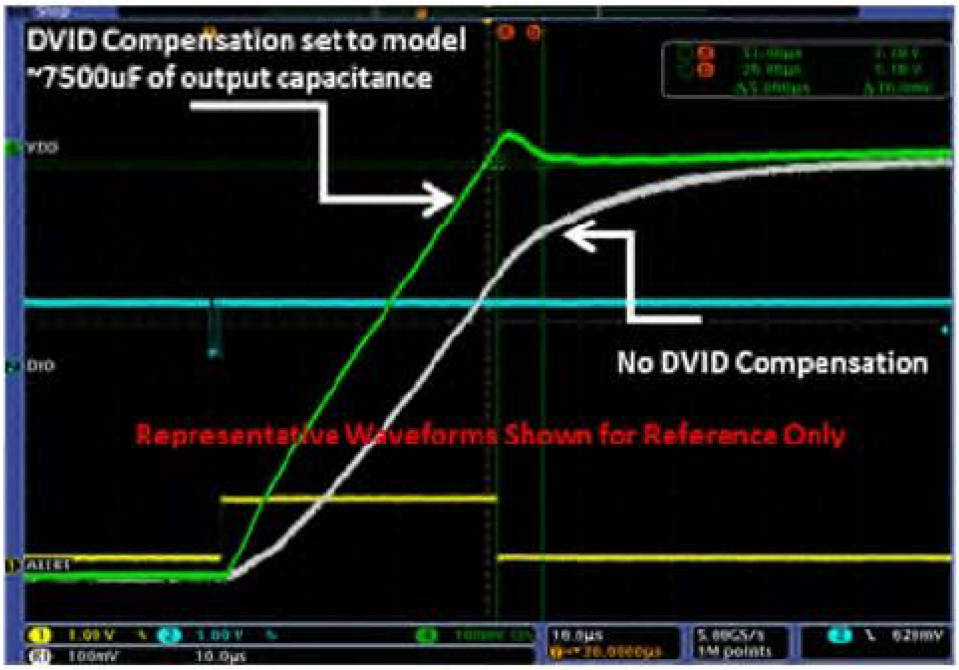

Figure 28 Dynamic Output Voltage Compensation

8.18 Efficiency Shaping

In addition to CPU-specified Power States, the XDPE132G5D features Efficiency Shaping Technology that enables VR designers to cost-effectively maximize system efficiency. Efficiency Shaping Technology consists of Dynamic Phase Control to achieve the best VR efficiency at a given cost point.

8.18.1 Power-Mode States

The XDPE132G5D uses Power States to set the power-savings mode. These are summarized in Table 14 .

Table 14 Power States

Power State	Mode	Recommended Current
PS0	Full Power	Maximum
PS1	Light Load 1-2Φ	<20 A
PS2	1Φ Active Discontinuous (Diode Emulation)	<5 A

The Power States may be commanded through the I2C/PMBus interface, the AVSBus interface, or the XDPE132G5D can autonomously step through the Power States based upon the regulator conditions as summarized in Table 15.

Table 15 Power State Entry/Exit

Power State	Command Mode	Auto Mode
PS1 Entry	a) Command	n/a if Phase Shed enabled
PS1 Exit	a) Command to PS0 b) During DVID event c) Current limit to PS0	n/a if Phase Shed enabled
PS2 Entry	a) Command	Current level in 1Φ
PS2 Exit	a) Command to PS1/0	Fsw > Fsw_desired

Power State	Command Mode	Auto Mode
	b) During DVID event c) Current limit to PS0	to PS0, DVID to PS0, Current limit to PS0

8.18.2 Dynamic Phase Control (DPC) in PS0

The XDPE132G5D optionally supports the ability to autonomously adjust the number of phases with load current, thus optimizing efficiency over a wide range of loads. The output current level at which a phase is added can be programmed individually for each phase for optimum results (Table 16).

Table 16 DPC Thresholds

Register (2A steps)	Function
Phase1_thresh	2Φ when Iout > Phase1_thresh
Phase2_delta	3Φ when Iout > Phase1_thresh + Phase2_delta
Phase3_delta	4Φ when Iout > Phase1_thresh + Phase2_delta + Phase3_delta
Phase4_delta	5Φ when Iout > Phase1_thresh + Phase2_delta + Phase3_delta + Phase4_delta
Phase5_delta	6Φ when Iout > Phase1_thresh + Phase2_delta + Phase3_delta + Phase4_delta + Phase5_delta
Phase6_delta	7Φ to 16 Φ (incrementally) when Iout > Phase1_thresh + Phase2_delta + Phase3_delta + Phase4_delta + Phase5_delta + Phase_6 delta

As shown in Figure 29 (loop one, 8-phase example shown), the designer can configure the VR to dynamically add or shed phases as the load current varies. Both control loops of the XDPE132G5D have the DPC feature.

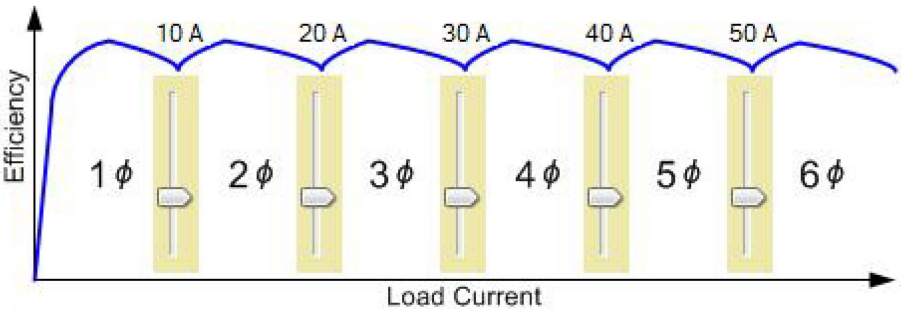

Figure 29 Dynamic Phase Control Regions

The XDPE132G5D Dynamic Phase Control reduces the number of phases (Figure 30) based upon monitoring both the filtered total current and the error voltage over the DPC filter window. Monitoring the error voltage ensures that the VR does not drop phases during large load changes.

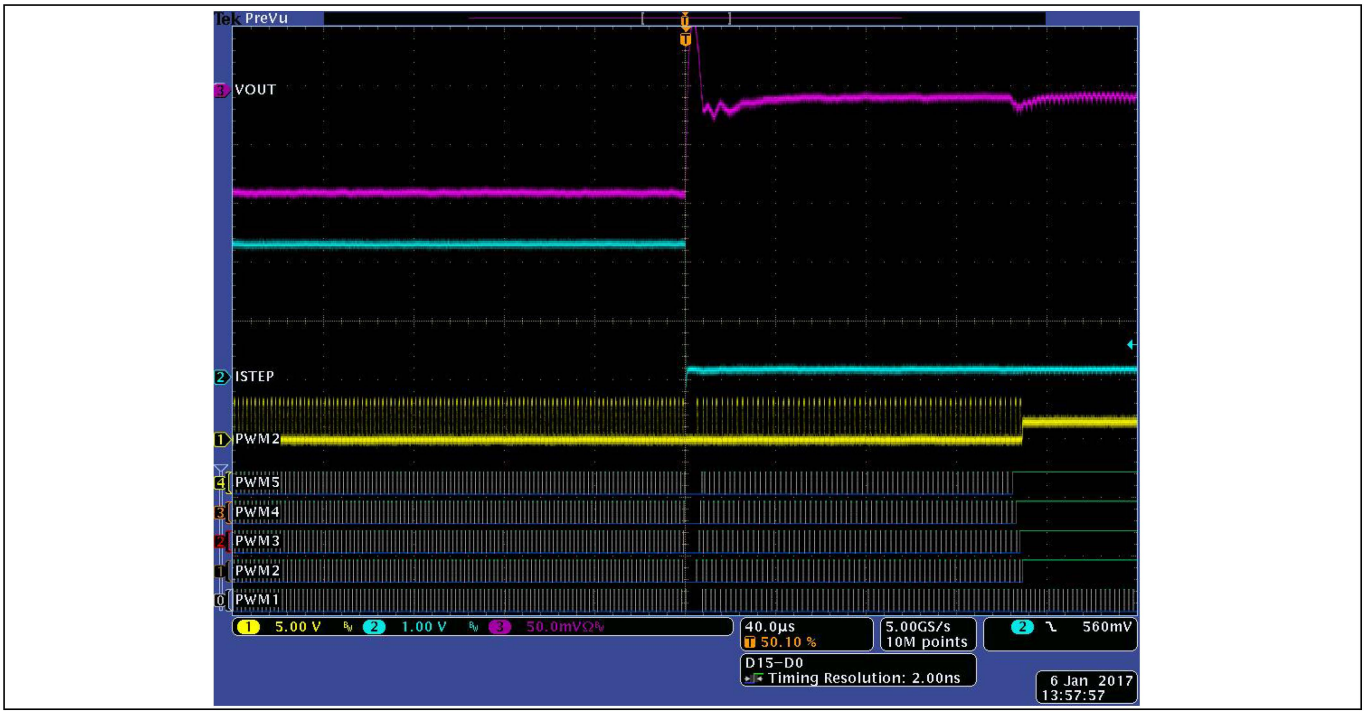

Figure 30 Phase Shed 5 to 1

During a large load step, and based on the error voltage, the controller instantly goes to the maximum number of phases. It remains at this level for a period equivalent to the DPC filter delay, after which phases get dropped depending on the load current. The Dynamic Phase Control (DPC) algorithm is designed to meet customer specifications even if the VR experiences a large load transient when operating with a lower number of phases. The ATA circuitry ensures that the idle phases are activated with optimum timing during a load step as shown in Figure 31 and Figure 32 below.

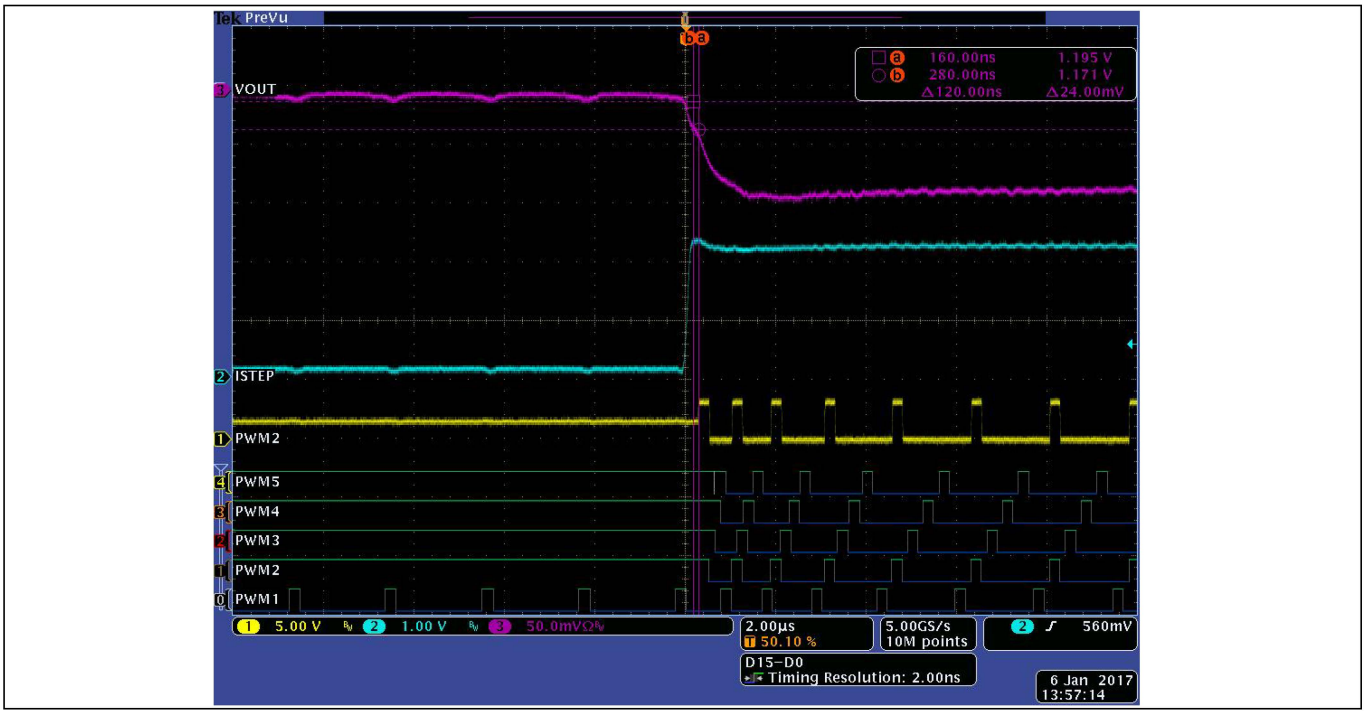

Figure 31 Phase Add 1 to 5

Figure 32 Zoomed-out View of Phase Shed/Add

Current limit and current balancing circuits remain active during ATA events to prevent inductor saturation and maintain even distribution of current across the active phases.

The add/drop points for each phase can be set in 2 A increments from 0 to 30 A per phase, with a fixed 4 A hysteresis. This results in a uniform per-phase current density as the load increases or decreases.

Having DPC enabled optimizes the number of phases used in real time, providing significant light and medium-load efficiency improvements, as shown in Figure 33.

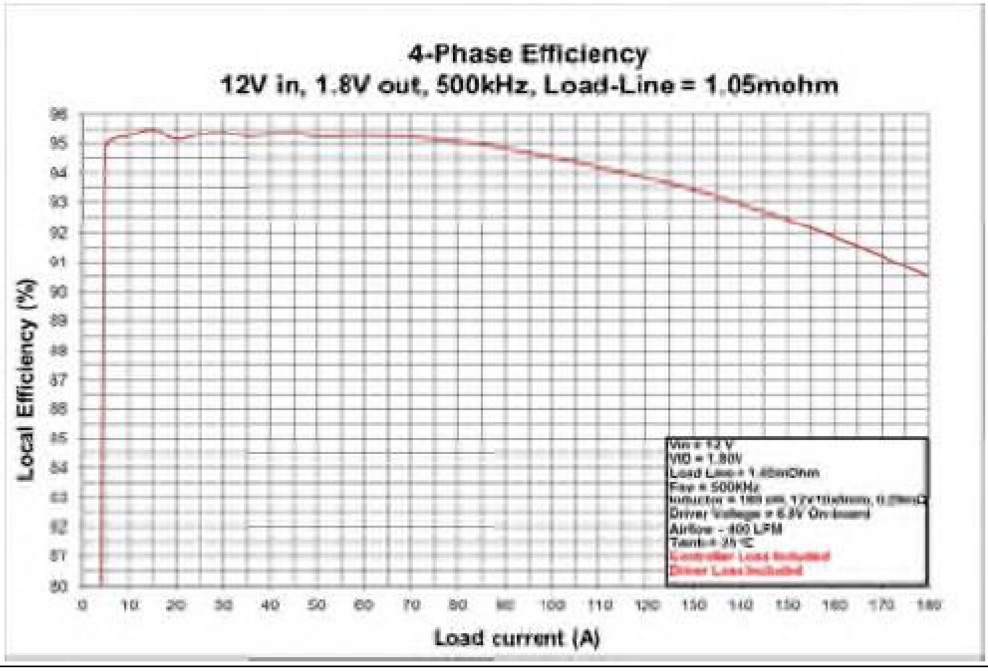

Figure 33 Light Load Efficiency Improvements with DPC

8.18.3 Discontinuous Mode of Operation – PS2

Under very light loads, the VR efficiency is dominated by MOSFET switching losses. In PS2 mode, the XDPE132G5D operates as a constant on-time controller where the user sets the desired peak-to-peak ripple by programming an error threshold and the on-time duration (Table 17).

Table 17 PS2 Mode Constant On-time Control

Register Variable	Function
ni_thresh	Sets the current level below which PS2 is entered.
diode_emu_thresh	Sets the error threshold to start a pulse during diode emulation, with 4 mV resolution.
Diode_emu_pw	Sets the duration of the ON-time pulse in 20 ns steps during diode emulation.
De_off_time_adjust	Reduces the calculated low-side FET ON-time during diode emulation in 62.5 ns steps. Useful for compensating for Power Stage or other drivers' tri-state delay for better zero-crossing prediction.

In PS2 mode (Active Diode Emulation Mode), the internal circuitry estimates when the inductor current declines to zero on a cycle-by-cycle basis, and shuts off the low-side MOSFET at an appropriate time in each cycle (Figure 34). This effectively lowers the switching frequency, resulting in lowered switching losses and improved efficiency.

Industry standard tri-state drivers typically have delays when entering tri-state, typically 150 ns to 300 ns, which allows negative current to build up, causing switch node ringing and reducing efficiency. The Reduce_DE_Off_Time variable allows for compensation of the tri-state delay by reducing the low-side FET on-time by an equivalent amount.

Figure 34 PS2 Active Diode Emulation Mode

9 Faults and Protections

The comprehensive fault coverage of the XDPE132G5D protects the VR against a variety of fault conditions. Fault detection can be configured and monitored through the PMBus Interface. This monitoring during system development is also assisted through the use of the OpenPower GUI. Fault indications in the PMBus can only be cleared with the CLEAR_FAULTS command, a rising edge of ENABLE or a 3.3 V power cycle. The list below shows the available fault protection.

- Output Over-voltage
- Output Under-voltage
- Output Over-current
- Per Phase Over-current
- Over-temperature
- Phase current imbalance
- Power Stage TOUT pin assertion
- Input Under-voltage
- Input Over-voltage

With two loops operating in one controller, the fault shutdown for each loop can be controlled through the Global Fault Enable. When enabled, any fault that occurs on one loop will cause the other loop to shutdown, else only the faulted loop reacts to its own fault.

9.1 Output Over-voltage Protection (OVP)

When the VR is disabled and during soft-start, a Fixed OVP Threshold is enabled and can be programmed to one of the thresholds shown in Table 18. If the output voltage happens to exceed this fixed threshold, the XDPE132G5D will detect an output over-voltage fault and turn on the low-side MOSFETS to limit the output voltage rise. Once soft-start is complete and the output voltage has reached its regulation point, the Fixed OVP Threshold is disabled. The XDPE132G5D now monitors the output voltage to a relative OVP Threshold that is user-programmable to values shown in Table 19. If the output voltage goes above the Output Voltage Set point by the programmed threshold, the XDPE132G5D will detect an output over-voltage fault and turn on the low-side MOSFETS to limit the output voltage rise. The OVP action on the low-side MOSFETS is programmable to either Latch the low-side MOSFETS ON indefinitely, or keep the low-side MOSFETS ON and release them when the output voltage drops to less than 248 mV.

Table 18 Fixed OVP Thresholds

Value	Threshold
0	2.5 V
1	1.2 V
2	1.275 V
3	1.35 V

Table 19 Relative OVP & UVP Thresholds

Value	Threshold
0	50 mV
1	100 mV
2	150 mV
3	200 mV
4	250 mV
5	300 mV
6	350 mV
7	400 mV

The ability to release the low-side MOSFETS reduces the under shoot of the output voltage during recovery from an OVP condition (See comparison of Figure 35 and Figure 36). If the output voltage rises above the OVP threshold during recovery, the low side MOSFET's will again be turned on until Vout drops below the release threshold level.

Note: Note that OVP is disabled during a DVID-down event to prevent false triggering.

Additionally, the OVP can be configured to have the Fixed OVP threshold enabled all the time while disabling the Relative OVP Threshold. Figure 37 and Figure 38 show the comparison between the two modes of OVP operation.

The OVP response can be configured to shut down and latch off or ignore through the VOUT_OV_FAULT_RESPONSE PMBus command.

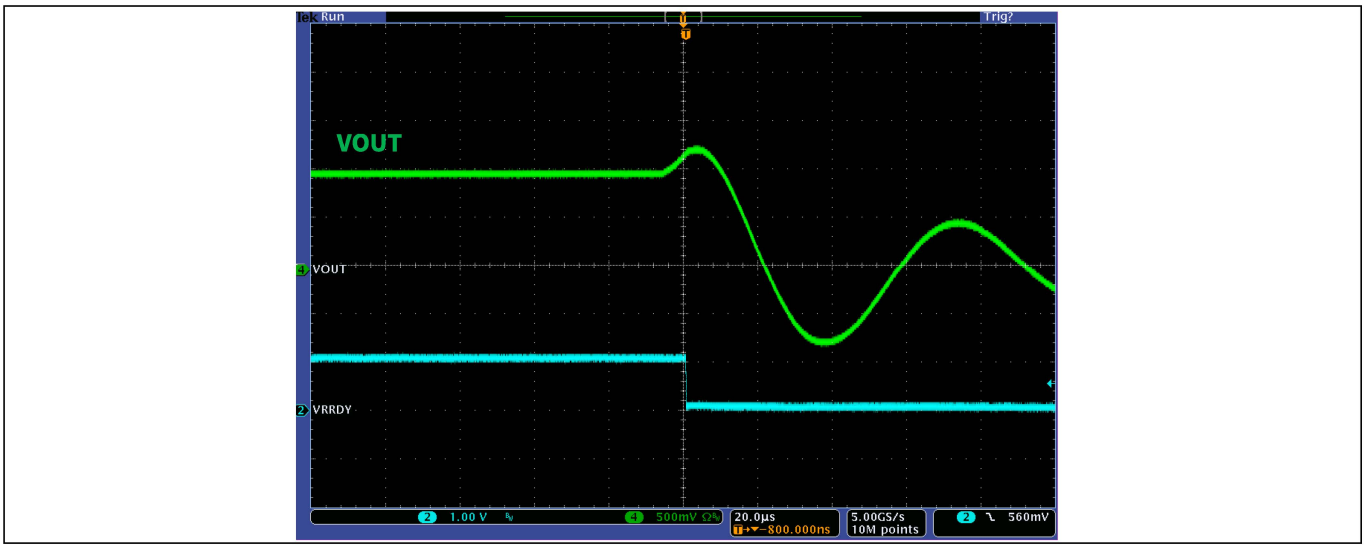

Figure 35 OVP – MOSFET Latched ON

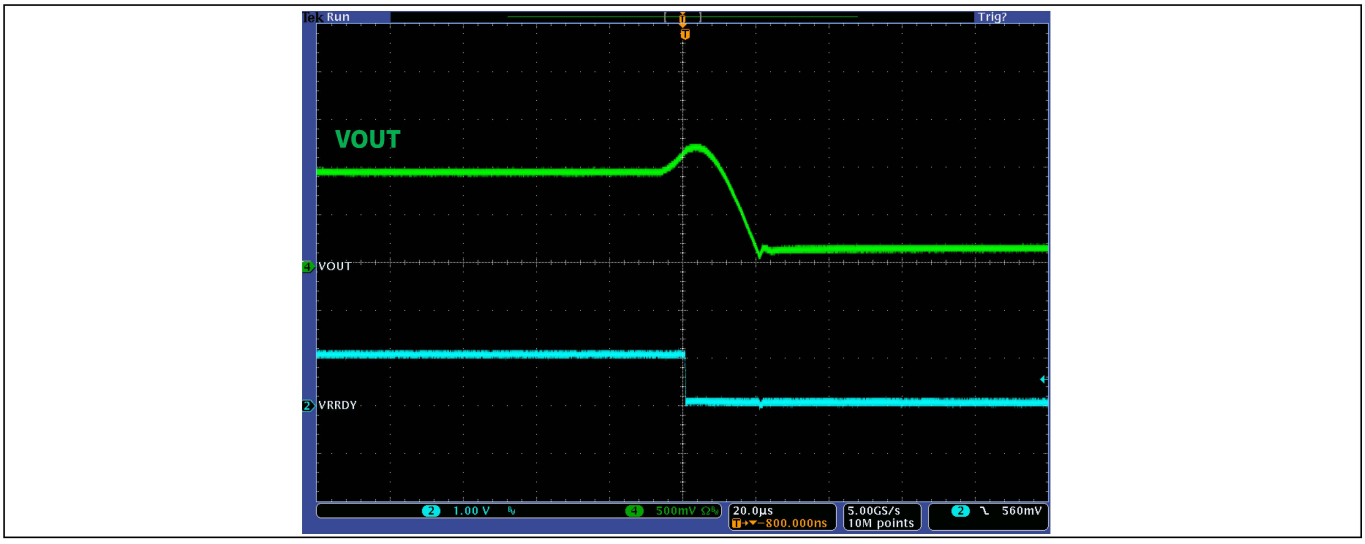

Figure 36 OVP – MOSFET Released when Output < 248 mV

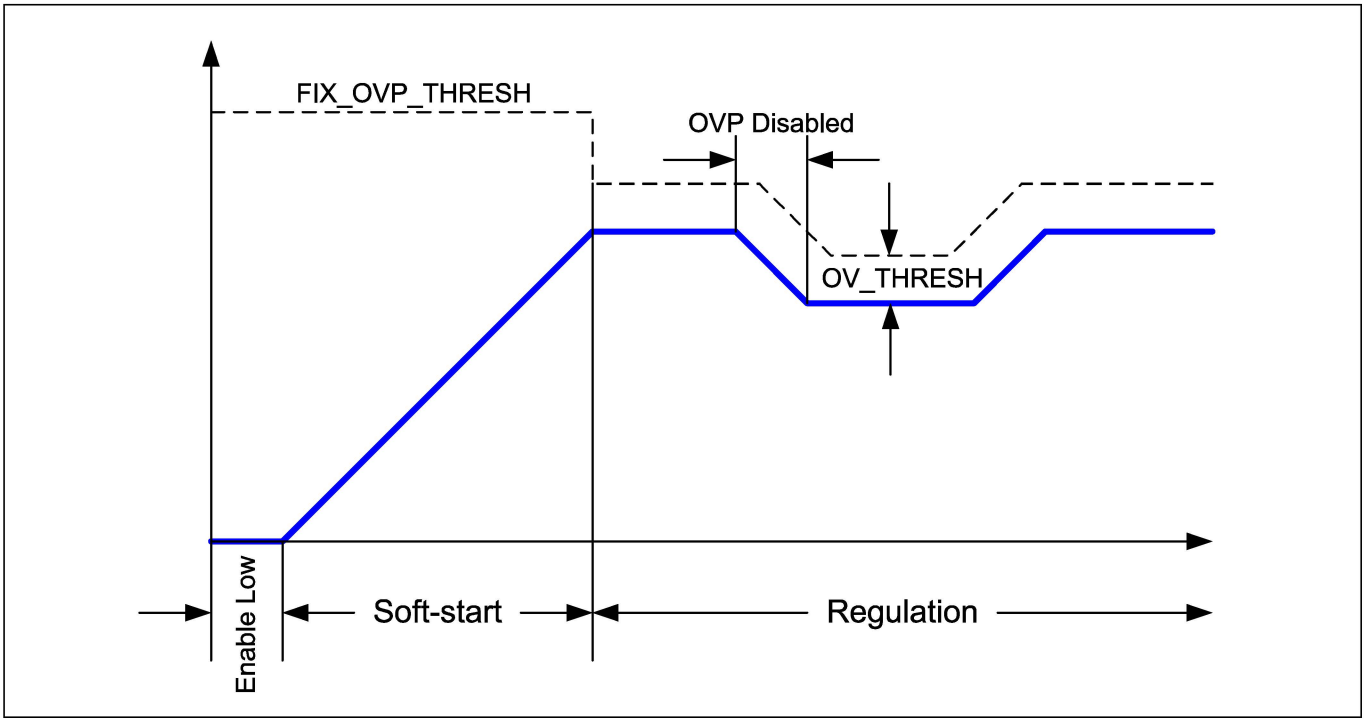

Figure 37 Mode of Operation with Fixed to Relative OVP Hand-off

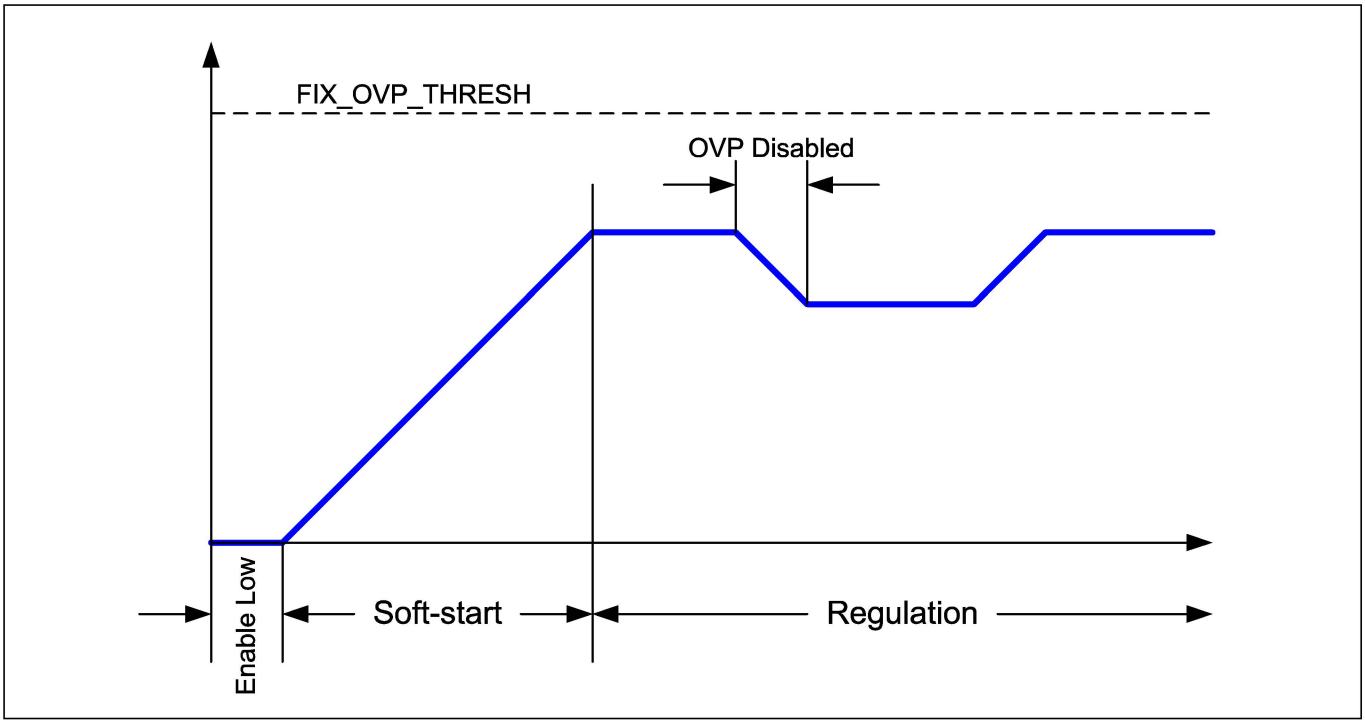

Figure 38 Mode of Operation with Fixed OVP always enabled.

9.2 Output Under-voltage Protection (UVP)

The XDPE132G5D detects an output under-voltage condition if the sensed voltage is below the user-programmable Relative UVP Threshold shown in 0 or below a fixed 248 mV if ADC detection is used instead of comparator detection. The relative thresholds will only be enabled if comparator detection is enabled. The UVP mode of operation is shown in Figure 39. UVP can be disabled by setting VOUT_UV_FAULT_RESPONSE to ignore.

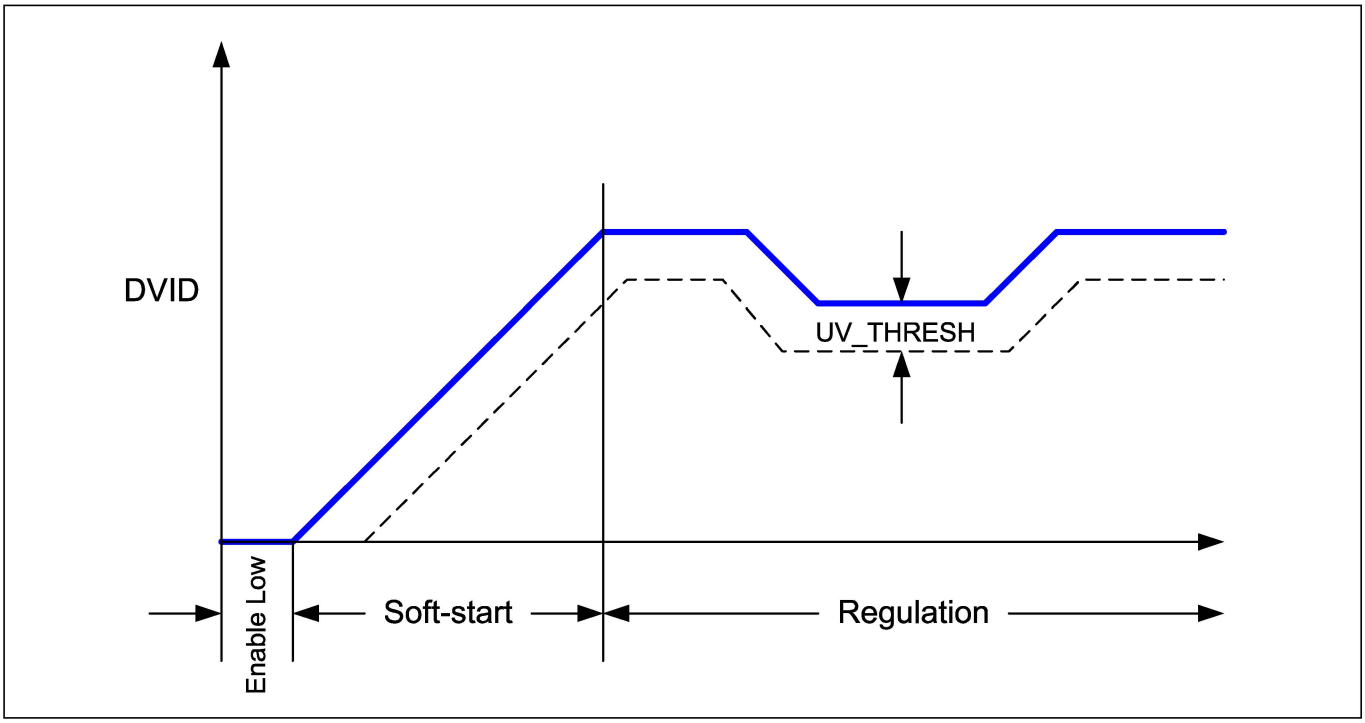

Figure 39 UVP Mode of Operation

9.3 Output Over-current Protection (OCP)

The XDPE132G5D provides a programmable output over-current protection threshold of up to 1022 A (510 A for loop2) through the IOUT_OC_FAULT_LIMIT setting, and the action that the controller can take when an OC condition is detected is set through the IOUT_OC_FAULT_RESPONSE command (Table 20).

Note: Note that the OCP protection is disabled during start up and during VOUT UP transitions.

Table 20 OCP Fault Response

IOUT_OC_FAULT_RESPONSE	OCP Behavior
0xC0	Shutdown Immediately
0xF8	Hiccup Forever
0xF0	Hiccup 6 times then shutdown

9.4 Phase over-current Protection

The XDPE132G5D provides a programmable phase over-current protection. When a phase current exceeds this threshold, the controller will truncate that PWM pulse instantaneously thereby preventing it from exceeding the programmed current setting. The threshold is programmable from 0 to 127 A at 0.5 A resolution. This protection greatly improves the system reliability by preventing excessive current in a phase due to inductor saturation or any power stage related failure.

9.5 Over-temperature Protection (OTP)

The XDPE132G5D measures the VR temperature via the TSENx pin. This temperature information is used for over-temperature protection shutdown, VR_HOT flag assertion, and temperature telemetry monitoring. The temperature is measured with the power stage temperature output pin (TOUT). The thresholds are programmable in 1 °C increments within the range shown in Table 21.

Table 21 OT Warning and Fault Threshold Range

Function	Range
OT Warning (VRHOT#)	64 °C to 255 °C
OT Fault	64 °C to 255 °C

9.5.1 OT Fault Response

The OT Fault threshold is set through the OT_FAULT_LIMIT and the response can be configured to one of the three settings shown in Table 22 through the OT_FAULT_RESPONSE.

Table 22 OT Fault Responses

OT_FAULT_RESPONSE	Response
0x00	Ignore
0x80	Shutdown and latch off
0xC0	Shutdown and restart when temperature goes below threshold

If the shutdown and latch off response is set, the XDPE132G5D will latch off the VR, requiring a system power recycle or an ENABLE recycle to resume operation.

9.5.2 OT Warning (VRHOT#)

The OT Warning threshold is set through the OT_WARN_LIMIT. When the temperature monitored on either TSEN1 or TSEN2 exceeds the threshold, the VRHOT# pin is asserted (Active-low). It will remain asserted until the temperature drops below 95% of the set threshold.

9.5.3 OptiMOS™ Power Stage Temperature Sensing (TOUT)

The controller is designed to interface directly with the OptiMOS™ Power Stage to receive temperature and fault information via the TSENx pin (Figure 40). The power stage temperature output is scaled to 8 mV/°C (0 °C=0.6 V) and it can be directly connected to the TSENx pin of the controller with just a decoupling capacitor near the controller's TSENx pin. Any fault within the Power Stage is communicated by pulling its temperature sense output (TOUT pin) to 3.3 V. 3.3 V on the TOUT pin indicates one of the following has occurred in the Power Stage:

1) An OptiMOS™ Power Stage phase fault

2) An OptiMOS™ Power Stage over-temperature fault

3) A persistent OptiMOS™ Power Stage over-current fault

4) An OptiMOS™ Power Stage over-voltage condition

The controller can be configured to shut down and latch off, shut down and auto restart (if the TOUT pin fault clears, or continue operating and assert the SMB_ALERT# pin upon receiving the TOUT pin fault.

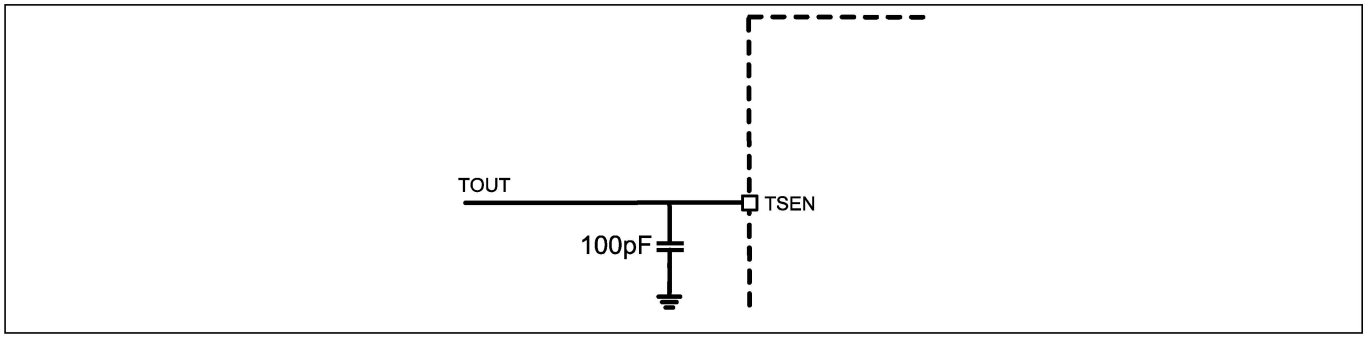

Figure 40 Temperature Sensing using TOUT

9.6 Fast OCP and Peak Current Control (PCC) Function

The XDPE132G5D can detect and flag an output over-current condition in less than 1 µs using the PCC pins (IOUT_WARN#x pins). The threshold is user selectable between 10 A and 1022 A. The typical setpoint accuracy is +/- 5% with IFX power stage R_{DS}on Isense . The alert assertion time is based on a comparator looking directly at the summed inductor current so all internal filtering is bypassed. The maximum delay from the time the summed inductor current exceeds the user set threshold to the time the PCC pin (IOUT_WARN#x pin) asserts is 4 µs.

Table 23 IOUT_WARN#x Pin Mode Selection

Warnx_src_sel	Flag Source
0	IOUT_OC_WARN loop1
1	IOUT_OC_WARN loop2
2	IOUT_OC_WARN loop1 or 2

Warnx_src_sel	Flag Source
3	PIN_OP_WARN

Table 24 FAST OCP and IOUT_WARN#x OC FLAG Pin Functionality

Register Name	Register Function
warnx_assert_duration	Sets the de-assertion delay after IOUT drops below the warning hysteresis. Range is 0 µS to 327 ms
Package_config	Used to assign IOUT_WARNx function to IO pin
Warnx_src_sel	Source assignment for IOUT_WARNx pin assertion
Loadline_bw	IOUT_WARNx pin assertion delay control
PMBUS command IOUT_OC_FAULT_LIMIT	Sets the IOUT level that will cause OCP. 2 A/LSB, 1022 A range(510 A for loop2)
PMBUS command IOUT_OC_WARN_LIMIT	Sets the IOUT level that will cause IOUT_WARN#x to assert. 2 A/LSB, 1022 A range, (510 A range for loop2)
iout_oc_fault_resp_delay	Sets the delay from IOUT crossing the OCP limit to VR shutdown. 5 µs/LSB, 0 to 155 µs range. This delay is added to the delay caused by the 60 kHz OCP filter

9.7 Input Over-voltage Protection

The XDPE132G5D offers protection against input supply over-voltage. When enabled, the VINSEN pin is compared to the programmed VIN_OV_FAULT_LIMIT and shuts down the IC if the threshold is exceeded. This fault can be disabled by setting the VIN_OV_FAULT_RESPONSE to ignore.

9.8 Phase Fault High and Low Detection

The XDPE132G5D can detect and declare a phase fault when the current in one or more phases is too high or too low. It detects the fault when the duty cycle adjustment register of a particular phase saturates at its minimum or maximum value. This feature helps detect severe imbalances in the phase currents, an unpowered or damaged MOSFET driver, or a phase that is disconnected from Vin. The phase fault feature can be enabled or disabled through an MTP bit. When a phase fault occurs, the controller shuts down the loop where the fault occurred, and sets register bits to display which phase had the fault and whether it faulted high or low. The phase fault registers are cleared via a register bit and the VR will restart once VR_EN or Vcc is cycled.

Table 25 Phase Fault Registers

Register Name	Register Description
Pi_fault_enable	Enables phase fault detection.
Clear_phase_fault	Clears all phase faults for each loop.
Phase_fault	High bit Indicates which phase has a phase current fault. 0 – phase1, 1 – phase2, 2 – phase3…15 – phase16

10 Telemetry Monitoring Functions

XDPE132G5D can provide real-time accurate measurement of input voltage, input current, output voltage, output current, phase current, and temperature. The XDPE132G5D provides this information over the I2C/PMBus interface. Some PMBus telemetry information associated to a particular control loop, such as READ_VOUT, READ_IIN, READ_POUT, and READ_PIN are calculated values, while other telemetry is directly measured and is common to both loops.

10.1 Real-time Telemetry

Table 26 shows the list of telemetry information with their associated update rates, filter bandwidths, and range and resolution.

Table 26 Telemetry

Parameter	Register	Sensing/ Estimation	Sampling Rate	Filter Bandwidth	Range	Resolution
Input voltage	READ_VIN	VINSEN pin	100 kHz	TEL_BW1	0 - 31.968 V	1/32 V
Input current	READ_IIN	Internally calculated (Iout x DC)	12 MHz	2 kHz	L1: 0 – 63.938 A L2: 0 – 31.968 A	L1: 1/16 A L2: 1/32 A
Output Voltage (Calculated)	READ_VOUT	VID – Iout x VOUT_DROOP	48 MHz (VID) 12 MHz (Iout)	LL_BW2 or 233 Hz	0 V to VOUT_MAX	VOUT_MODE
Phase Current	px_filt_i	ISENx pin	12 MHz	7.5 kHz	-19 A to +79 A	1 A
Total Output Current	READ_IOUT	Σ ISENx	12 MHz	TEL_BW1	L1: 0 A – 511.5 A or 0 A - 1023 A L2: 0 A – 511.5 A	L1: 0.5 A or 0.1 A L2: 0.5 A
Temperature	READ_ TEMPERATURE_x	TSEN1/2	100 kHz	4.6 kHz	-256 to 255 °C	1 °C
Auxiliary voltage	MFR_READ_VAUX or vaux_supply	VAUXSEN pin	100 kHz	4.6 kHz	0 – 7.992 V	VOUT_MODE or 1/128 V (I2C)
Input Power (Loop)	READ_PIN	Internally calculated (Vin x Iout x DC)	12 MHz	2 kHz	0 – 1023 W	1 W
Total Input Power	total_input_power	(IIN loop1+ IIN loop2) x VINSEN	269 kHz/ 38.5 kHz	4.6 kHz	0 – 1023 W	1 W
Output Power (Loop)	READ_POUT	Internally calculated	12 MHz	2 kHz	0 – 1023 W	1 W

Parameter	Register	Sensing/ Estimation	Sampling Rate	Filter Bandwidth	Range	Resolution
		(Vout x Iout)				

Note: 1) telemetry_bw is programmable: 2.1 Hz, 4.2 Hz, 8.4 Hz, 16.8 Hz, 33.6 Hz, 67.4 Hz, 134.7 Hz, 269.5 Hz

Note: 2) Loadline_BW is programmable: 30 kHz to 1 MHz in 30 kHz increments.

10.2 Min/Max Telemetry

Min/Max registers for IOUT, VOUT, VIN, and TEMPERATURE are available as shown in Table 27. The data is read through PMBus MFR READ registers. These registers store high and low values from startup or the last read, whichever was the latest to occur. The registers are automatically cleared when the data is read.

Table 27 Min/Max Registers

Parameter	Filter Bandwidth	Range	Resolution
VIN	TEL_BW1	0 - 31.968 V	1/32 V
VOUT	60 kHz	0 V to VOUT_MAX	VOUT_MODE
IOUT	60 kHz	L1: 0 A – 511.5 A or 0 A - 1023 A L2: 0 A – 511.5 A	L1: 0.5 A or 1 A L2: 0.5 A
Temperature	4.6 kHz	-256 °C to 255 °C	1 °C

10.3 Accuracy Optimization Registers

The XDPE132G5D provides excellent factory-trimmed chip accuracy. In addition, the designer has calibration capability that can be used to optimize reporting accuracy for a given design, with minimum component changes. Once a design is optimized, the XDPE132G5D provides excellent repeatability from board to board. The XDPE132G5D also provides capability for individual board calibration and programming in production for best accuracy. Table 28 shows the MTP registers used to fine tune the accuracy of the reported measurements. Figure 41 and Figure 42 show the typical accuracy of the output current and input voltage measurements using the XDPE132G5D.

Table 28 Accuracy Optimization Registers

NVM Register	Function
IIN Fixed Offset	Offsets the input current in 1/32 A steps.
IIN Per Phase Offset	Offsets the input current dependent on the number of active phases in 1/128 A steps, e.g. the drive current for the MOSFETs. This current increases every time a new phase is added.
Duty Cycle Adjust	Adjusts the input current calculation to compensate for a non-ideal driver.
Phase Current Offset	Offsets individual phase current from -8 A to +7.75 A in 0.25 A steps
Phase Current Gain	Adjust the individual phase current gain from -32/128 to +31/128 in 1/128 steps. Adjusted gain is 5 mV/A * (1 + IOUT Current Gain)
IOUT Current Offset	Offsets the total output current from -16 A to +15.75 A in 0.25 A steps
IOUT Current Gain	Adjust the total output current gain from -32/128 to +31/128 in 1/128 steps. Adjusted gain is 5 mV/A * (1 + IOUT Current Gain)
Vout Offset	Offsets the output voltage +40 mV to -35 mV in 5 mV steps
Temperature Offset	Offsets the temperature -32 °C to +31 °C in 1 °C steps to compensate for offset between the hottest component and power stage.

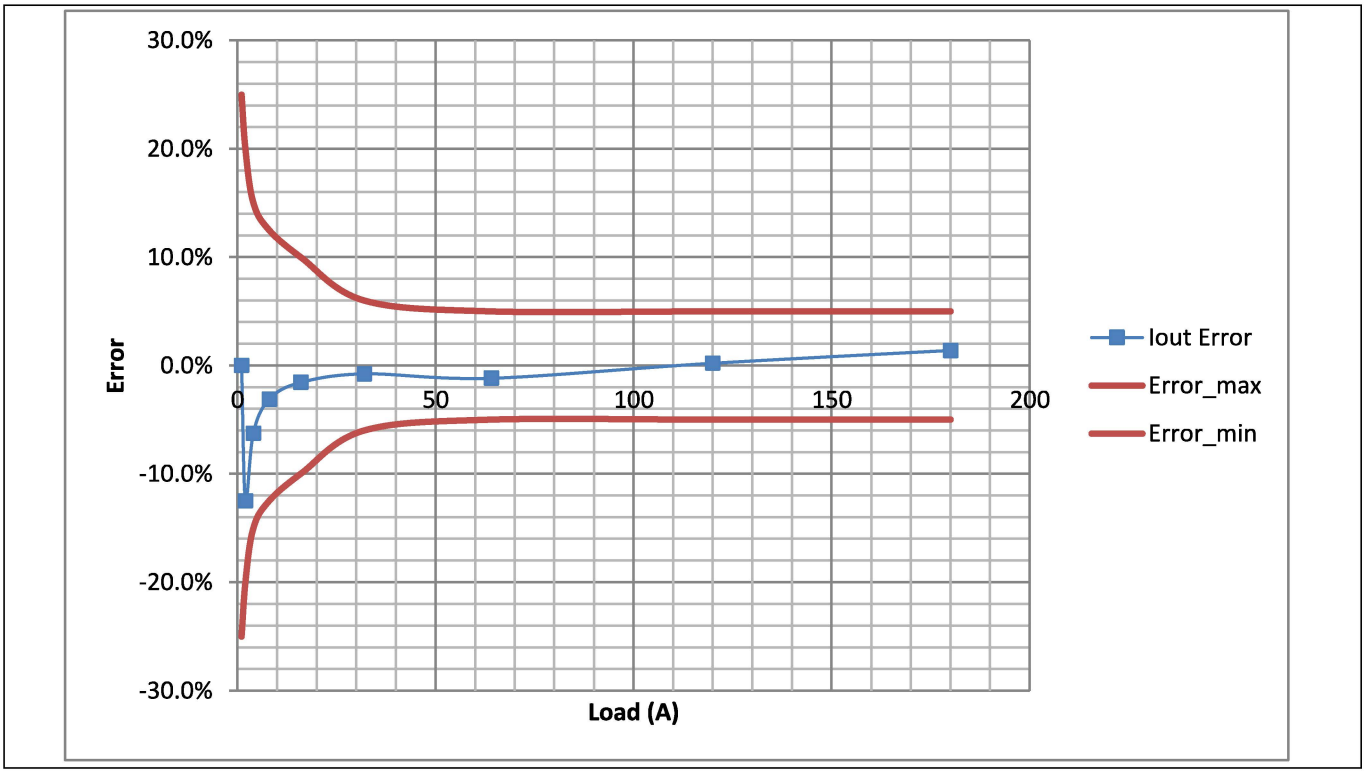

Figure 41 IOUT Error using Power Stage Iout

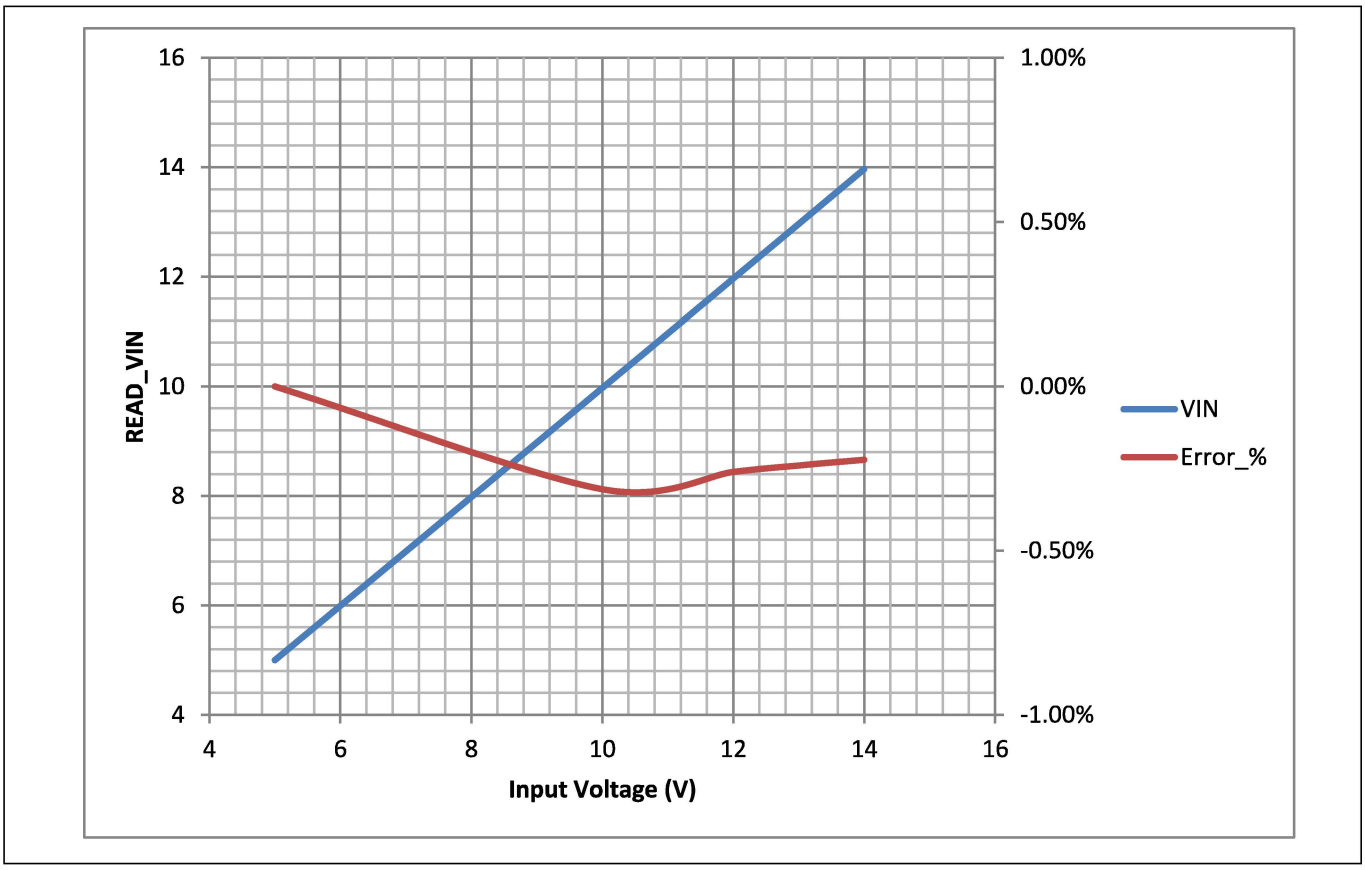

Figure 42 Input Voltage Measurement

11 AVSBus

11.1 Interface

The XDPE132G5D implements a fully compliant AVSBus interface. This is typically a three-wire interface (Figure 42) between a processor and a VR that consists of clock, master data and slave data signals. The XDPE132G5D implements all the required AVSBus commands per PMBus Rev 1.3 Part III. A list of supported commands is shown in Table 32.

Alternatively, a 2-wire interface (Figure 44) can be implemented making the slave data signal optional. This renders the system incapable of sending data back to the master, but may be useful in simplifying the bus interface.

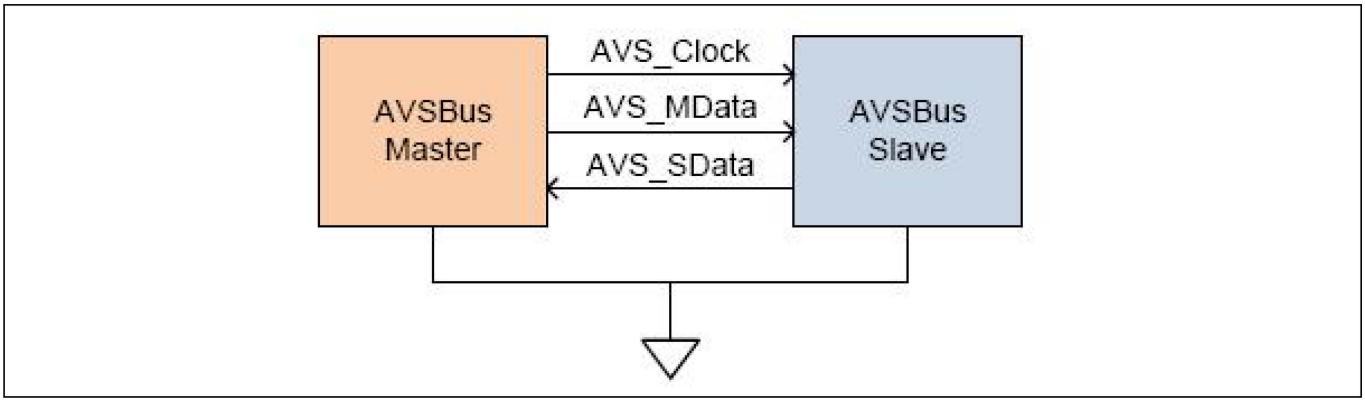

Figure 43 AVSBus 3-wire Interface

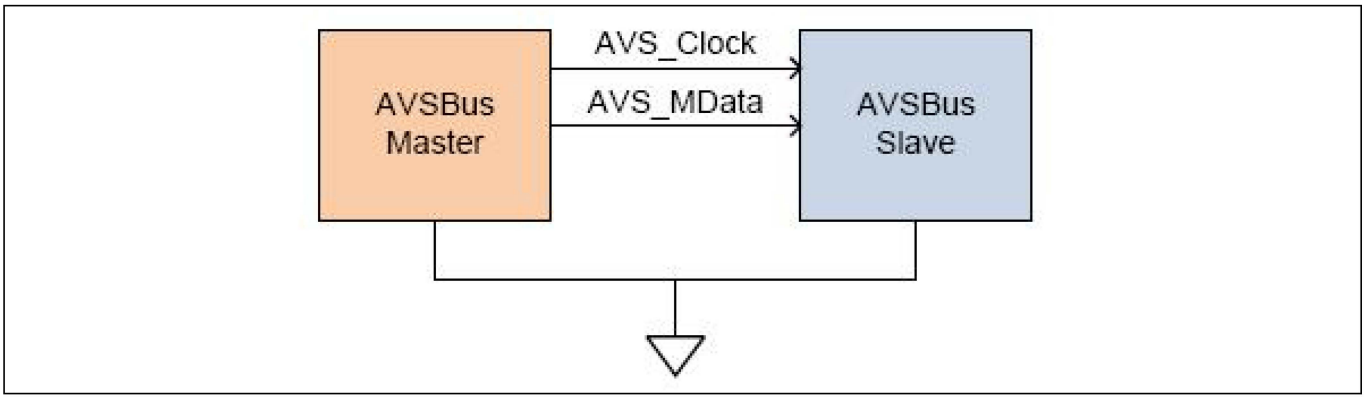

Figure 44 AVSBus 2-wire Interface

11.2 Operation

The interface operation consists of complementary functions in the master and the slave devices. The AVSBus Master must initiate all data transfers and it must guarantee that AVS_MData is held at a logic value ‘1’ when the clock is not running. This must occur during initialization prior to any bus transfers, as well as during idling between frames. AVS_MData is not allowed to be at a logic value ‘0’ when the clock starts.

The AVSBus Slave listens for and may respond to master commands but cannot initiate a transfer under any circumstances. In general, the slave must guarantee that AVS_SData is held at a logic value ‘1’ when the clock is not running. This must occur during initialization prior to any bus transfers, between frames, as well as at any time during a transfer when the slave is not sending data to the master. An exception to this rule is that the

AVSBus

AVSBus Slave will set AVS_SData to a logic value '0' when it needs to alert the AVSBus Master to start a frame so that it can send a "Status Response Frame"

The XDPE132G5D implements mechanisms that allow recovery of the bus in case noise or some other artifact causes the bus to enter an incorrect state. One mechanism is slave resynchronization. After receiving 34 clocks while the AVS_MData is held high, the device will resynchronize its bus interface and wait for the next start code. The second mechanism is a Bus Timeout. When the device determines that an ongoing transfer has been effectively aborted because the clock stopped running for a user programmable amount of time (Timeout), the device will reset the bus interface and again wait for the next start code.

11.3 Electrical Drive Levels and Filtering

The XDPE132G5D will accept Clock and Data signals from the Master driven to the VDDIO level, and will also provide its Data to the master, also driven to the VDDIO level. This is shown in Figure 45. The device also provides the ability to turn on some weak pull-ups (~50 kΩ) so that all three lines are in a known state before the bus is initialized.

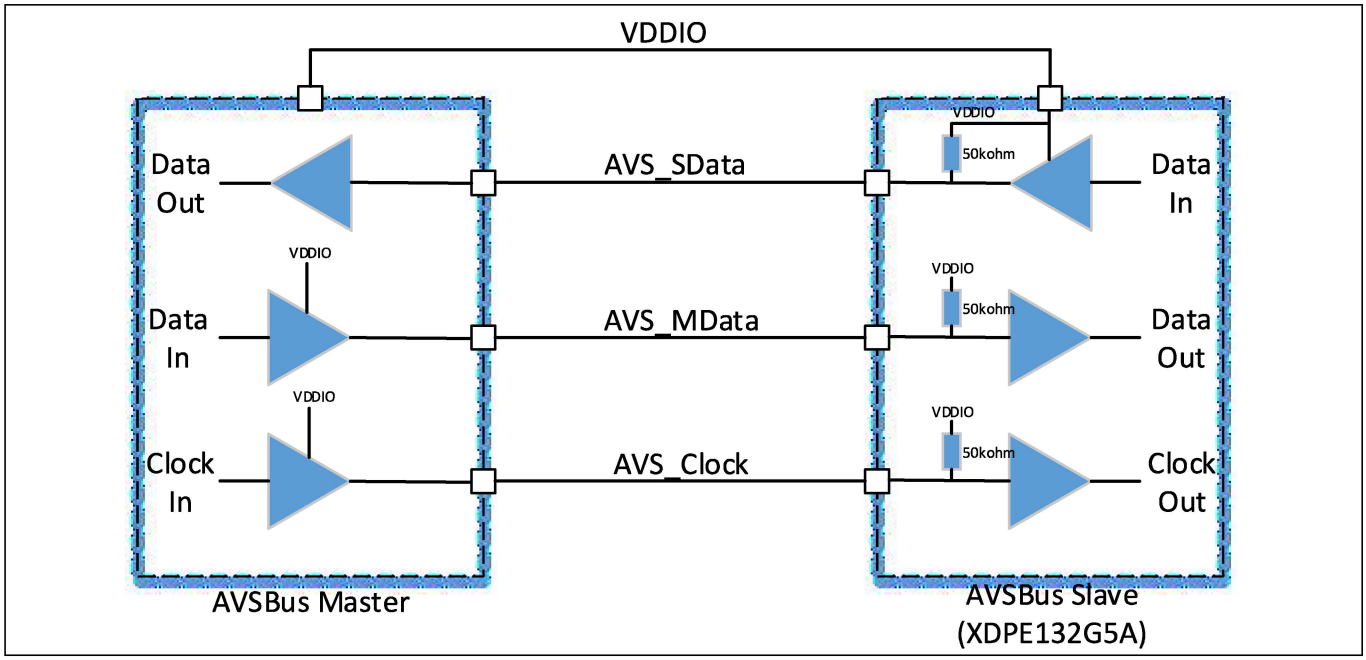

Figure 45 Electrical Interface

The XDPE132G5D has programmable threshold levels for the incoming Clock and Master Data lines. The levels are set per Table 29, and are typically set in accordance to the VDDIO voltage level being used.

Table 29 Clock and Data Threshold Levels

Setting	Vih, Vil	Nominal VDDIO
0	0.55 V, 0.45 V	1 V
1	0.65 V, 0.55 V	1.2 V
2	0.80 V, 0.70 V	1.5 V
3	0.90 V, 0.80 V	1.8 V

In addition to programmable threshold levels, the XDPE132G5D incorporates analog filtering of the clock and data, and programmable digital filters and delays (Table 30). These Digital Bus Utilities are used to help with noisy bus issues and to make the bus more robust within the system environment.

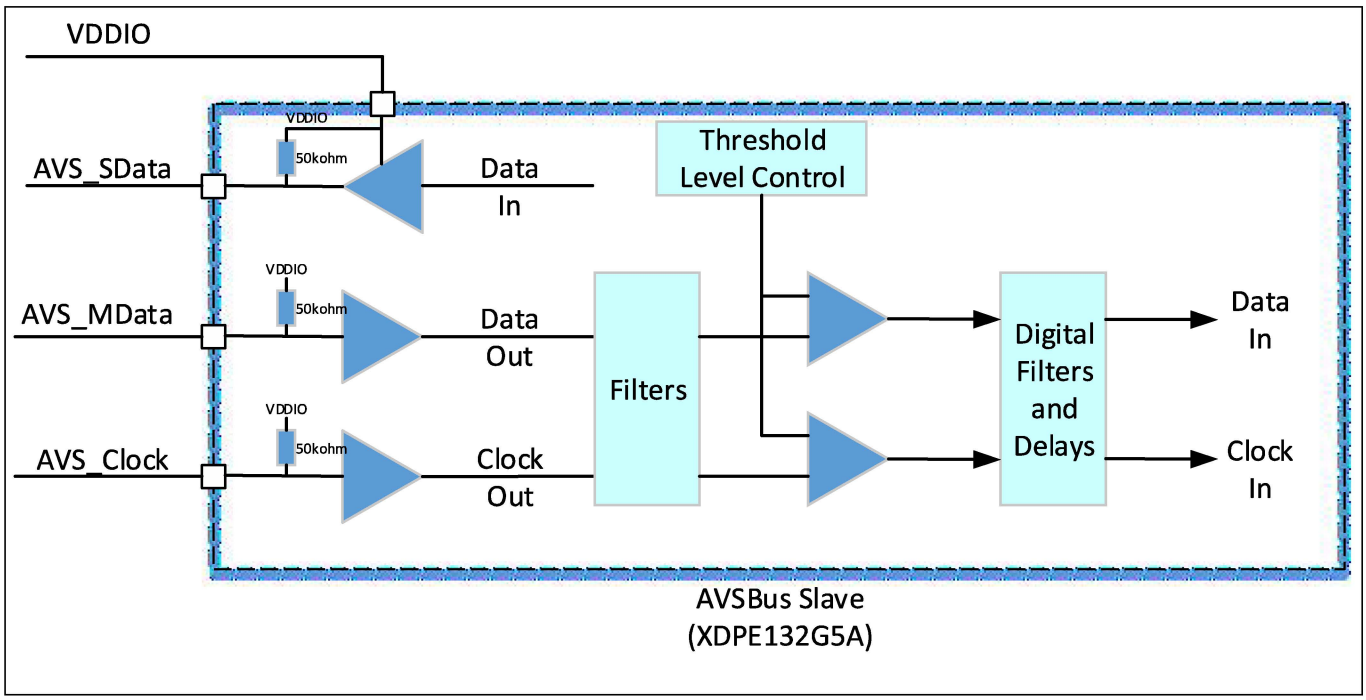

Figure 46 Threshold Control, Filters, and Digital Bus Utilities

Table 30 Bus Utilities

Utility	Description
MData to Clock Delay Enable	Enables the Glitch Filter Delay
Glitch Eater Delay	Blocked pulse width on both Mdata and Clock
Clock Delay Skew	Added delay to clock before it enters the core interface.
RC Filter	RC Filter setting for both MData and Clock

11.4 AVSBus Telemetry Filters

The AVSBus interface can read telemetry information for Output Current and Temperature. Each of the telemetry information data streams has a specific digital filter associated with it. Temperature has a fixed 4.6 kHz digital filter. Output Current has a programmable digital filter whose settings are shown in Table 31.

Table 31 Output Current Digital Filter

Setting	Filter
0	2 KHz
1	5 KHz
2	7.5 KHz
3	60 KHz

11.5 AVSBus Status Alert Mask

The XDPE132G5D Slave will alert the Master that its status has changed by asserting the AVS_SDATA low. This will happen when the following Warnings or Fault bits are set.

- OCW = Output Over-current Warning (STATUS_IOUT, bit 5)
- UVW = Output Under-voltage Warning (STATUS_VOUT, bit 5)
- OTW = Over-temperature Warning (STATUS_TEMP, bit 6)
- OPW = Output Over-power Warning (STATUS_IOUT, bit 0)
- Faults or Warnings in MFR_SPECIFIC (STATUS_MFR_SPECIFIC, bits 7:0)

The XDPE132G5D has a Mask Register that can mask any or all chosen warnings or faults listed above. Setting the associated bit to a '1' will mask that warning or fault from asserting the AVS_SDATA low. The Status Alert and specific warning bits will still be set and can be seen when an AVS Status Read command is performed.

11.6 AVSBus Command Group

Table 32 AVSBus Command Group 0b

Data Types	Command Name	Transaction Type	Range/Resolution	Description
0000b	Voltage	Read/Write	16-bit unsigned integer field with 1 LSB = 1 mV	This type allows the AVSBus Master to read or write a new voltage target for a rail on an AVSBus Slave.
0001b	Vout Transition Rate	Read/Write	8-bit unsigned integer field with 1 LSB = 1 mV/µs	This type allows the AVSBus Master to read or write a new transition rate for a rail on an AVSBus Slave.
0010b	Current	Read	16-bit unsigned integer field with 1 LSB = 10 mA	This type allows the AVSBus Master to read the current for a rail on an AVSBus Slave. Writes are not supported. Filtering can be set by PMBUS MFR_AVS_IOUT_BW
0011b	Temperature	Read	16-bit signed integer field with 1 LSB = 1 °C	This type allows the AVSBus Master to read the temperature for a rail on an AVSBus Slave. Writes are not supported.
0100b	Voltage Reset	Write	All 0's	This type allows the AVSBus Master to force a "Predetermined Value" for an AVSBus Slave rail, particularly while handling exceptions that could otherwise cause damage. The "Predetermined Value" is set by PMBus VOUT_COMMAND.
0101b	Power Mode	Read/Write	000b – 111b	This type allows the AVSBus Master to set the mode of operation for the output of an AVSBus Slave rail. The Power Mode settings are the same as the PMBus

AVSBus

Data Types	Command Name	Transaction Type	Range/Resolution	Description
				Power Mode descriptions.
0110b	Reserved for Future Use			
0111b	Reserved for Future Use			
1000b	Reserved for Future Use			
1001b	Reserved for Future Use			
1010b	Reserved for Future Use			
1011b	Reserved for Future Use			
1100b	Reserved for Future Use			
1101b	Reserved for Future Use			
1110b	AVSBus Status	Read/Write	<VDONE> <OCW> <UVW> <OTW> <OPW> <RSV_3> <MFR_SPEC_8>	This type allows the AVSBus Master to read the <AVSBus_Status> of an AVSBus Slave, or to clear the slave's <AVSBus_Status> by a write. When writing to this data type, all Status bits written with a 1(binary) are cleared. All others remain unchanged. Persistent faults will be immediately re-asserted. MFR_SPEC_8 = PMBus STATUS_MFR_SPECIFIC Register.
1111b	AVSBus Version	Read	0000b	This type allows the AVSBus Master to read the version of AVSBus implemented by an AVSBus Slave.

Note: AVSBus Command Group 1b is not defined for this device. It is reserved for future use.

11.7 AVSBus Addressing

The XDPE132G5D can control two loops with one device. This requires addressing control to differentiate between the two loops that use the same AVSBus interface. This is accomplished by address registers 0x3C [7:4] for Loop1 and 0x3C[3:0] for Loop2 that can be set to a value of 0 – 14 for each loop. Note that address 15 should not be used since this is the all call address on the AVSBus.

Table 33 AVS Address Registers

Register	Description	Value
0x3C[7:4]	AVSBus Address Loop1	0 to 14
0x3C[3:0]	AVSBus Address Loop2	0 to 14

12 AMD SVI2 Mode

12.1 Interface

The XDPE132G5D implements a fully compliant AMD SVI2 Serial VID interface (SVI). SVI2 is a three-wire interface between an SVI2 compliant processor and a VR. It consists of clock, data, and telemetry/alert signals. The processor will send a data packet with the clock (SVC) and data (SVD) lines. This packet has SVI commands to change VID, go to a low power state, enable and configure telemetry, change load line slope and change VID offset. The VR, when configured to do so, will send telemetry to the processor. The telemetry data consists of either voltage only, or voltage and current, of each output rail (VDD, VDDNB). See Table 36 for the telemetry data selection. The telemetry line (SVT) is also used as an alert signal (VID On The Fly complete) to alert the processor when a positive going VID change is complete, or an offset or load line scale change has occurred.

Note: When operating the XDPE132G5D with only 1 output (single loop operation), in order to have correct operation of the VID On The Fly complete (VOTF Complete) signal; 1) the non-operating loop must be set to 'enabled', 2) the number of active phases must be set to 1, 3) the boot voltage register must be set to FEh (VID OFF), and 4) all loop2 fault responses must be set to 'ignore'

12.2 Operation

12.2.1 Boot Voltage

When the power-on sequence is initiated, both rails will ramp to the configured Vboot voltage and assert the PWRGD on each loop. The soft-start ramp time is the time programmed per loop with the TON_RISE PMbus command.The boot voltage is decoded from the SVC and SVD pin levels when the EN pin is asserted high as shown in Table 34. This value is latched and will be re-used in the event of a soft reset (de-assertion and re-assertion of PWROK).

Note: VDDIO must be stable for a minimum 0.2 ms before the IC is enabled to ensure that the boot voltage is decoded from the SVC and SVD pins correctly.

Table 34 AMD SVI Boot Table

Boot Voltage	SVC	SVD
1.1 V	0	0
1.0 V	0	1
0.9 V	1	0
0.8 V	1	1

Alternatively, the AMD boot voltage can be set by an MTP register instead of decoding the SVC and SVD pins as shown in Table 34. Boot values are shown in Table 35.

Table 35 Boot Voltage Location

MTP Boot Register	Boot Location
Bit [7] = low	Decode From SVC and SVD pins per Table 34
Bit [7] = high	Use MTP boot register bits [6:0]

12.2.2 PWROK De-assertion

The XDPE132G5D responds to SVI commands on the SVI bus interface when PWROK is high. In the event that PWROK is de-asserted, the controller resets the SVI state machine, drives the SVT pin high and returns to the Boot voltage, initial load line slope and offset.

Figure 47 PWROK De-assertion

12.2.3 PSI(x) and TFN

PSI0_L is Power State Indicator Level 0. When this bit is asserted the XDPE132G5D will drop to 1 phase. This will only occur if the output current is low enough (typically <20 A) to enter PSI0, else the VR will remain in full phase operation.

PSI1_L is Power State Indicator Level 1. When this bit is asserted along with the PSI0_L bit, the XDPE132G5D will enter diode emulation mode. This will only occur if the output current is low enough (typically <5 A) to enter PSI1, else the VR will enter PSI0_L mode of operation.

TFN is an active high signal that allows the processor to control the telemetry functionality of the VR. If TFN=1, then the VR telemetry will be configured per Table 36.

Table 36 TFN Truth Table

Telemetry	VDD Domain Bit	VDDNB Domain Bit
Telemetry is for output voltage only	0	0
Telemetry is output voltage and output current	0	1
Telemetry is Disabled	1	0
Reserved	1	1

12.2.4 SVT Telemetry

The XDPE132G5D has the ability to sample and report voltage and current for the VDD and VDDNB domains. The XDPE132G5D reports this telemetry serially over the SVT wire which is clocked by the processor-driven SVC. If in voltage only telemetry mode, then the sampled voltage for VDD and VDDNB are sent together in every SVT telemetry packet at a rate of 20 kHz. If in voltage and current mode, then the sampled voltage and current for VDD is sent out in one SVT telemetry packet followed by the sampled voltage and current for VDDNB in the next SVT telemetry packet at a rate of 40 kHz. If only 1 domain is active (if the controller is set for 1 loop operation), the voltage for the 'inactive' loop will be reported as 1F7h and the current will be reported as 00h. The voltage and current are moving averages based on the filters and update rates specified in Table 5. The voltage is reported as a function of the Set VID minus Iout times the Load Line Resistance. The current is reported as a percentage of the Icc_max register, where a value of FFh represents 100% and 00h represents 0% of the Icc_max setting. Resolution of the current reporting is 0.39% (1/256) of ICCMAX. ICCMAX can be set to a minimum value of 50 A (32h) and a maximum value of 1023 A (3FFh)

12.2.5 Load Line Slope Trim

The XDPE132G5D has the ability for the processor to change the load line slope of each loop independently through the SVI2 bus while ENABLE and PWROK are asserted via the serial VID interface. The slope change applies to initial load line slope as set by the VOUT_DROOP PMBUS command. The load line slope can be disabled or adjusted by -40%, -20%, 0%, +20%, +40%, +60%, or +80%.

12.2.6 Offset Trim

The XDPE132G5D has the ability for the processor to change the offset of each loop independently while ENABLE and PWROK are asserted via the serial VID interface. The offset can be left unchanged, disabled, or changed +25 mV or -25 mV.

12.2.7 Ispike/Dual OCP Support

The XDPE132G5D has two current limit thresholds. One threshold is for short duration current spikes (Fast OCP). When this threshold (typically a percentage above the peak processor current) is exceeded, the VR quickly shuts down. The other threshold (typically a percentage above the thermal design current (TDC)) is heavily filtered (Slow OCP) and shuts down the VR when the average current exceeds it. To meet AMD specifications, exceeding both thresholds will assert the OCP_L (VR_HOT) pin and delay the over-current shut-down by typical values of 10µs for FAST threshold and 20µs for the SLOW threshold. Figure 48 shows the delay action of the OCP shutdown with the OCP_L (VR_HOT) and PWRGD pins.

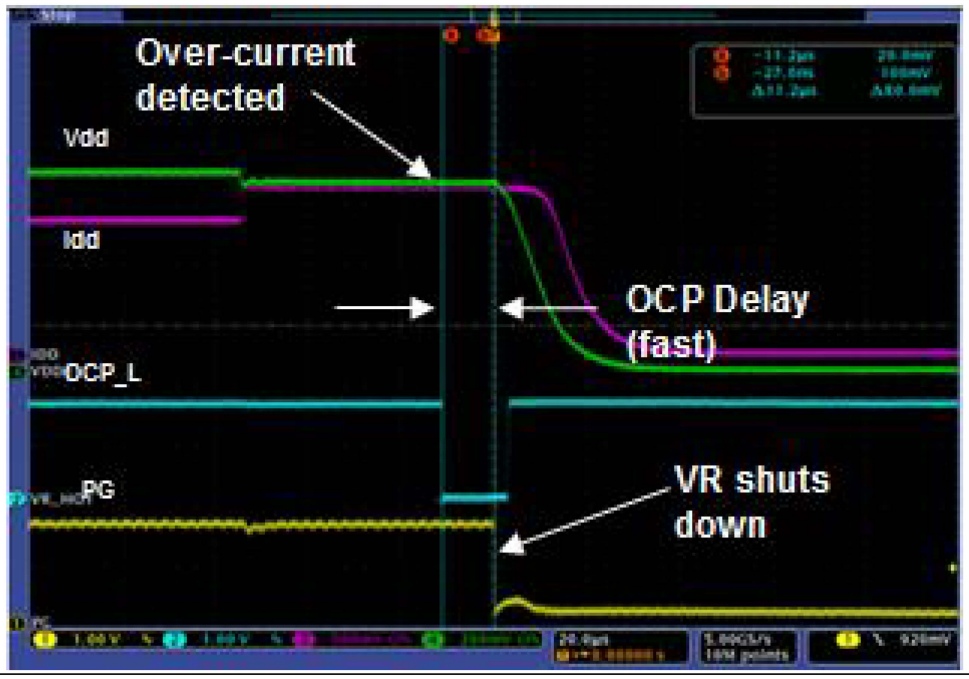

Figure 48 OCP_L (VR_HOT) assertion with OCP_spike (Fast) threshold. OCP delay action (11µs)

12.2.8 Thermal Based Protection

The XDPE132G5D can also assert the PROC_HOT_L (VR_HOT) pin when the temperature of the VR exceeds a configurable temp_max threshold (typically 100 °C). If the temperature continues to rise and exceeds a second configurable threshold (OTP_thresh), the VR will shut down and latch off. The VR can only be restarted if ENABLE or VCC is cycled.

12.2.9 VR_HOT/ICRIT# Pin Functionality Options

The functionality of the VR_HOT_ICRIT pin can be set to assert when levels of Temp_max, Icc_max, and/or OCP levels are exceeded. The list below shows the multiple configurations of the VR_HOT_ICRIT pin.

- VR_HOT temperature only
- VR_HOT temperature or ICRIT current threshold
- VR_HOT temperature or over-current protection threshold
- ICRIT current threshold

12.2.10 I_Critical Flag

The XDPE132G5D VR_HOT/ICRIT# pin can be programmed to assert when a user programmable output current level is exceeded. The assertion is not a fault, and the VR continues to regulate. I_CRIT monitors a long term averaged output current, which is a useful indicator of average operating current and thermal condition. The user can select the I_CRIT filter bandwidths in Table 37.

Table 37 ICRIT Filter Bandwidths

Register Value	Bandwidth (Hz)
0	2.1
1	4.2
2	8.4

Register Value	Bandwidth (Hz)
3	16.8
4	33.6
5	67.4
6	134.7
7	269.5

12.2.11 Peak Current Control (PCC)

The XDPE132G5D can be configured to detect and flag an output over-current condition in less than 4 µs using the IOUT_WARN#x pins. The PCC assertion threshold is user-selectable between 10 A and 1022 A (10 A and 510 A for loop2). The typical setpoint accuracy is +/- 5% when using IFX power stage RDSon Isense. The PCC assertion delay time is based on a comparator looking at the filtered inductor current not the load (output) current. The inductor current always lags the output current as shown in Figure 49. The filter band width can be set between 30 kHz and 1 MHz by the user. A low filter BW will add additional PCC assertion delay time to the delay time caused by the inductor current lag time. The recommended filter BW range is between 300 kHz and 390 kHz to give adequate filtering and not add additional delay. The maximum delay from the time the summed inductor current exceeds the user set threshold to the time the IOUT_WARN# (PCC) pin asserts is less than 1 µs . The PCC function can be assigned to IOUT_WARN#1 (pin 22) or IOUT_WARN#2 (pin21). The source of the PCC assertion is defined by the user and can be set to;

- Loop1 only or
- Loop2 only or
- Loop1 and loop2 (not logically 'ANDed' together; either loop1 or loop2 will assert one common PCC pin)

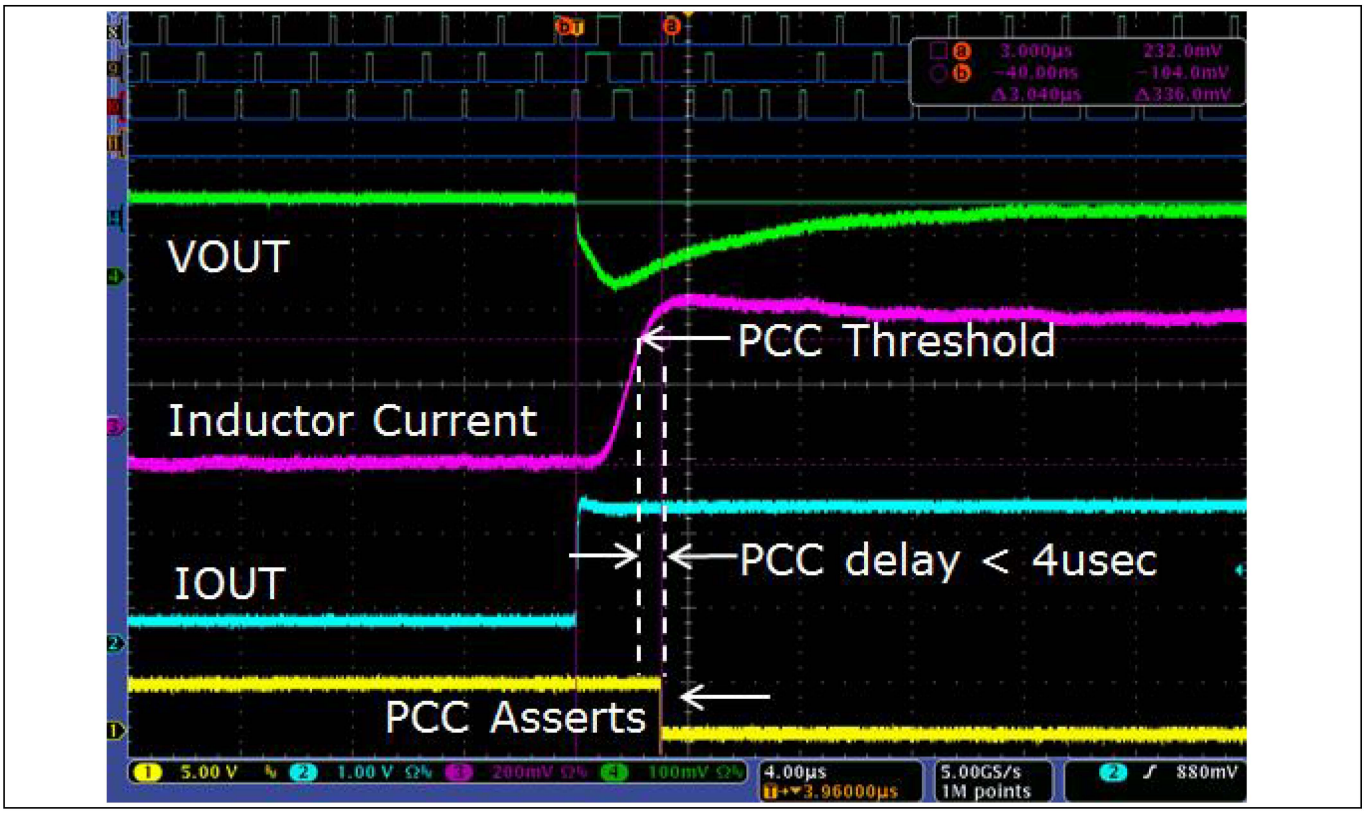

Figure 49 PCC assertion delay due to inductor current lag time

12.2.12 AMD SVI Address Programming

By default, loop 1 is addressed as the VDD rail and loop 2 is addressed as the VDDNB rail which is sufficient for most applications. The XDPE132G5D can also be configured with a single bit change to swap this addressing scheme so that loop 1 can be addressed as the VDDNB rail and loop 2 can be addressed as the VDD rail. This is for applications where the VDDNB rail requires more phases than the VDD rail.

12.2.13 VID Change

The XDPE132G5D accepts an 8-bit VID within the SVD packet and will change the output voltage at the VOUT_TRANSITION_RATE, specified per loop, of one or both of the loops based on the VID in Table 38. This is a VID-on-the-fly-request (VOTF Request). A VOTF request to 0V (VID OFF) will result in the loop transitioning to 0V and the PG pin for that loop remaining asserted as specified in AMD SVI2 specification Rev 1.08

Table 38 SVI2 VID Table

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
0	1.55000	32	1.23750	64	0.92500	96	0.61250	C8	0.30000
1	1.54375	33	1.23125	65	0.91875	97	0.60625	C9	0.29375
2	1.53750	34	1.22500	66	0.91250	98	0.60000	CA	0.28750
3	1.53125	35	1.21875	67	0.90625	99	0.59375	CB	0.28125
4	1.52500	36	1.21250	68	0.90000	9A	0.58750	CC	0.27500
5	1.51875	37	1.20625	69	0.89375	9B	0.58125	CD	0.26875
6	1.51250	38	1.20000	6A	0.88750	9C	0.57500	CE	0.26250
7	1.50625	39	1.19375	6B	0.88125	9D	0.56875	CF	0.25625
8	1.50000	3A	1.18750	6C	0.87500	9E	0.56250	D0	0.25000
9	1.49375	3B	1.18125	6D	0.86875	9F	0.55625	D1	0.24375
A	1.48750	3C	1.17500	6E	0.86250	A0	0.55000	D2	0.23750
B	1.48125	3D	1.16875	6F	0.85625	A1	0.54375	D3	0.23125
C	1.47500	3E	1.16250	70	0.85000	A2	0.53750	D4	0.22500
D	1.46875	3F	1.15625	71	0.84375	A3	0.53125	D5	0.21875
E	1.46250	40	1.15000	72	0.83750	A4	0.52500	D6	0.21250
F	1.45625	41	1.14375	73	0.83125	A5	0.51875	D7	0.20625
10	1.45000	42	1.13750	74	0.82500	A6	0.51250	D8	0.20000
11	1.44375	43	1.13125	75	0.81875	A7	0.50625	D9	0.19375
12	1.43750	44	1.12500	76	0.81250	A8	0.50000	DA	0.18750
13	1.43125	45	1.11875	77	0.80625	A9	0.49375	DB	0.18125
14	1.42500	46	1.11250	78	0.80000	AA	0.48750	DC	0.17500
15	1.41875	47	1.10625	79	0.79375	AB	0.48125	DD	0.16875
16	1.41250	48	1.10000	7A	0.78750	AC	0.47500	DE	0.16250
17	1.40625	49	1.09375	7B	0.78125	AD	0.46875	DF	0.15625
18	1.40000	4A	1.08750	7C	0.77500	AE	0.46250	E0	0.15000
19	1.39375	4B	1.08125	7D	0.76875	AF	0.45625	E1	0.14375
1A	1.38750	4C	1.07500	7E	0.76250	B0	0.45000	E2	0.13750
1B	1.38125	4D	1.06875	7F	0.75625	B1	0.44375	E3	0.13125
1C	1.37500	4E	1.06250	80	0.75000	B2	0.43750	E4	0.12500
1D	1.36875	4F	1.05625	81	0.74375	B3	0.43125	E5	0.11875
1E	1.36250	50	1.05000	82	0.73750	B4	0.42500	E6	0.11250
1F	1.35625	51	1.04375	83	0.73125	B5	0.41875	E7	0.10625
20	1.35000	52	1.03750	84	0.72500	B6	0.41250	E8	0.10000
21	1.34375	53	1.03125	85	0.71875	B7	0.40625	E9	0.09375
22	1.33750	54	1.02500	86	0.71250	B8	0.40000	EA	0.08750
23	1.33125	55	1.01875	87	0.70625	B9	0.39375	EB	0.08125
24	1.32500	56	1.01250	88	0.70000	BA	0.38750	EC	0.07500

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
25	1.31875	57	1.00625	89	0.69375	BB	0.38125	ED	0.06875
26	1.31250	58	1.00000	8A	0.68750	BC	0.37500	EE	0.06250
27	1.30625	59	0.99375	8B	0.68125	BD	0.36875	EF	0.05625
28	1.30000	5A	0.98750	8C	0.67500	BE	0.36250	F0	0.05000
29	1.29375	5B	0.98125	8D	0.66875	BF	0.35625	F1	0.04375
2A	1.28750	5C	0.97500	8E	0.66250	C0	0.35000	F2	0.03750
2B	1.28125	5D	0.96875	8F	0.65625	C1	0.34375	F3	0.03125
2C	1.27500	5E	0.96250	90	0.65000	C2	0.33750	F4	0.02500
2D	1.26875	5F	0.95625	91	0.64375	C3	0.33125	F5	0.01875
2E	1.26250	60	0.95000	92	0.63750	C4	0.32500	F6	0.01250
2F	1.25625	61	0.94375	93	0.63125	C5	0.31875	F7	0.00625
30	1.25000	62	0.93750	94	0.62500	C6	0.31250	F6-FF	OFF
31	1.24375	63	0.93125	95	0.61875	C7	0.30625		

Note: The minimum output voltage that can be programmed for the XDPE132G5D is 0.0125 V. VID code F7h is not supported. All VID codes from F7h to FFh sent in the SVD data packet are VID OFF commands and will be reported back in the SVT data packet as 1F7h

13 nVIDIA PWM VID Mode

13.1 Interface

The XDPE132G5D implements a fully compliant nVIDIA PWM-VID interface. PWM-VID is a single wire voltage interface between the nVIDIA GPU and VR. It is a control circuit allowing the output voltage to be dynamically controlled by the pulse width of the signal going into PWM_VID Input pin. The LSB resolution of the PWM VID interface can be configured by the user to be 5 mV or 10 mV. The interface also consist of a standby mode and a low performance mode . Standby mode keeps the GPU in a low voltage state for quick recovery. A logic high on the V_STANDBY pin activates standby mode. The L_PERF# pin controls the power state of the VR. A logic high indicates normal operation and a logic low indicates low performance operation.

13.2 Operation

When the power-on sequence is initiated, if VBOOT is set to greater than POWER_GOOD_ON, the output voltage will ramp to its configured boot voltage and assert PWRGOOD_Lx. The GPU can now drive the PWM_VID pin to change the output voltage in normal operation. When the PWM signal from PWM-VID is off, the output voltage falls back to its Vboot voltage. The VR will enter its standby output voltage when it receives a high signal from the Standby Mode pin and returns to the Vboot voltage when the signal goes low. The operation of nVIDIA PWM VID mode is shown in the timing diagram in Figure 50.

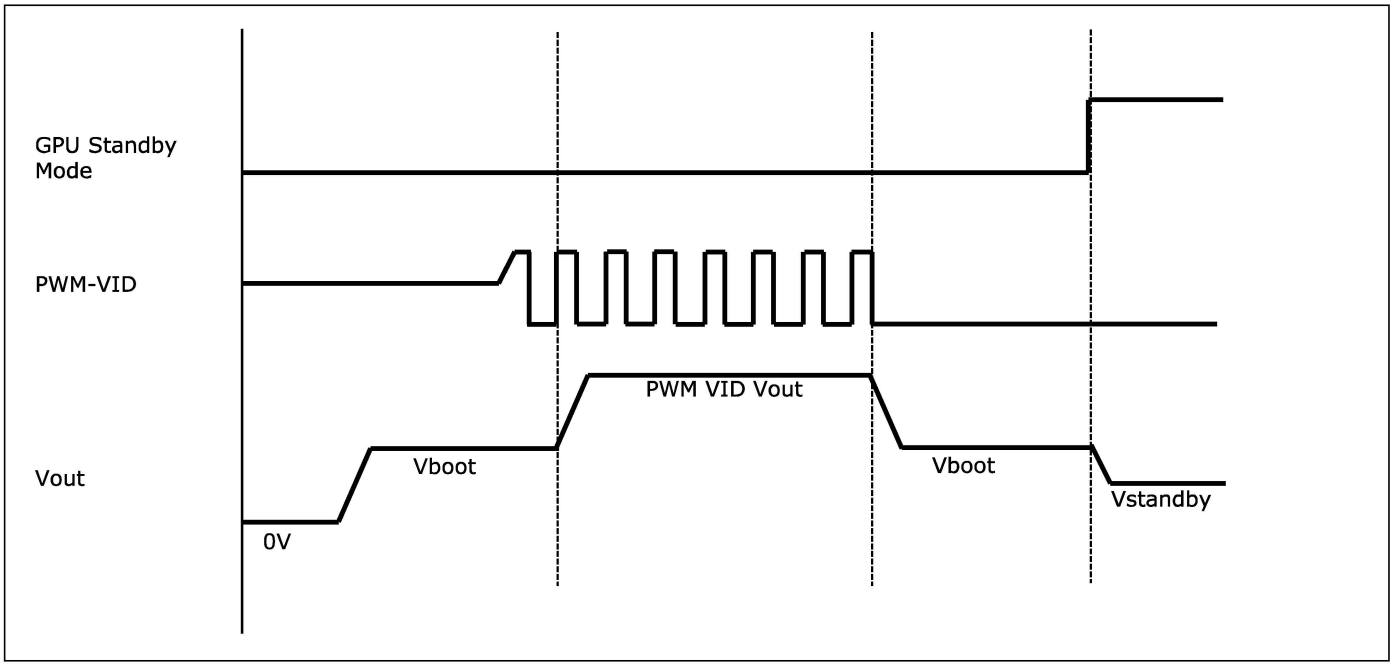

Figure 50 nVIDIA PWM VID Operation Timing Diagram

13.2.1 Boot Voltage

The Vboot voltage is an 8-bit value that can be configured in the I2C loop specific register, vboot. Vboot can range from 0 V to 1.275 V in 5 mV steps or from 0 V to 2.55 V in 10 mV steps. The VBOOT voltage is the output voltage the VR ramps to when power-on sequence is first initiated or when the PWM-VID signal goes to tri-state. The PWM-VID pin must go to a low state when the input from the GPU goes to high impedance. The resistor from the PWM-VID pin to ground is required. The recommended resistor value is 10 kΩ

13.2.2 PWM VID Change

The XDPE132G5D accepts a PWM signal that steps the output voltage based on the duty cycle of the signal. The operating VID can be increased from 0.6 V in 5 mV or 10 mV increments with a maximum of 127 increments. The output voltage in 5 mV VID resolution can range from 0.6 V to 1.235 V and in 10 mV VID resolution can range from 0.6 V to 1.87 V. Additional VID offset can be added to increase the maximum output voltage range

13.2.3 Low Performance Mode

The XDPE132G5D has an input pin that communicates to the controller that one or more of the auxiliary 12V supplies are not connected. This is the L_PERF# pin. When this pin is asserted low, the controller will be in low performance mode. The PWM outputs will be limited to PWM1 (and PWM2 if configured). The Vboot ramp time at start up will be eight times the programmed TON_RISE time. The VOUT transition time for a PWM VID change will be eight times slower than the programmed VOUT_TRANSITION_RATE. The over-current protection threshold will be the limit set in the psi_oc_fault register.

13.2.4 VID Min/Max & Standby

The XDPE132G5D has the ability to set the maximum and minimum output voltage that the controller cannot exceed when commanded by the PWM VID interface. The VID values for the 8-bit commands can range from 0 V to 1.275 V in 5 mV steps or from 0 V to 2.55 V in 10 mV steps.

13.2.5 Standby Voltage

The XDPE132G5D has an input pin that communicates to the controller that the output voltage must go to the user programmed standby voltage. The V_STANDBY pin must be pulled high for the controller to ramp to the standby voltage.

14 I2C/PMBus Communication

14.1 Addressing

The XDPE132G5D simultaneously supports I2C and PMBus through the use of exclusive addressing. By using a 7-bit address, the user can configure the device to any one of 127 different I2C/PMBus addresses. Once the address of the XDPE132G5D is set, it can be locked to protect it from being overridden. Optionally, a resistor can be tied to the SM_ADDR/PROG pin to generate an offset as shown in Table 39 (note that a 6.8 nF capacitor is required across the resistor per Figure 51).

As an example, setting a base 7-bit I2C address of 28h with a resistor offset of +15 sets the 7-bit I2C address to 37h. Similarly, setting a base 7-bit PMBus address of 40h with a resistor offset of +15 sets the 7-bit PMBus address to 4Fh.

For default programmed devices, the I2C/PMBus address can be temporarily forced to 0Ah for I2C and 0Dh for PMBus by driving the PROG pin high (3.3 V).

Table 39 PROG Resistor Offset

Resistor	I2C Address Offset
0.845 kΩ	+0
1.30 kΩ	+1
1.78 kΩ	+2
2.32 kΩ	+3
2.87 kΩ	+4
3.48 kΩ	+5
4.12 kΩ	+6
4.75 kΩ	+7
5.49 kΩ	+8
6.34 kΩ	+9
7.15 kΩ	+10
8.06 kΩ	+11
9.09 kΩ	+12
10.00 kΩ	+13
11.00 kΩ	+14
12.10 kΩ	+15

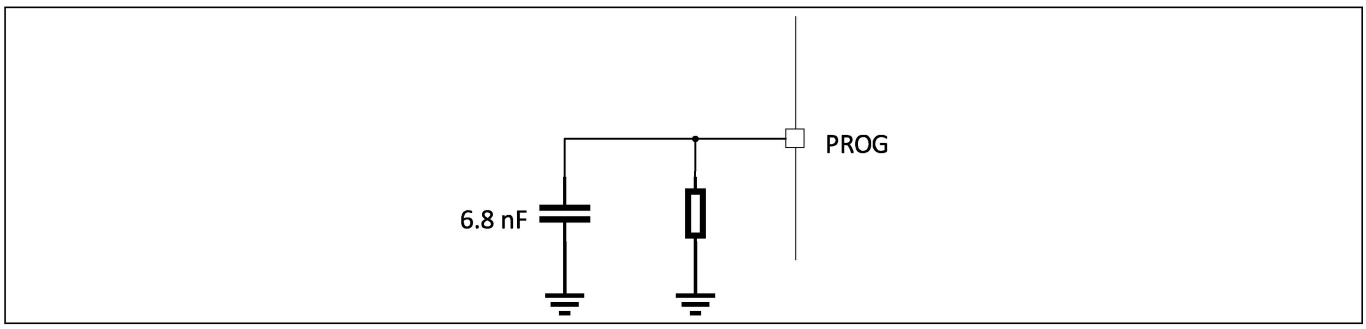

Figure 51 PROG Pin Components

14.2 I2C Security

The XDPE132G5D provides robust and flexible security options to meet a wide variety of customer applications. 16-bit software passwords are used to prevent accidental overwrites, discourage hackers, and secure custom configurations and operating data. The Read and Write Security can be in set in MTP per Table 40 and Table 41, and the Unlock Option can be set as shown in Table 42.

Table 40 Read Security

Setting	Description
0	No Protection
1	Configuration Registers Only
2	Protect All Registers but Telemetry
3	Protect All

Table 41 Write Security

Setting	Description
0	No Protection
1	Configuration Registers Only
2	Protect All

Table 42 Read or Write Unlock Options

Setting	Description
0	Password Only
1	Lock Forever

14.2.1 Password Protection

The system designer can set any 16-bit password (other than 00h). This password is stored in MTP. To unlock the security, a user must write the correct password into the “Password Try” register, which is a volatile read/write register. After four incorrect tries, the IC will lock up to prevent unauthorized access.

Table 43 Password Registers

Register	Length	Location
Password	16 bit (2 bytes)	MTP
Try	16 bit (2 bytes)	R/W

The following pseudo-code illustrates how to change a password:

 # first unlock the IC

Write old password to the Try register

 # now write new password into MTP

Write new password to the Password register

 # password has changed ,status is locked

 # Need to write new password to the Try register to unlock

For additional information refer to AN_1802_PL17_1802_020746, XDPE132G5D Customer Reg Map document.

14.3 I2C Protocol

All registers may be accessed using either I2C or PMBus protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. Figure 52 shows the I2C format employed by the XDPE132G5D.

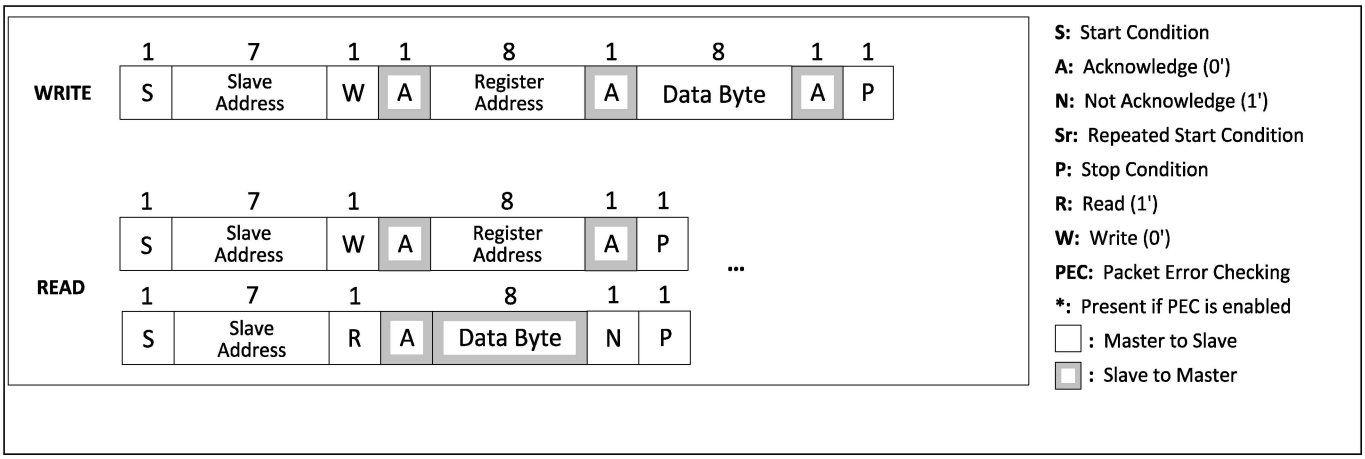

Figure 52 I2C Format

14.4 PMBus Protocol

To access the device's configuration and monitoring registers, 4 different protocols are required:

- the PMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)
- the PMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)
- the PMBus Block Read and Block Write protocols with Byte Count = 1 and Byte Count = 2
- the PMBus Block Read Process call (for accessing Configuration Registers)

An explanation of which command codes and protocols are required to access them is given in Table 44.

In addition, the XDPE132G5D supports:

- Alert Response Address (ARA)
- Bus timeout (30 ms)
- Group Command for writing to many VRs within one command

S: Start Condition
A: Acknowledge(0')
N: Not Acknowledge(1')
Sr:
P: Stop Condition
R: Read(1')
W: Write(0')
PEC: Calculated from Command
*: Data is optional
: Master to Slave
: Slave to Master
Note: PEC is required for the
MFR_REG_ACCESS command

Figure 53 PMBus Protocol Legend

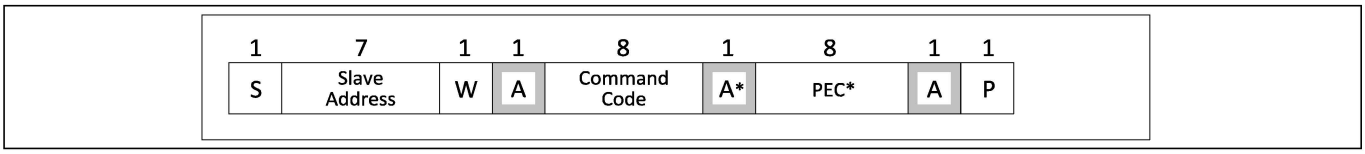

Figure 54 PMBus Send Byte

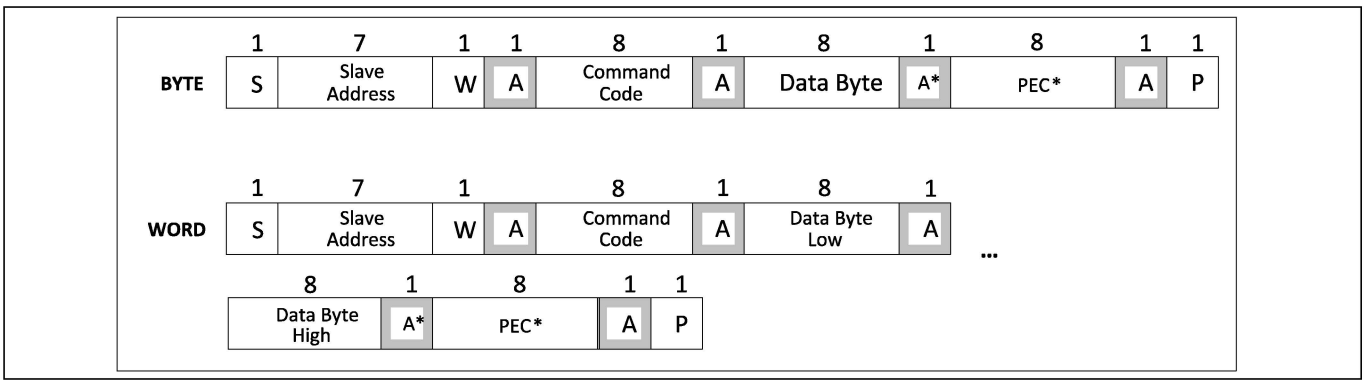

Figure 55 PMBus Write Byte/Word

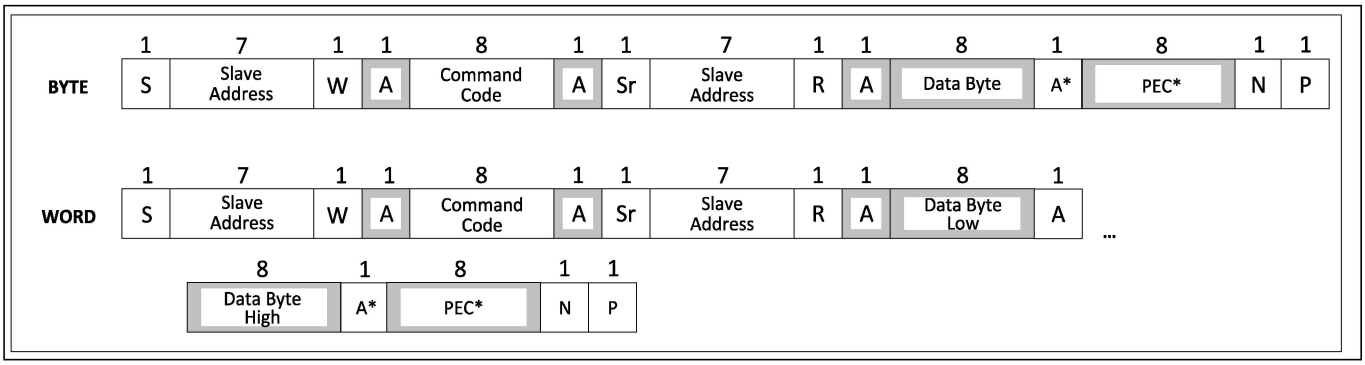

Figure 56 PMBus Read Byte/Word

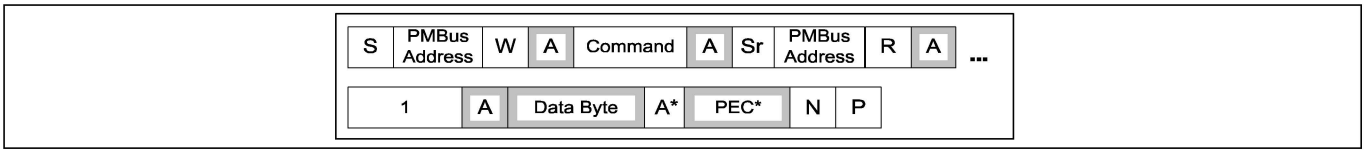

Figure 57 PMBus Block Read with Byte Count = 1

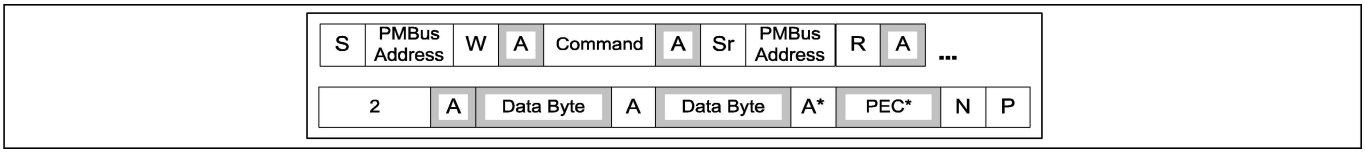

Figure 58 PMBus Block Read with Byte Count = 2

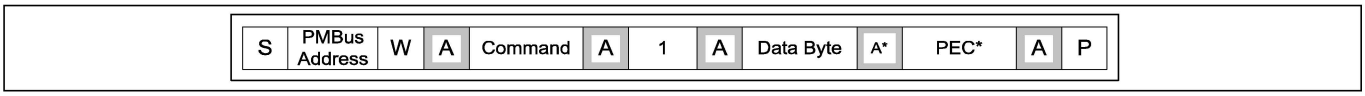

Figure 59 PMBus Block Write with Byte Count = 1

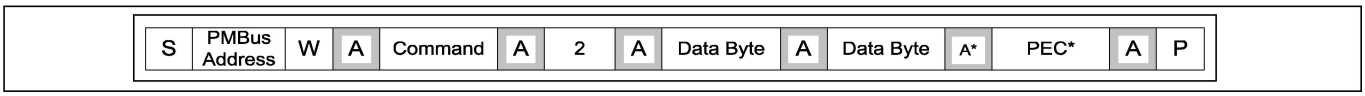

Figure 60 PMBus Block Write with Byte Count = 2

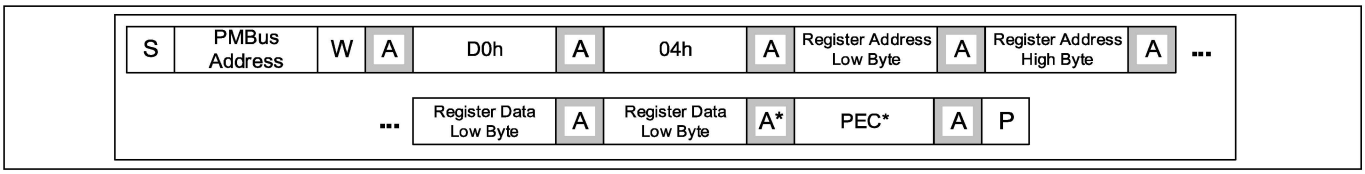

Figure 61 MFR_REG_ACCESS (Write)

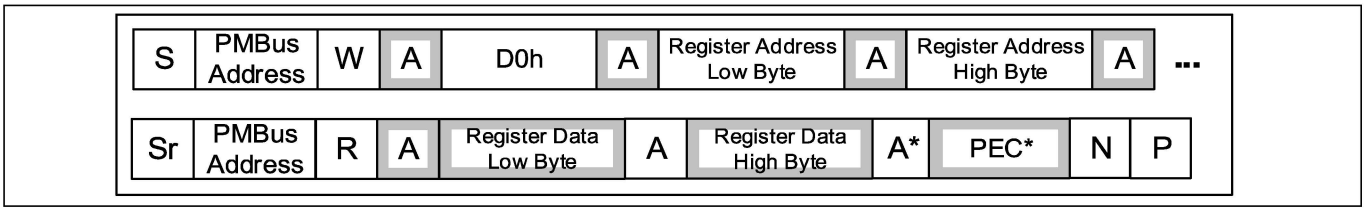

Figure 62 MFR_REG_ACCESS (Read)

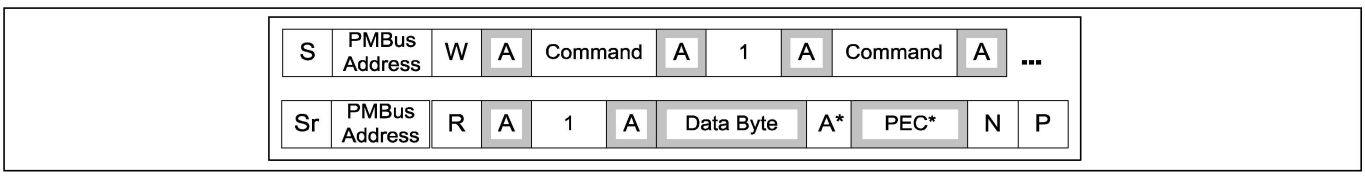

Figure 63 Block Read Process Call

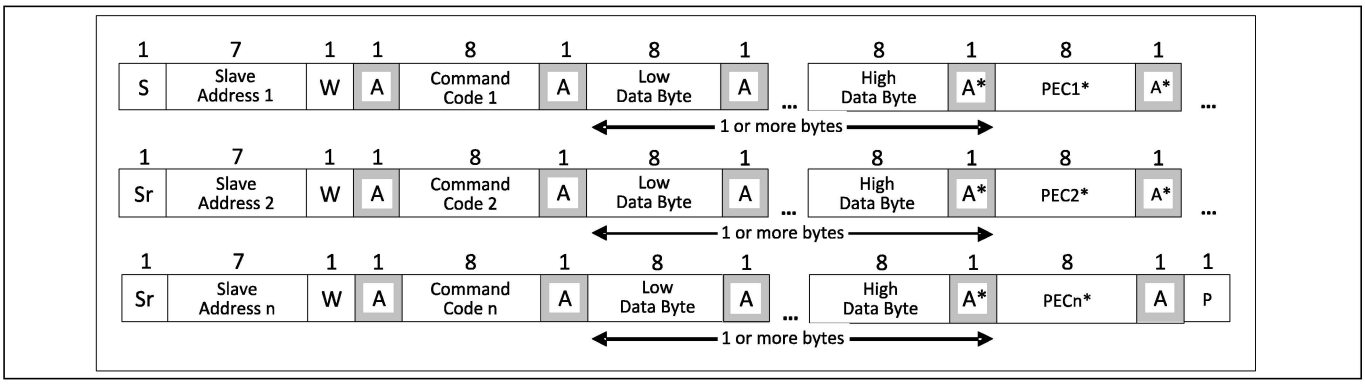

Figure 64 Group Command

14.5 PMBus Command Set

Table 44 PMBus Command Set

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
PAGE	Read/Write Byte	00h	Allows access of each loop via paging. Page 0 = L1, Page 1 = L2, Page FF = all pages
OPERATION	Read/Write Byte	01h	Enables or disables the output and controls margining. Ignores OVP on Margin High, UVP on Margin Low. Controls if VOUT_COMMAND or AVSBus Voltage Command controls the output voltage.
ON_OFF_CONFIG	Read/Write Byte	02h	Configures the combination of CONTROL pin and OPERATION command needed to turn the unit on and off.
CLEAR FAULTS	Send Byte	03h	Clear contents of Fault registers
PAGE_PLUS_WRITE	Send Byte	05h	This command is used to set a page within a device and send the command & data in one packet
PAGE_PLUS_READ	Send Byte	06h	This command is used to set a page within a device and send the command & read the returned data in one packet
WRITE_PROTECT	Read/Write Byte	10h	Provides protection from accidental changes
RESTORE_DEFAULT_ALL	Send Byte	12h	Reloads the OTP
STORE_USER_ALL	Send Byte	15h	Stores the user OTP section
RESTORE_USER_ALL	Send Byte	16h	Reloads the user OTP section
CAPABILITY	Read Byte	19h	Returns 0xB4 to indicate Packet Error Checking is supported, Maximum bus speed is 400 kHz, and AVS is supported.
SMBALERT_MASK	Block Write/ Block Read Process Call	1Bh	Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register to be masked in the low byte, the bit to be masked in the High byte.
VOUT_MODE	Read/Write	20h	Sets the format for VOUT related commands.

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
	Byte		Linear mode, -8, -9, -10, -11 and -12 exponents supported.
VOUT_COMMAND	Read/Write Word	21h	Sets the voltage to which the device should set the output. Format according to VOUT_MODE.
VOUT_TRIM	Read/Write Word	22h	Applies a fixed offset to the output voltage command value. Format according to VOUT_MODE.
VOUT_MAX	Read/Write Word	24h	Sets an upper limit on the output voltage the unit can command. Format according to VOUT_MODE.
VOUT_MARGIN_HIGH	Read/Write Word	25h	Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE.
VOUT_MARGIN_LOW	Read/Write Word	26h	Sets the margin low voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE.
VOUT_TRANSITION_RATE	Read/Write Word	27h	Sets the rate at which the output changes voltage during regulation due to VOUT_COMMAND command. mV/µs; exp = -3
VOUT_DROOP	Read/Write Word	28h	Sets the slope at which the output voltage decreases or increases with increasing or decreasing output current for use with Adaptive Voltage Positioning. 5/256 mΩ per LSB.
VOUT_MIN	Read/Write Word	2Bh	Sets a lower limit on the output voltage the unit can command. Format according to VOUT_MODE.
FREQUENCY_SWITCH	Read/Write Word	33h	Sets the switching frequency in kHz from 200 to 2000; Exp = 0, 1
POWER_MODE	Read/Write Word	34h	Sets the device power state for Max Efficiency (Auto PS Mode), Max Power (PS0), or MFR Specific power state PS1 (1 or 2 phases) or PS2 (Diode Emulation).
VIN_ON	Read/Write Word	35h	Sets the value of the input voltage at which the unit should begin power conversion. Exp = -2.
VIN_OFF	Read/Write Word	36h	Sets the value of the input voltage that the unit, once operation has started, should stop power conversion. Exp = -2.
IOUT_CAL_GAIN	Read/Write Word	38h	Set the current sense gain for Total Iout. 2's complement with exp = -7.
IOUT_CAL_OFFSET	Read/Write Word	39h	Used to null out any offsets in the output current sensing circuitry for Total Iout. 2's complement Exp = -2.
VOUT_OV_FAULT_LIMIT	Read/Write Word	40h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output over-voltage fault. Format according to VOUT_MODE. Will be ignored if relative_ovp_en =

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			1.
VOUT_OV_FAULT_RESPONSE	Read/Write Byte	41h	Instructs the device on what action to take in response to an output over-voltage fault. Only shutdown and ignore are supported.
VOUT_OV_WARN_LIMIT	Read/Write Word	42h	Sets the value of the output voltage, measured at the sense or output pins, that causes an output over-voltage warning. Format as determined by VOUT_MODE.
VOUT_UV_WARN_LIMIT	Read/Write Word	43h	Sets the value of the output voltage, measured at the sense or output pins, that causes an output voltage low warning. Format as determined by VOUT_MODE.
VOUT_UV_FAULT_LIMIT	Read/Write Word	44h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output under-voltage fault. Format according to VOUT_MODE. Will be ignored if relative_uvp_en = 1.
VOUT_UV_FAULT_RESPONSE	Read/Write Byte	45h	Instructs the device on what action to take in response to an output under-voltage fault. Only shutdown and ignore are supported.
IOUT_OC_FAULT_LIMIT	Read/Write Word	46h	Sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition. Exp = 1.
IOUT_OC_FAULT_RESPONSE	Read/Write Byte	47h	Instructs the device on what action to take in response to an output over-current fault. C0h (shutdown immediately), F8h (hiccup forever), and F0 (hiccup 6 times) are supported.
IOUT_OC_WARN_LIMIT	Read/Write Word	4Ah	Sets the value of the output current that causes an output over-current warning. Exp = 1.
OT_FAULT_LIMIT	Read/Write Word	4Fh	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an over-temperature fault. Exp = 0.
OT_FAULT_RESPONSE	Read/Write Byte	50h	Instructs the device on what action to take in response to an over-temperature fault. Shutdown, inhibit (re-start when fault is no longer present), and ignore are supported.
OT_WARN_LIMIT	Read/Write Word	51h	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over-temperature Warning alarm. Exp = 0.
VIN_OV_FAULT_LIMIT	Read/Write Word	55h	Sets the value of the input voltage that causes an input over-voltage fault. Exp = -4.
VIN_OV_FAULT_RESPONSE	Read/Write Byte	56h	Instructs the device on what action to take in response to an input over-voltage fault. Only shutdown and ignore are supported.

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
VIN_UV_WARN_LIMIT	Read/Write Word	58h	Sets the value of the input voltage that causes an input voltage low warning. Exp = -4.
IIN_OC_WARN_LIMIT	Read/Write Word	5Dh	Sets the value of the input current, in amperes, that causes a warning that the input current is high. Exp = -1.
POWER_GOOD_ON	Read/Write Word	5Eh	Sets the output voltage at which an optional POWER_GOOD signal should be asserted. Format according to VOUT_MODE.
POWER_GOOD_OFF	Read/Write Word	5Fh	Sets the output voltage at which an optional POWER_GOOD signal should be negated. Format according to VOUT_MODE.
TON_DELAY	Read/Write Word	60h	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Exp = -1.
TON_RISE	Read/Write Word	61h	Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exp = -2.
TON_MAX_FAULT_LIMIT	Read/Write Word	62h	Sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output. Exp = -2.
TON_MAX_FAULT_RESPONSE	Read/Write Byte	63h	Instructs the device on what action to take in response to a TON_MAX fault. Only shutdown and ignore are supported.
TOFF_DELAY	Read/Write Word	64h	Sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Exp = -1.
TOFF_FALL	Read/Write Word	65h	Sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. Exp = -2.
POUT_OP_WARN_LIMIT	Read/Write Word	6Ah	Sets the value of the output power, in watts, that causes a warning that the output power is high. Exp = 1.
PIN_OP_WARN_LIMIT	Read/Write Word	6Bh	Sets the value of the input power, in watts, that causes a warning that the input power is high. Exp = 1.
STATUS_BYTE	Read/Write Byte	78h	Returns 1 byte where the bit meanings are: Bit <7> Reserved Bit <6> Output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input Under-voltage fault

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: None of the Above
STATUS_WORD	Read/Write Word	79h	Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are: Bit <7> VOUT fault Bit <6> IOUT fault Bit <5> INPUT fault Bit <4> MFR_SPECIFIC Bit <3> POWER_GOOD# Bit <2:0> Reserved
STATUS_VOUT	Read/Write Byte	7Ah	Bit <7> Output Over-voltage Fault Bit <6> Output Over-voltage Warning Bit <5> Output Under-voltage Warning Bit <4> Output Under-voltage Fault Bit <3> VOUT_MAX_MIN Warning Bit <2> TON_MAX_FAULT Bit <1> Reserved Bit <0> Reserved
STATUS_IOUT	Read/Write Byte	7Bh	Bit <7> Output Over-current Fault Bit <6> Reserved Bit <5> Output Over-current Warning Bit <4:1> Reserved Bit <0> Output Power Warning
STATUS_INPUT	Read/Write Byte	7Ch	Bit <7> Input Over-voltage Fault Bit <6> Reserved Bit <5> Input Under-voltage Warning Bit <4> Reserved Bit <3> Unit Off For Insufficient Input Voltage Bit <2> Reserved Bit <1> Input Over-current Warning Bit <0> Input Power Warning
STATUS_TEMPERATURE	Read/Write Byte	7Dh	Bit <7> Over-Temperature Fault Bit <6> Over-Temperature Warning Bit <5:0> Reserved
STATUS_CML	Read/Write Byte	7Eh	Returns 1 byte where the bit meanings are: Bit <7> Invalid or unsupported command Bit <6> Invalid or unsupported data Bit <5> PEC fault Bit <4:2> Reserved Bit <1> Other communication fault not listed here Bit <0> Reserved

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
STATUS_MFR_SPECIFIC	Read/Write Byte	80h	Returns 1 byte where the bit meanings are: Bit <7> Phase Fault High/Low Bit <6> Per Phase Current Limit Warning Bit <5:3> Reserved Bit <2> Vaux Under-voltage Fault Bit <1> TSEN High Fault Bit <0> Phase Fault High/Low
READ_VIN	Read Word	88h	Returns the input voltage in Volts. Exp = -5
READ_IIN	Read Word	89h	Returns the input current in amperes. Loop1 Exp = -3. Loop2 Exp = -4
READ_VOUT	Read Word	8Bh	Returns the output voltage in the format set by VOUT_MODE
READ_IOUT	Read Word	8Ch	Returns the output current in amperes. Loop1 Exp = 0, -1 or -2. Loop2 Exp = -1 or -2
READ_TEMPERATURE_1	Read Word	8Dh	Returns the addressed loop power stage temperature in degrees Celsius. Exp = 0
READ_DUTY_CYCLE	Read Word	94h	Returns the duty cycle of the PMBus device's mainpower converter in percent. Exp = -10
READ_POUT	Read Word	96h	Returns the output power in watts. Loop1 Exp =1, 0, or -1. Loop2 Exp 0 or -1
READ_PIN	Read Word	97h	Returns the input power in watts. Loop1 Exp =1, 0, or -1. Loop2 Exp 0 or -1
PMBUS_REVISION	Read Byte	98h	Reports PMBus Part I, Part II & Part III Rev 1.3 (33h)
MFR_ID	Block Read/Write Byte count = 2	99h	The MFR_ID is set to IR (ASCII 52 49) unless programmed different in the USER registers of the controller.
MFR_MODEL	Block Read, byte count = 1	9Ah	The MFR_Model is the same as the device ID if the USER register for Manufacturer model is 00. Otherwise MFR_Model command returns the value in the USER register for MFR_Model.
MFR_REVISION	Block Read, byte count = 2	9Bh	The MFR_Revision is the same as the device revision if the USER register for Manufacturer revision is 00. Otherwise MFR_Revision command returns the value in the USER register for MFR_Revison.
MFR_DATE	Block Read/Write Byte count = 2	9Dh	The MFR_DATE command returns the value in the USER register called MFR_DATE
IC_DEVICE_ID	Block Read	ADh	Returns a 1 byte code with the following values: 7Ch = XDPE132G5D
IC_DEVICE_REV	Block Read	AEh	The IC revision that is stored inside the IC
MFR_READ_VAUX	Read Word	C4h	Returns the Vaux voltage in the format set by VOUT_MODE
MFR_VIN_PEAK	Read Word	C5h	Returns the maximum input voltage in volts. Value

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			is cleared after reading. Exp = -5
MFR_VOUT_PEAK	Read Word	C6h	Returns the maximum output voltage in the format set by VOUT_MODE. Value is cleared after reading.
MFR_IOUT_PEAK	Read Word	C7h	Returns the maximum output current in amperes. Value is cleared after reading. Loop1 Exp = 0. Loop2 Exp = -1
MFR_TEMP_PEAK	Read Word	C8h	Returns the maximum temperature in Celsius. Value is cleared after reading. Exp = 0
MFR_VIN_VALLEY	Read Word	C9h	Returns the minimum input voltage in volts. Value is cleared after reading. Exp = -5
MFR_VOUT_VALLEY	Read Word	CAh	Returns the minimum output voltage in the format set by VOUT_MODE. Value is cleared after reading.
MFR_IOUT_VALLEY	Read Word	CBh	Returns the mimimum output current in amperes. Value is cleared after reading. . Loop1 Exp = 0. Loop2 Exp = -1
MFR_TEMP_VALLEY	Read Word	CCh	Returns the minimum temperature in degrees Celsius. Value is cleared after reading. Exp = 0
VOUT_RESET	Read/Write Word	CEh	Returns or sets the Reset Voltage for the AVS command "Voltage Reset". This is the voltage the VR goes to when it receives the "Voltage Reset" command. Format is set by VOUT_MODE
RESET_TRANSITION_RATE	Read/Write Word	CFh	Returns or sets the transition rate that the voltage will slew at when an AVS Voltage Reset Command is received. Exp = -3.
USER_DATA_00	Block Read/Write	B0h	Scratch pad register
USER_DATA_01	Block Read/Write	B1h	Scratch pad register
MFR_ REG_ACCESS	Custom MFR protocol	D0h	Read/Write I2C registers
MFR_I2C_ADDRESS	Read/Write Word	D6h	Sets the I2C address of the device. This will over-write the I2C register only if the I2C Address lock is set to 0.

14.6 11-bit Linear Format

Monitored parameters use the Linear Data Format (Figure 65) encoding into 1 Word (2 bytes), where:

$$Value = Y \times 2^{N}$$

Note N and Y are “signed” values. All commands, other than those using the format described by VOUT_MODE, use this format.

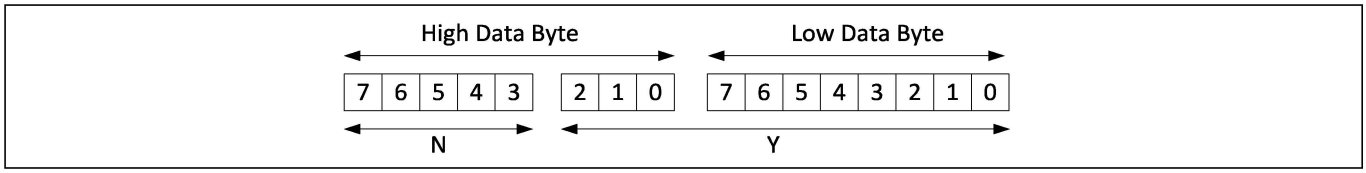

Figure 65 11-bit Linear Data Format

14.7 16-bit Linear Format

This format is only used for VOUT related commands (i.e. READ_VOUT, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, POWER_GOOD_ON, POWER_GOOD_OFF):

$$Value = Y \times 2^{N}$$

Note N and Y are “signed” values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

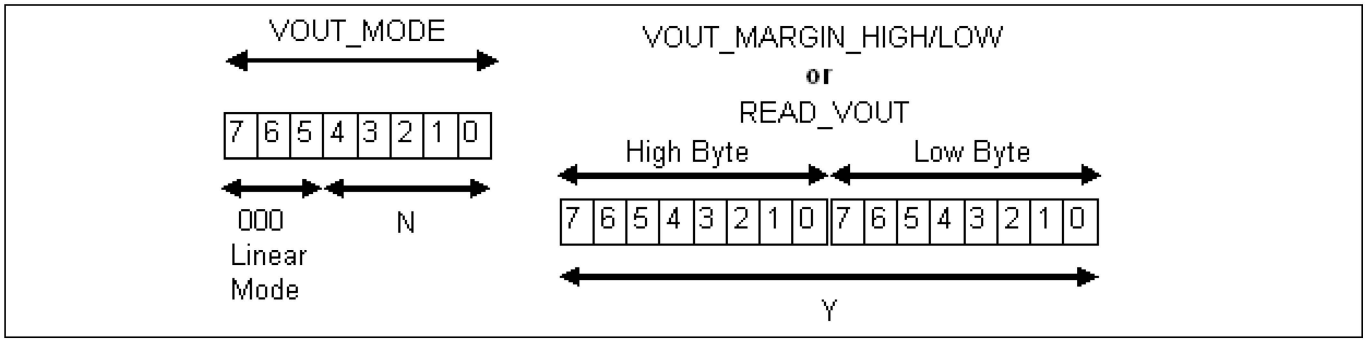

Figure 66 16-bit Linear Data Format

15 Package

15.1 Marking Information

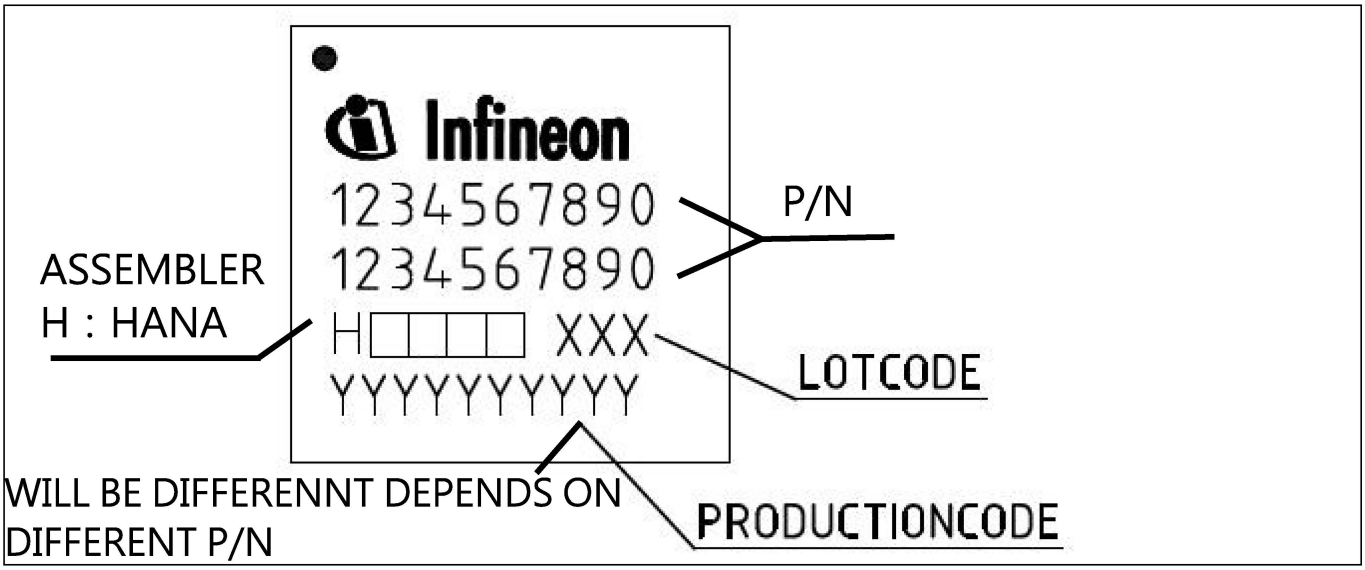

Figure 67 Package Marking

15.2 Package Dimensions

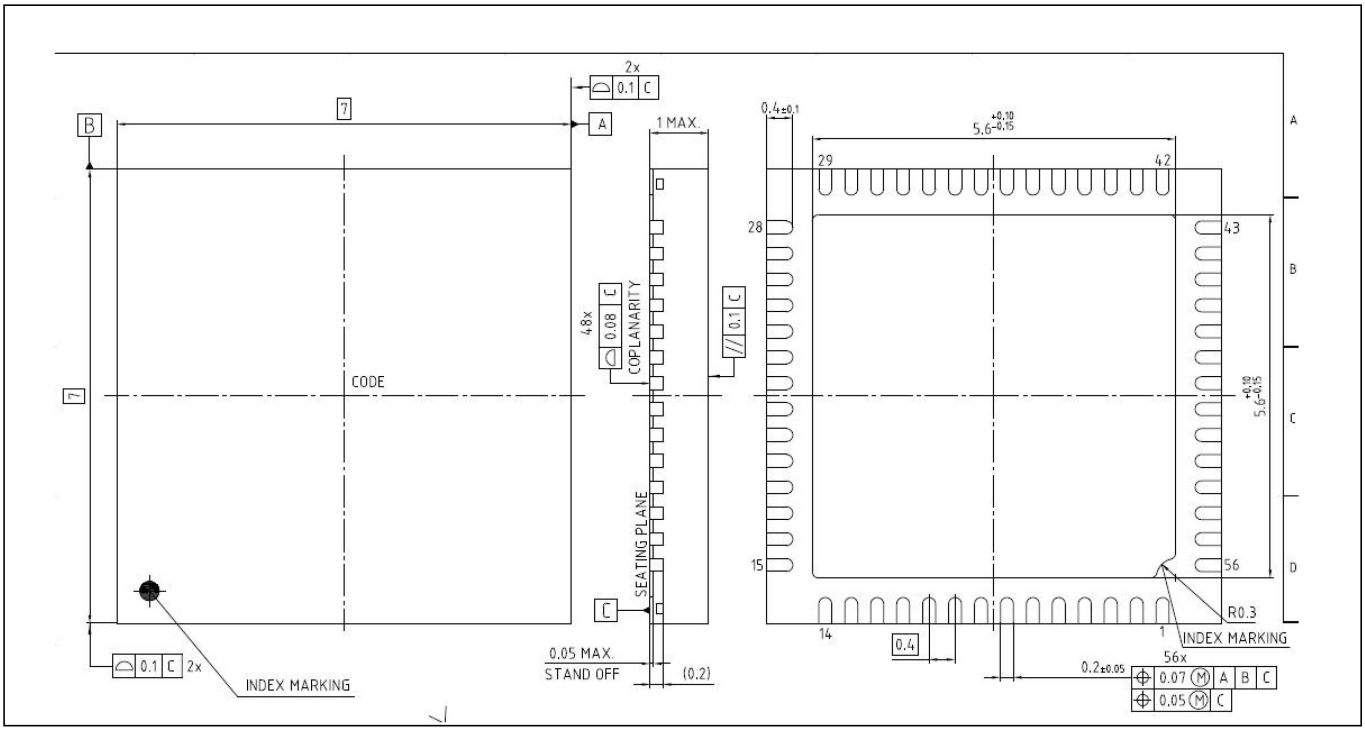

Figure 68 Package Dimensions

15.3 PCB Pad Dimensions

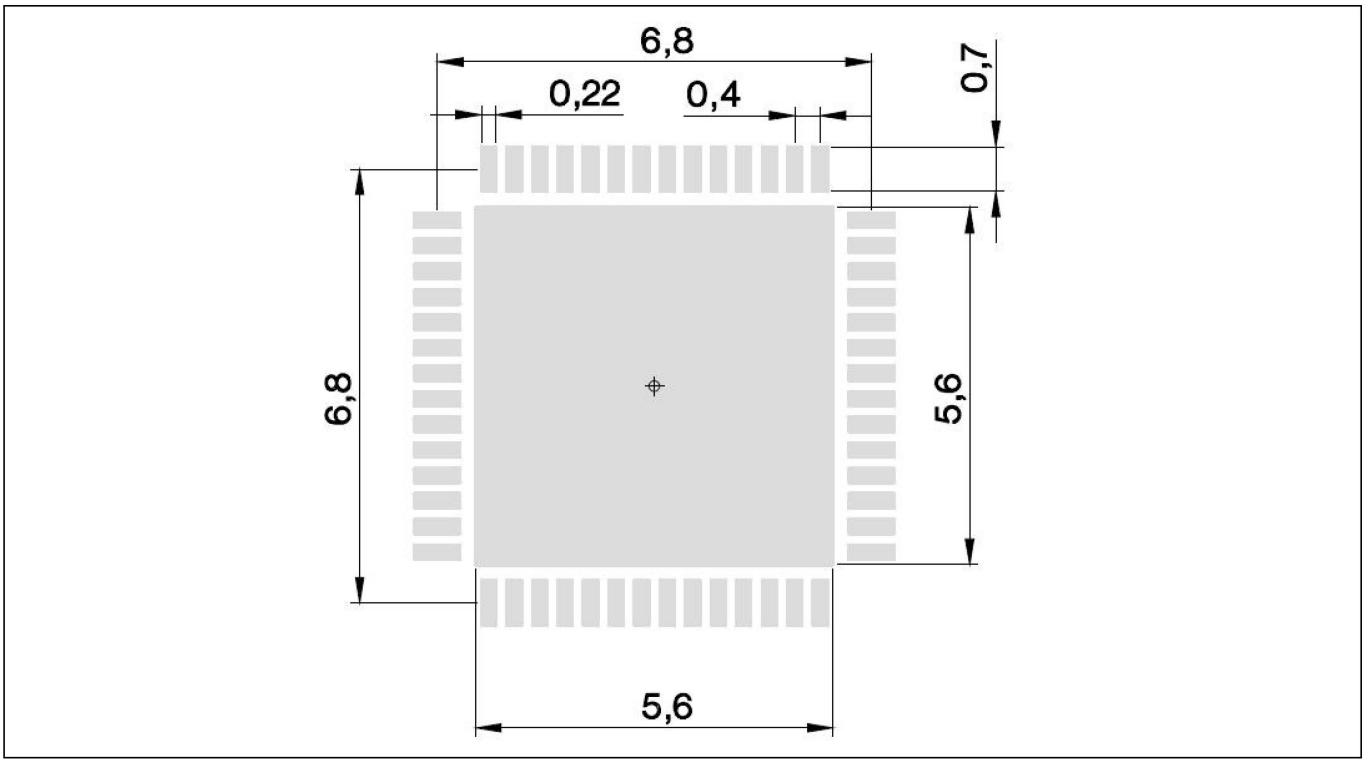

Figure 69 PCB PAD Dimensions

15.4 Paste Mask Dimensions

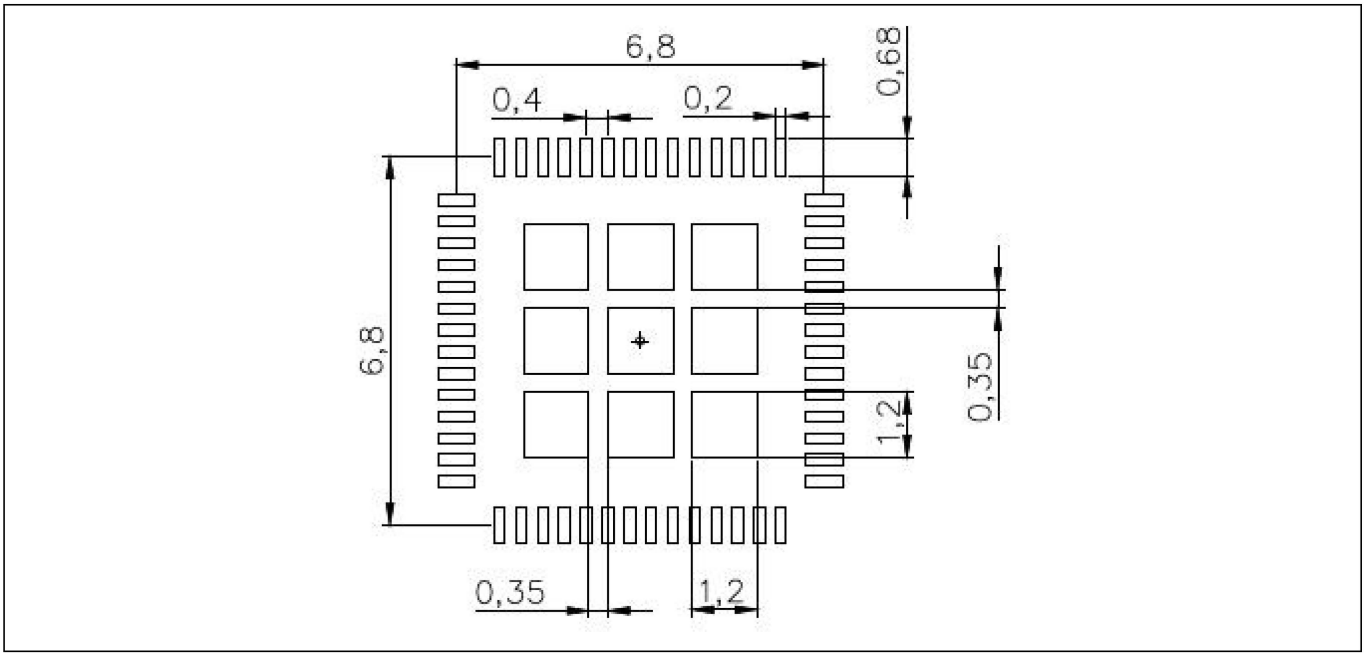

Figure 70 Paste Mask Dimensions

15.5 Environmental Qualifications

Table 45

Qualification Level		**Industrial**	
Moisture Sensitivity		QFN Package	MSL3
ESD	**Human Body Model**	JESD22-A114-F, Class 2	
	Charged Device Model	JESD22-C101-F, Class C3	
	Latch-up	JESD78, Class II, Level A	
RoHS Compliant		Yes	

16 References

[1] AN_1802_PL17_1802_020746 XDPE132G5D Register Map

[2] AN_1802_PL17_1802_172546 XDPE132G5D Programming Guide

[3] AN_1802_PL17_1802_201226 XDPE132G5D PMBus Command Set

[4] AN0042 AVSBus Bus Implementation in Infineon Digital Controllers

Revision History

Major changes since the last revision

Revision	Description of change	Date	Modified by	Approved by
1.0	- Initial Release	1/06/2020	D. Caron	

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