PG142-B00

DP + DP + DP + HDMI/DP

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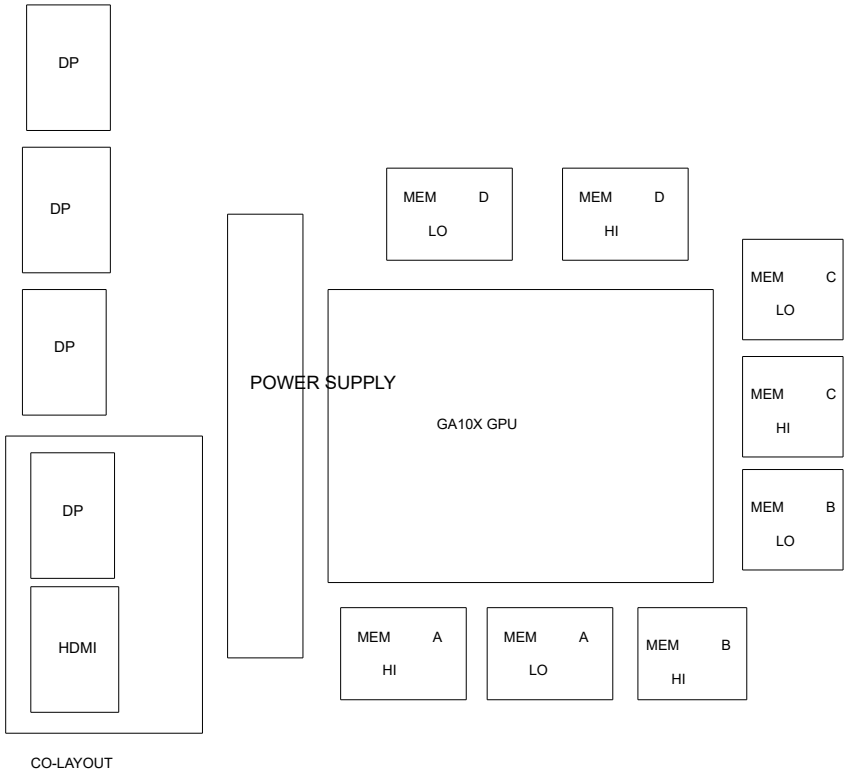

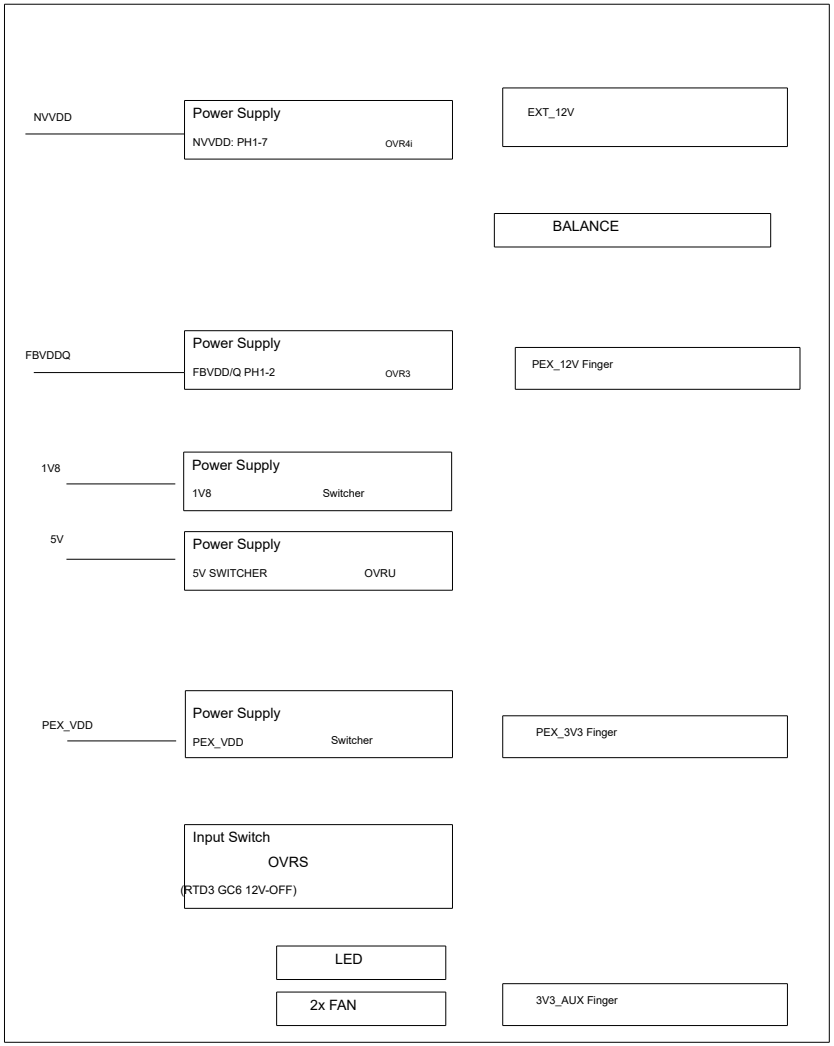

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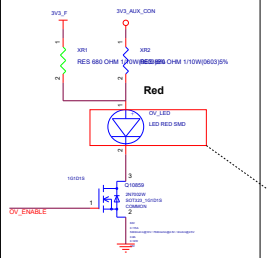
OV Enable status LED



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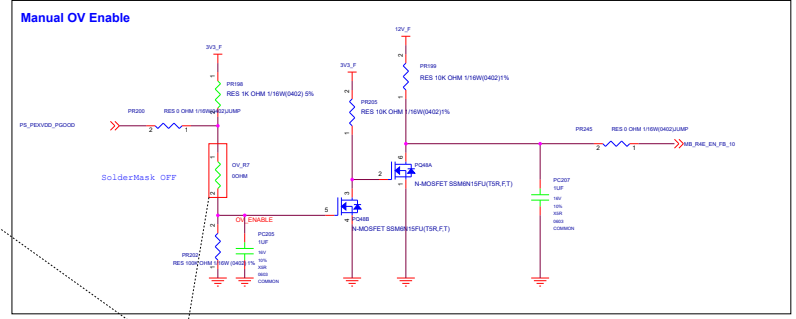
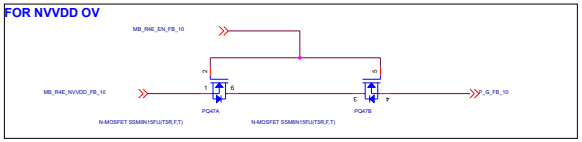


PLACE TOGETHER

FOR NVVDD OV



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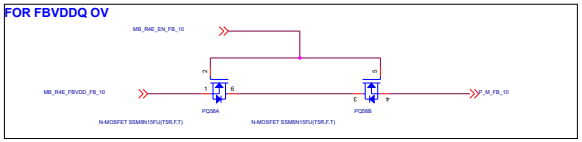

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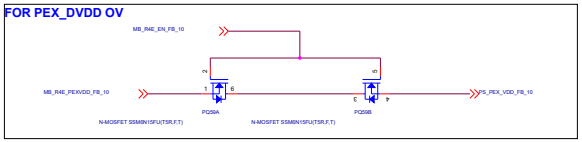

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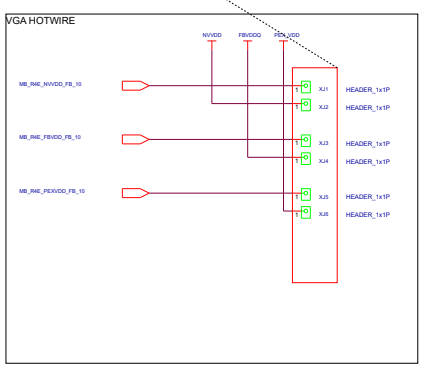

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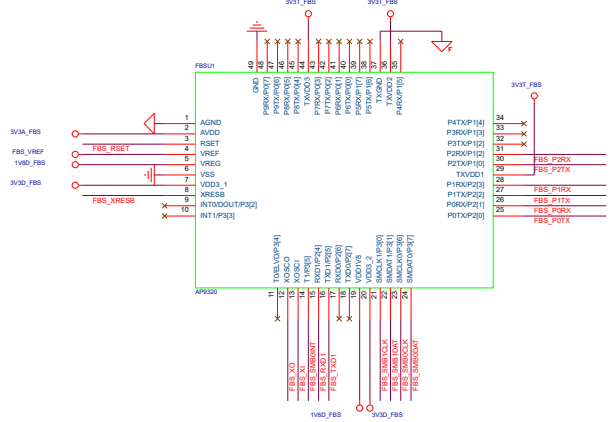

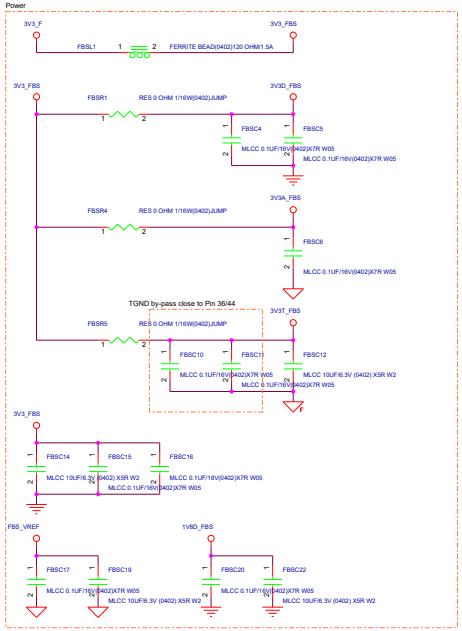

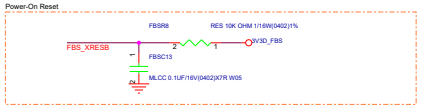

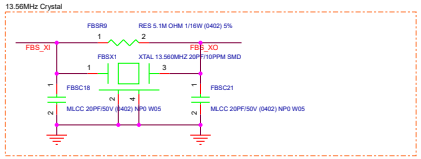

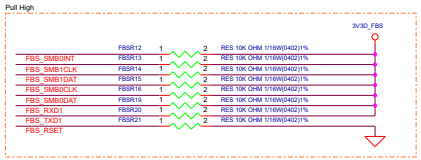

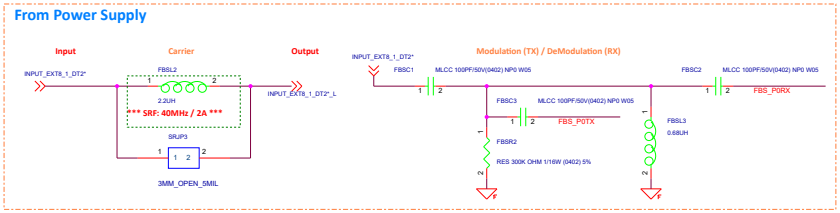

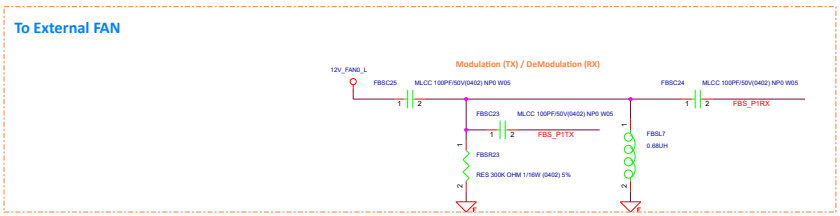

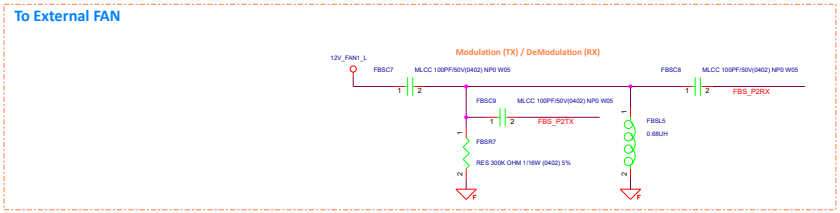

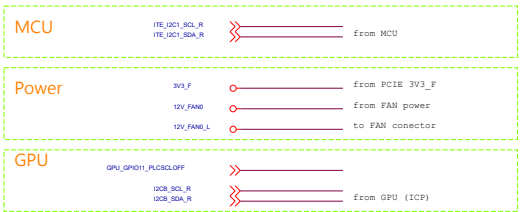

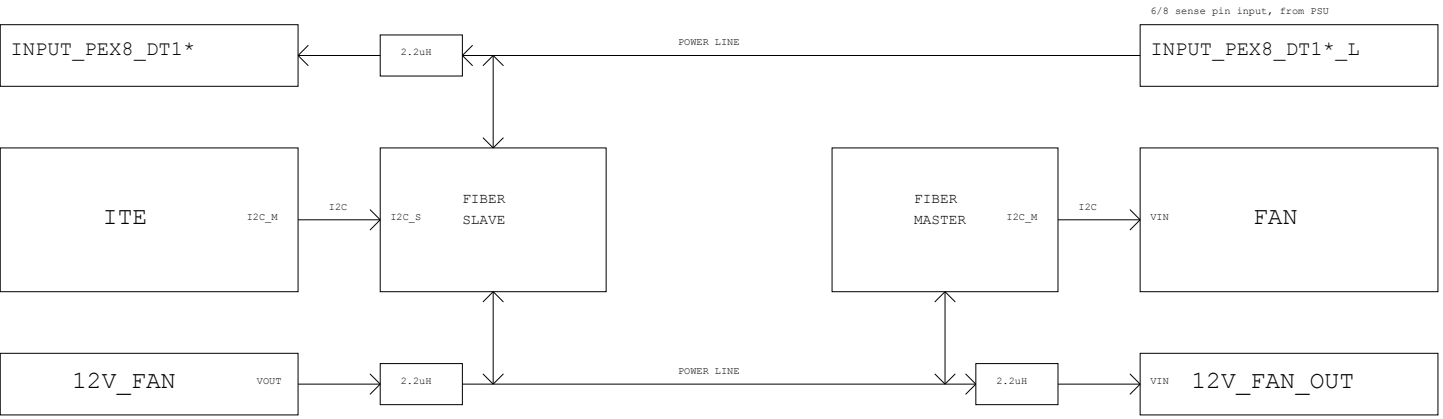

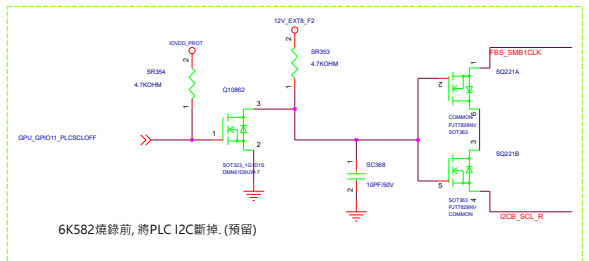

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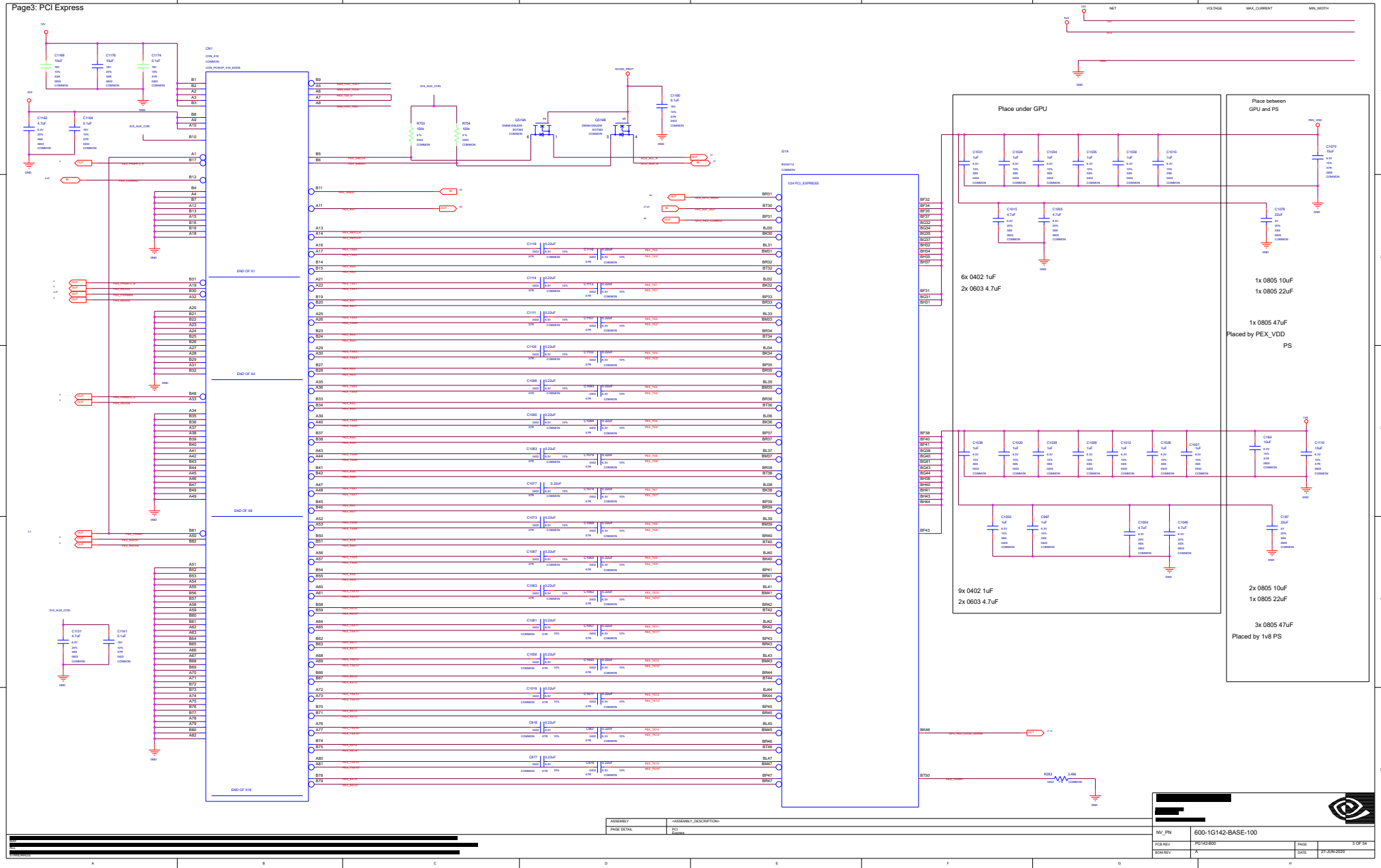
Page3: PCI Express



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Page5: MEMORY: GPU Partition A/B

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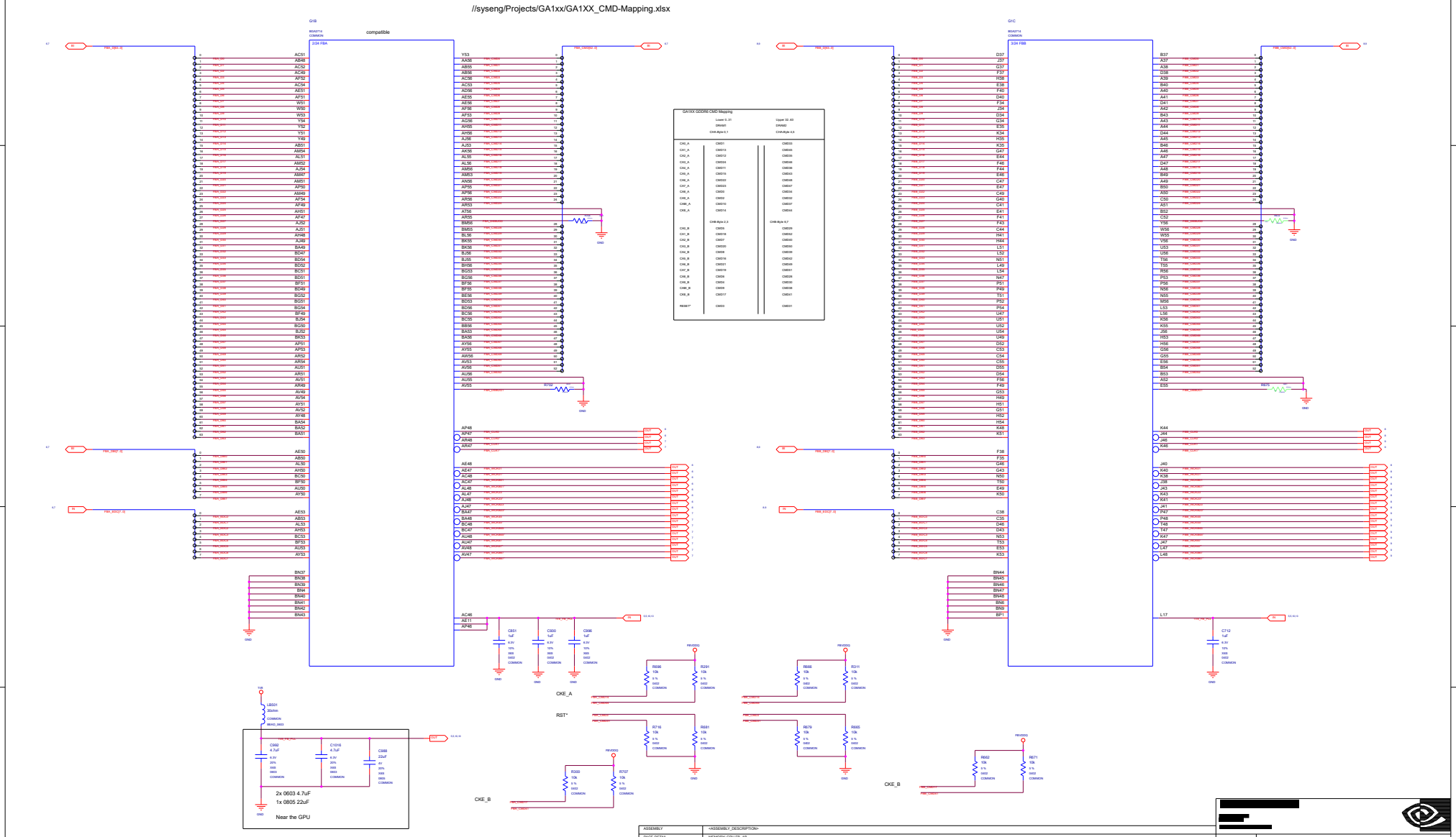

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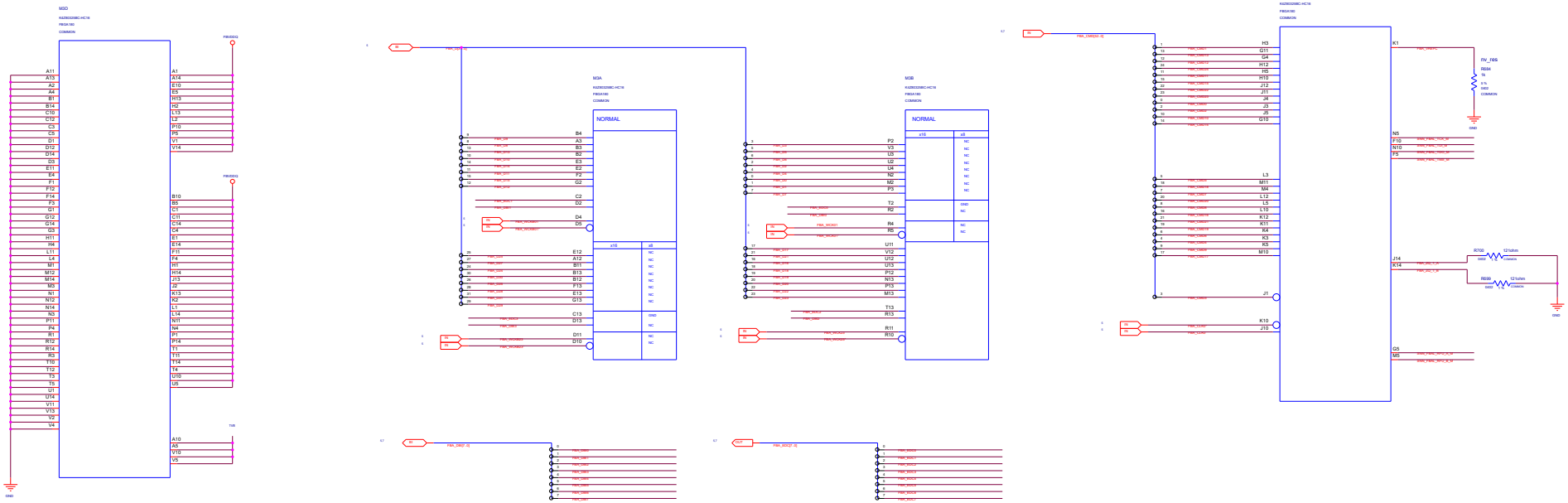
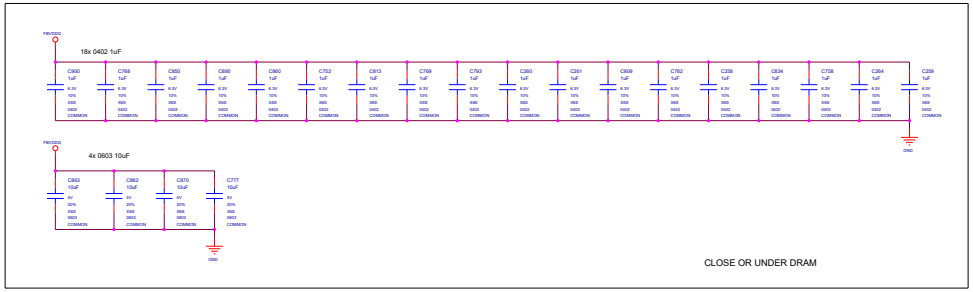
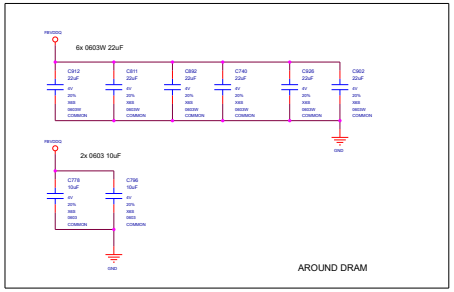
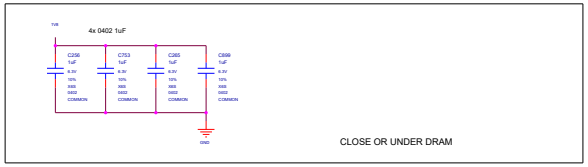
Page6: MEMORY: FBA Partition 31..0



decap via : at least 2 gnd vias and 2 power vias for each cap







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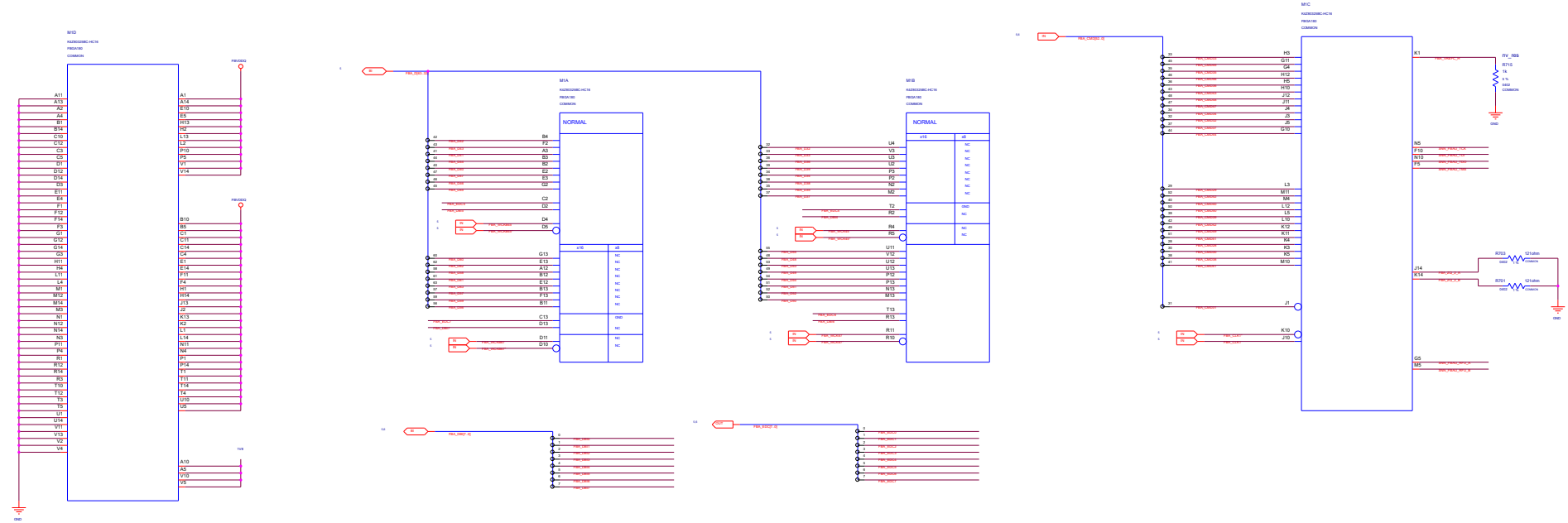

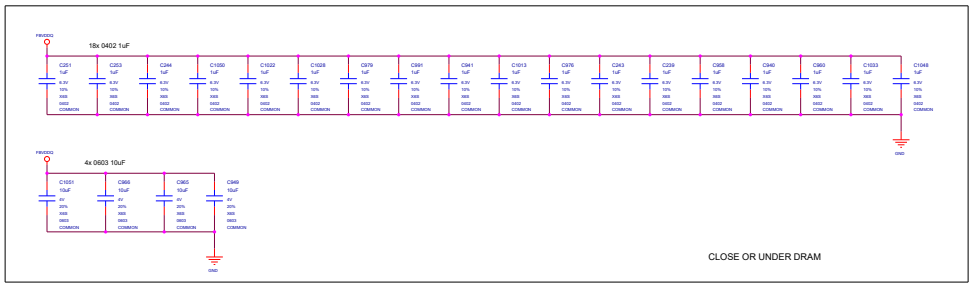

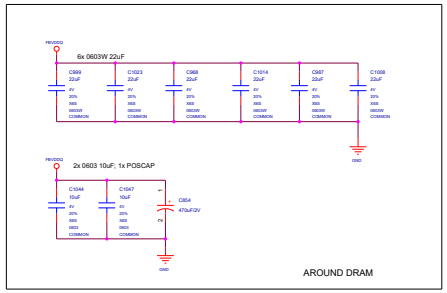

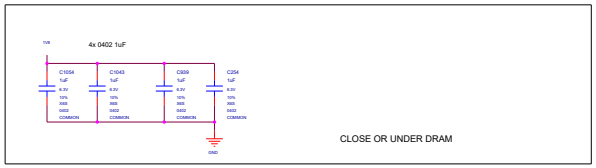

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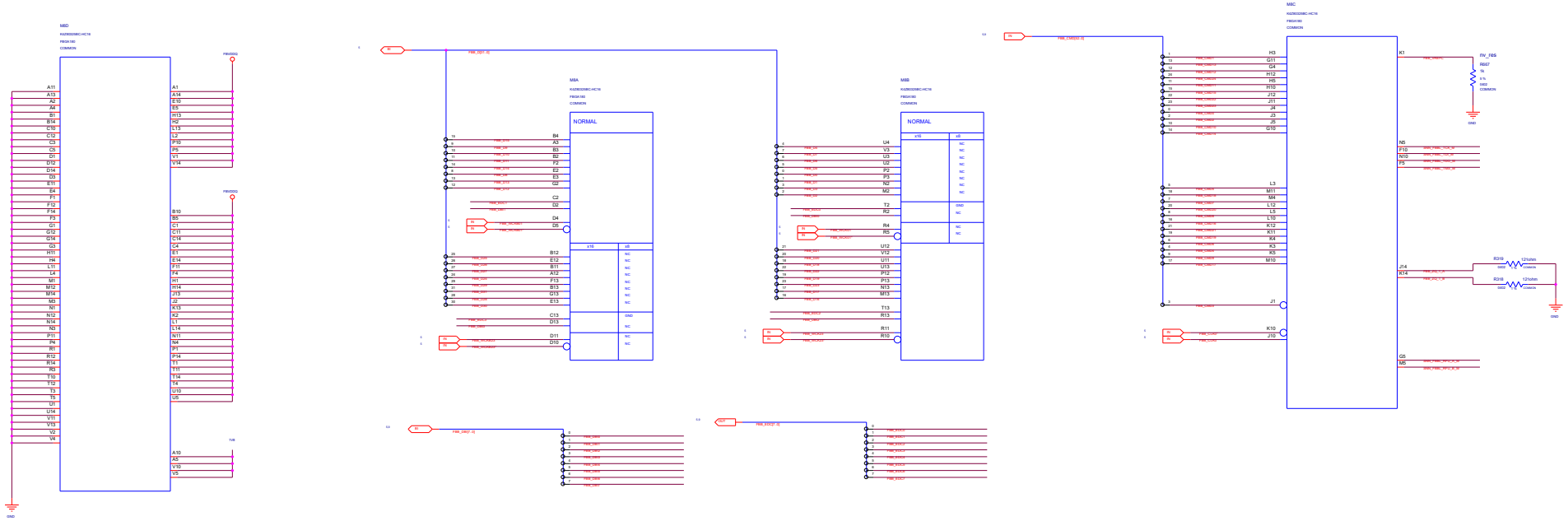

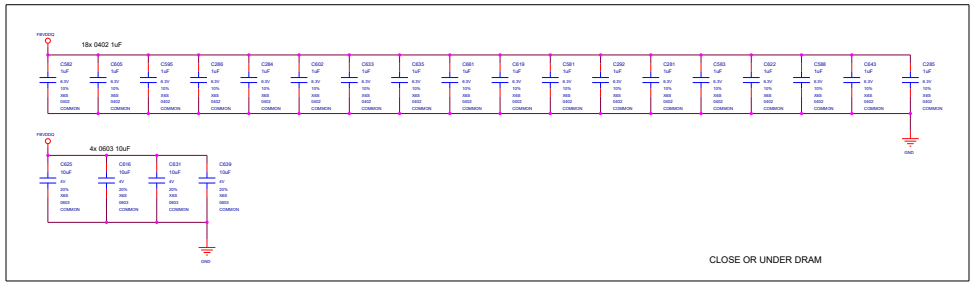

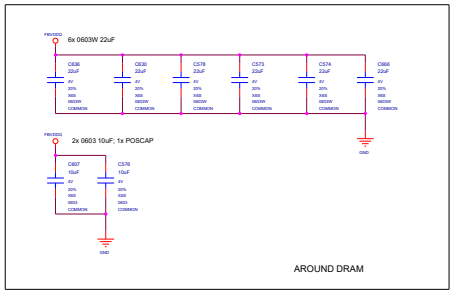

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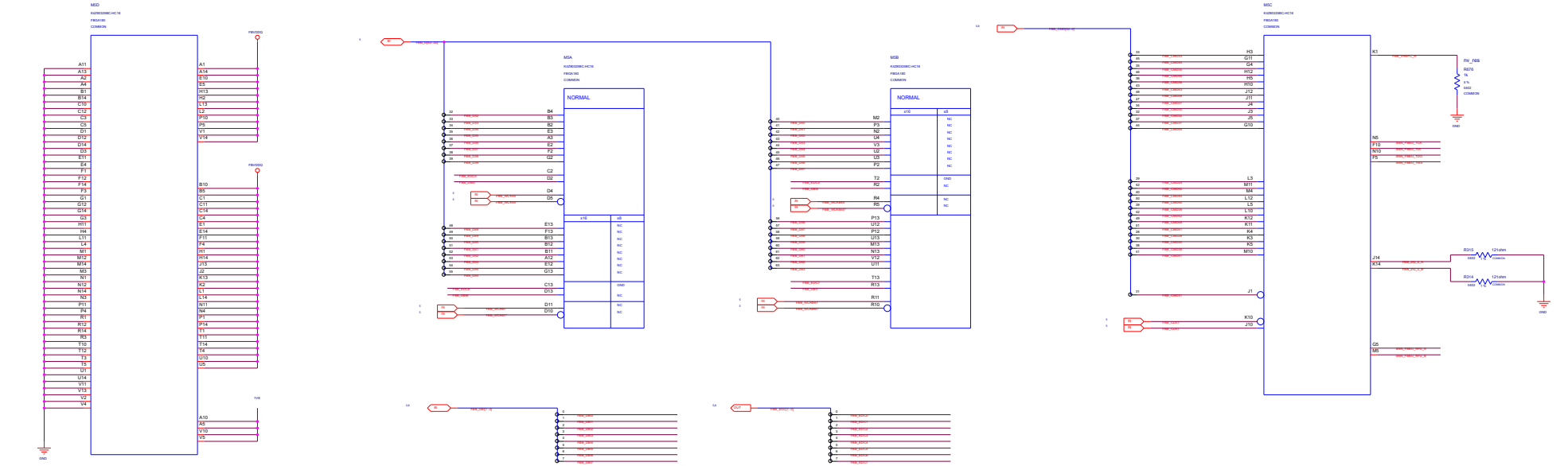

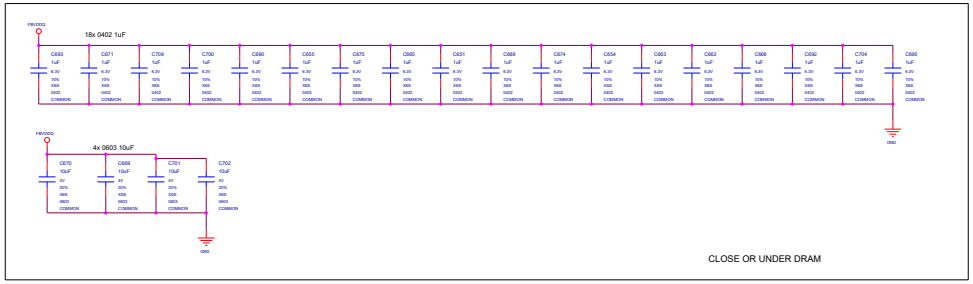

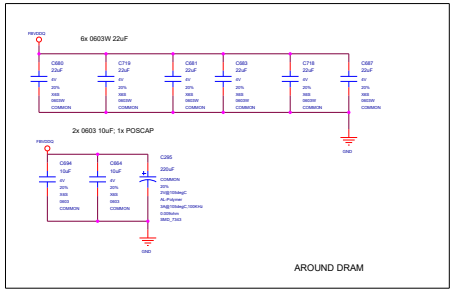

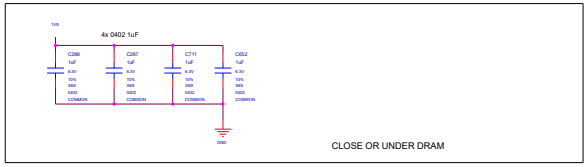

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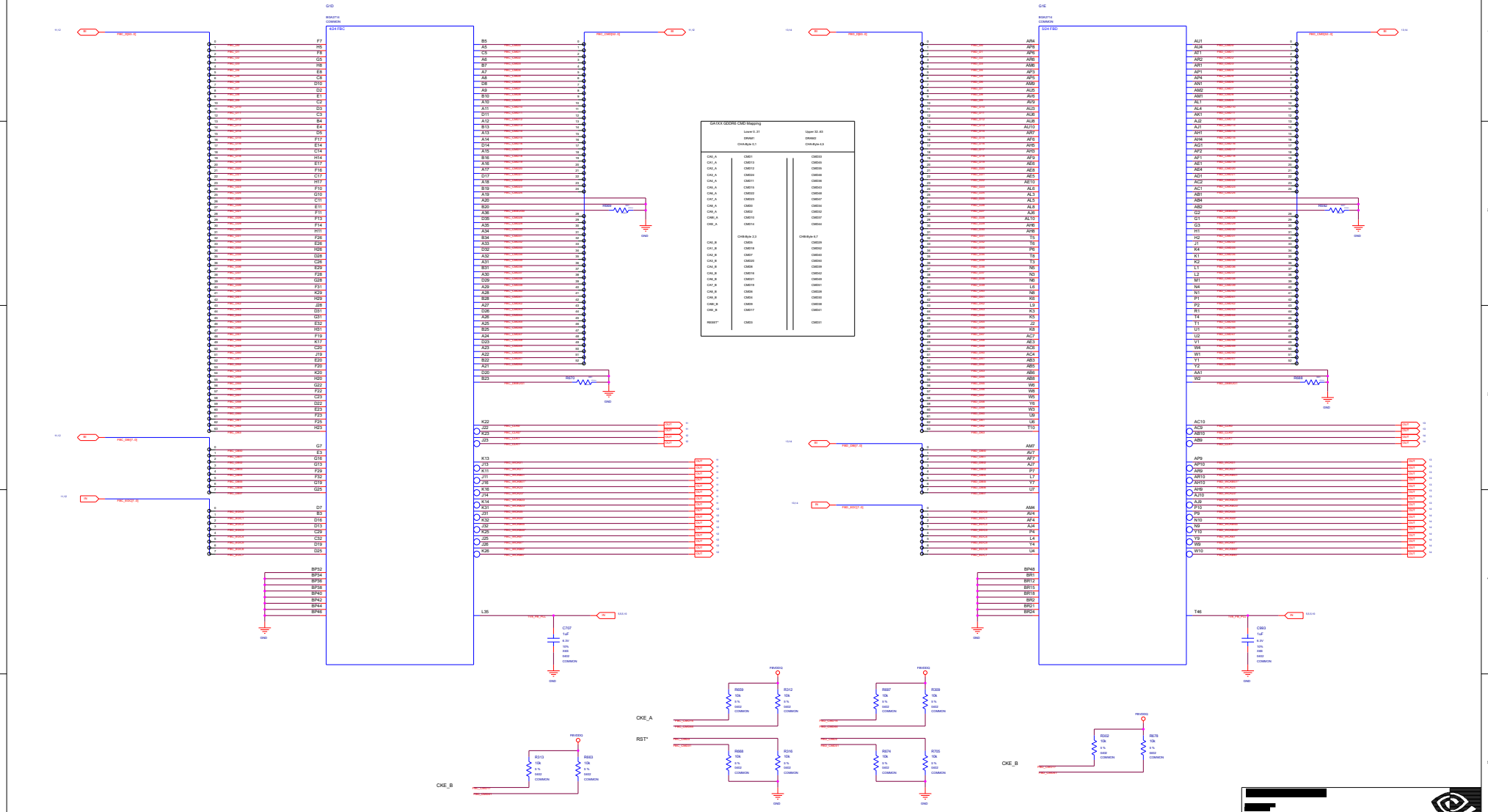

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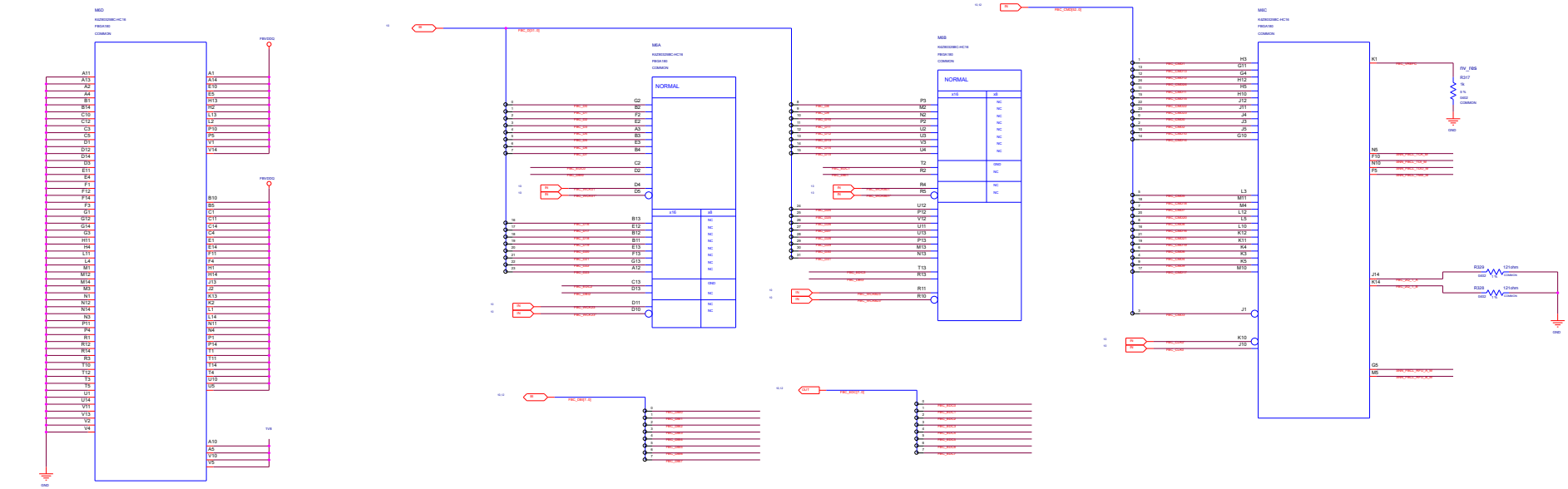

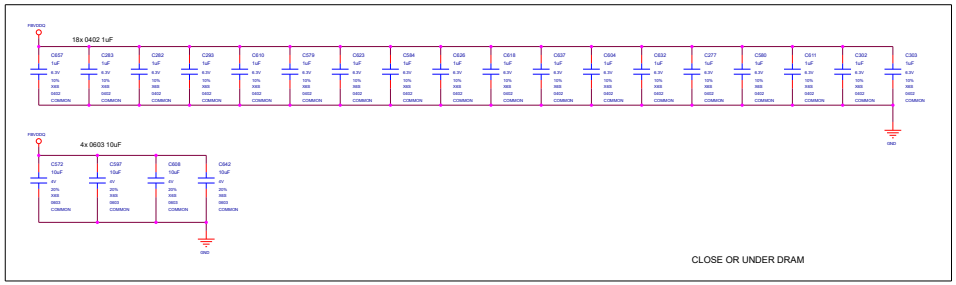

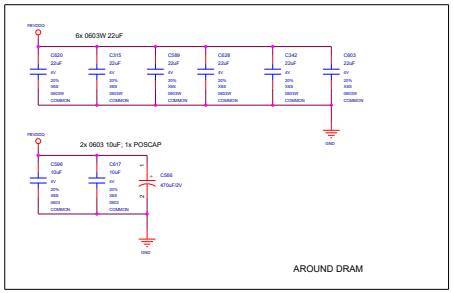

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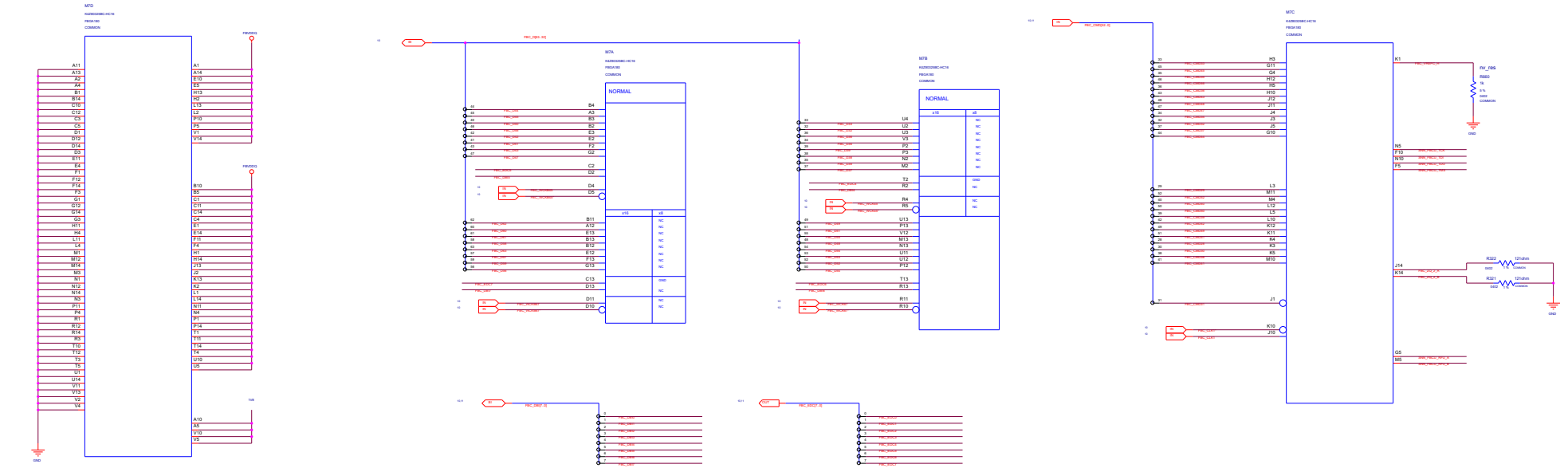

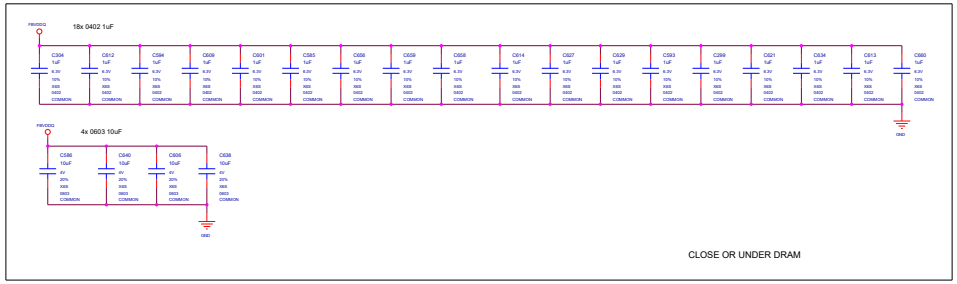

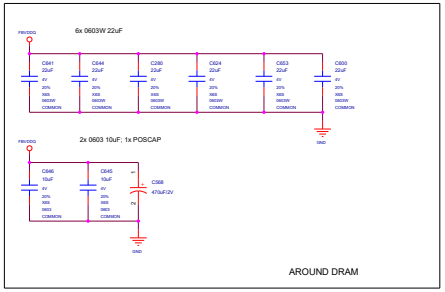

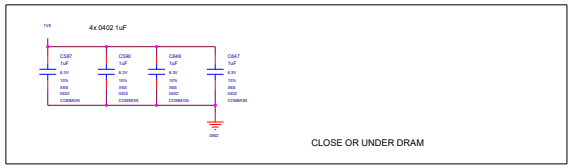

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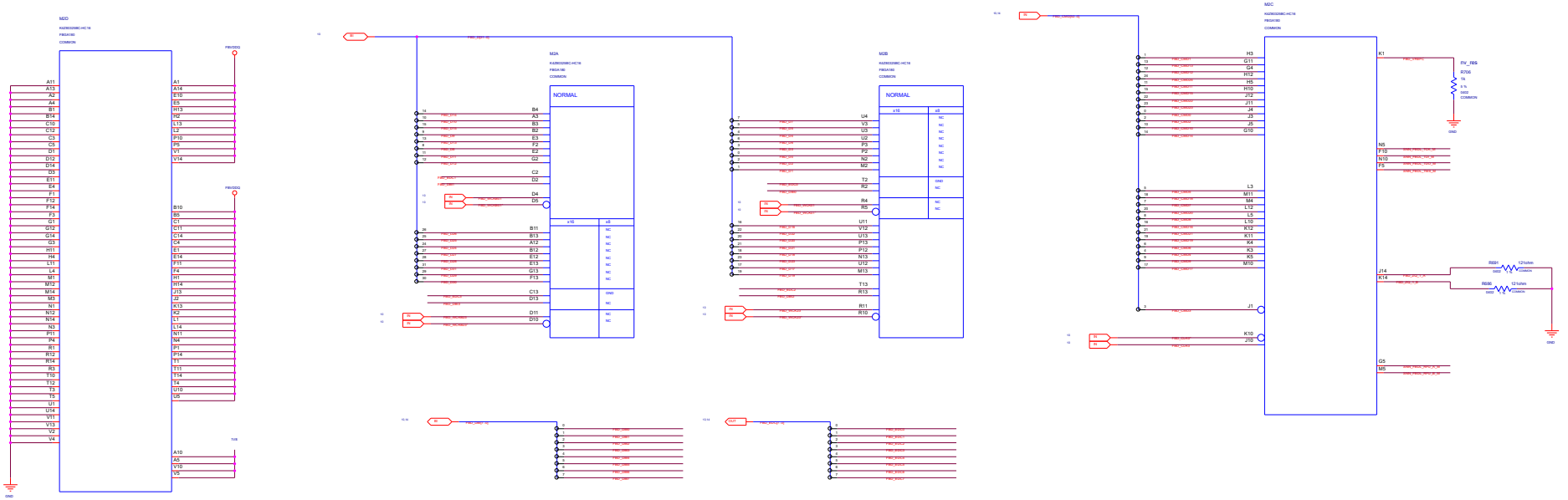

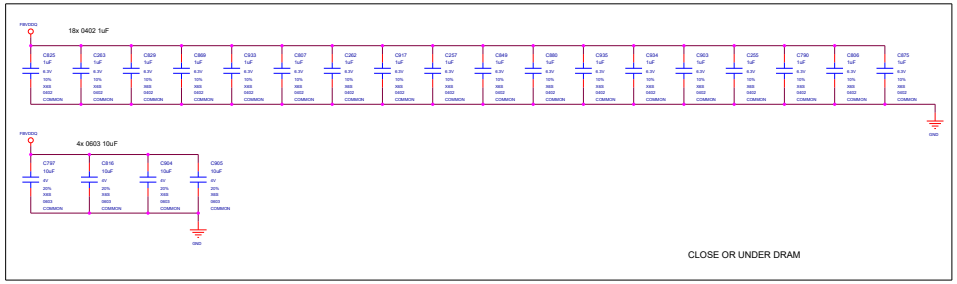

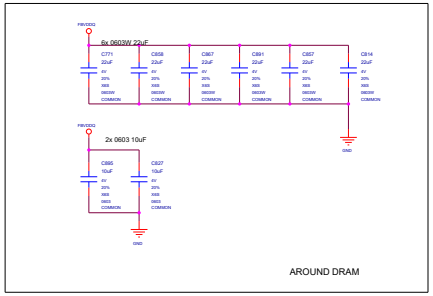

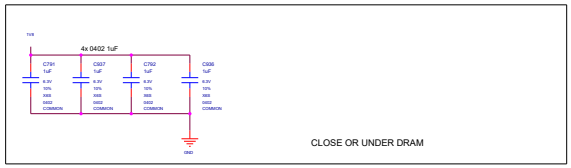

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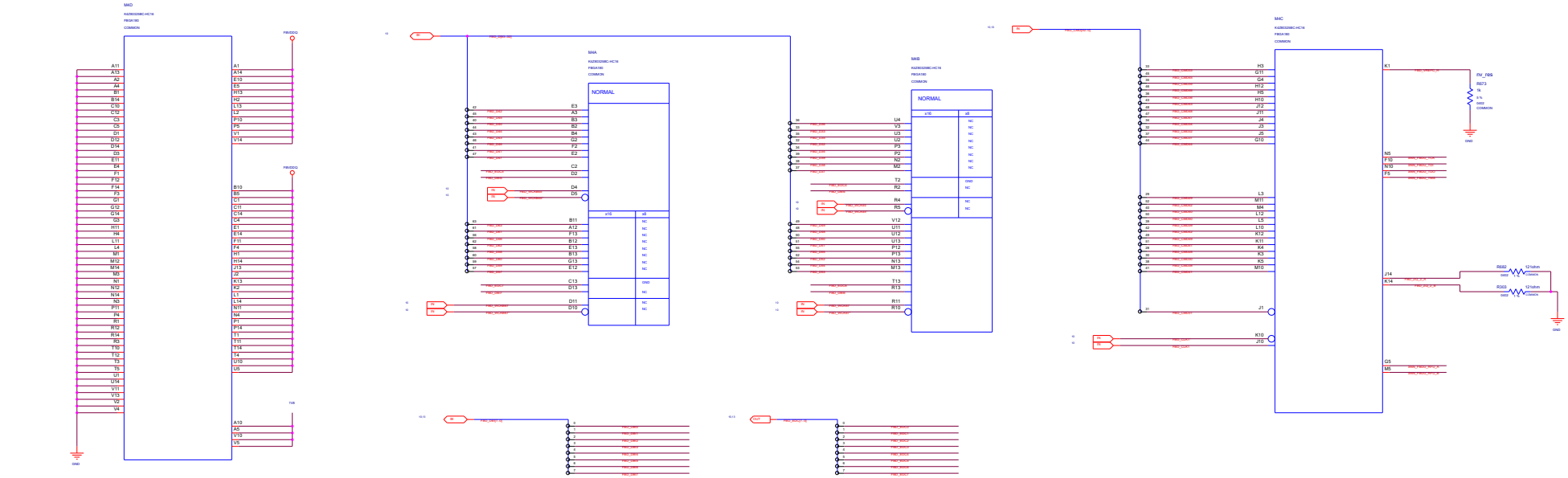
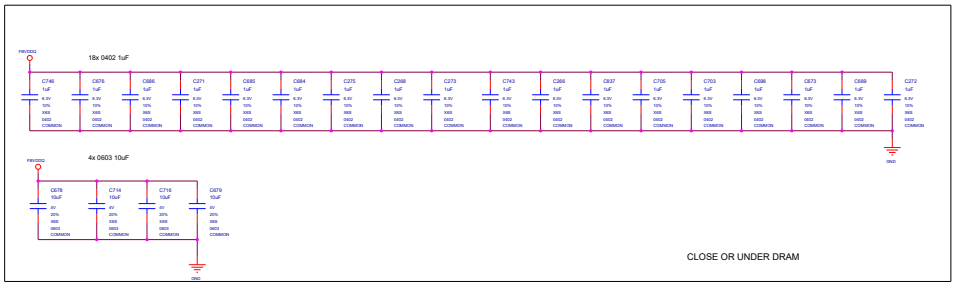
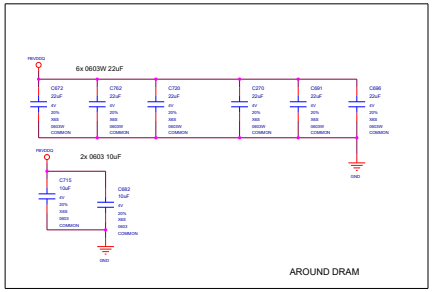
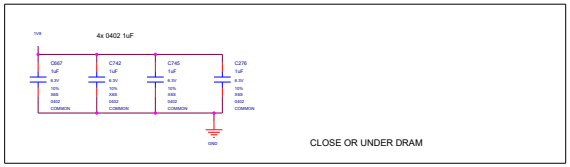




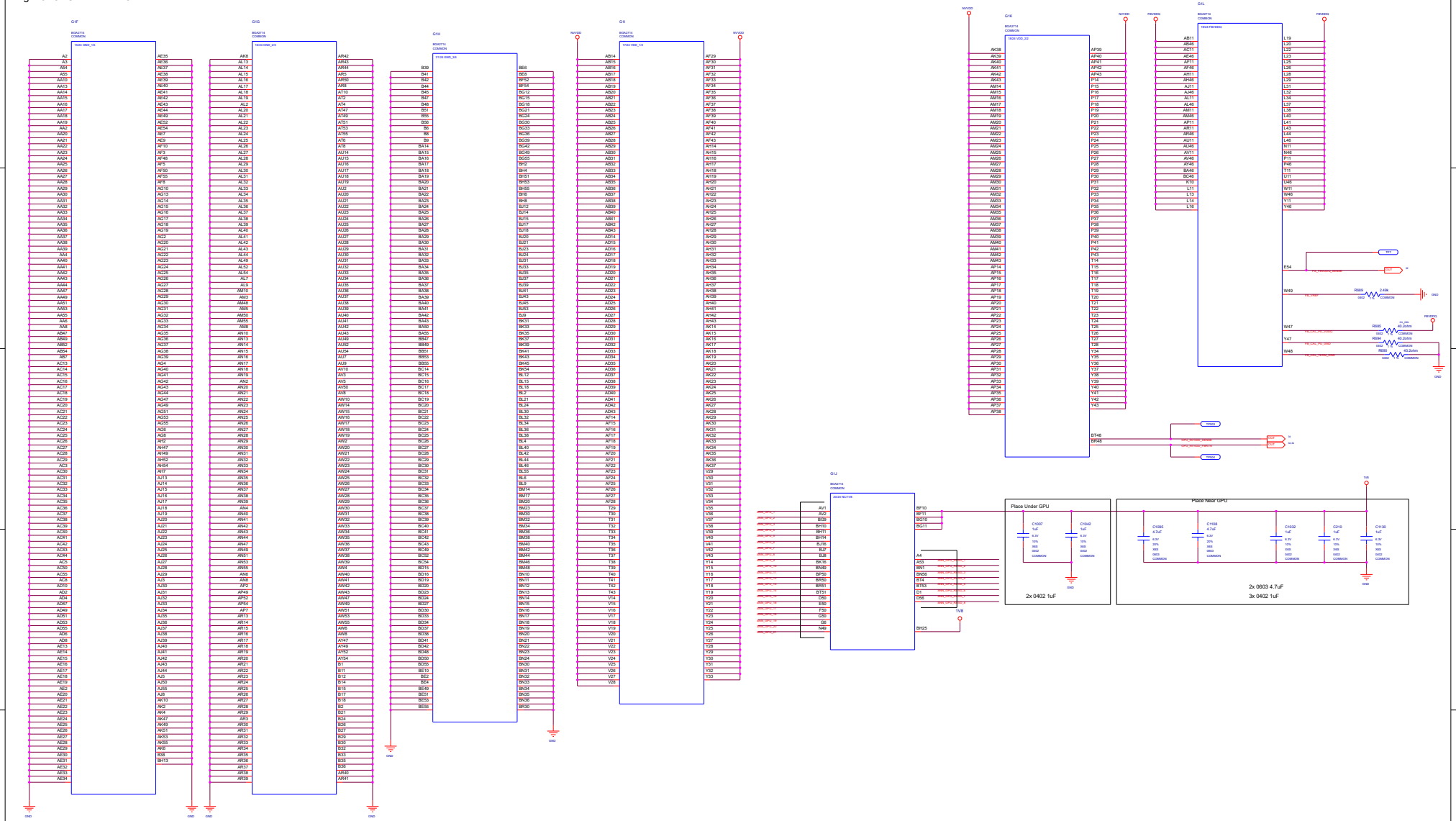




ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD[63:32]

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	14 OF 54
DATE	27-JUN-2020

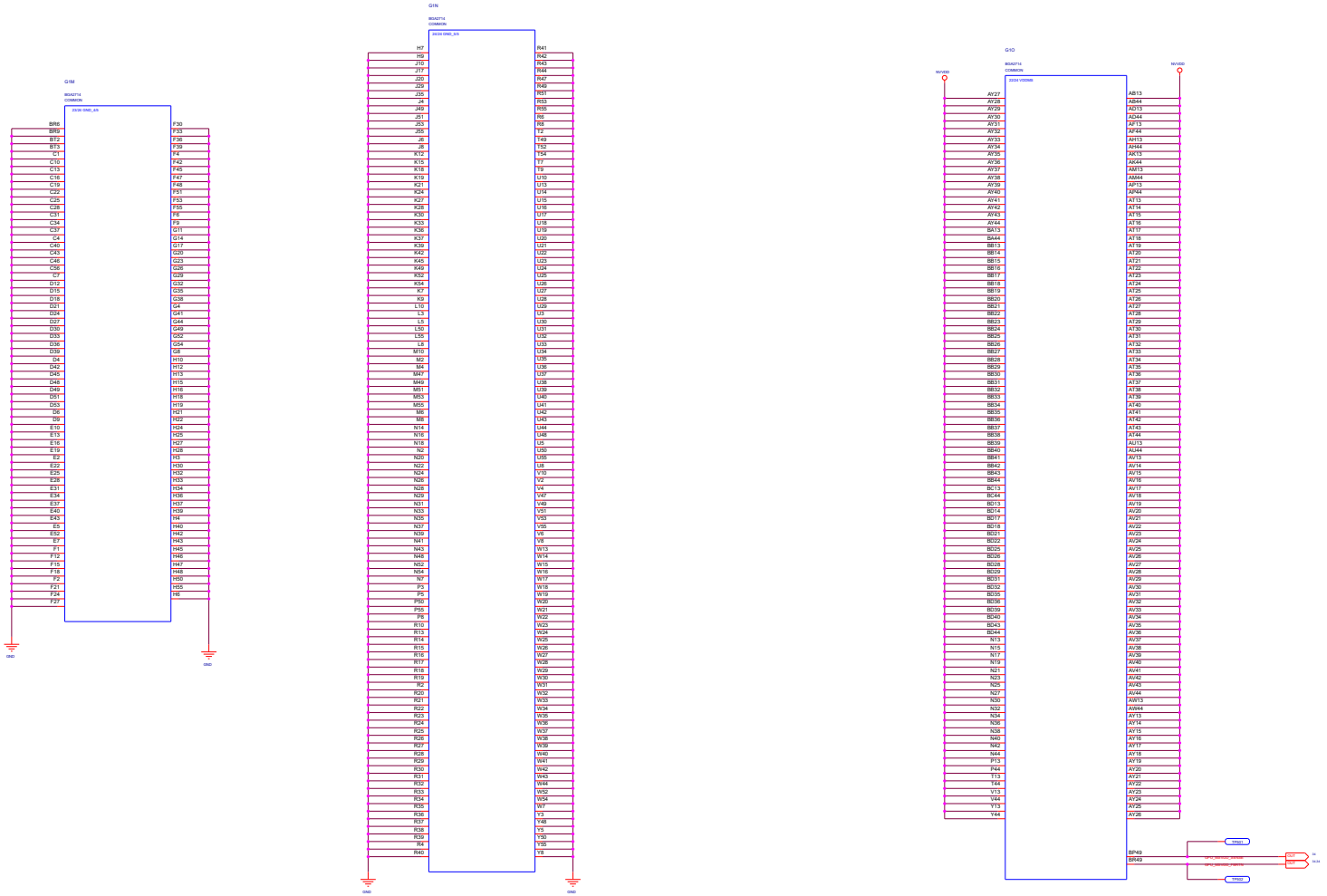
Page15: GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	15 OF 54
BOM REV	A	DATE	27-JUN-2020

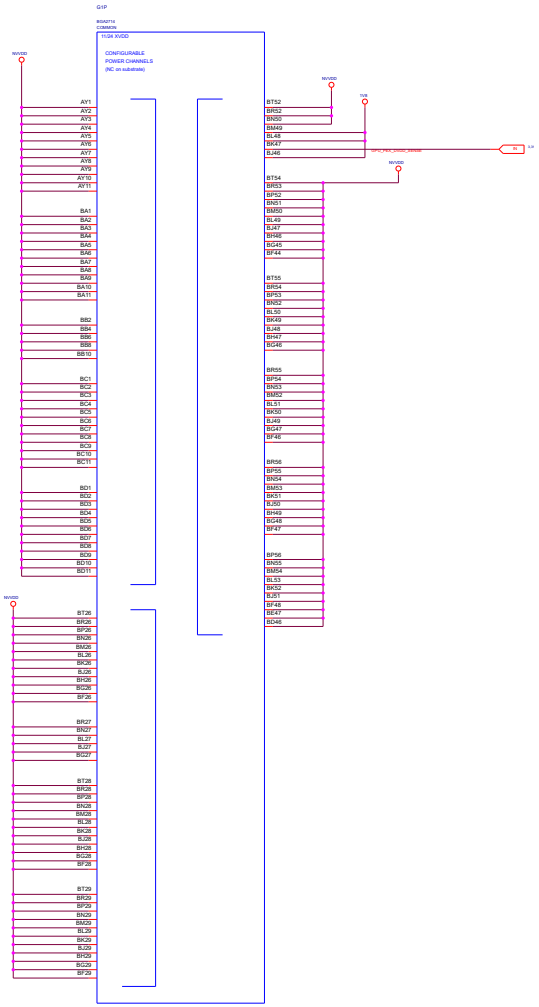
Page16: GPU PWR and GND 2



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND 2

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	16 OF 54
BOM REV	A	DATE	27-JUN-2020

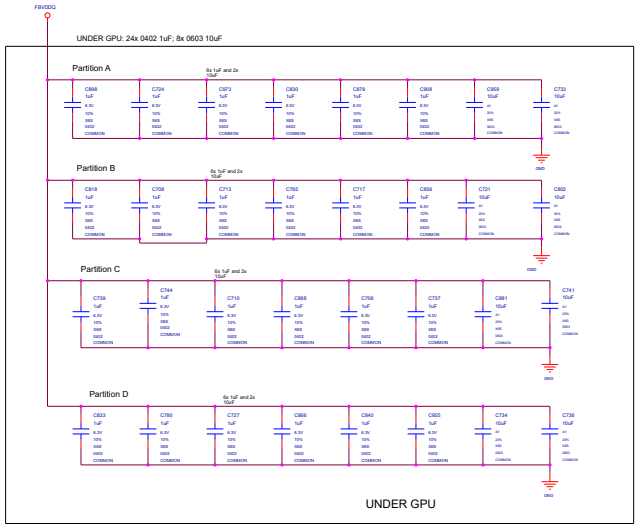


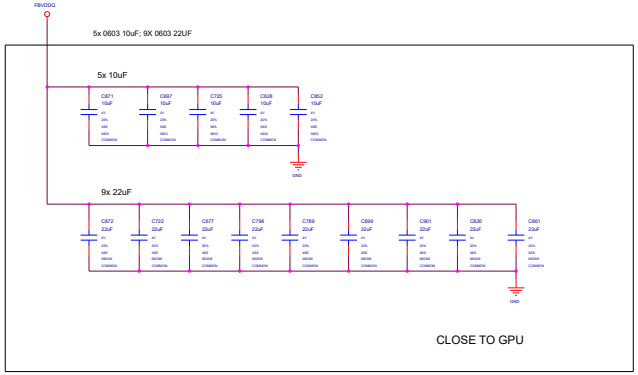
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND 3 (NVDD)

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	17 OF 54
BOM REV	A	DATE	27-JUN-2020

FBVDDQ





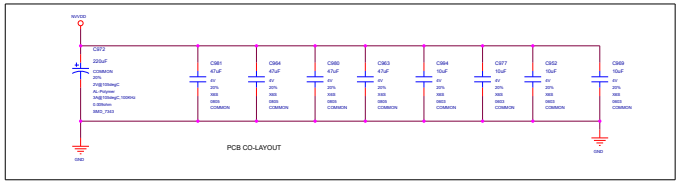
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING FBVDDQ

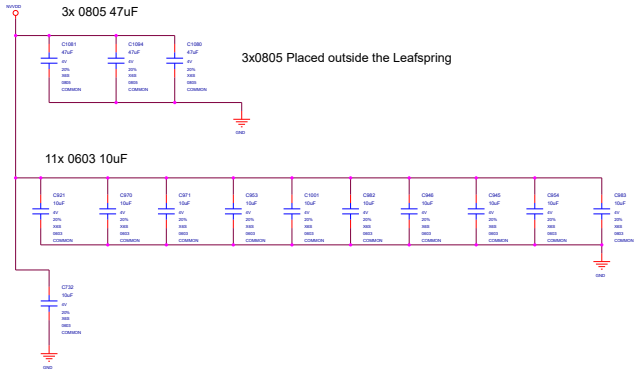
[redacted]

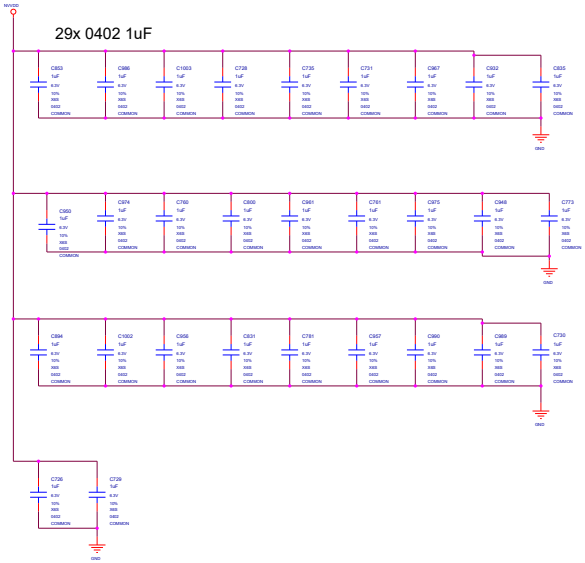
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	18 OF 54
BOM REV	A	DATE	27-JUN-2020

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	19 OF 54
DATE	27-JUN-2020



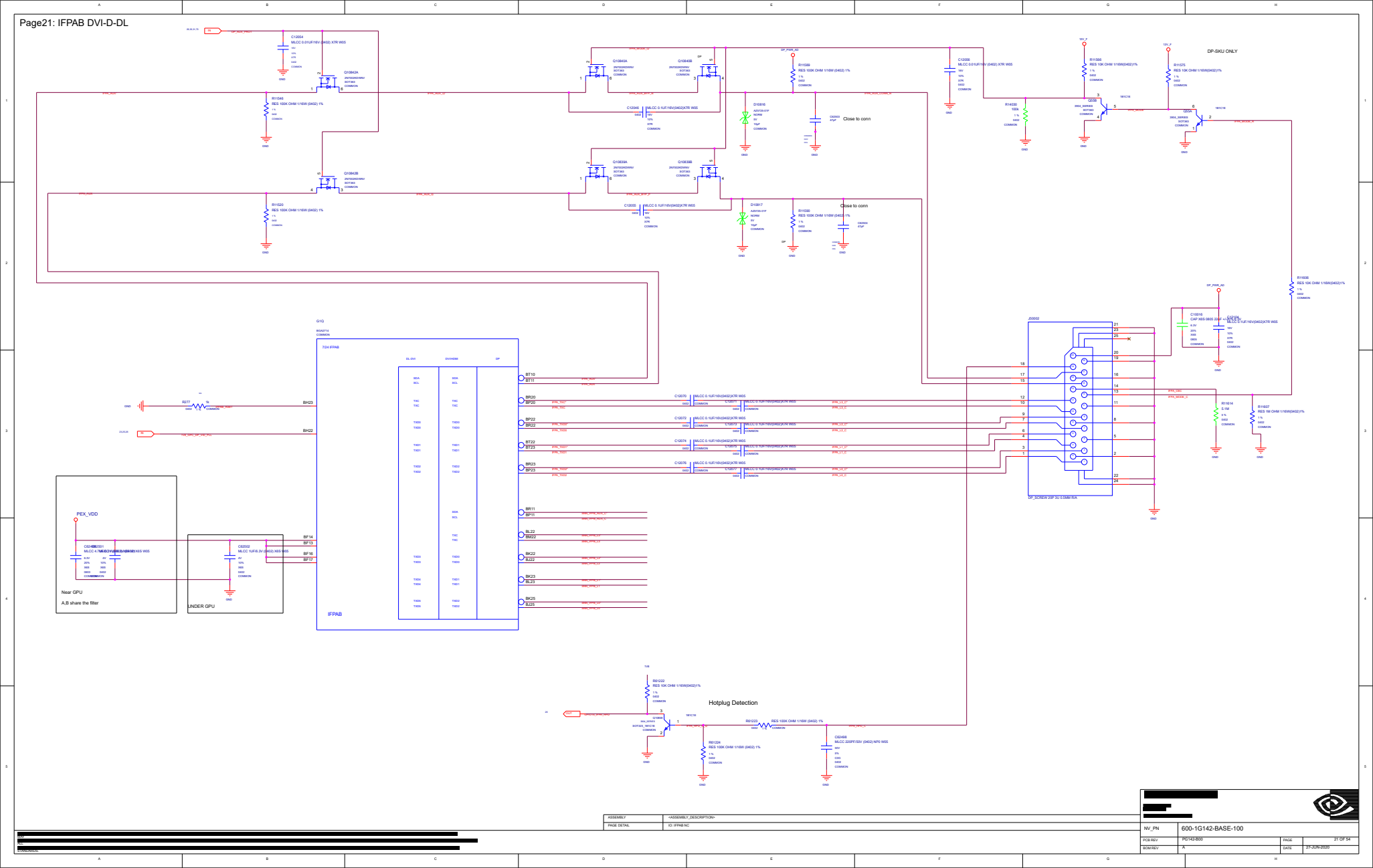




UNDER GPU

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

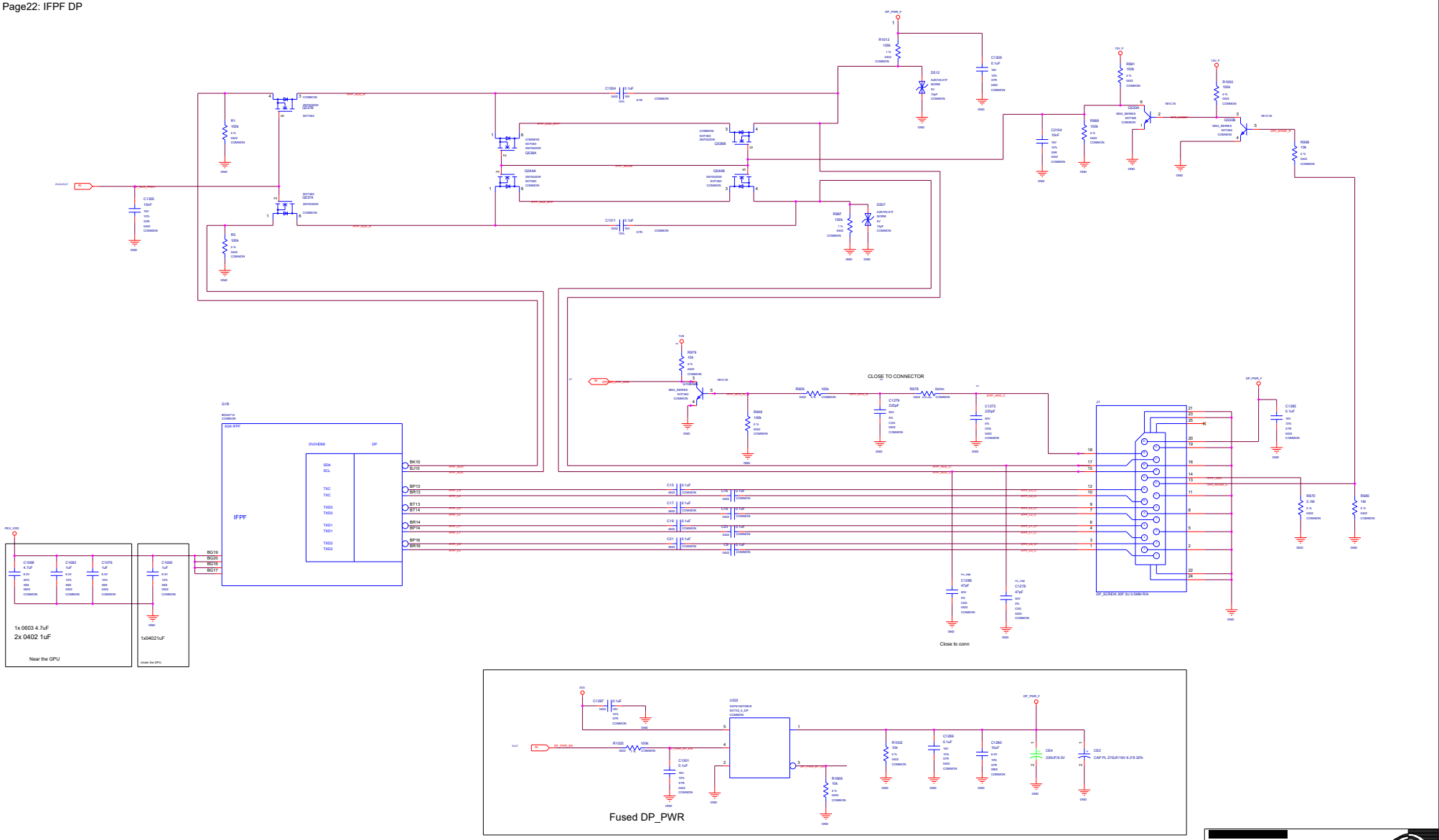
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	20 OF 54
DATE	27-JUN-2020



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPAB NC

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
PAGE	21 OF 54
BOM REV	A
DATE	27-JUN-2020

Page22: IFPF DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPF DP

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	22 OF 54
DATE	27-JUN-2020

1. DP AUX to DP connector: AUX AC coupled

2. DP AUX to DP-DVI dongle: AUX pass through

Close to conn

Close to conn

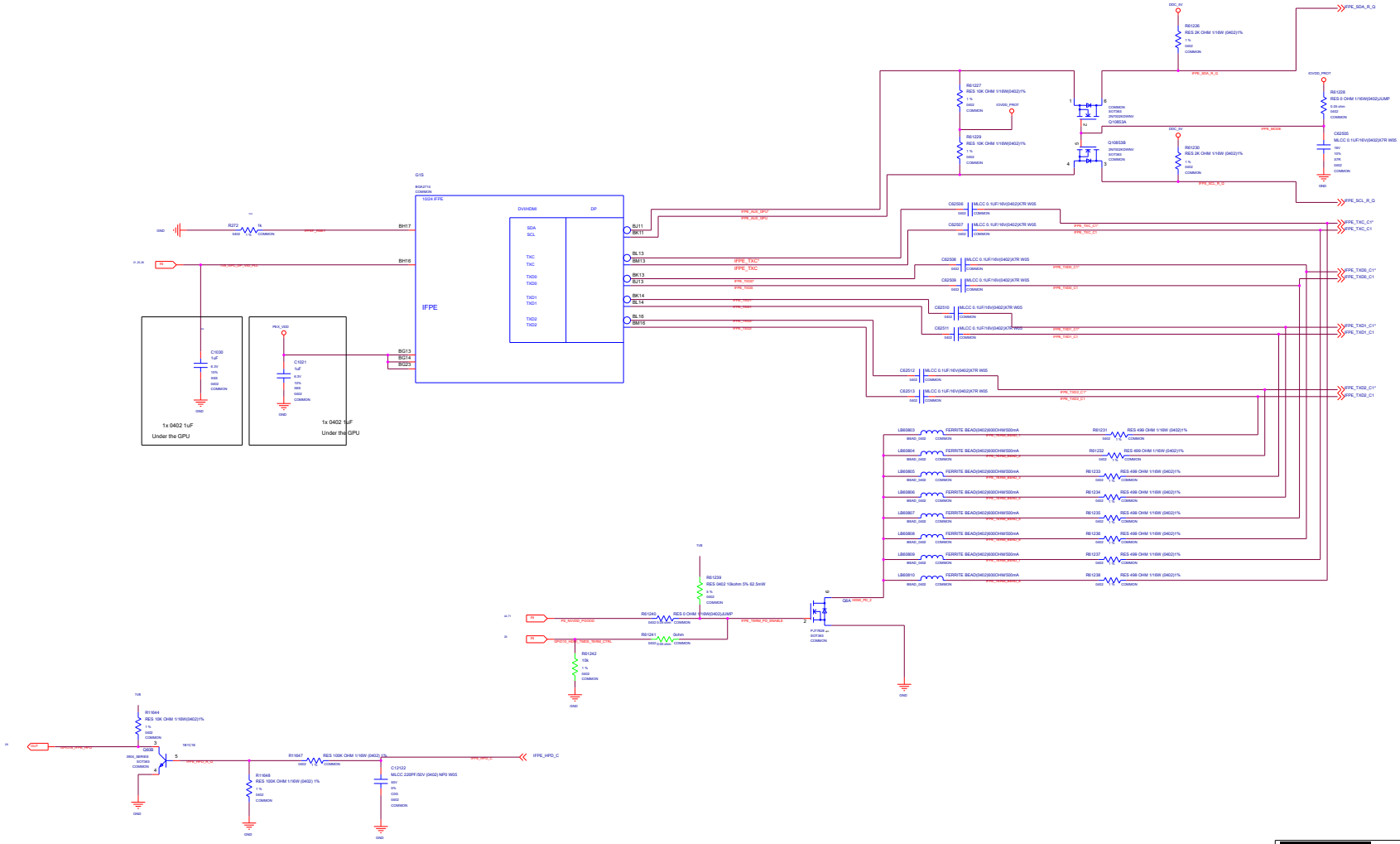
Hotplug Detection

1x 0402 1uF

(was 1x 0201W 0.47uF)

Fused DP_PWR

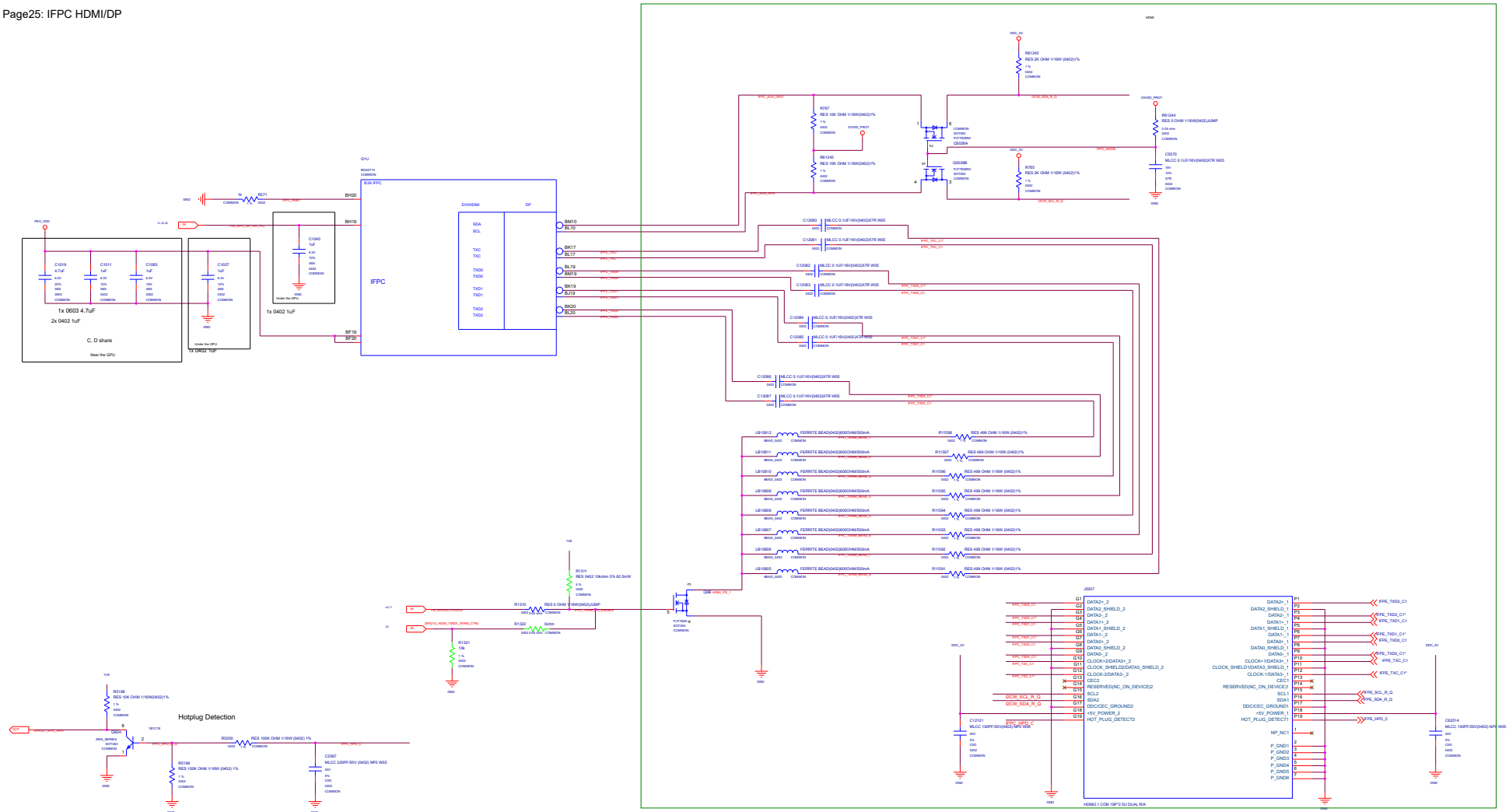
IFPE UPPER HDMI



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPE DP

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
PAGE	23 OF 54
BOM REV	A
DATE	27-JUN-2020

Page25: IFPC HDMI/DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI/DP

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	25 OF 54
DATE	27-JUN-2020

Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

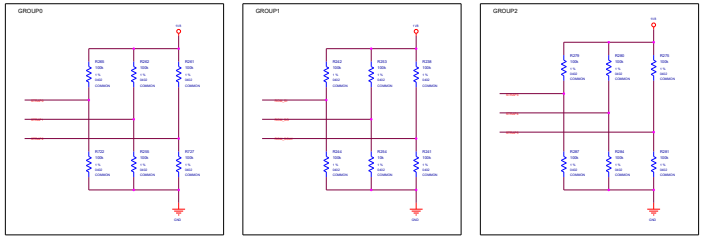
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

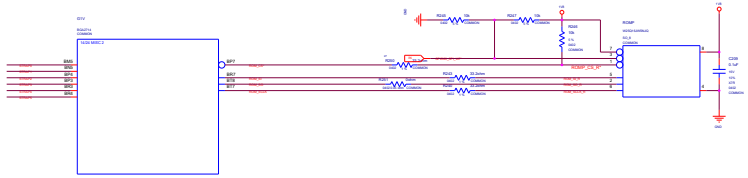
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

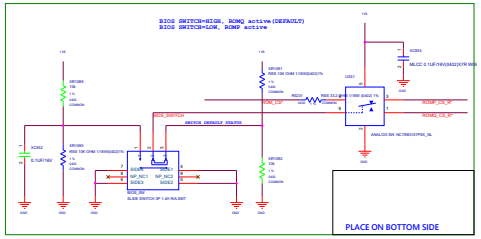
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

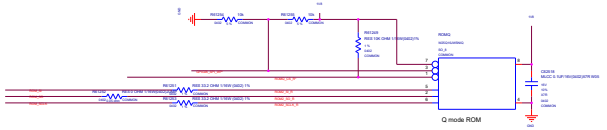
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

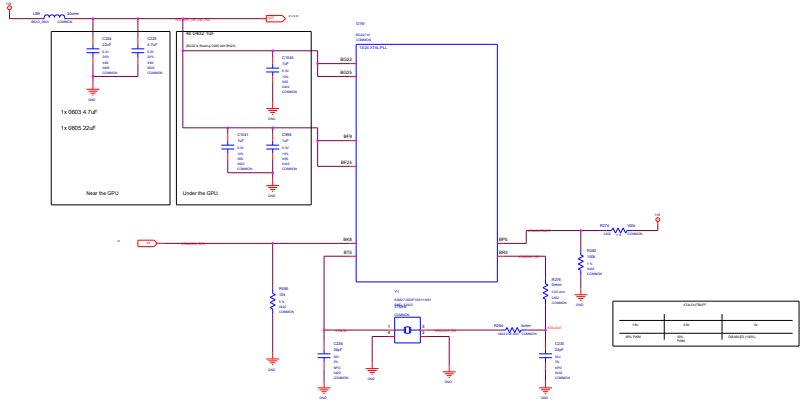






Default

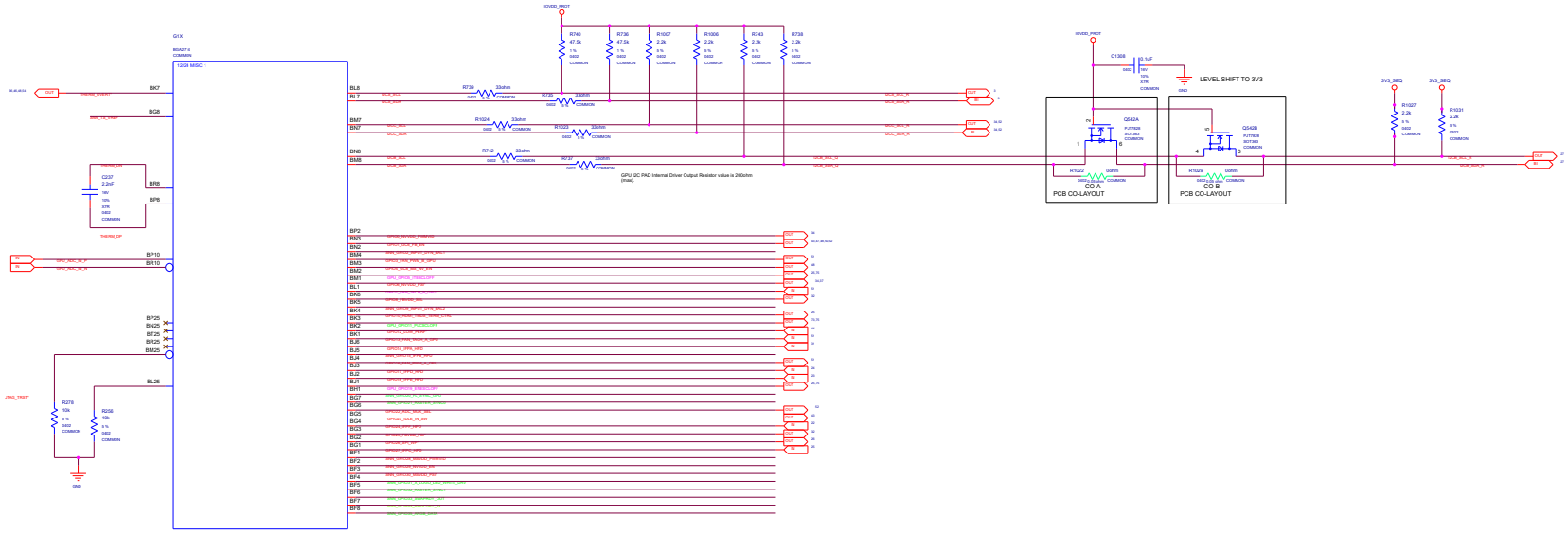




ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE TITLE	MISC2: ROM, XTAL, STRAPS

NV_PN	600-1G142-BASE-100
TITLE	TITLE Block
PAGE	26 OF 54
SCH REV	A
DATE	07-JUN-2020

Page27: MISC1: JTAG, GPIO, ADC, I2C, OVERT



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: JTAG,GPIO,ADC,I2C,FL,STEERO

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	27 OF 54
DATE	27-JUN-2020

Page28: RGB

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC3: RGB

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	28 OF 54
BOM REV	A	DATE	27-JUN-2020

BLANK PAGE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	BLANK PAGE

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	35 OF 54
BOM REV	A	DATE	27-JUN-2020

Page42: Input Power Balancing Switcher

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: OVRS_INPUT POWER BALANCE

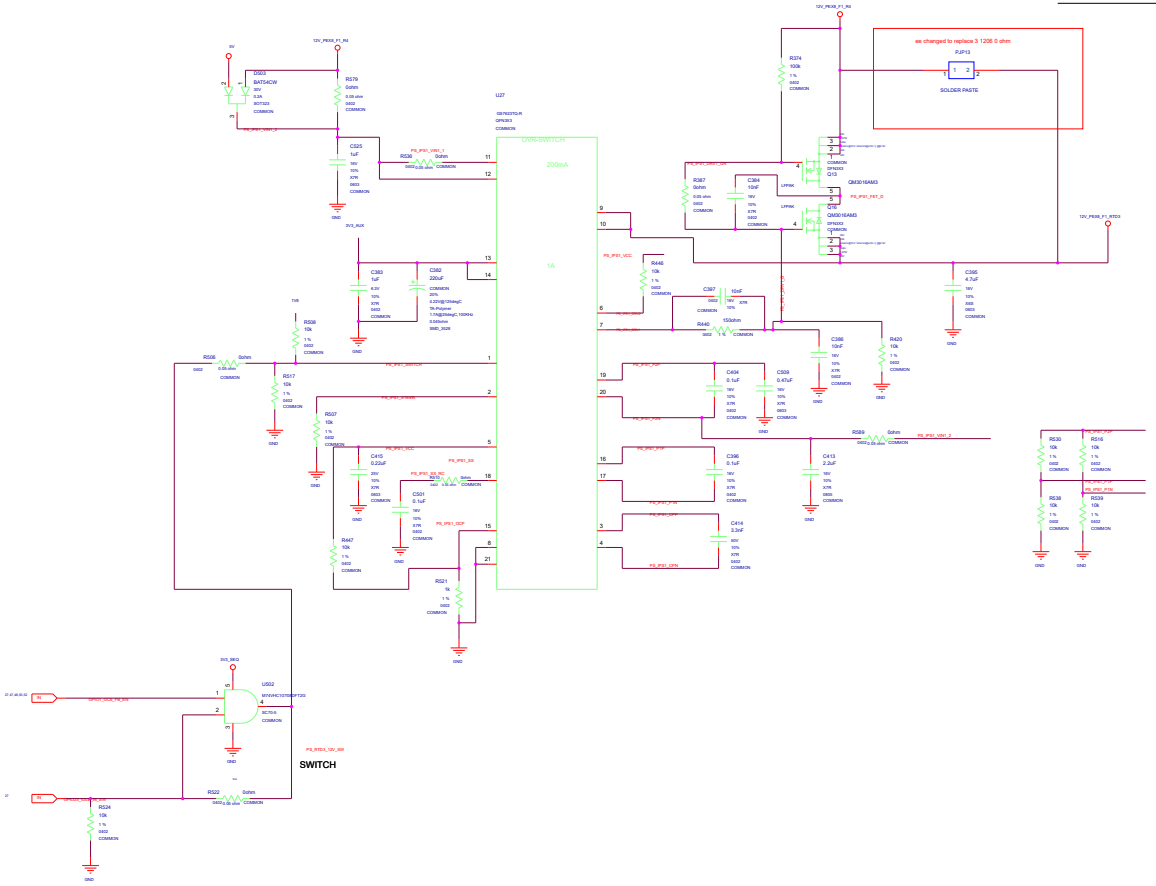
[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	42 OF 54
BOM REV	A	DATE	27-JUN-2020

AND GATE LOGIC

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

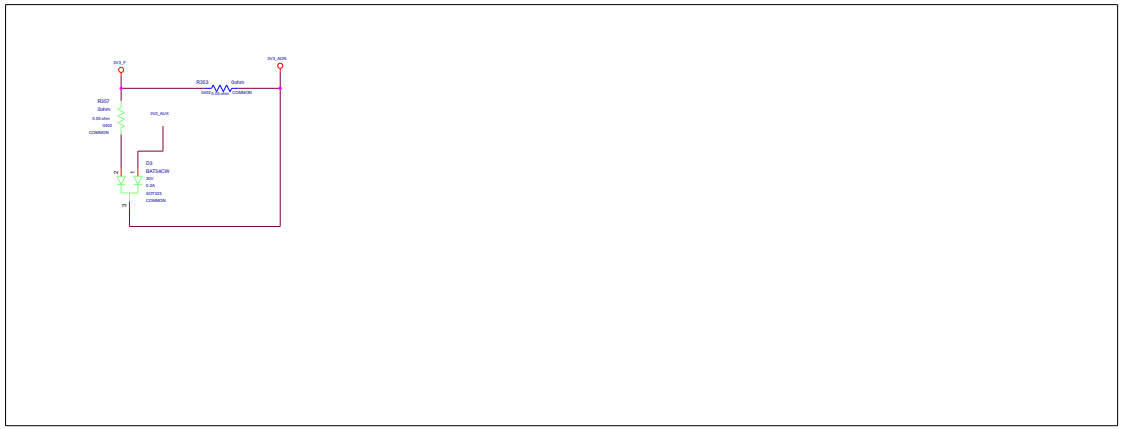
SWITCH	VOUT
0	VOUT = VIN1
1	VOUT = VIN2



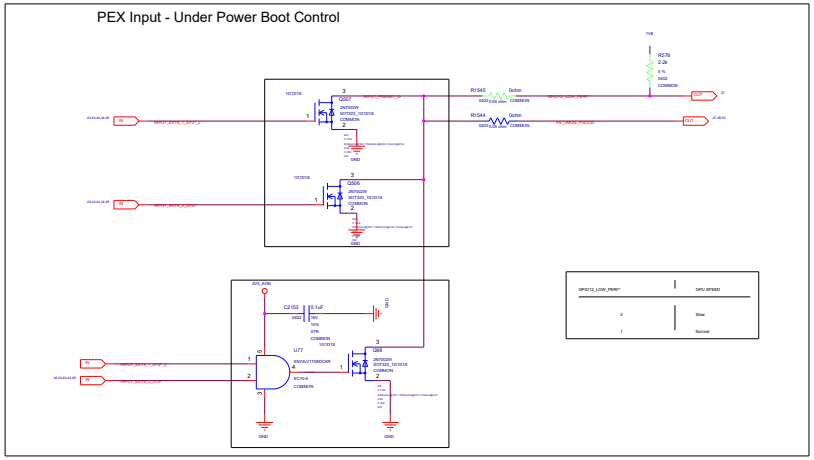
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: RDT3_12V & 3V3_A Switcher

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	43 OF 54
BOM REV	A	DATE	27-JUN-2020

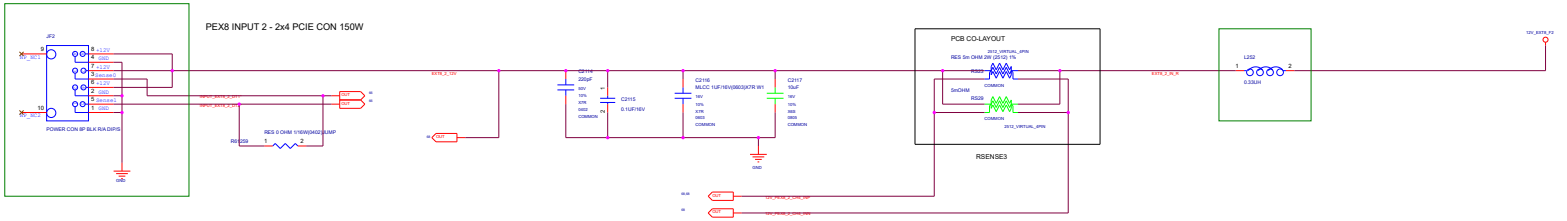
Page44: 12V_EXT_INPUT, FILTERING & UNDER POWER BOOT



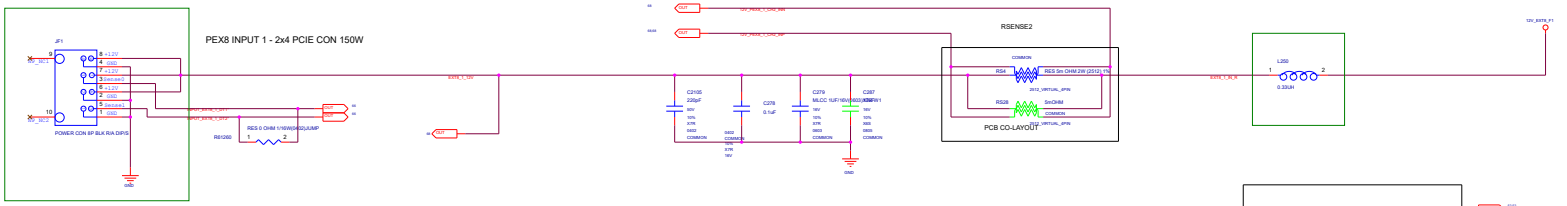
PEX Input - Under Power Boot Control

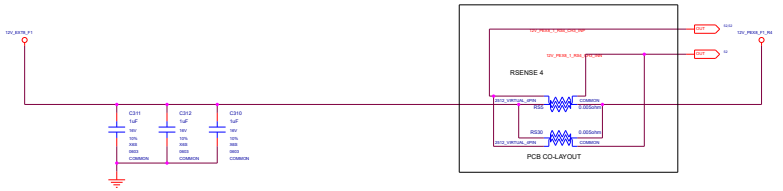


PEX8 INPUT 2 - 2x4 PCIE CON 150W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



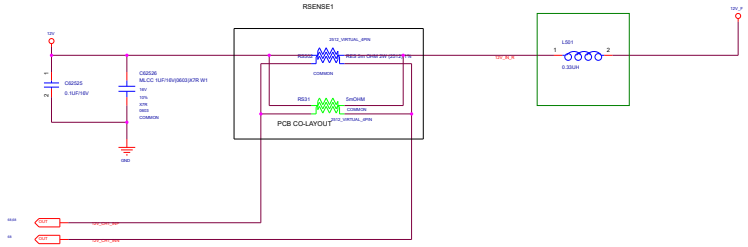


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUTS, FILTERING and MONITORING

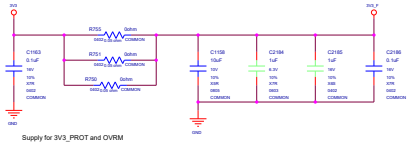
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
PAGE	44 OF 54
BOM REV	A
DATE	27-JUN-2020

Page45: PEX_INPUT & FILTERING, PEX_3V3, 3V3_AUX

PEX_12V INPUT - 66W

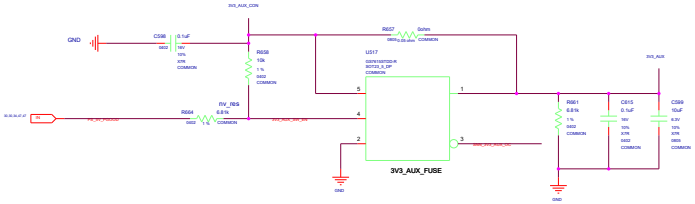


PEX 3V3 INPUT - 10W



Supply for 3V3_PROT and OVRM

3V3_AUX



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEX_12V, PEX_3V3 AND A3V3_AUX

[redacted]

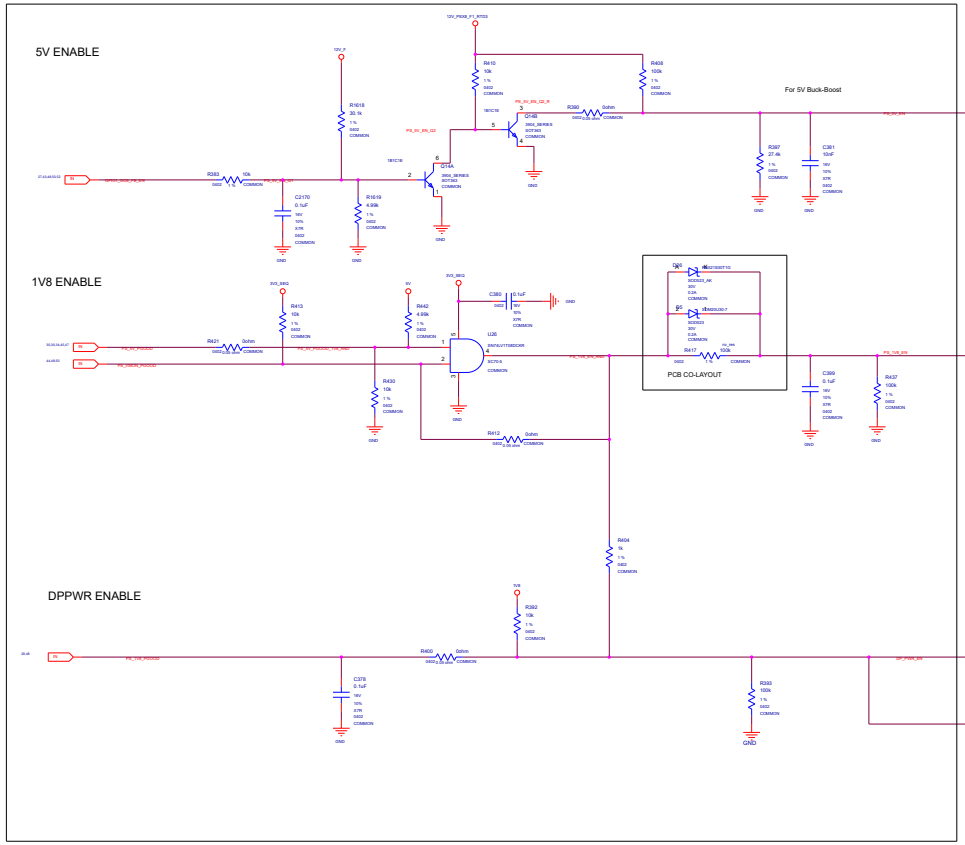
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	45 OF 54
BOM REV	A	DATE	27-JUN-2020

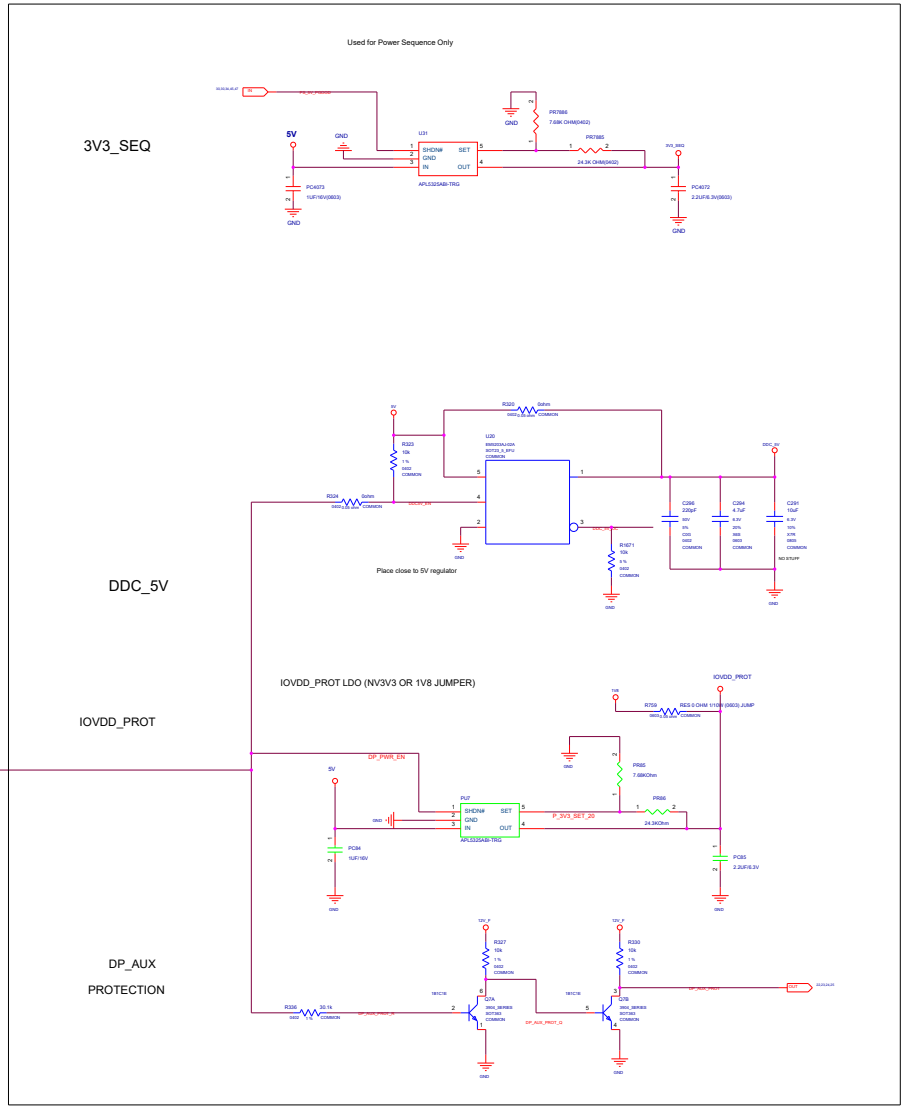
[redacted]

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPR, HOT UNPLUG

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	46 OF 54
BOM REV	A	DATE	27-JUN-2020



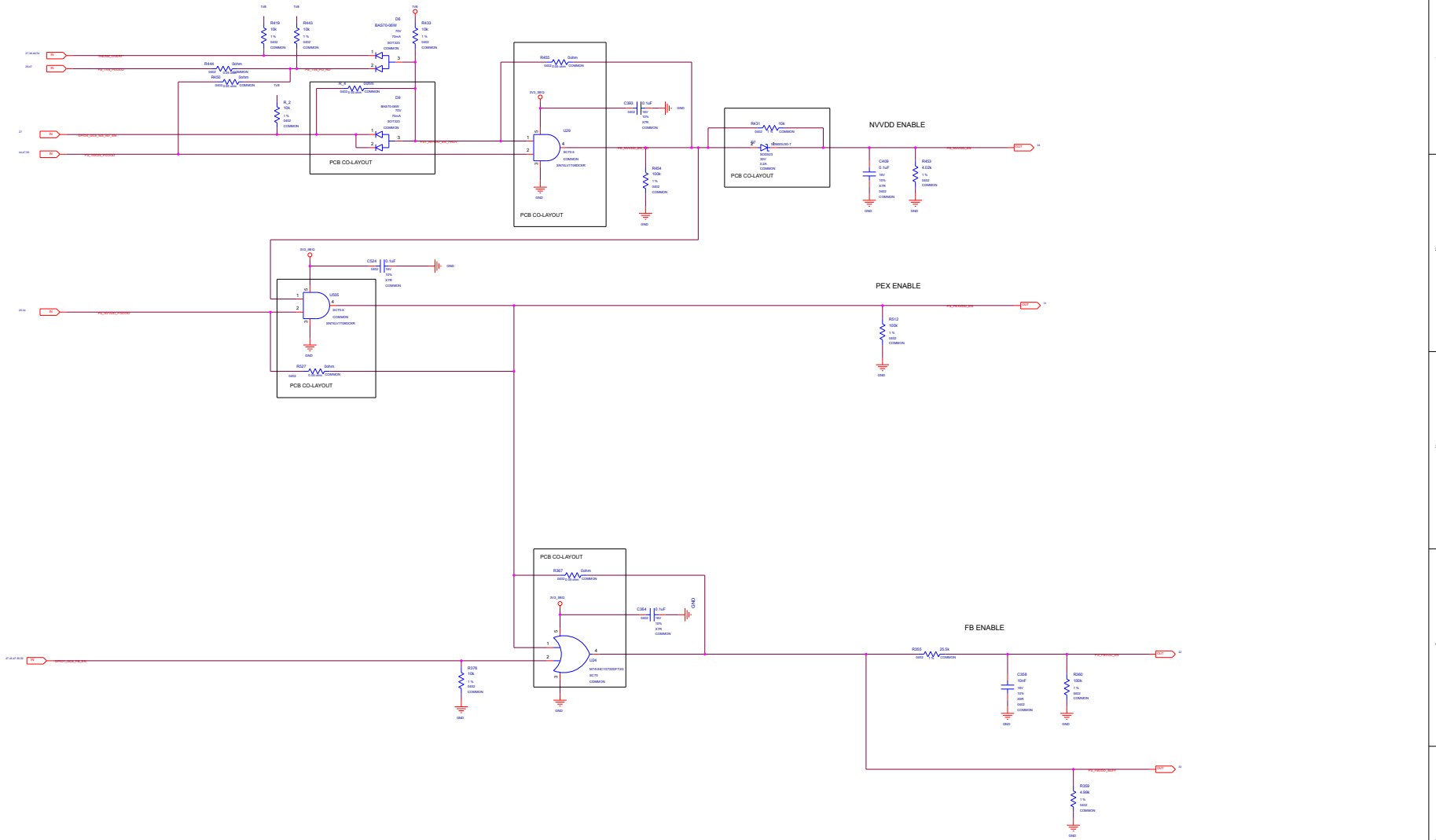


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: 5V, 1V8, 3V3_SEQ

[redacted]

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
PAGE	47 OF 54
BOM REV	A
DATE	27-JUN-2020

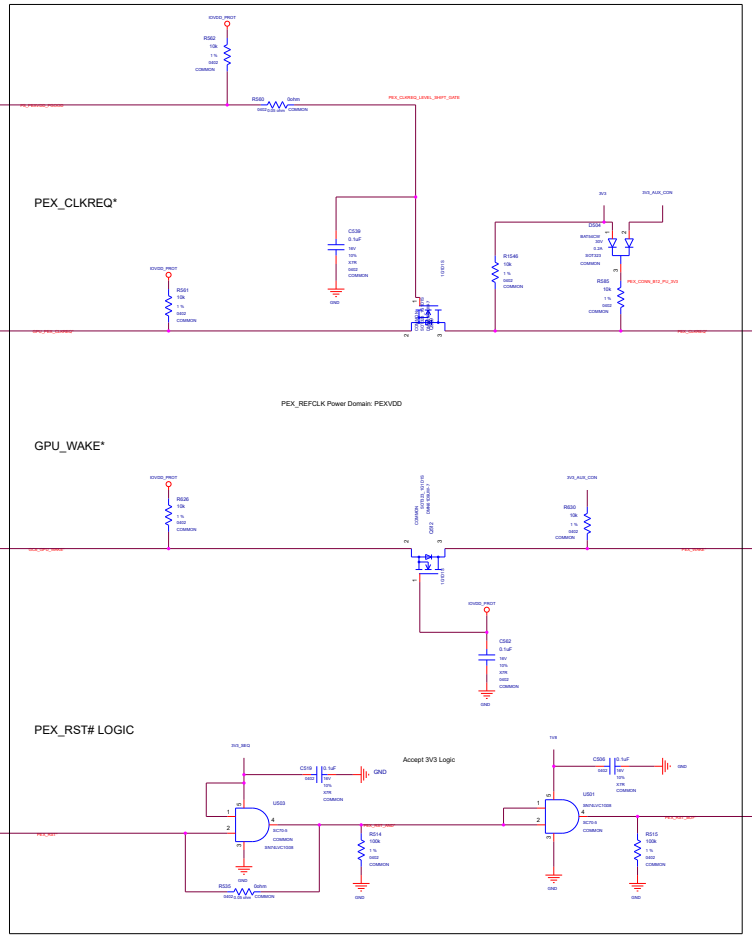
Page48: SEQ:NVVDD, PEX, FBVDDQ ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	48 OF 54
DATE	27-JUN-2020

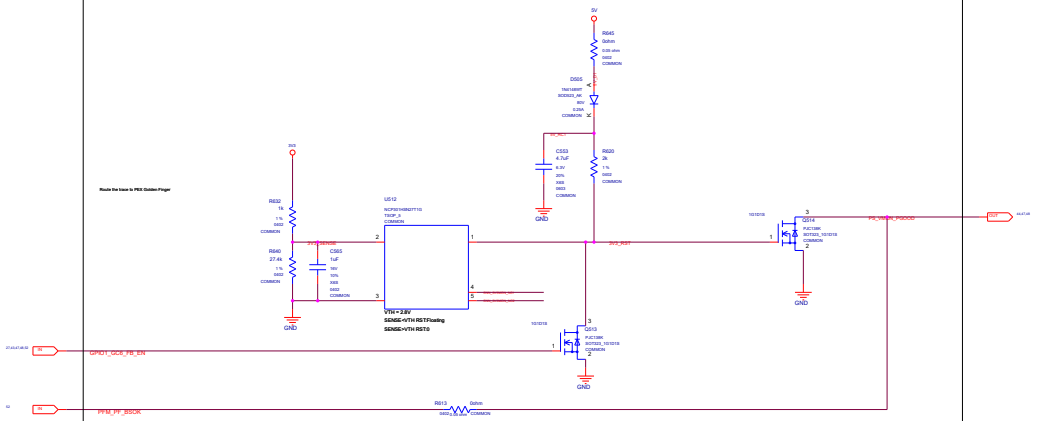
Page49: SEQ:MISC



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: MISC

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
PAGE	49 OF 54
BOM REV	A
DATE	27-JUN-2020

3V3PEX Voltage Monitor

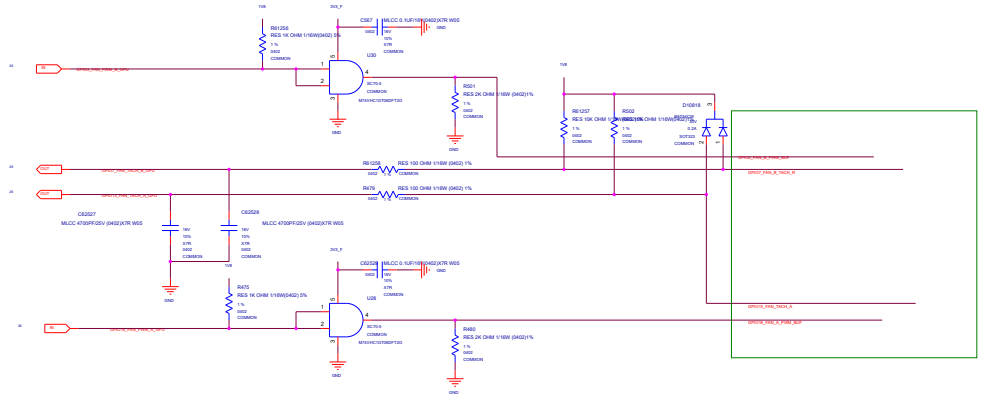


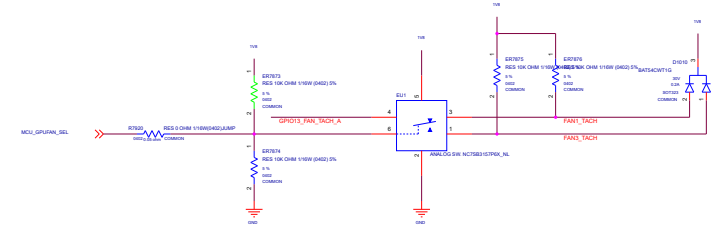
BOM Configuration

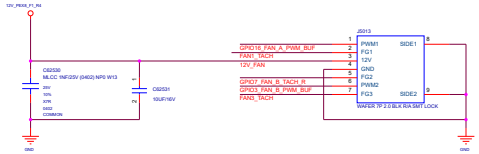
OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	**Pre-Filter**	**Pre-Filter**	**Pre-Filter**
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

Page51: FAN&LED







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FAN & LED

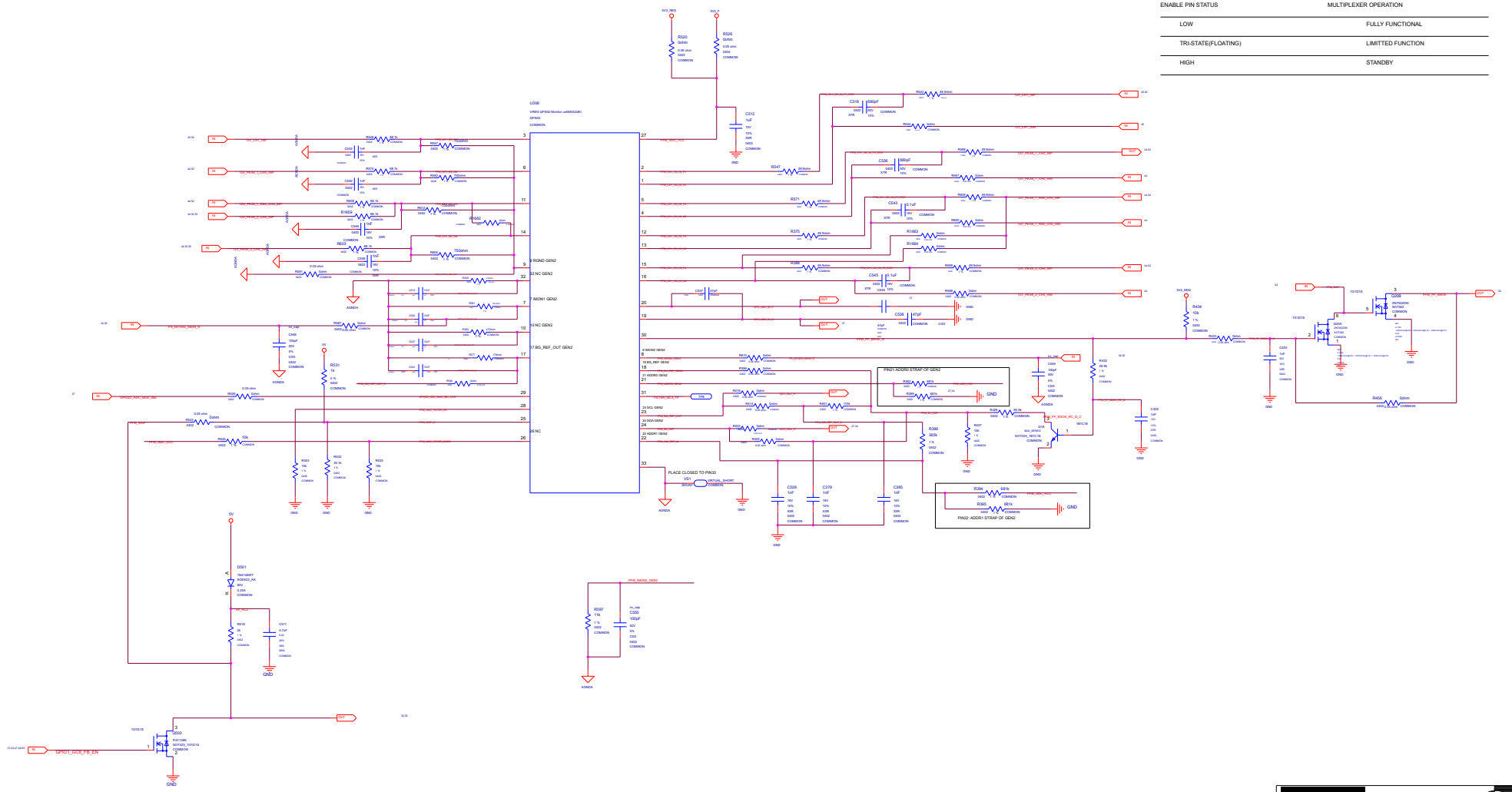
[redacted]

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	51 OF 54
DATE	27-JUN-2020

Page52: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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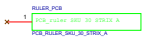
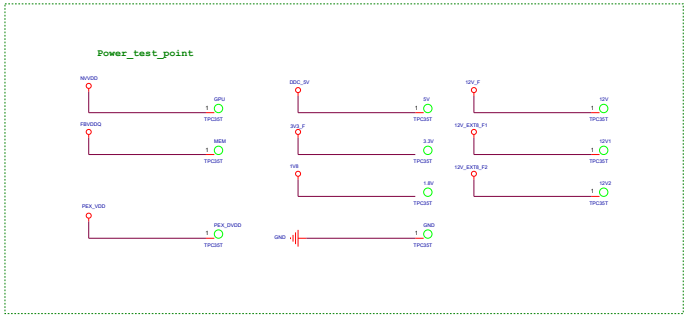
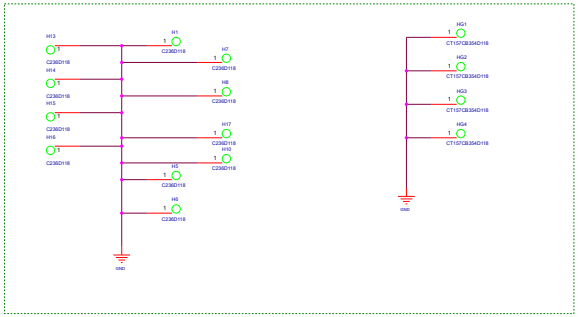
PAGE	52 OF 54
DATE	27-JUN-2020

Page53: MECH







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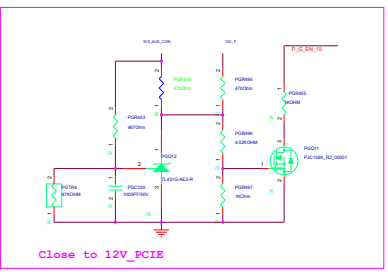
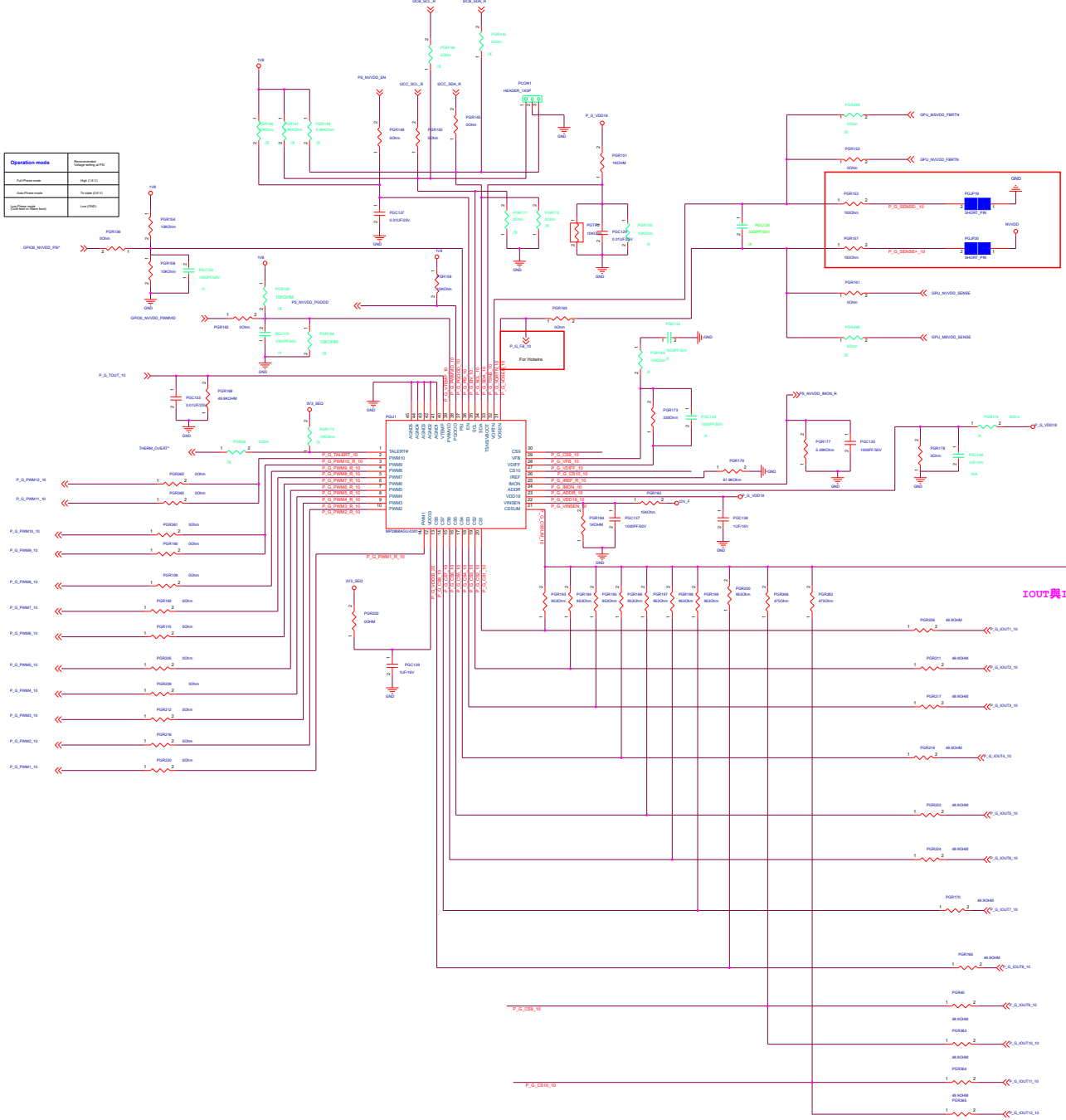
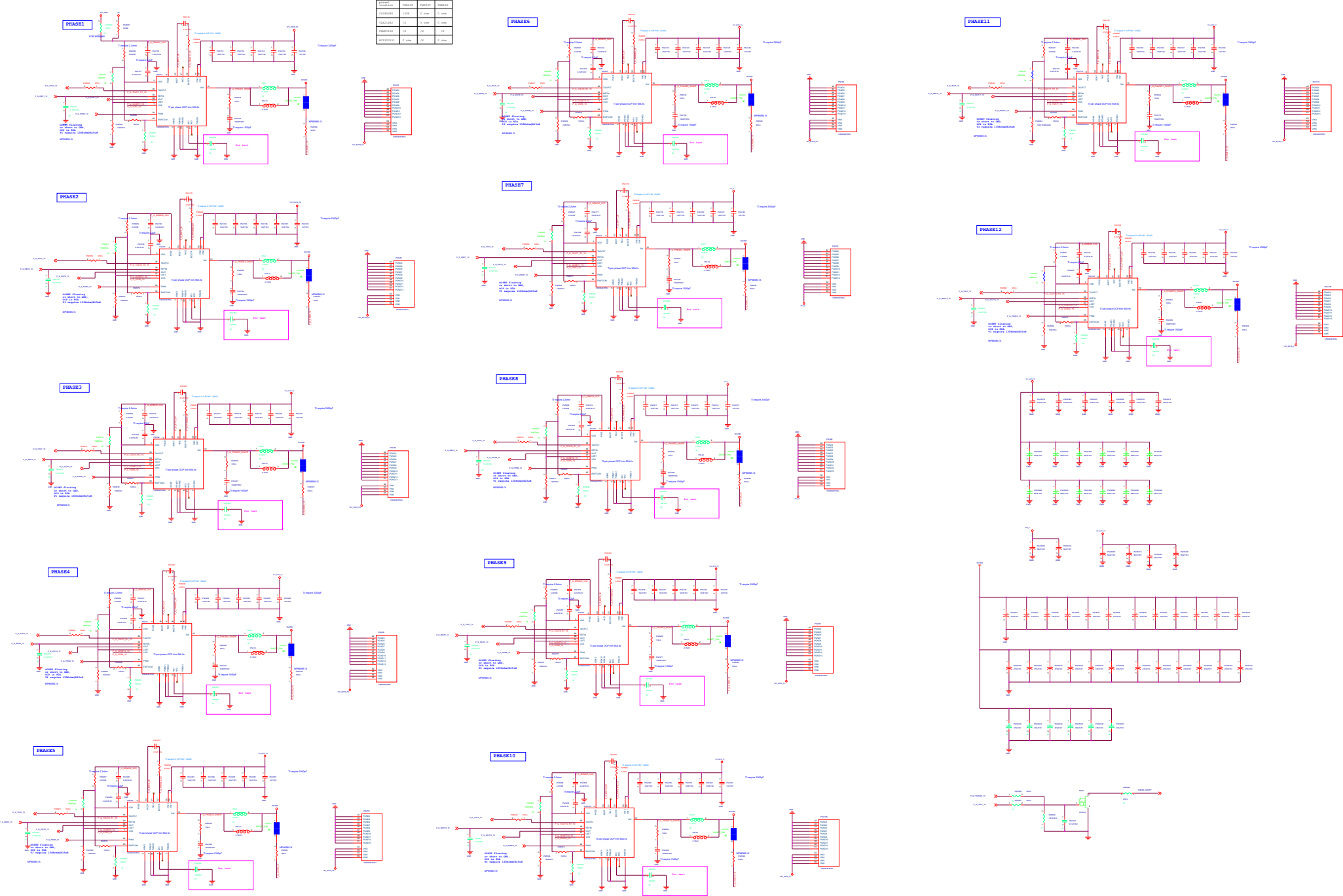
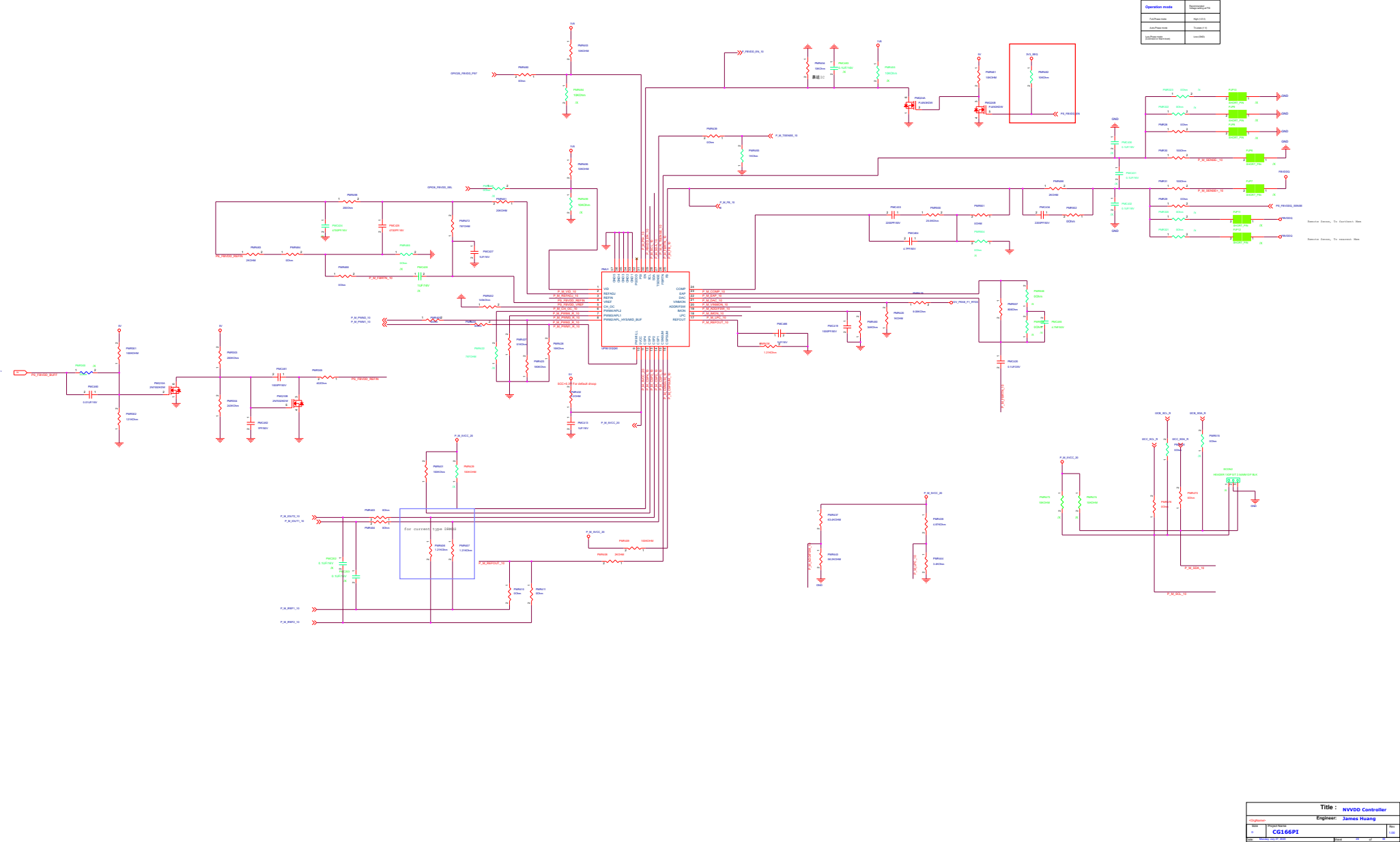
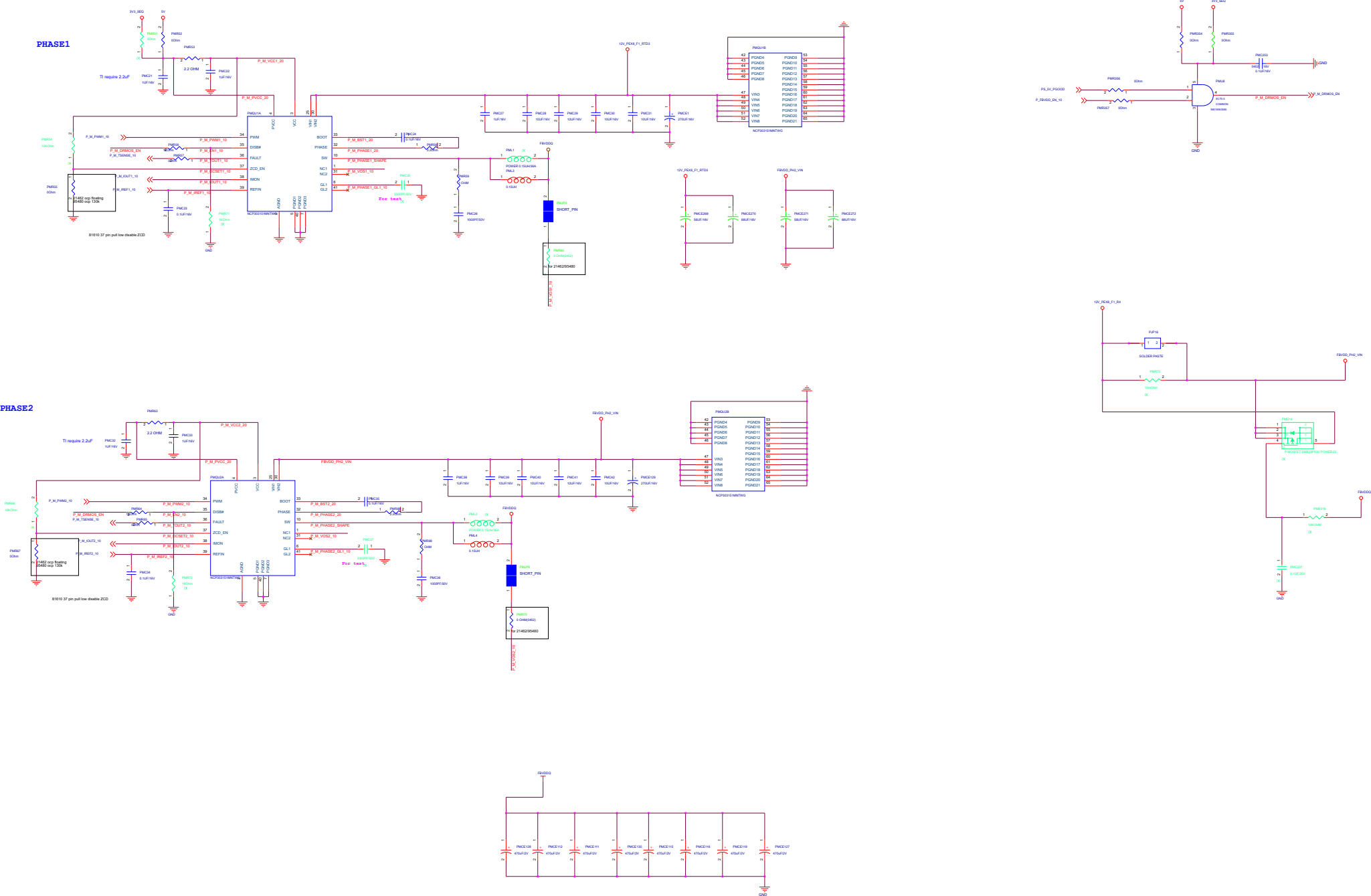


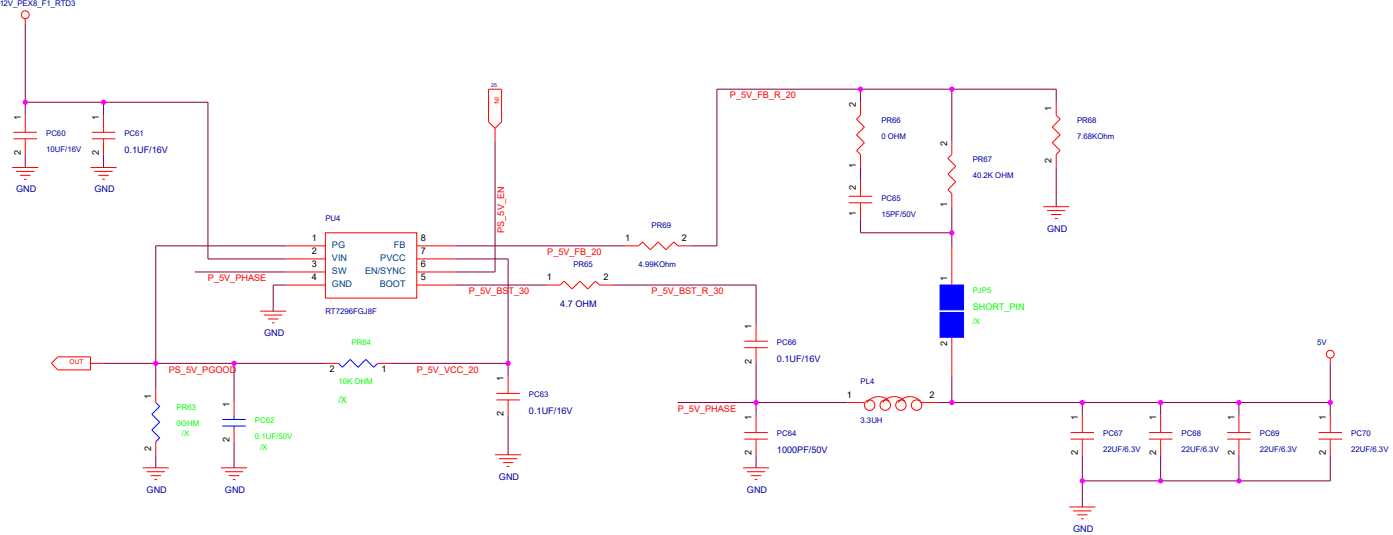
Operation mode	Recommended Voltage setting at PS5
Full Phase mode	High (1.8 V)
Auto Phase mode	Tri-state (0.9 V)
Low Power mode (Load detect on MB is level)	Low (GND)

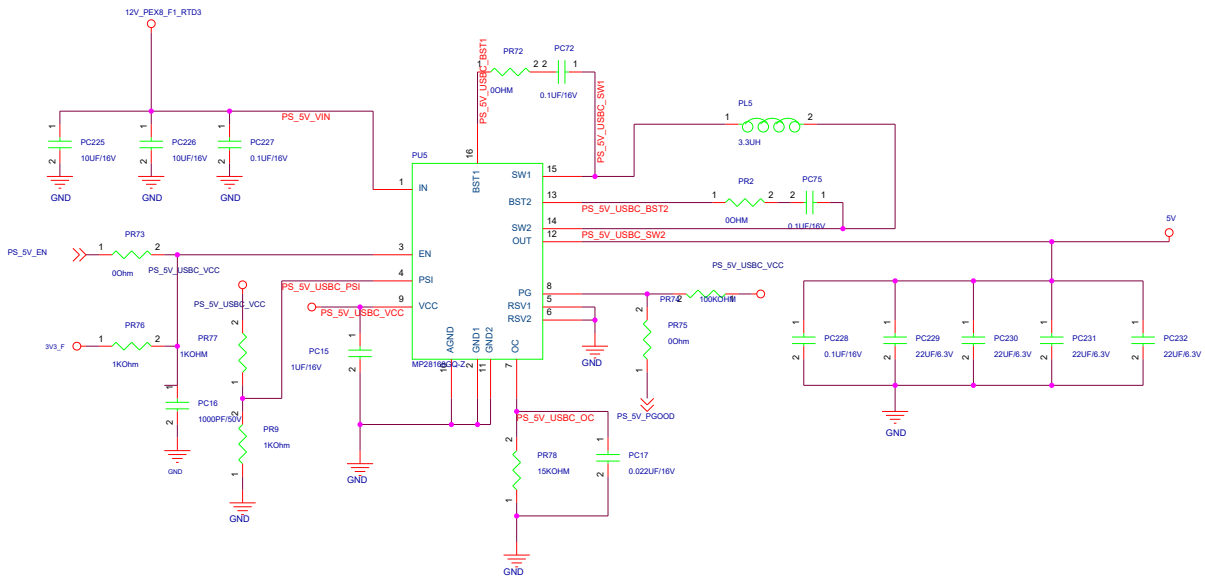



PHASE1
PHASE2
PHASE3
PHASE4
PHASE5
PHASE6
PHASE7
PHASE8
PHASE9
PHASE10
PHASE11
PHASE12


Operation mode
Recommended Voltage setting up Vin
Full Phase mode
High (>3.3V)
Auto Phase mode
Floating (1.1V)
Low Phase mode (Controlled or Hardwired)
Low (GND)
for current type DRMOS
Remote Sense, To Earthest Mem
Remote Sense, To nearest Mem
Title : NVVDD Controller
Engineer: James Huang
<Orgfalsion>
Size: D
Project Name: CG166PI
Rev: 1.00
Date: Monday, may 07, 2018
Sheet 19 of 30


PHASE1
PHASE2
TI require 2.2uF
2.2 OHM
For test
SHORT_PIN
SOLDER PASTE
GND





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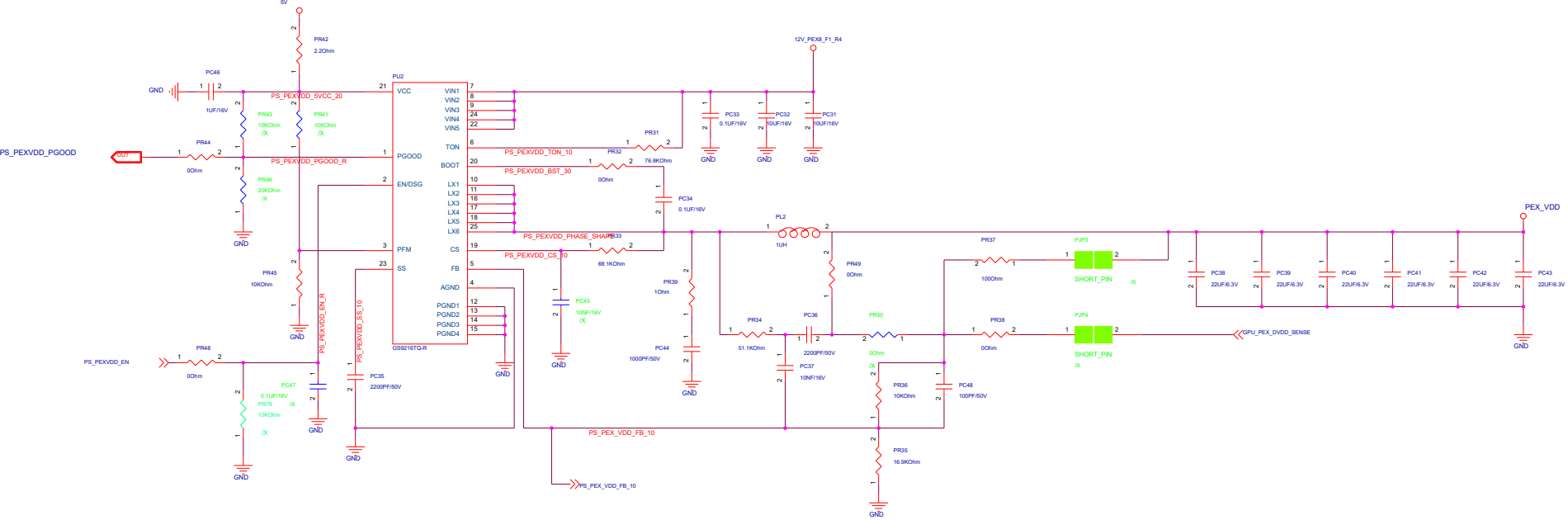

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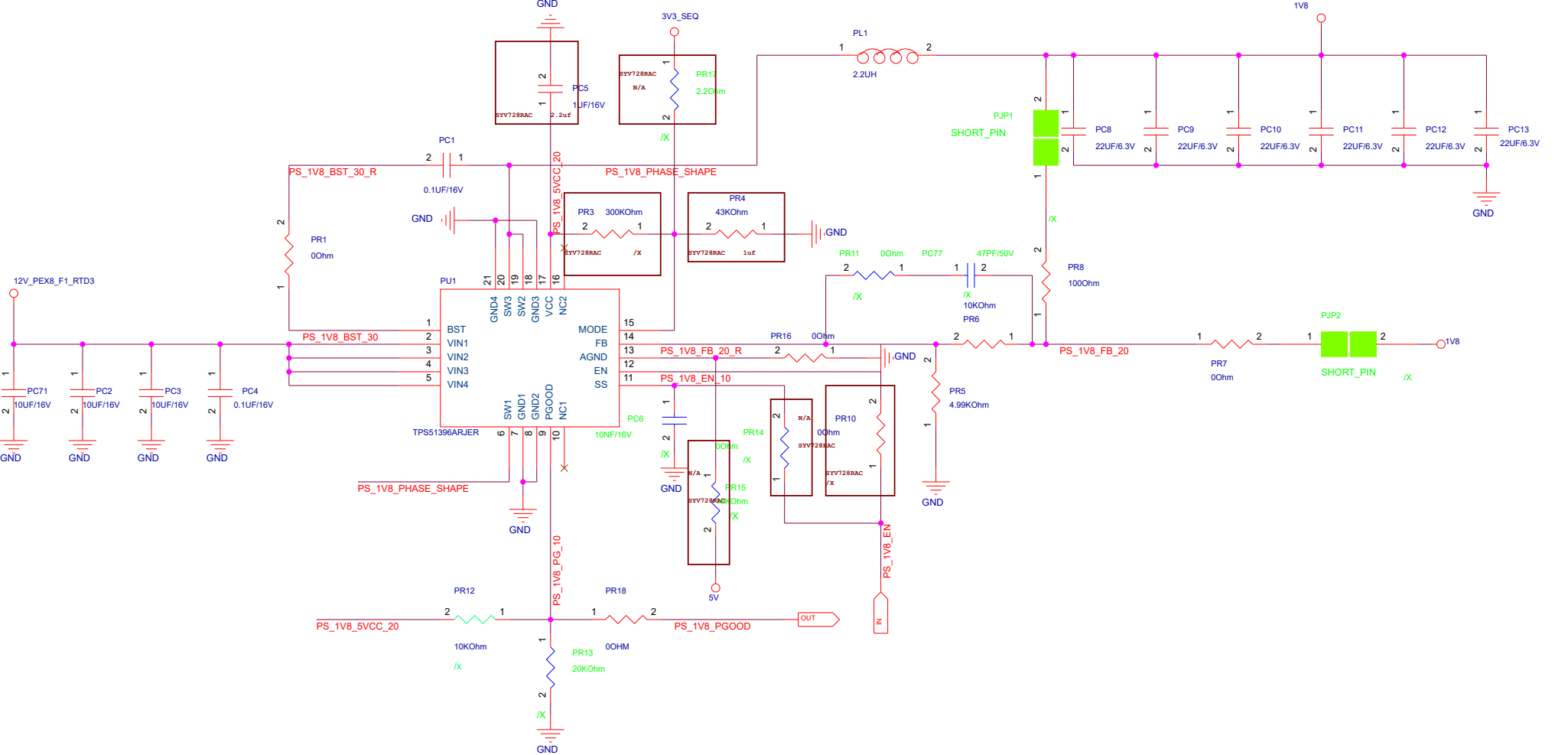

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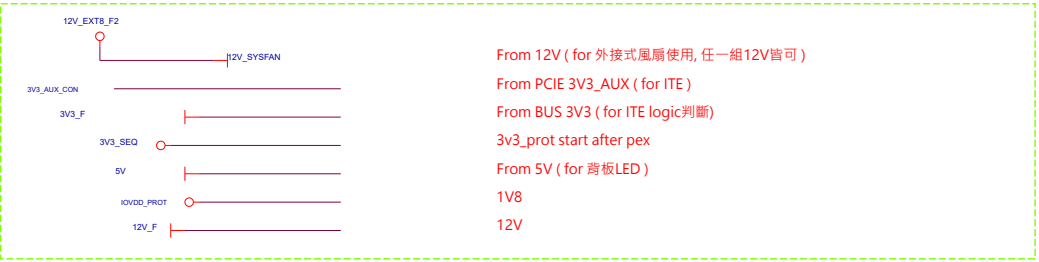
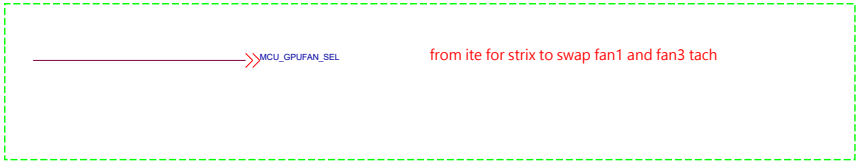
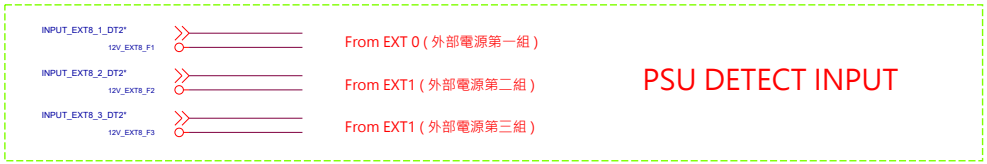
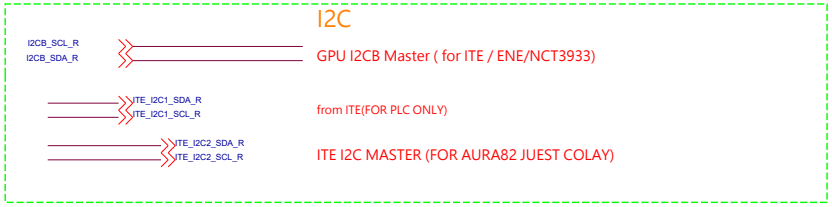
Date:	Sheet	of

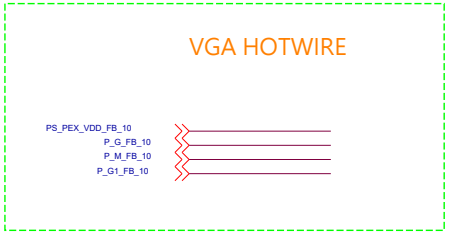
Power











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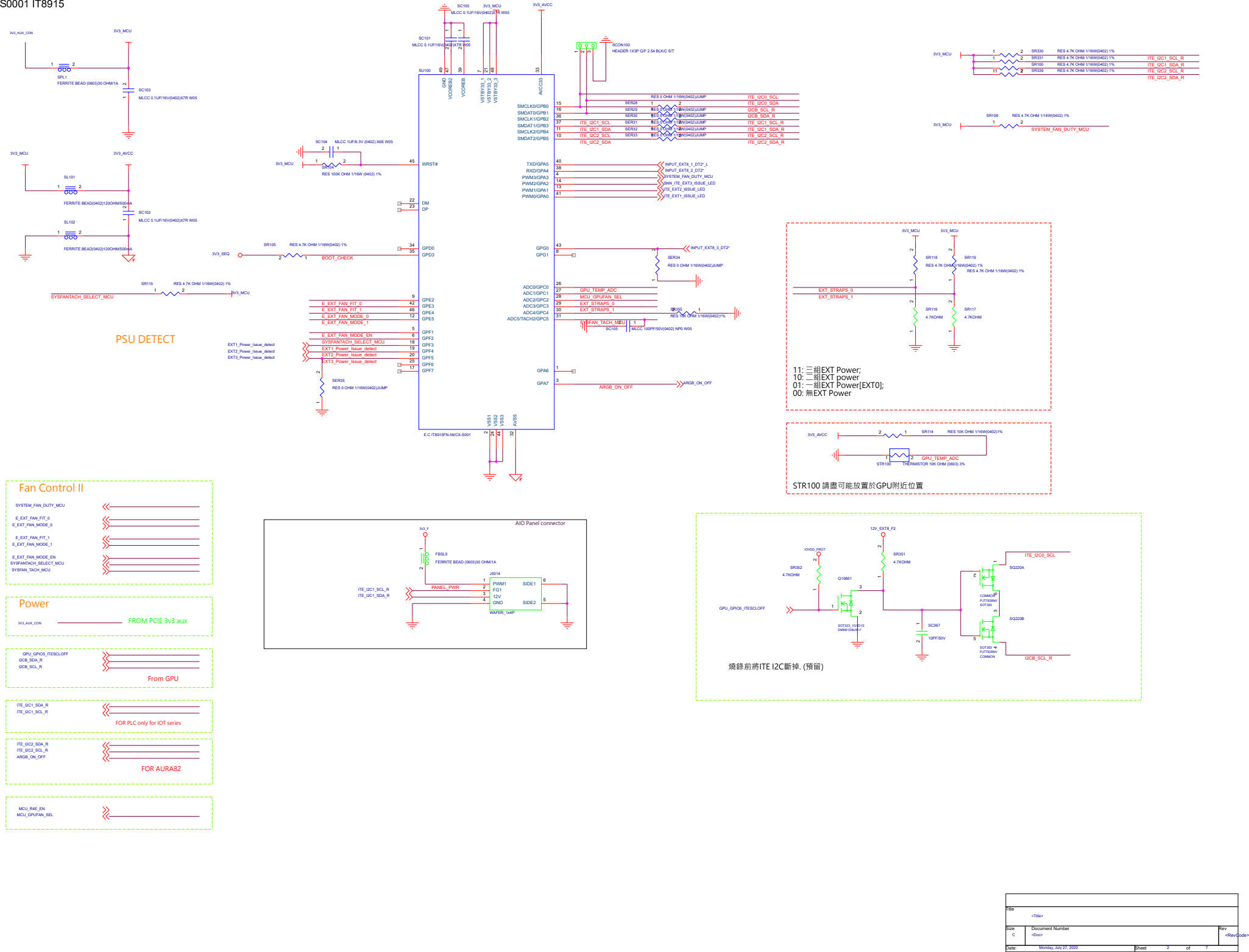

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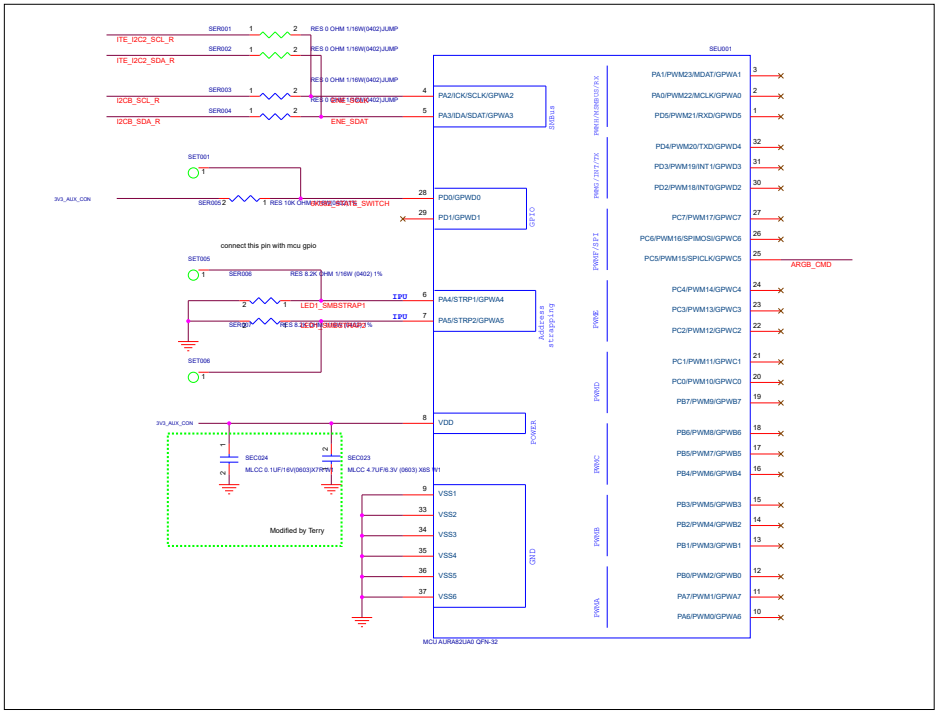

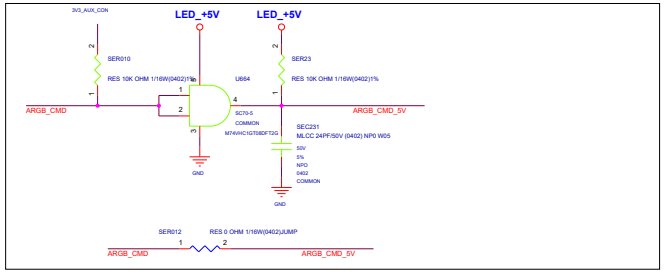

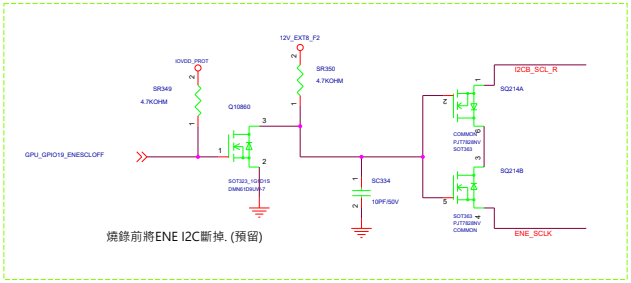

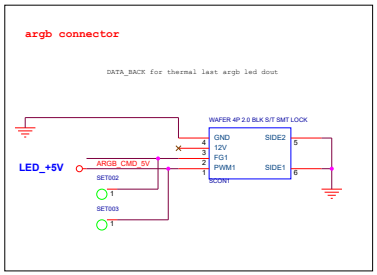

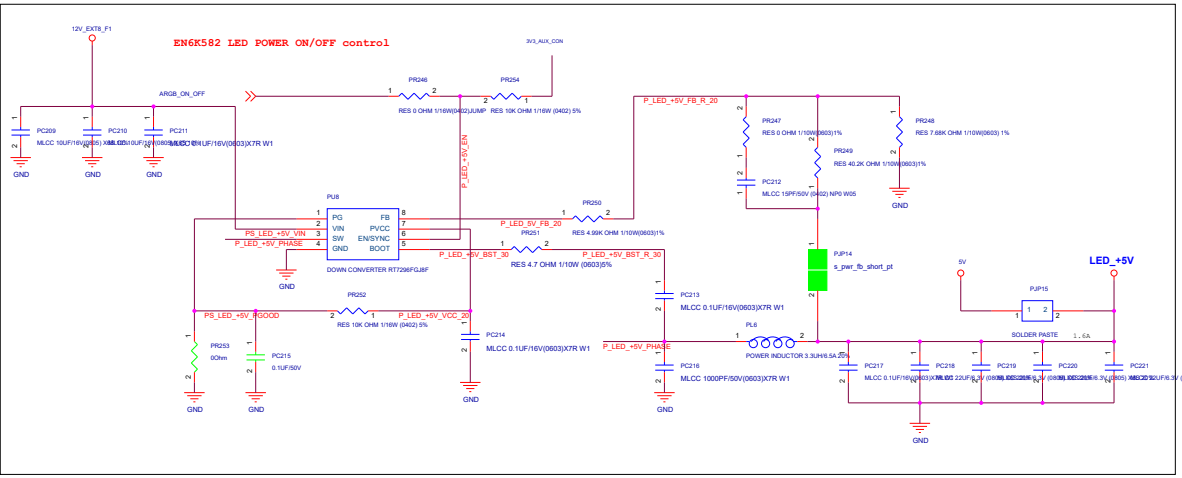

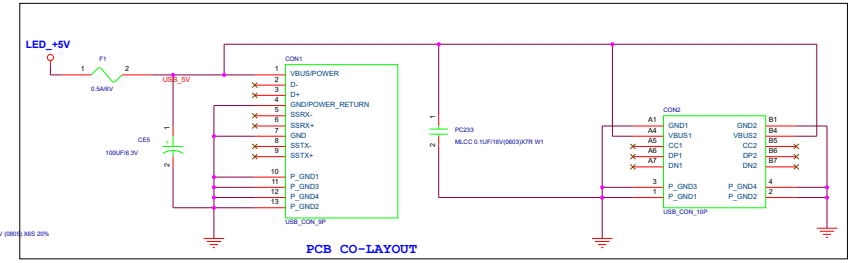

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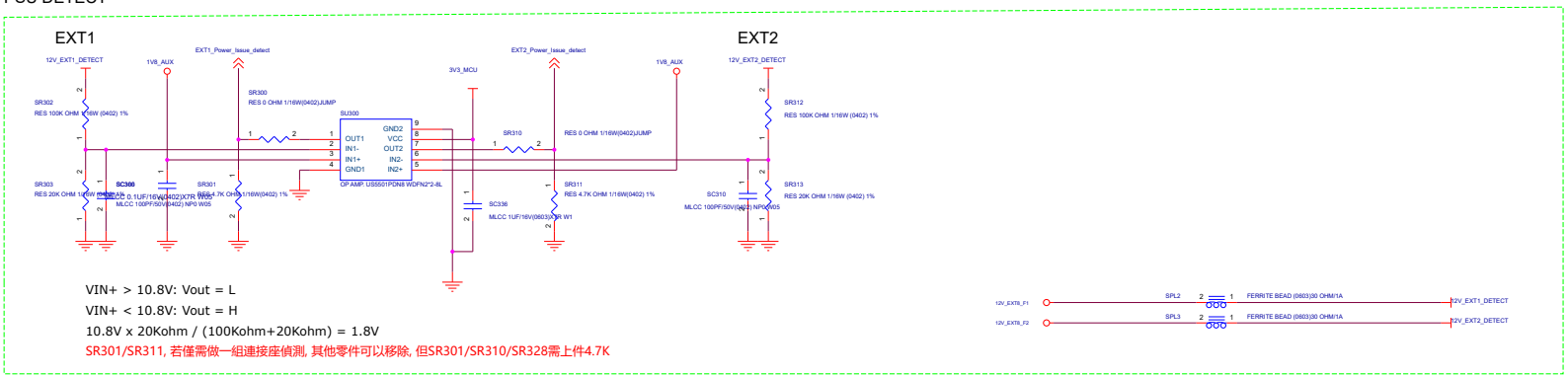

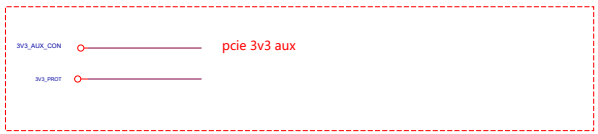

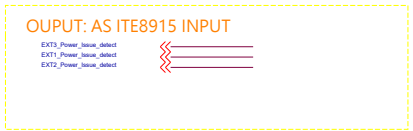

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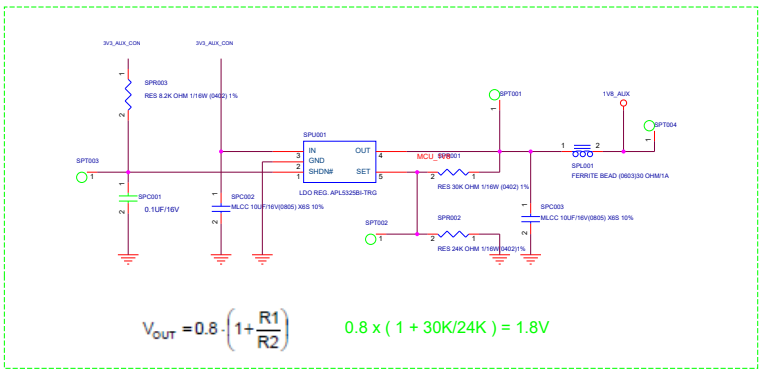

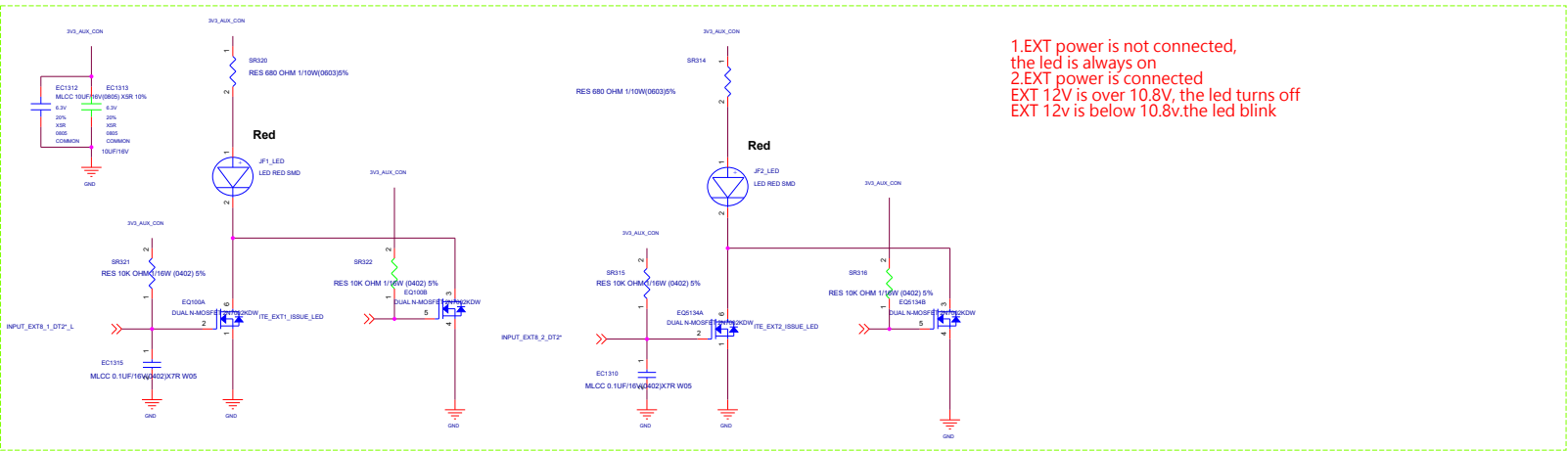

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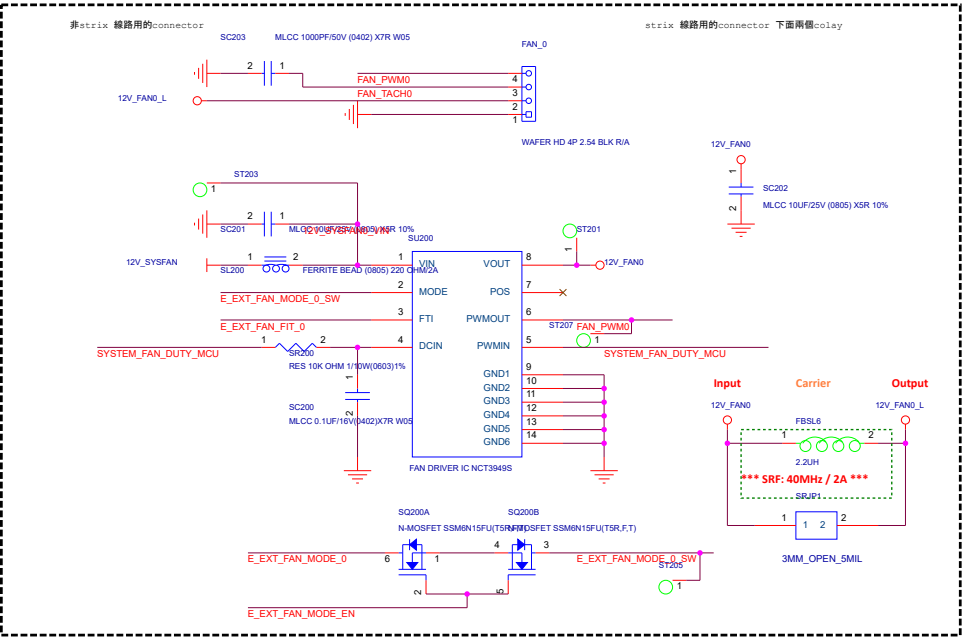
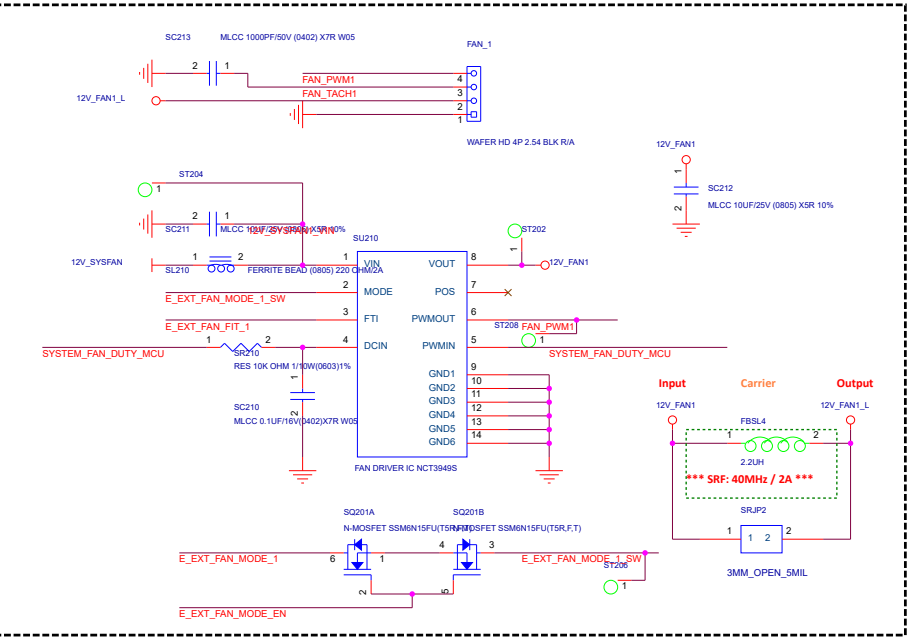
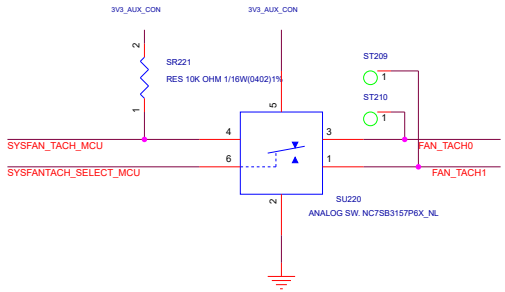
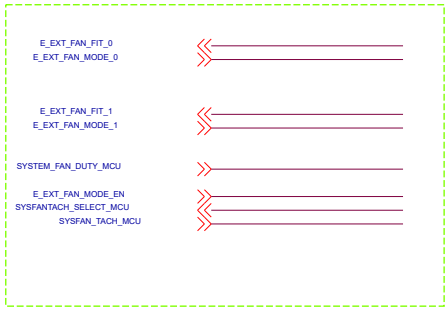
S0002 SYSTEM FAN CONTROL







Fan Control II



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