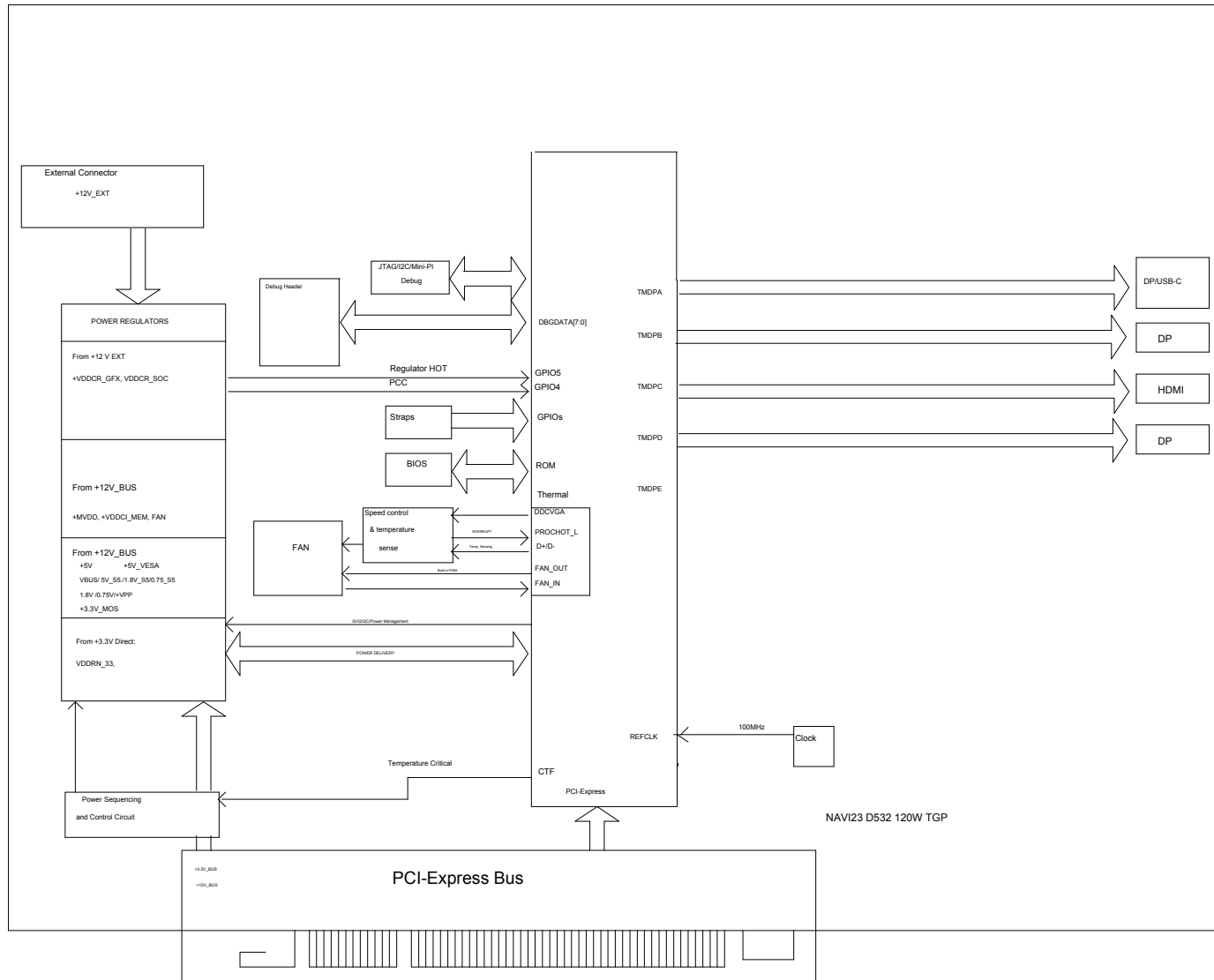
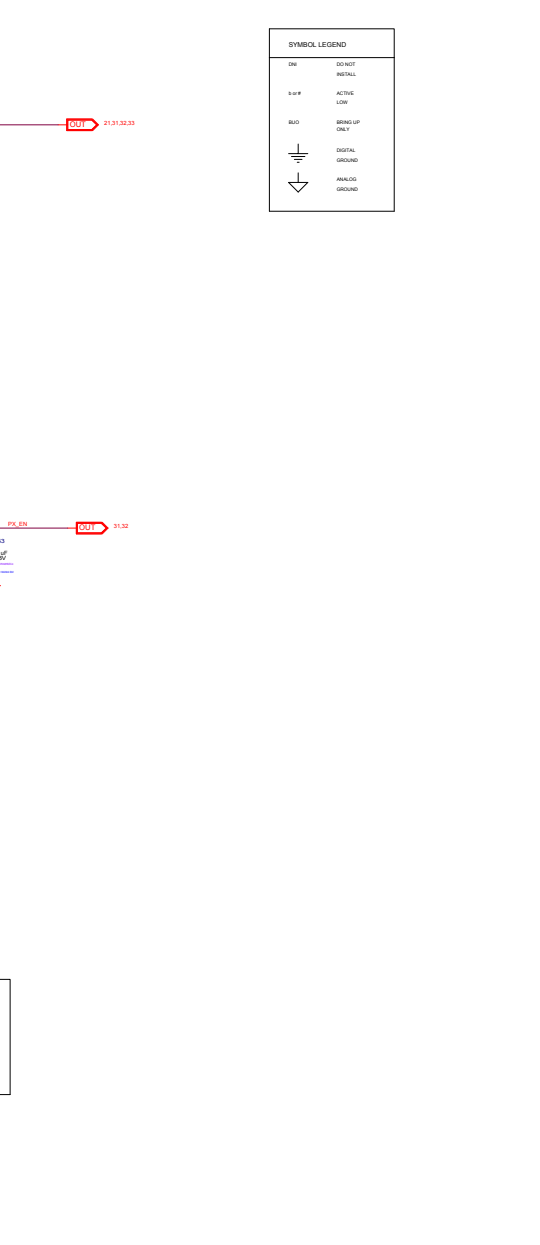
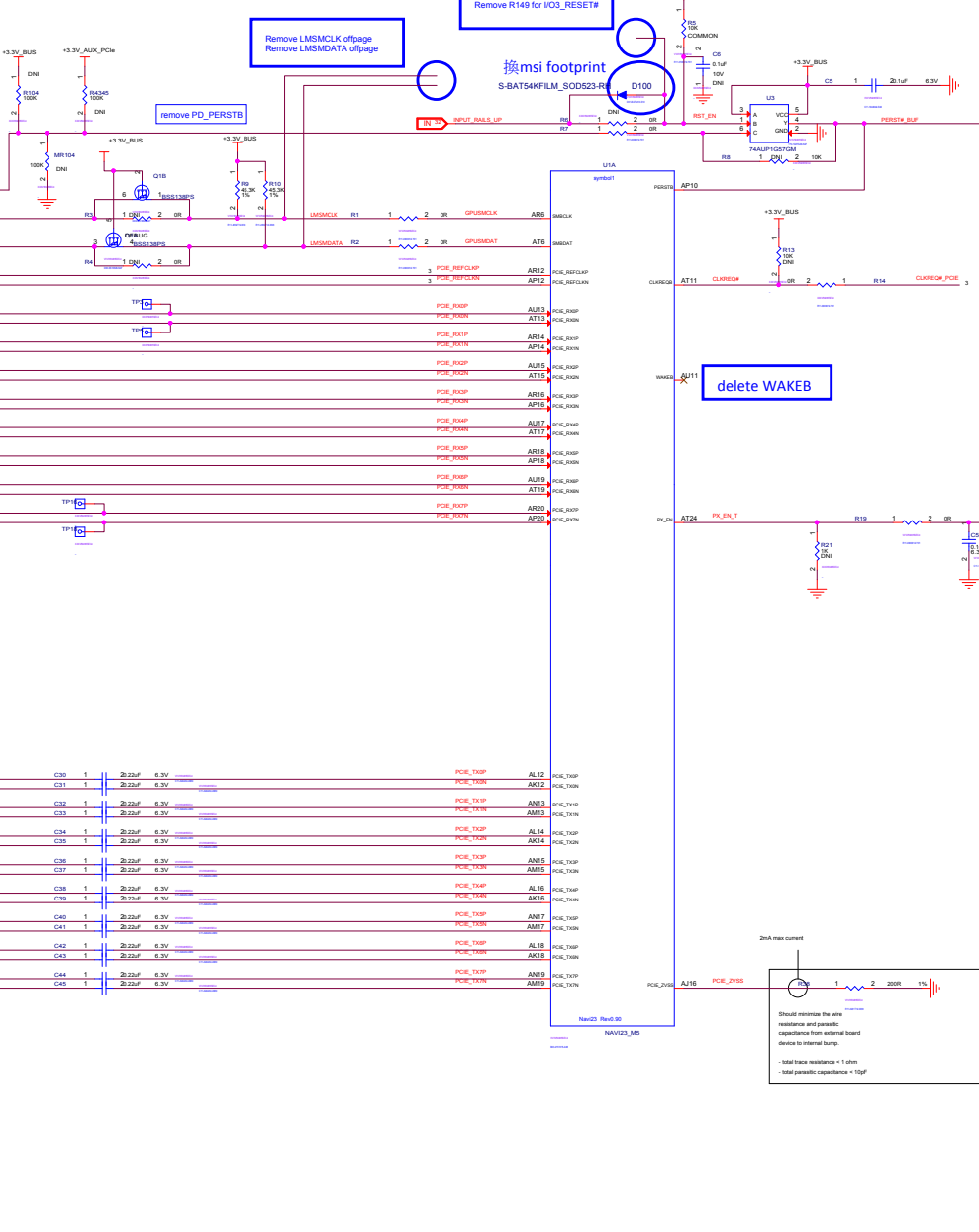
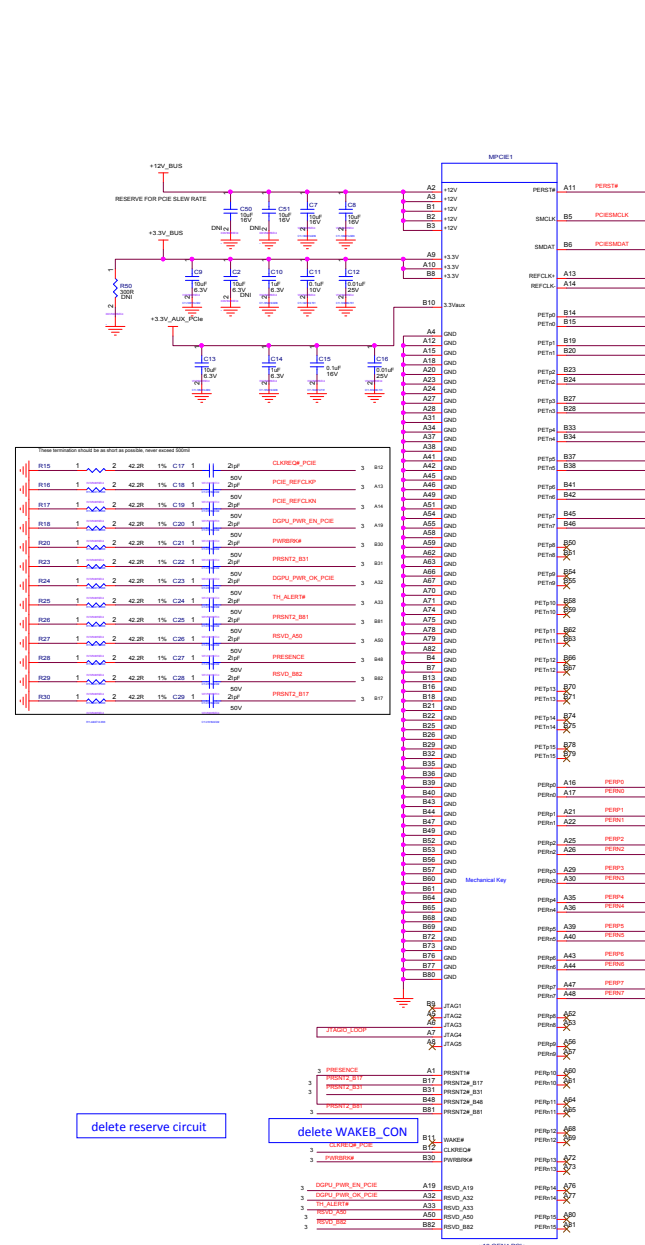


NAVI23 GDDR6 4PCS,8L DP/USB-C + DP + HDMI + DP
 105-D532xx-00 Rev00B Desktop board(120W TGP)

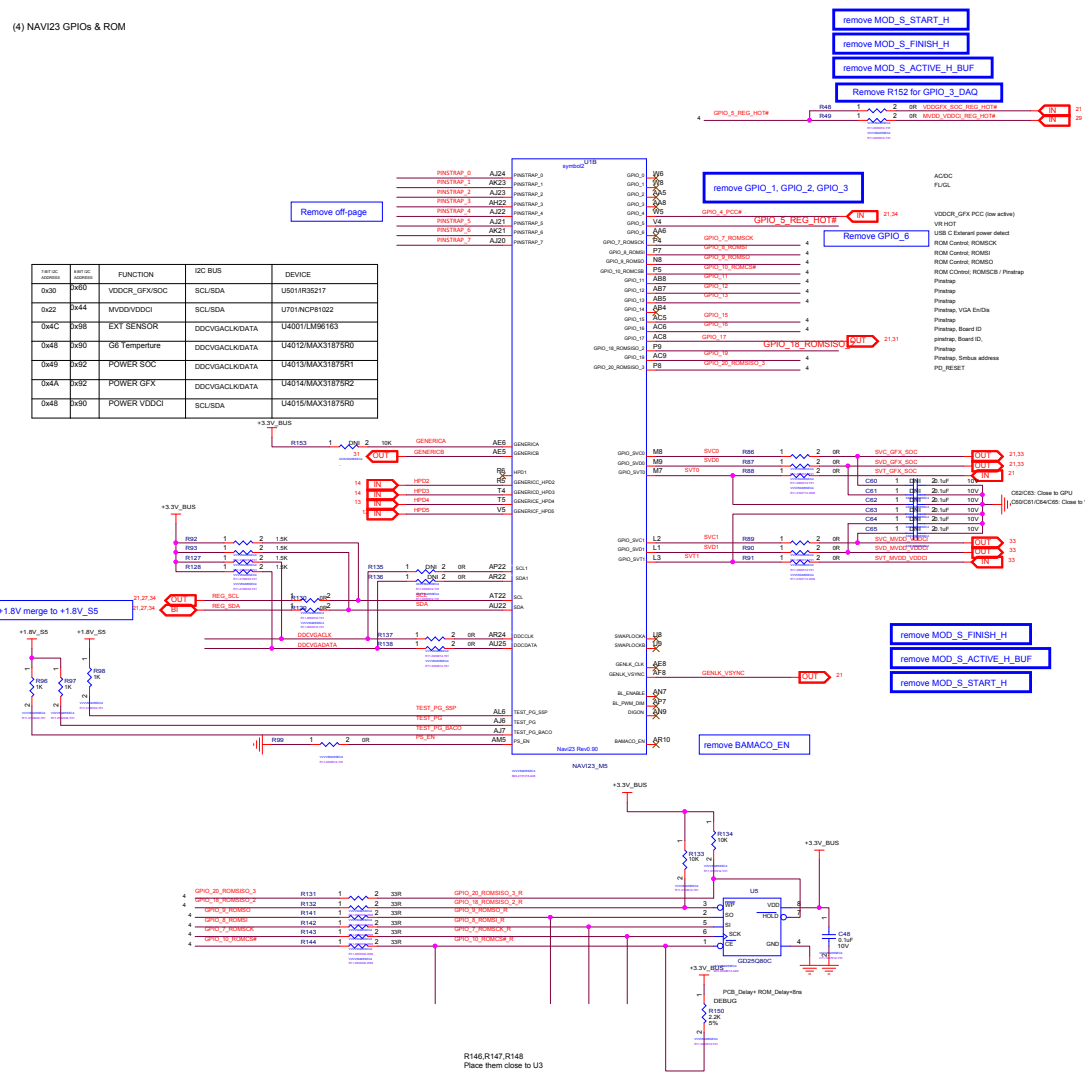
TABLE OF CONTENTS

SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	REG 5V
2	BLOCK DIAGRAM	27	MVDD_VDDCI CONTROLLER
3	NAVI23 - PCIe Interface	28	REG MVDD
4	NAVI23 - GPIO, EXTRA	29	REG VDDCI
5	NAVI23 - XTAL	30	SMALL RAIL LDO
6	NAVI23 - POWER and GND	31	MECHANICAL AND THERMAL
7	NAVI23 - Decaps	32	POWER MANAGEMENT
8	NAVI23 - MEM CH AB	33	SV12
9	NAVI23 - MEM CH CD	34	DEBUG CIRCUITS
10	GDDR6 x16 - MEM CH AB	35	MINI PI
11	GDDR6 x16 - MEM CH CD	36	REVISION HISTORY
12	NAVI23 - TMDPA - USB/DP		
13	NAVI23 - TMDPB - DP		
14	NAVI23 - TMDPCD- HDMI,DP		
15	PD CONTROLLER		
16	USB-C PORT 1& DP		
17	3.3V_AUX		
18	USB_VBUS 5V SS_Rails		
19	REG 1.8V 0.75V VPP		
20	MODS CONTROL & POWER		
21	GFX & SOC CONTROLLER		
22	VDDCR_GFX PHASES 2 and 5		
23	VDDCR_GFX PHASES 1 and 4		
24	VDDCR_GFX PHASES 3 and 6		
25	VDDCR_SOC		

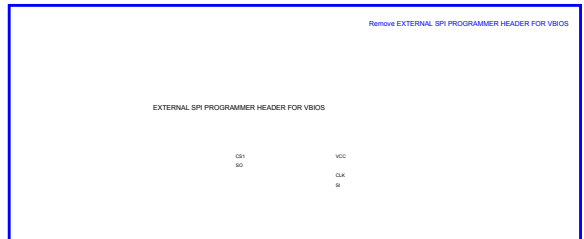




Part ref. address	Part ref. number	FUNCTION	I2C BUS	DEVICE
0x30	0x00	VDDCR_GFXVDDC	SCL:SDA	U501:IR35217
0x22	0x44	MVDDVDDCI	SCL:SDA	U701:NC91802
0x4C	0x98	EXT SENSOR	DDCVGACLKDATA	U4001:LM98183
0x48	0x50	GE Temperature	DDCVGACLKDATA	U4012:MAX31878R2
0x49	0x52	POWER SOC	DDCVGACLKDATA	U4013:MAX31878R1
0x4A	0x52	POWER GFX	DDCVGACLKDATA	U4014:MAX31878R2
0x48	0x50	POWER VDDCI	SCL:SDA	U4015:MAX31878R0

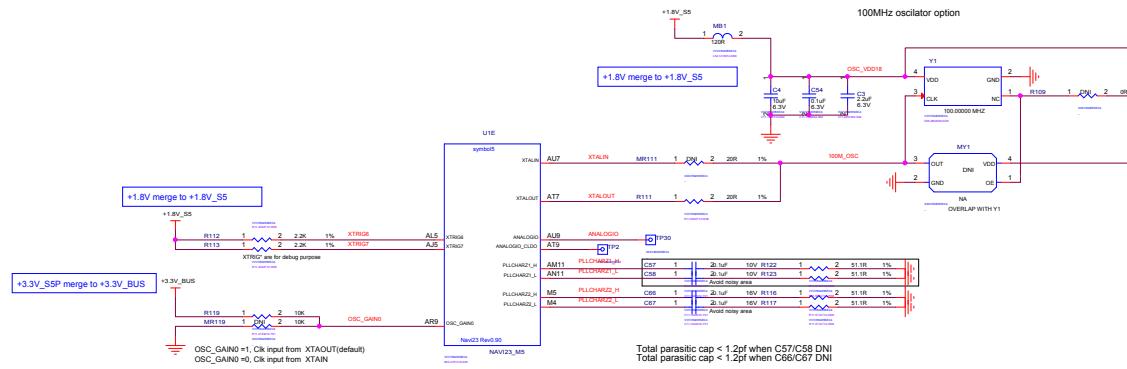


R146,R147,R148
Place them close to U3

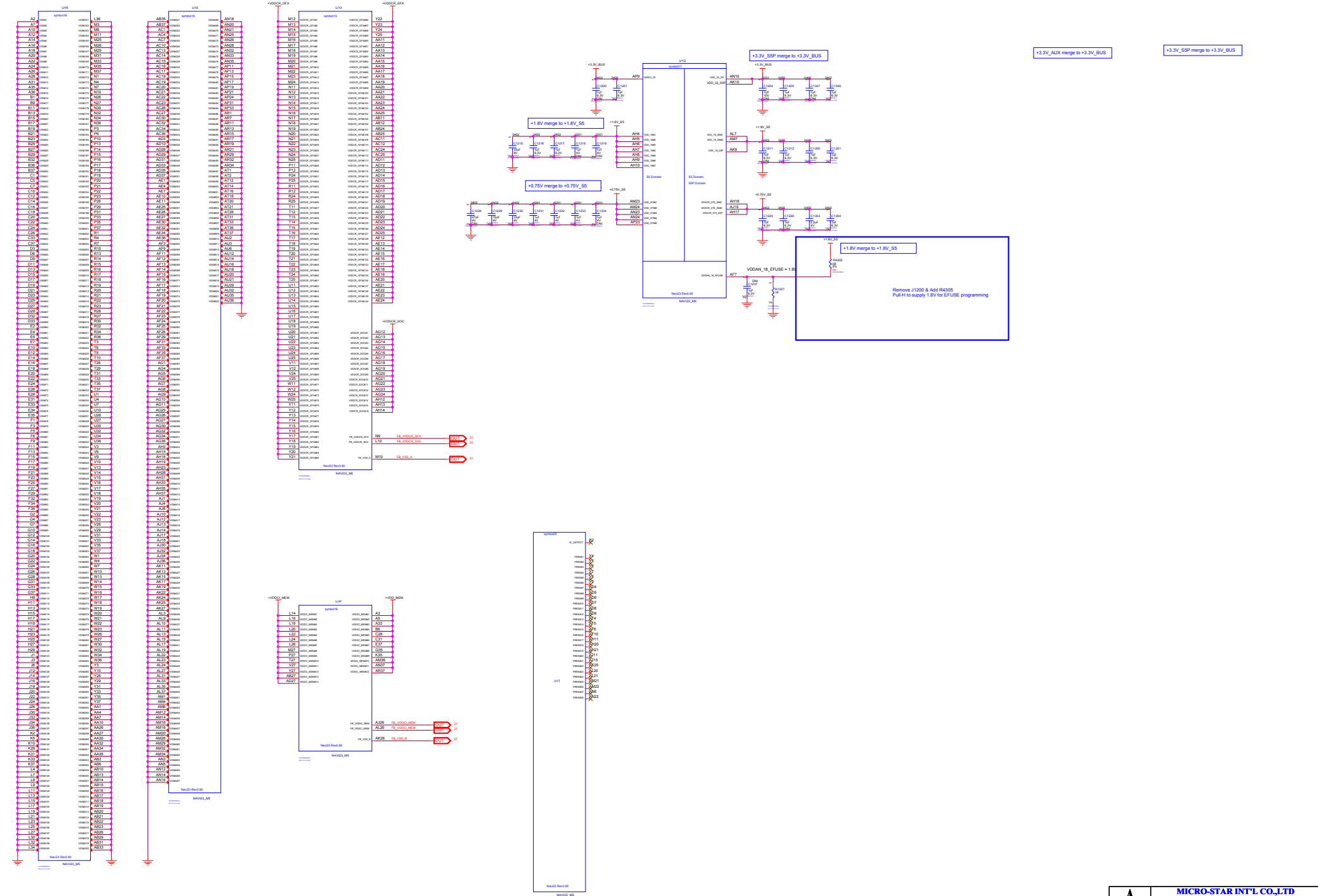


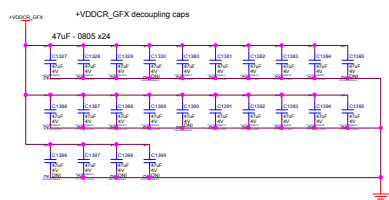
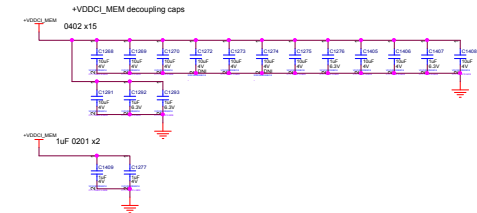
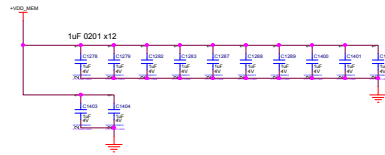
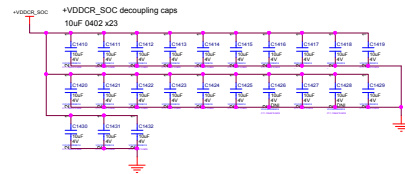
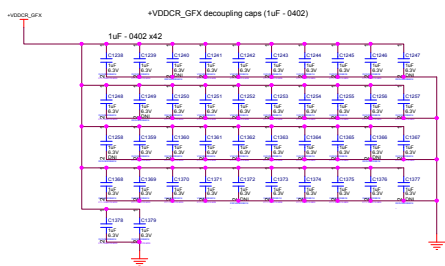
Note: Internal PUPD at GPIO pad is ~40k strength in 14nm design spec

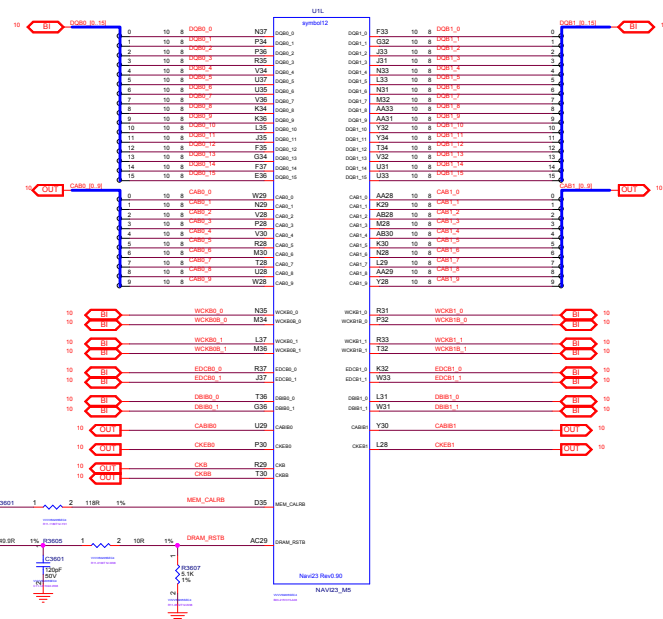
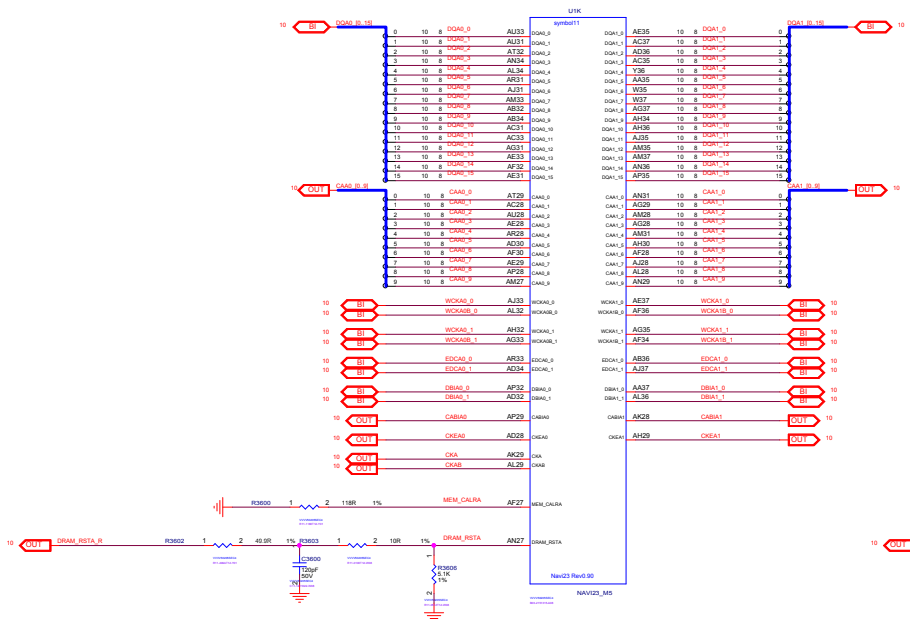
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GENA_DIS_A 0: PCLK GEN4 supported 1: PCLK GEN4 not supported
	0	PINSTRAP_BIF_CLK_PM_EN 0: CLMTRAC power management capability is disabled 1: CLMTRAC power management capability is enabled
	0	PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing (mode1/2/3/4)
	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller outputs enabled 1: The device won't be recognized as the system's VGA controller
DOE	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 8 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected Default=(PINSTRAP_PINSRAMA+PINSTRAPC3) = 000
	0	PINSTRAP_AUD[1:0]
	0	PINSTRAP_AUD[1:0] - No definition on NV 1: Audible for DisplayPort only 2: Audible for DisplayPort and HDMI if dongle is detected 3: Audible for both DisplayPort and HDMI Default=(GPIO12.GPIO11) = 11
	0	PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
Platform	0	PINSTRAP_FIG[1:0] - No definition on NV
	0	PINSTRAP_MVDD_FB_DIVIDER_CONFIG
	0	PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100: 512KBIT (BT) M2SP0A 101: 1MBIT (BT) M2SP0A 102: 2MBIT (BT) M2SP0A 103: 4MBIT (BT) M2SP0A 104: 8MBIT (BT) M2SP0A 105: 16MBIT (BT) M2SP0A 106: 32MBIT (BT) M2SP0A 107: 64MBIT (BT) M2SP0A 108: 128MBIT (BT) M2SP0A 109: 256MBIT (BT) M2SP0A 110: 512MBIT (BT) M2SP0A 111: 1024MBIT (BT) M2SP0A Default=(PINSTRAP_PINSRAMA+PINSTRAPC3) = 001
	0	PINSTRAP_SMBUS_ADDR 0: 0x47h 1: 0x49h
SMU	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device
	0	PINSTRAP_BIOS_ROM_EN
	0	PINSTRAP_BIOS_ROM_EN
	0	PINSTRAP_BIOS_ROM_EN

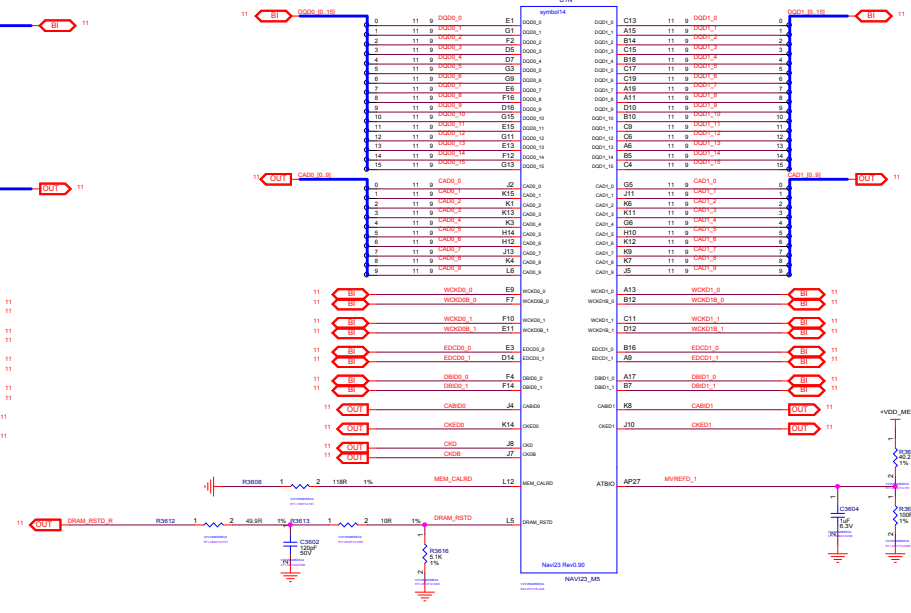
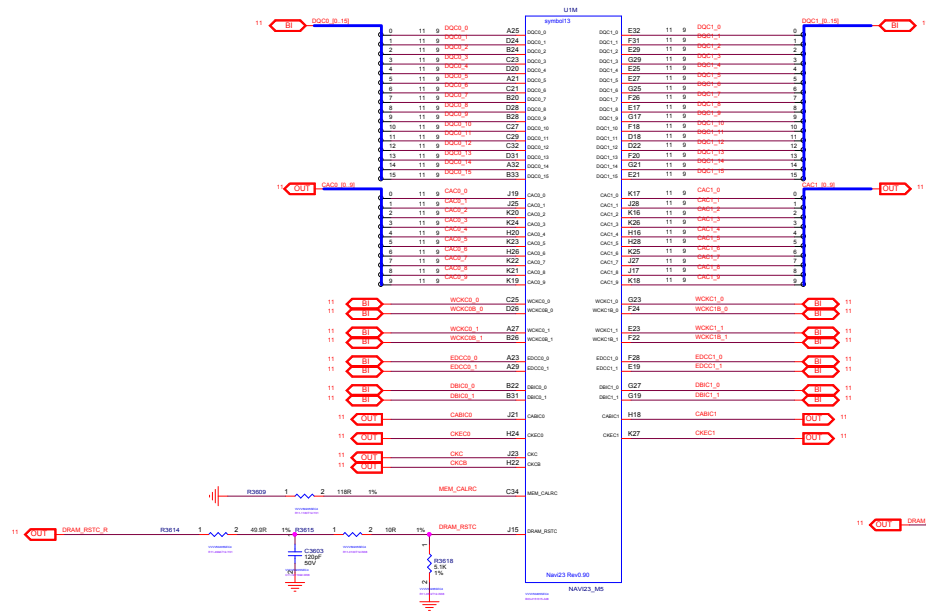


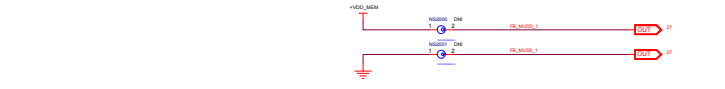
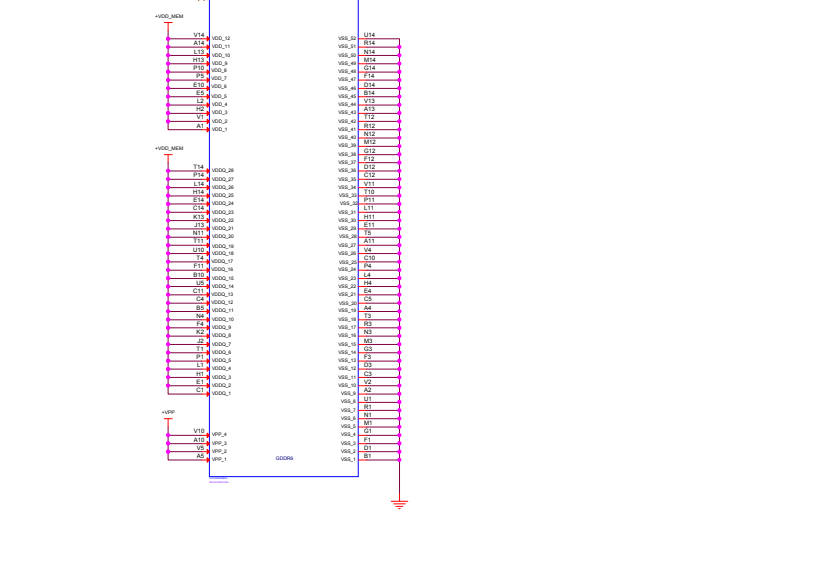
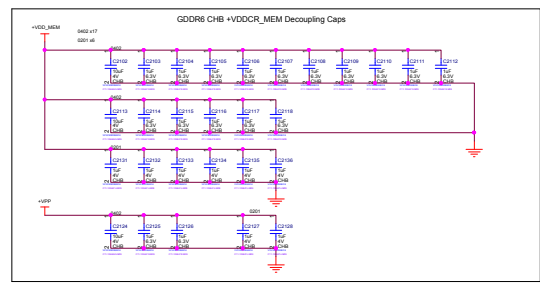
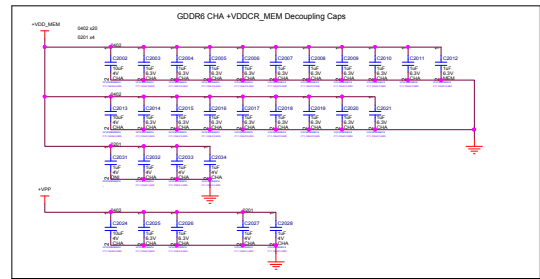
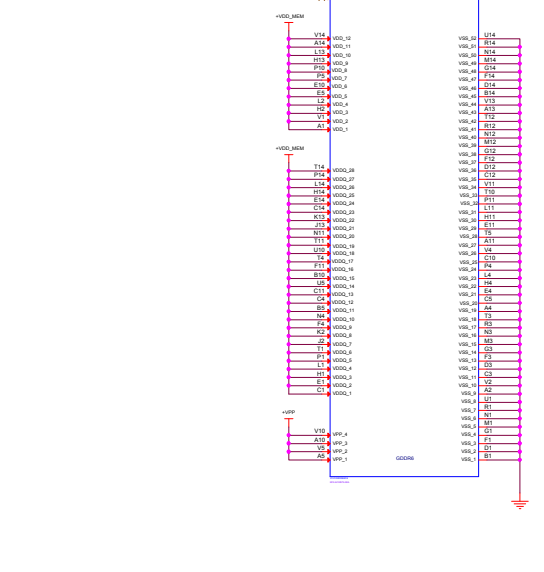
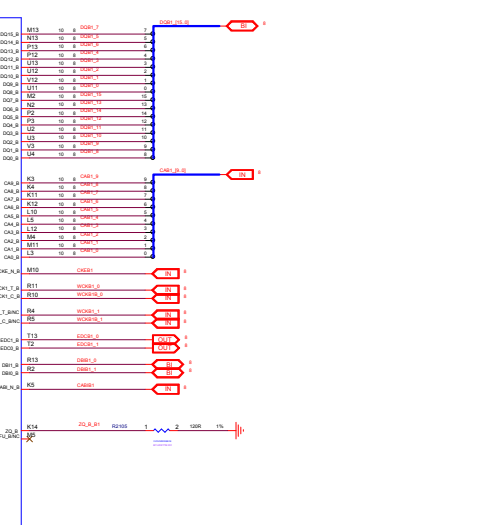
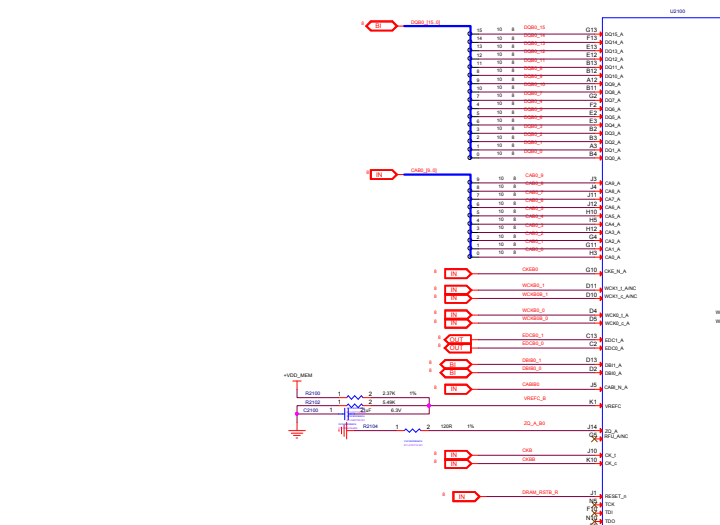
(6) NAVI23 POWER AND GND

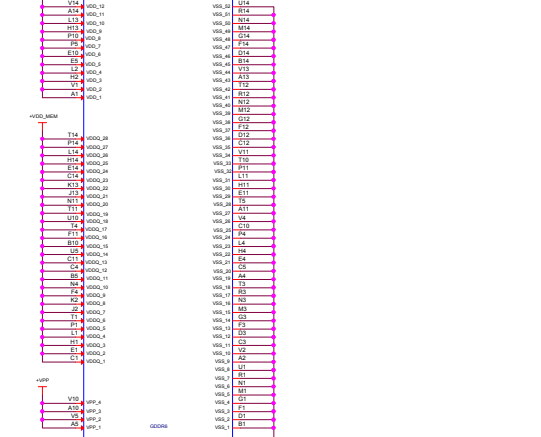
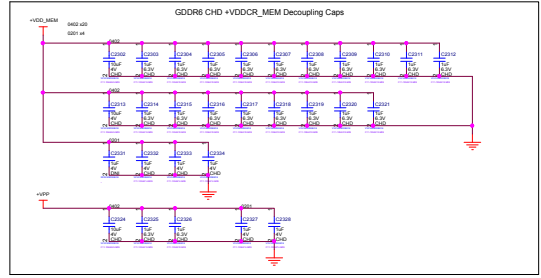
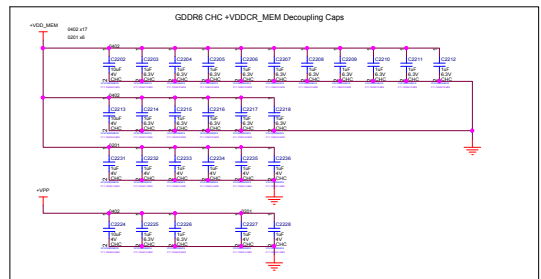
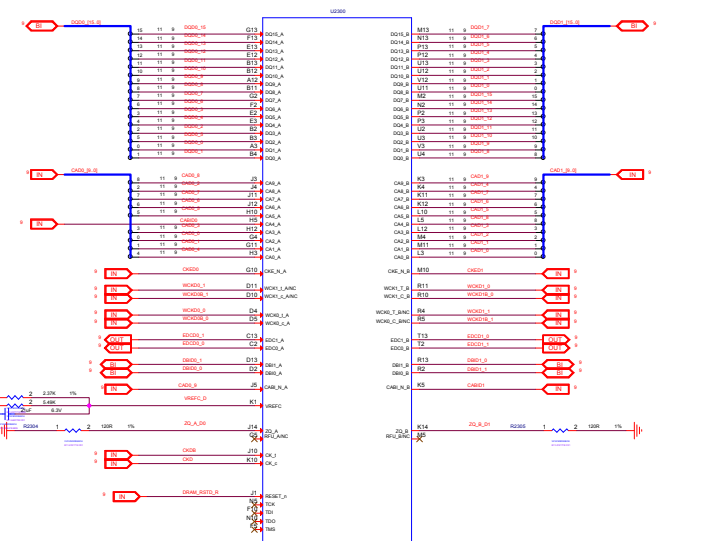
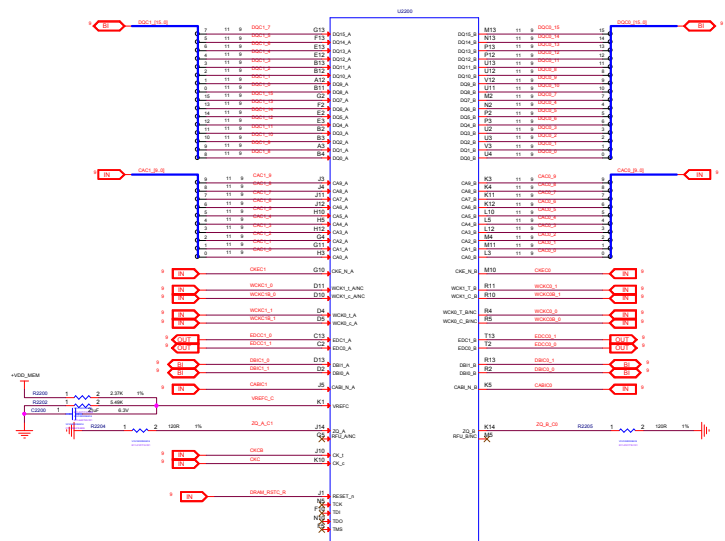


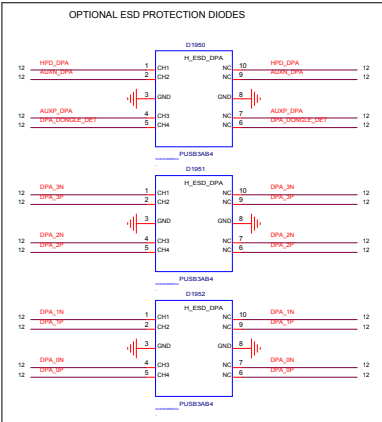
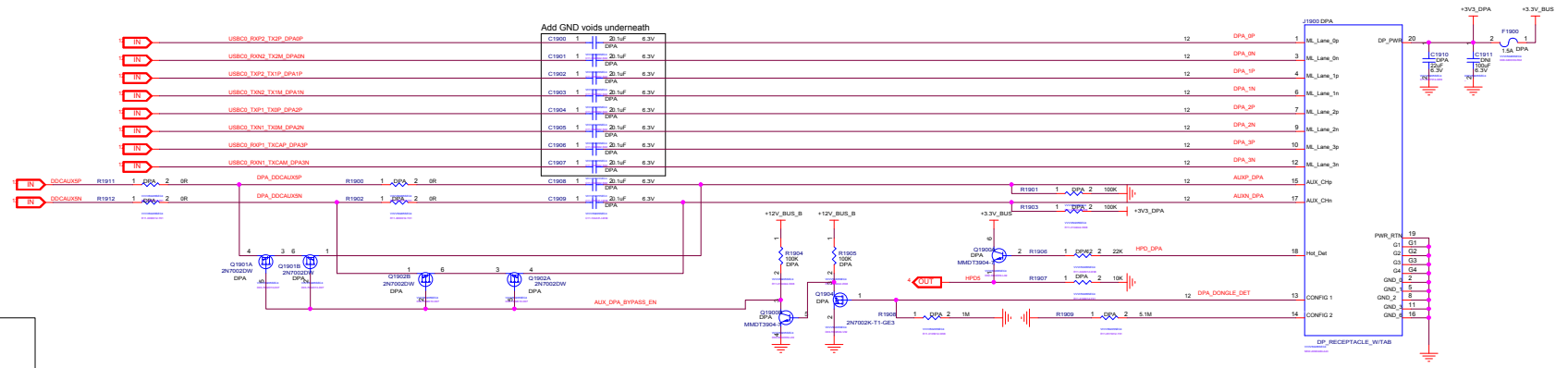
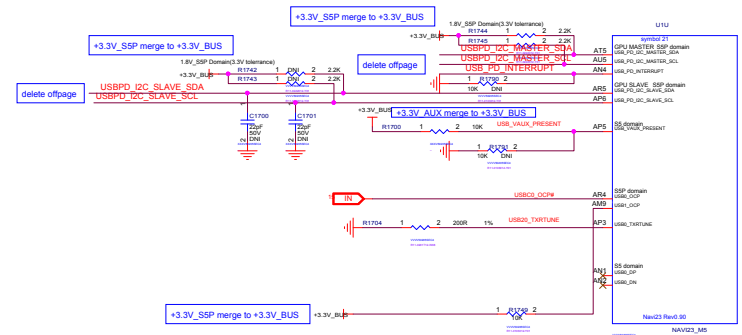
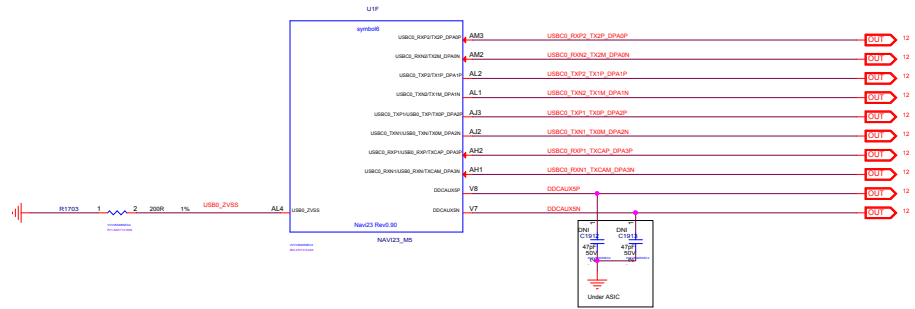


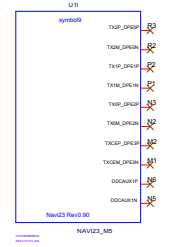
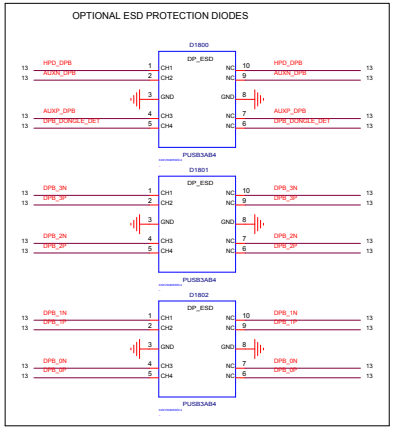
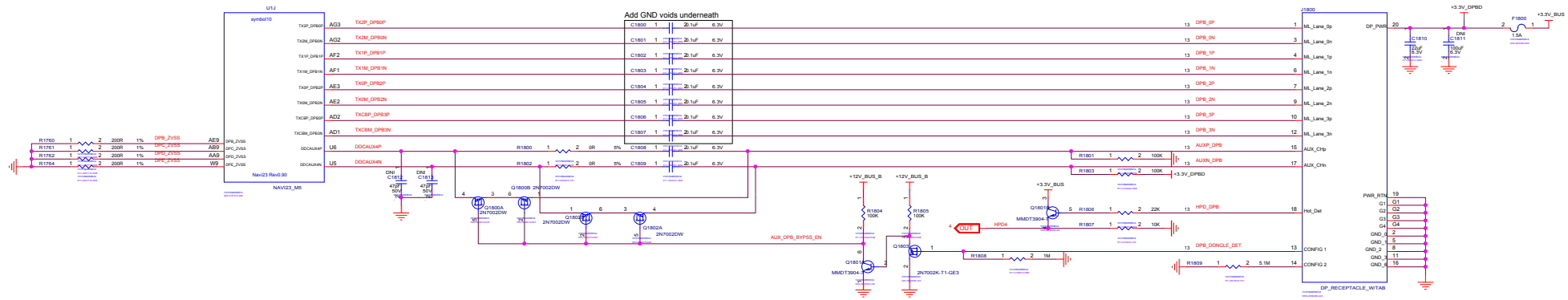


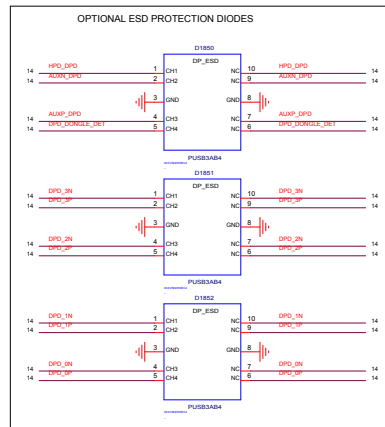
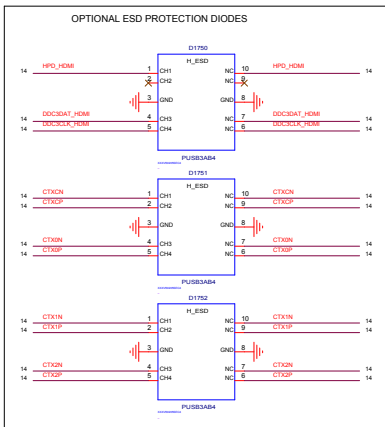
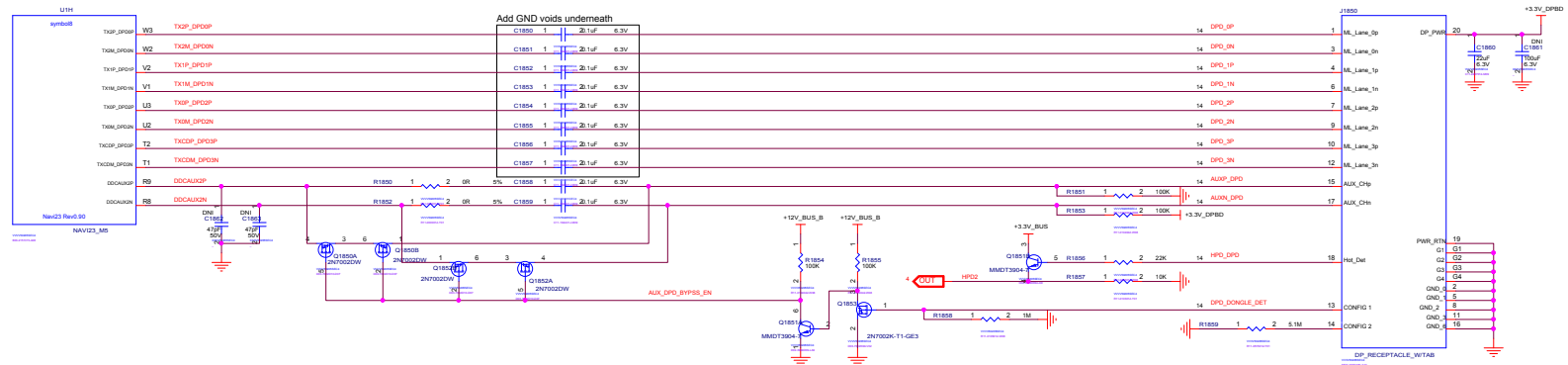
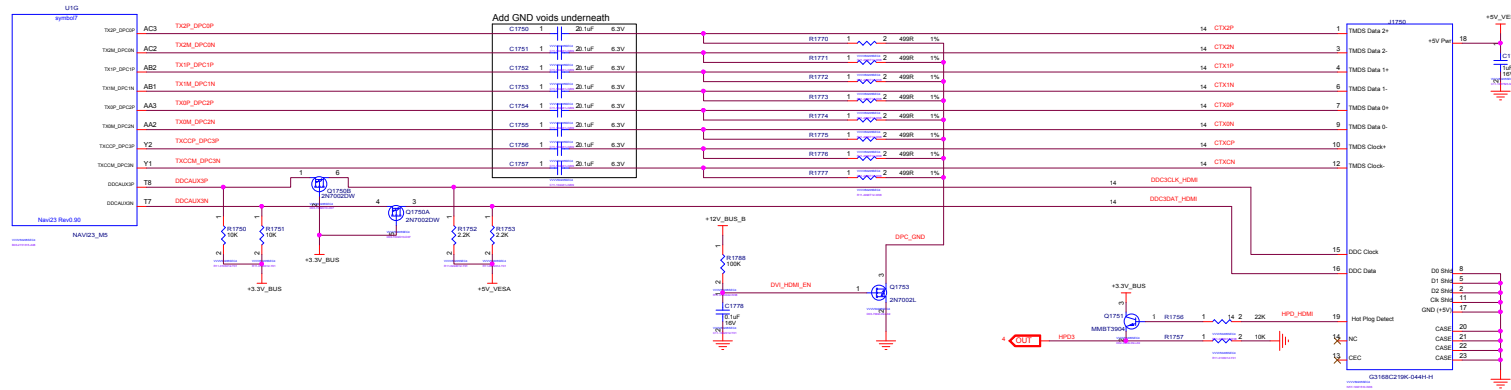


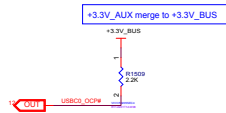













remove

Figure

remove

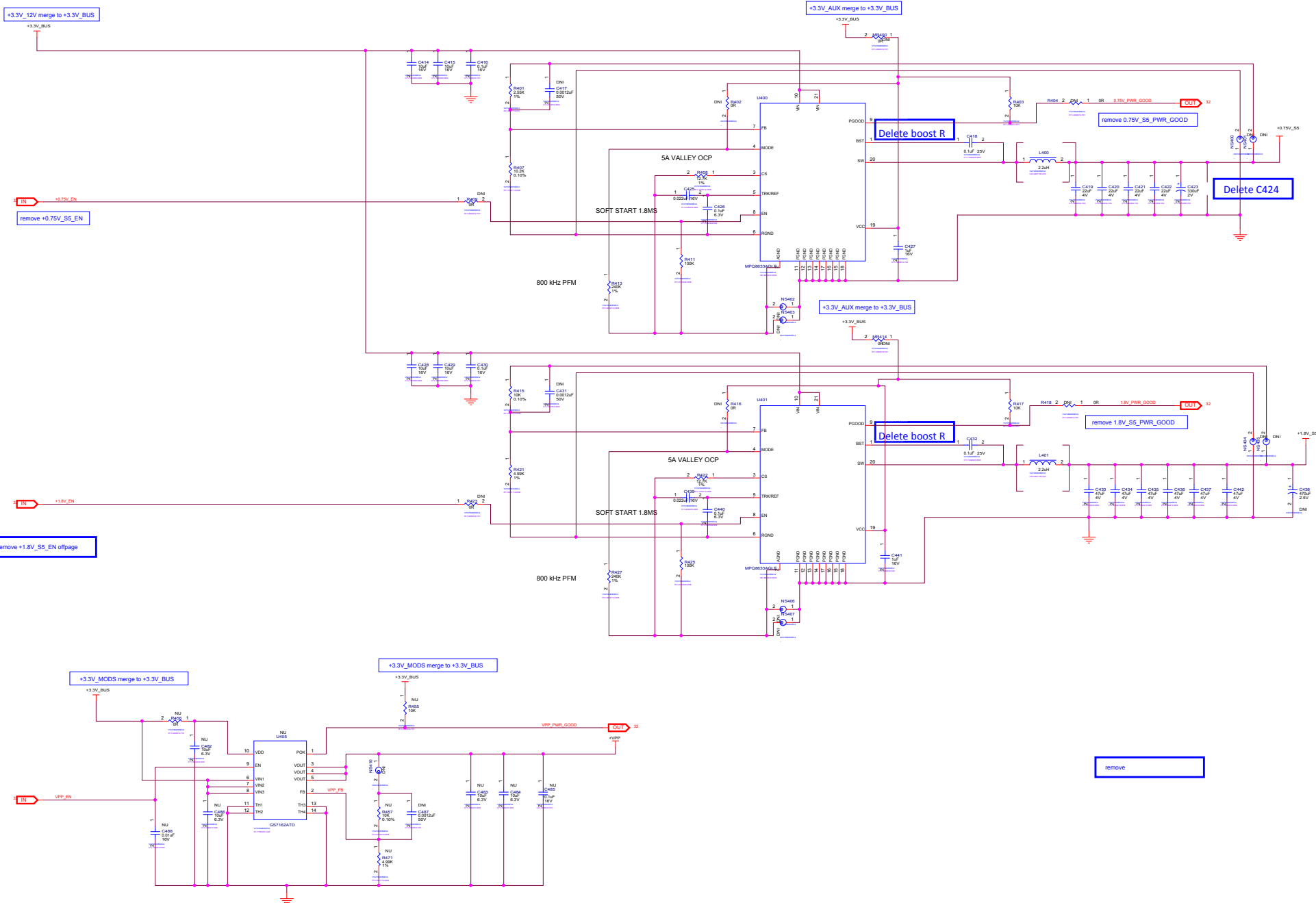
	MICRO-STAR INT'L CO.,LTD	
	MS-V502	
	Size Custom	Document Description 0017 3.3V_AUX
Date: Wednesday, May 19, 2021		Sheet 17 of 37

+3.3V_12V merge to +3.3V_BUS

remove

+0.75V merge to +0.75V_S5

+1.8V merge to +1.8V_S5



remove

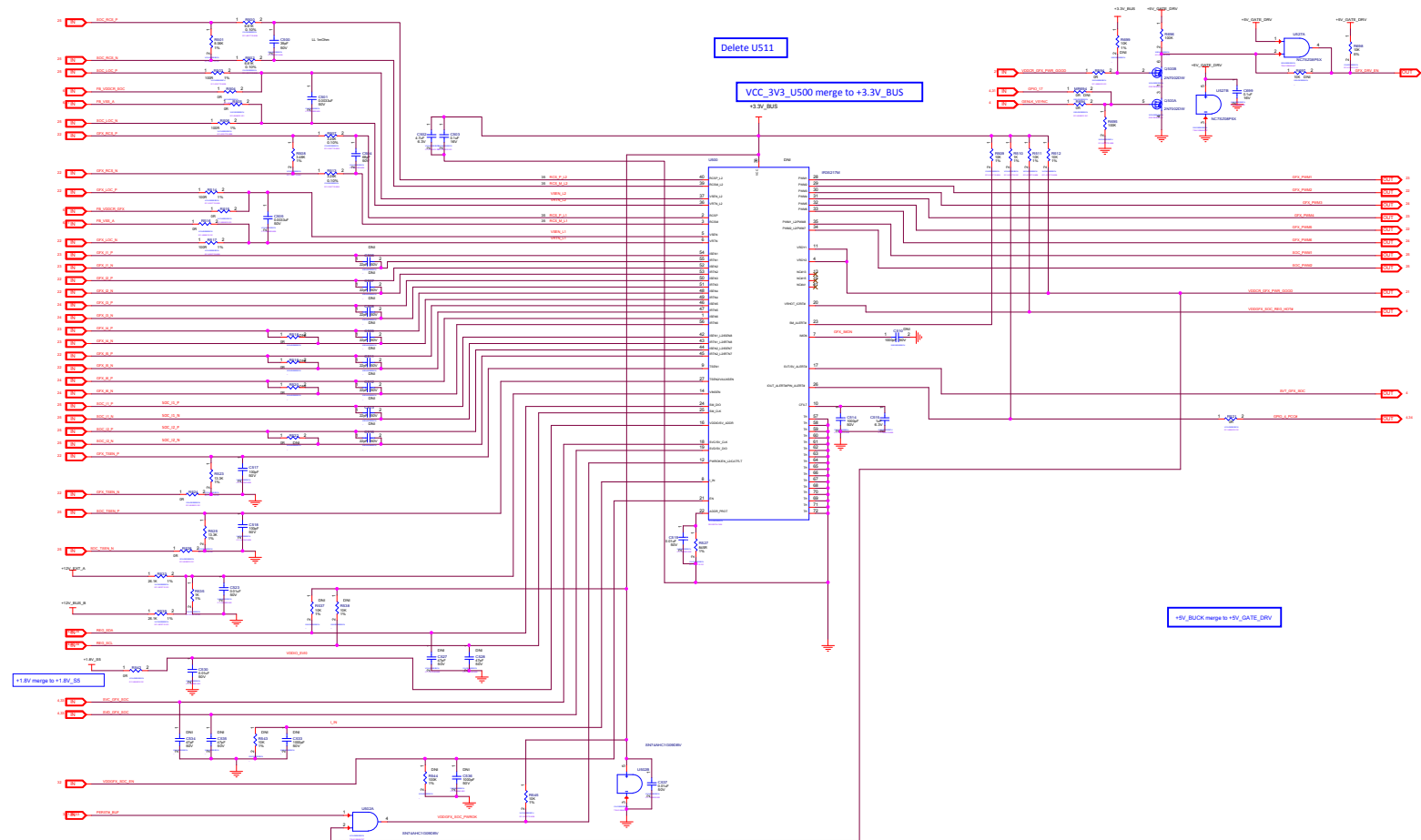
remove

remove +5V_S5 offpage

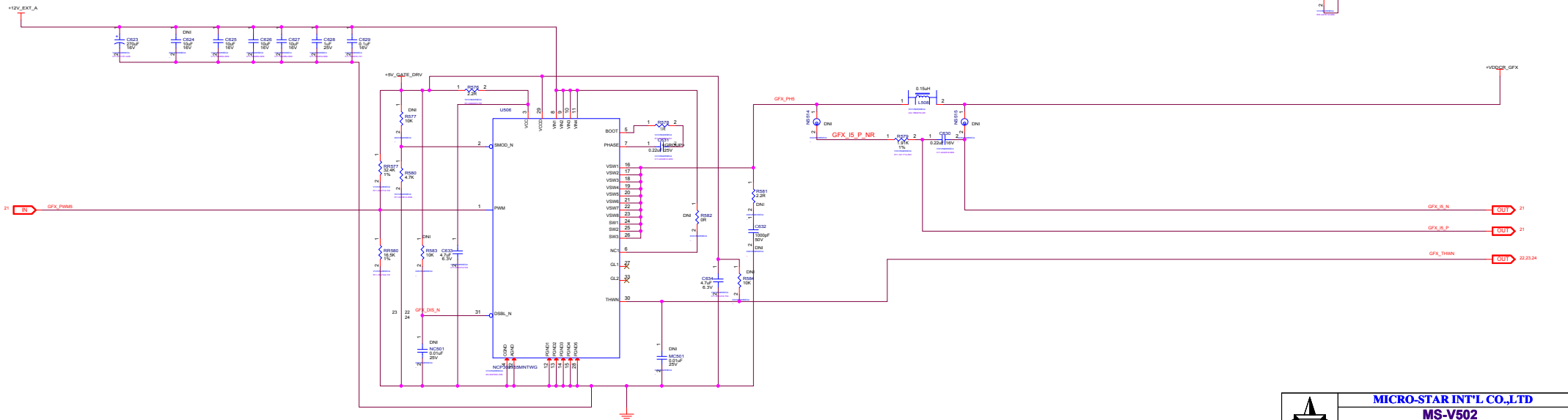
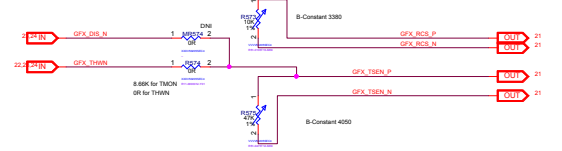
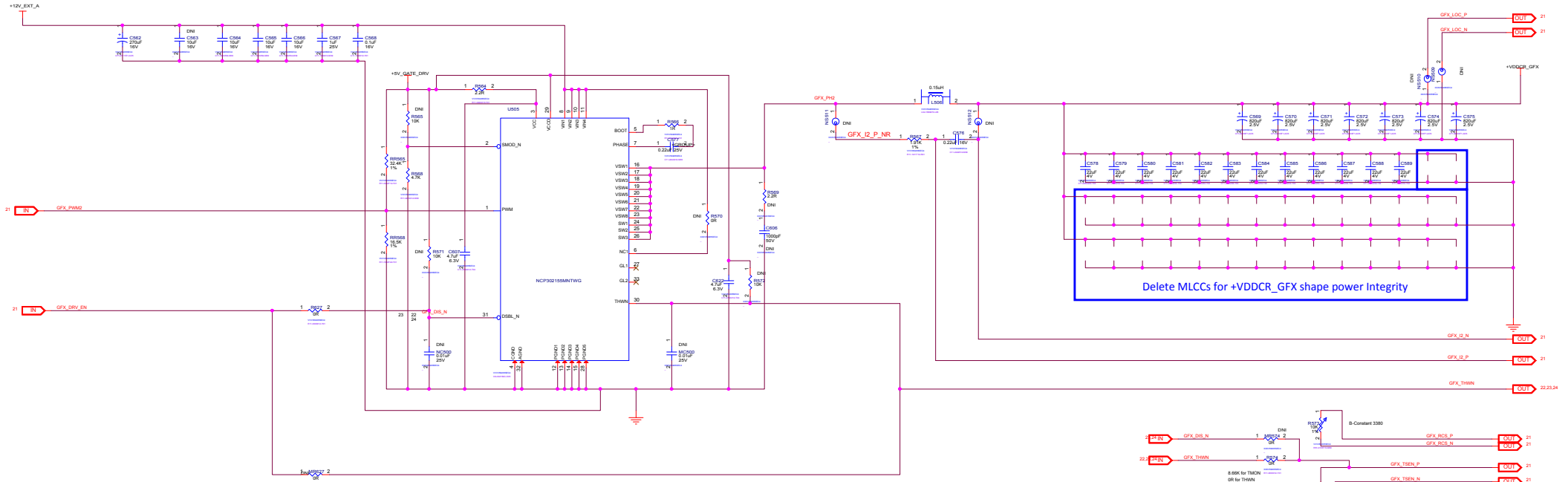
MVDD_PWR change to +12V_BUS_B

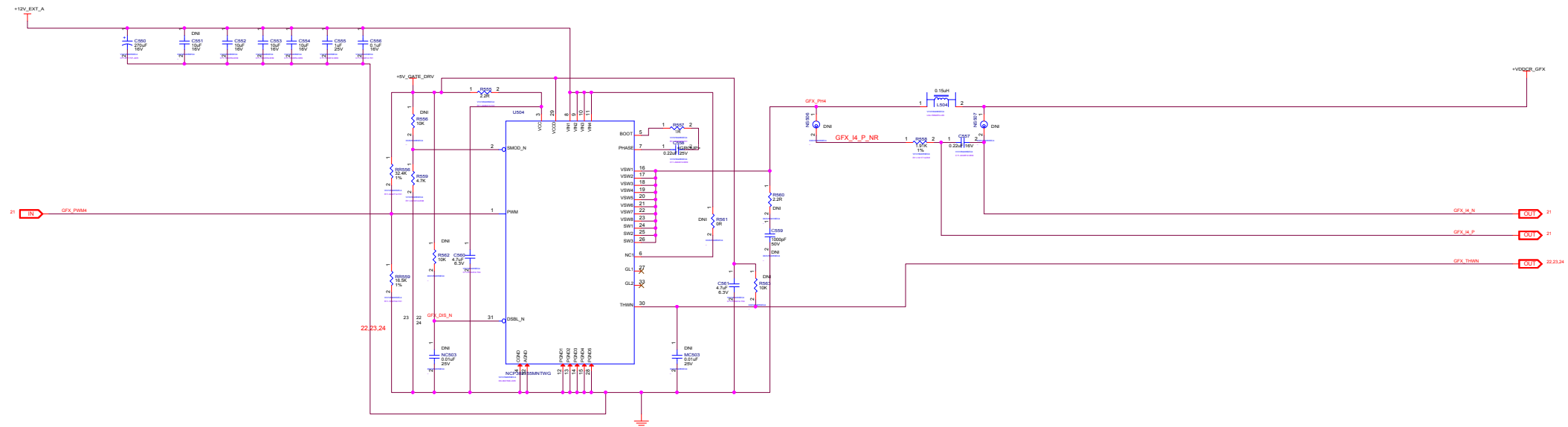
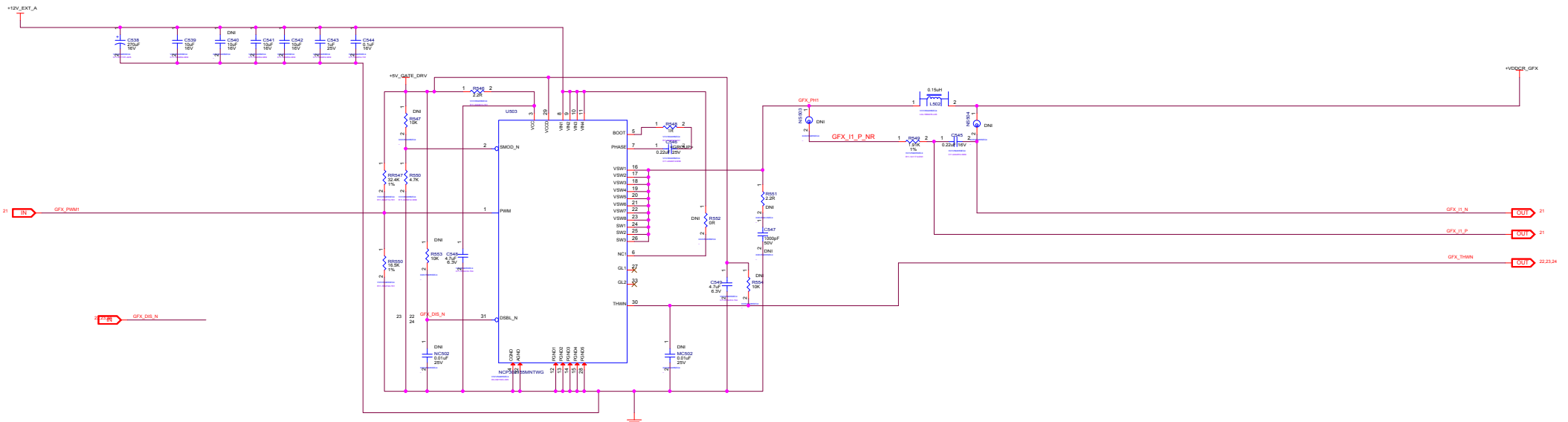
remove

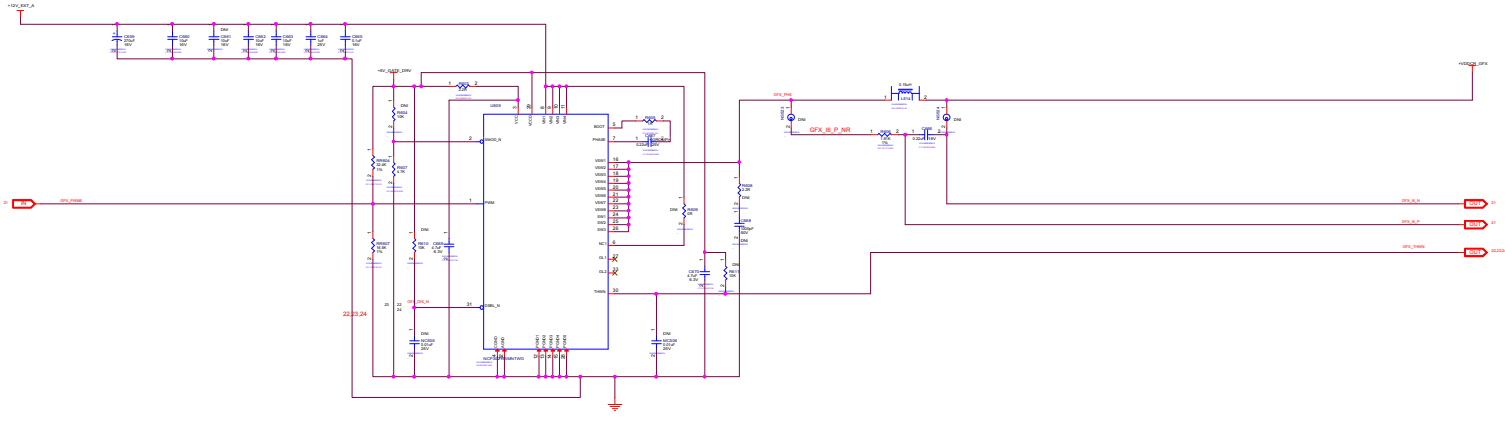
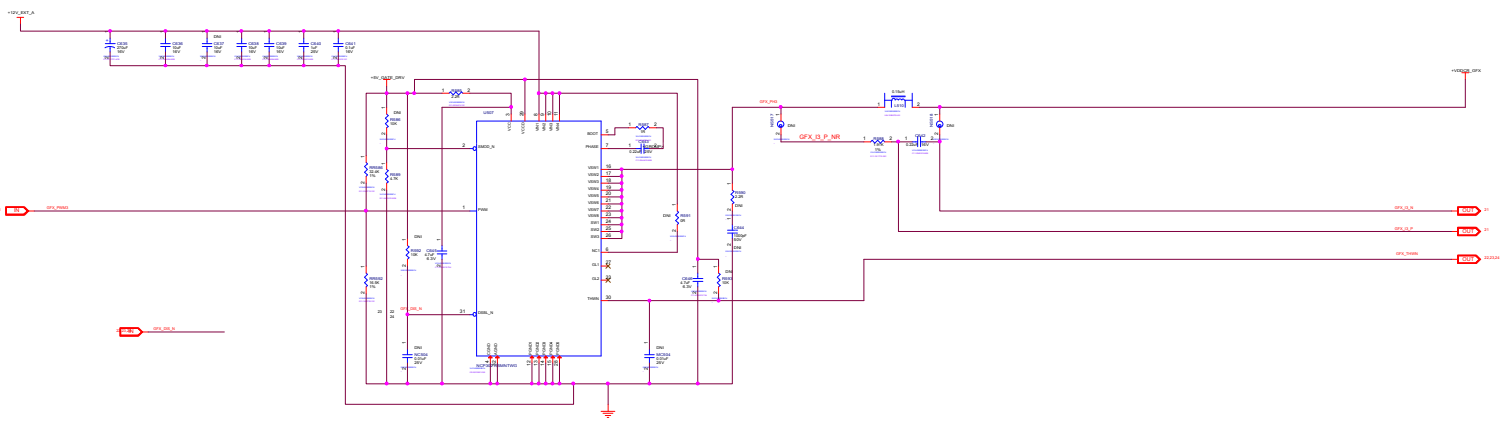
remove



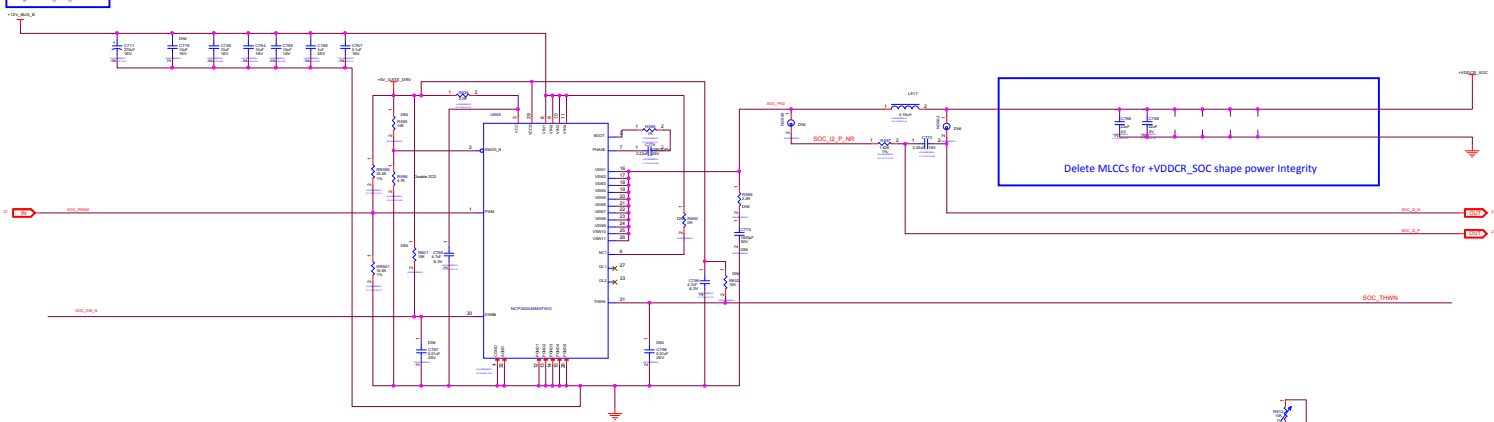
6+2 PHASES : I32-35217HC-I08
 5+1 PHASES : I32-35217JC-I08



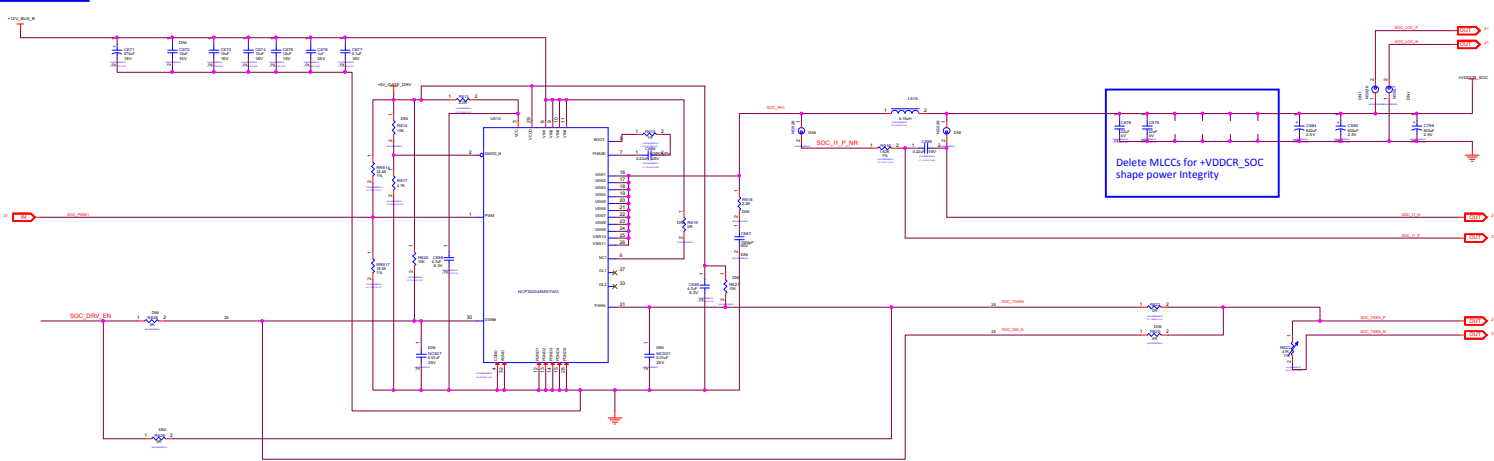


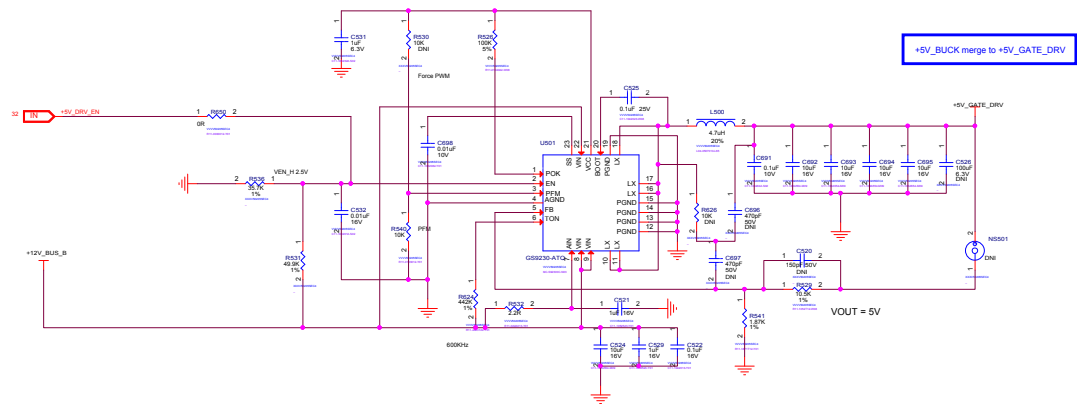


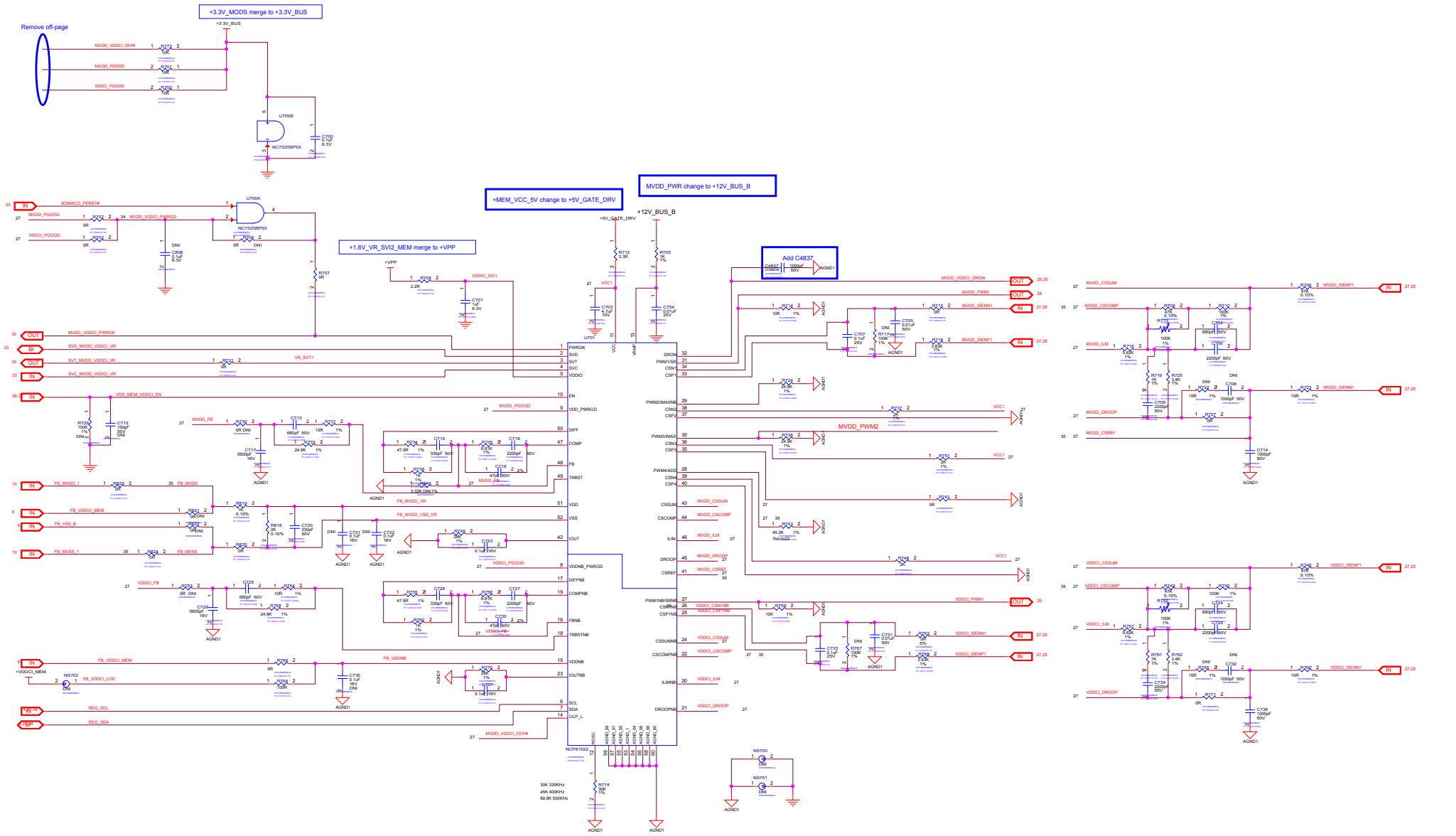
Remove +VDD30C_SOURCE2
change to +12V_BUS_B



Remove +VDD30C_SOURCE1
change to +12V_BUS_B







MVDD_PWR change to +12V_BUS_B

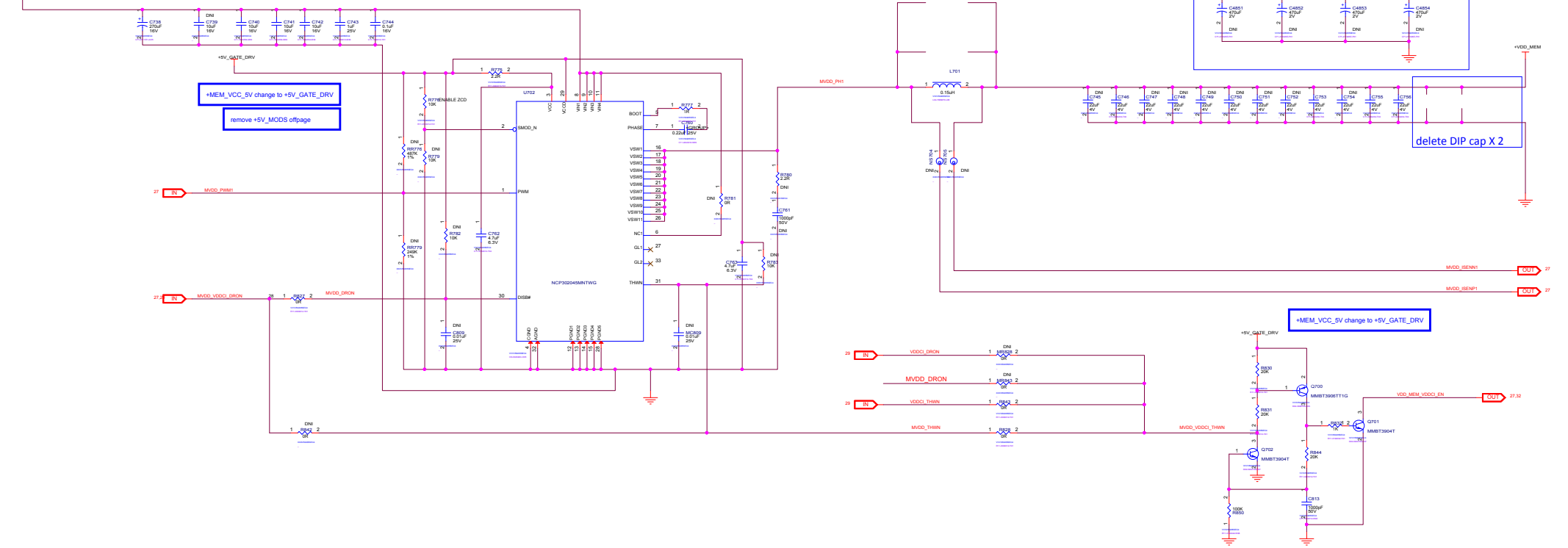
+12V_BUS_B

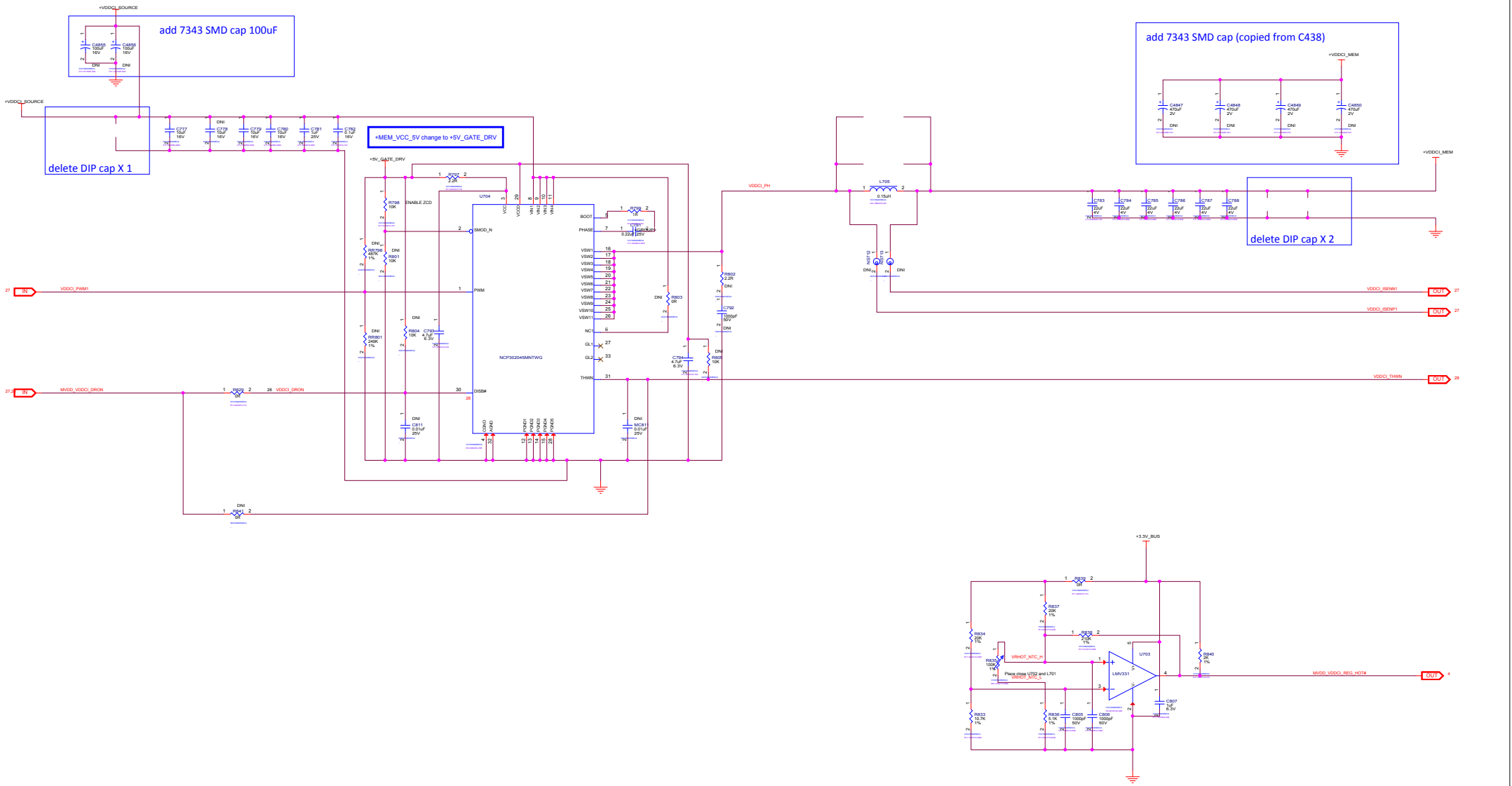
+MEM_VCC_5V change to +5V_GATE_DRV
remove +5V_MODS offpage

add 7343 SMD cap (copied from C438)

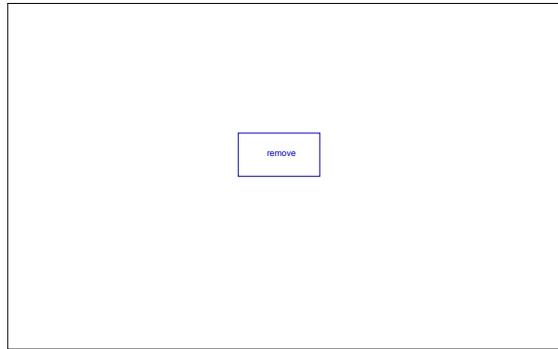
delete DIP cap X 2

+MEM_VCC_5V change to +5V_GATE_DRV

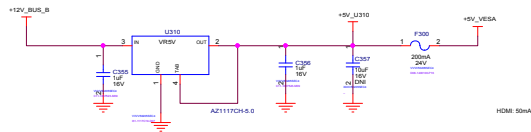


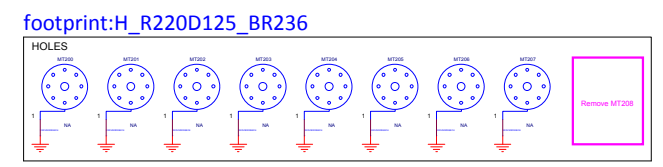
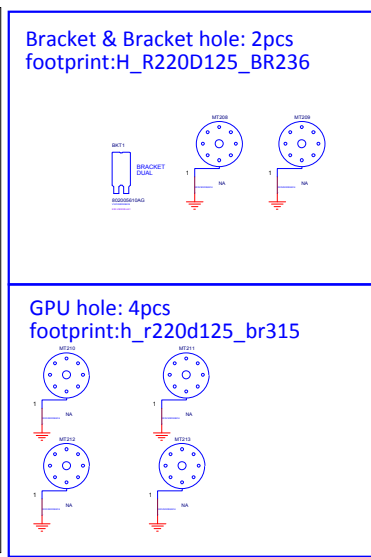
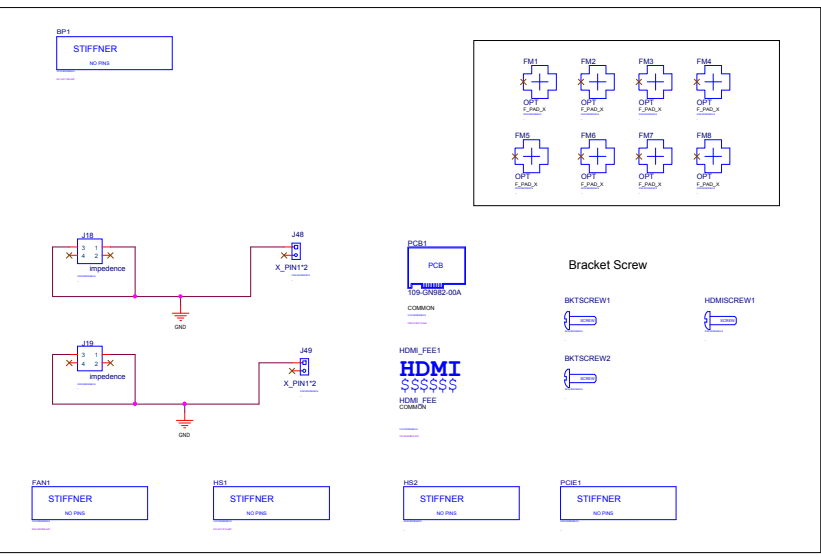
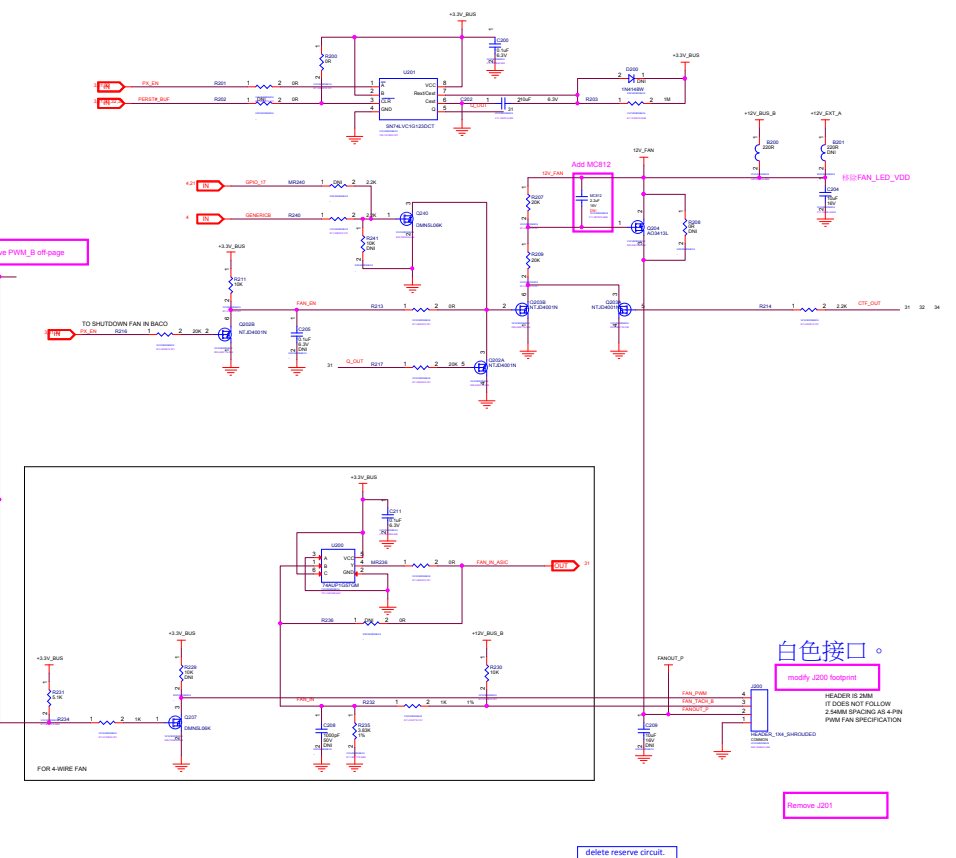
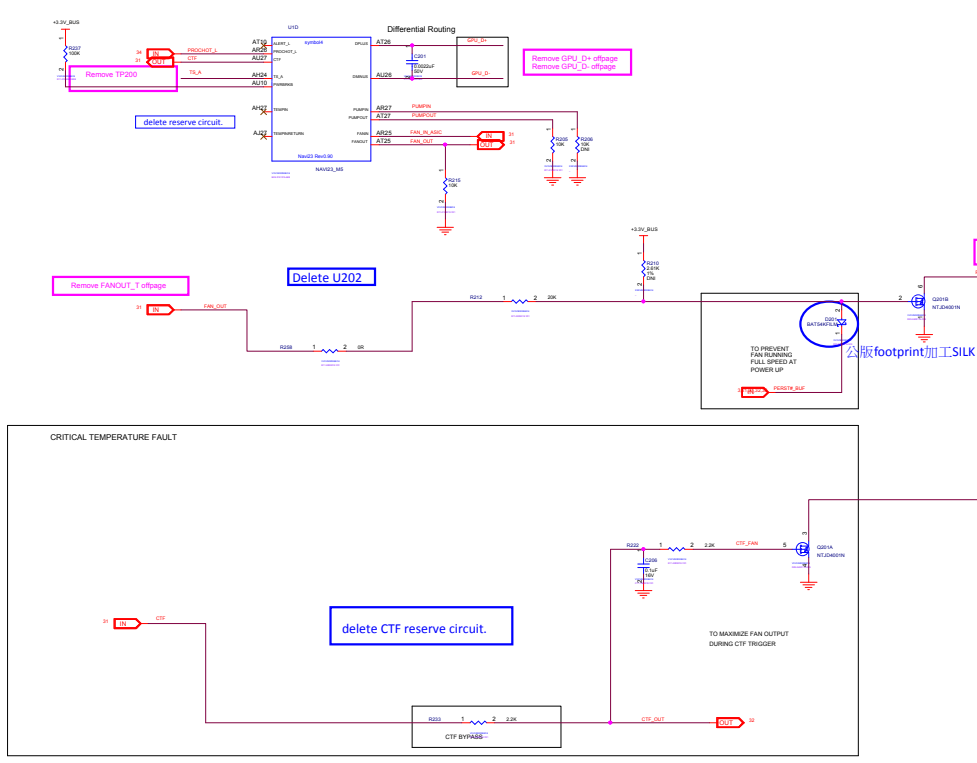


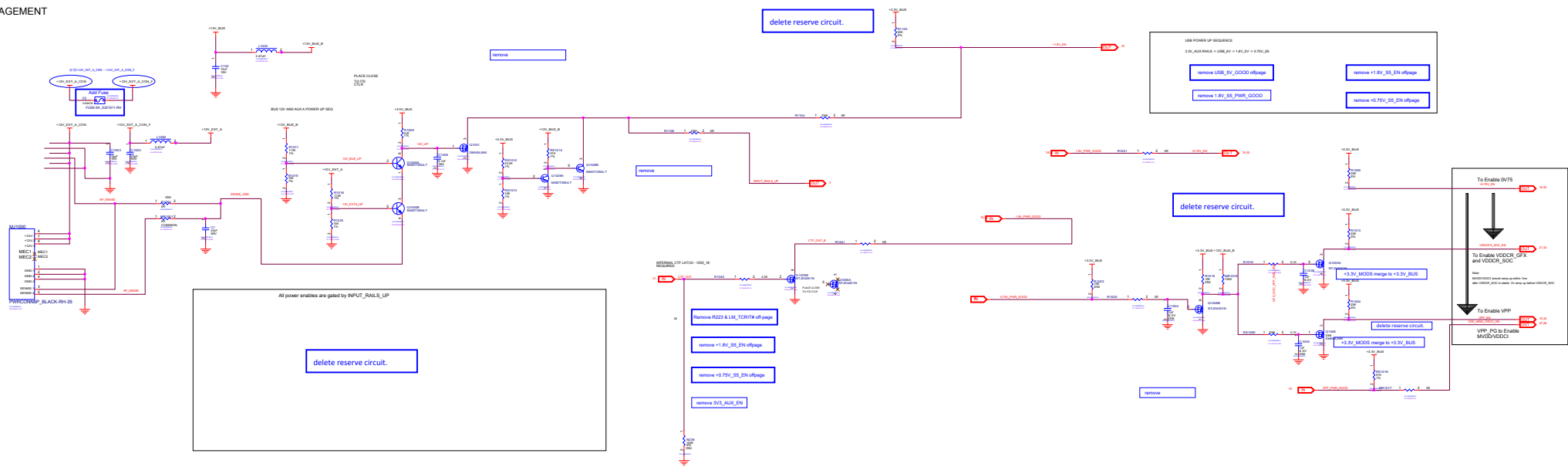
+1.8V FOR BOMACO



+5V_VESA FOR HDMI







All power enables are gated by INPUT_RAILS_UP

delete reserve circuit.

remove R22 & LM_TCR14 offlag

remove 1.8V_S1_EN offlag

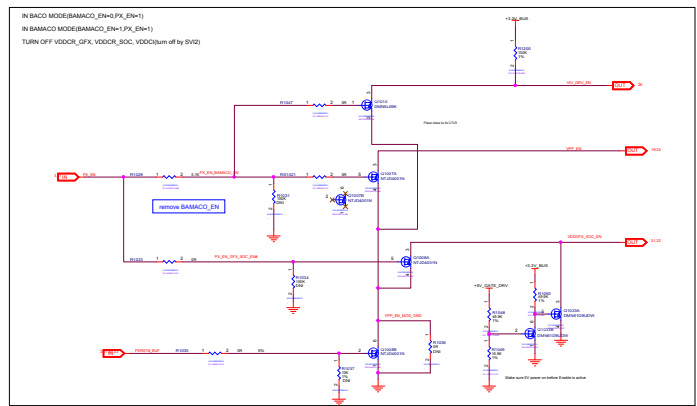
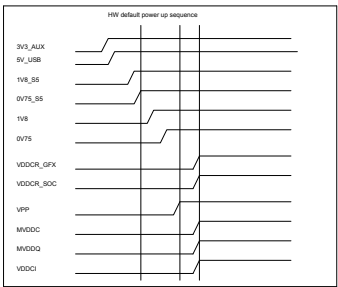
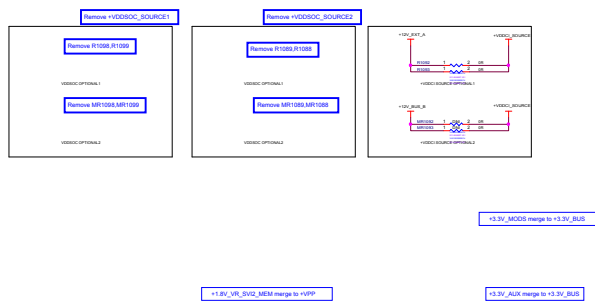
remove 0.75V_S1_EN offlag

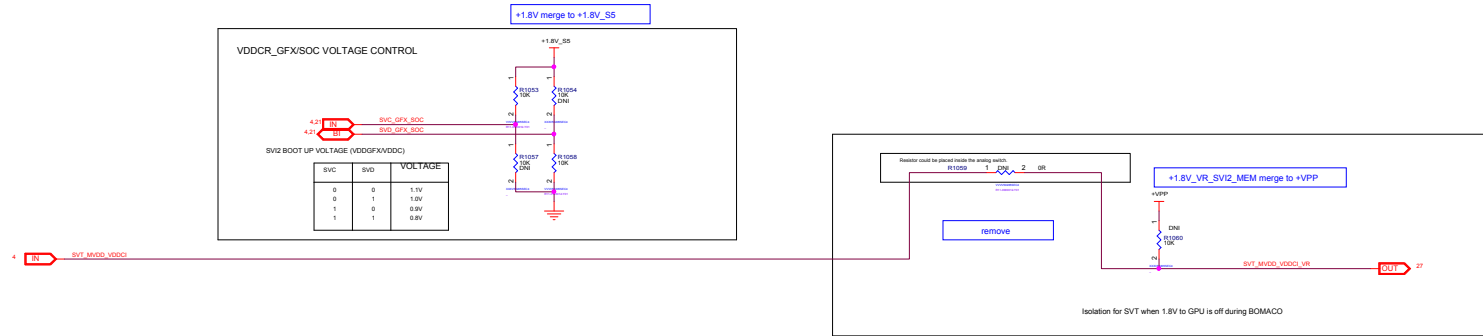
remove 3V3_AUX_EN

To Enable 0V75
VDDCR_S0C

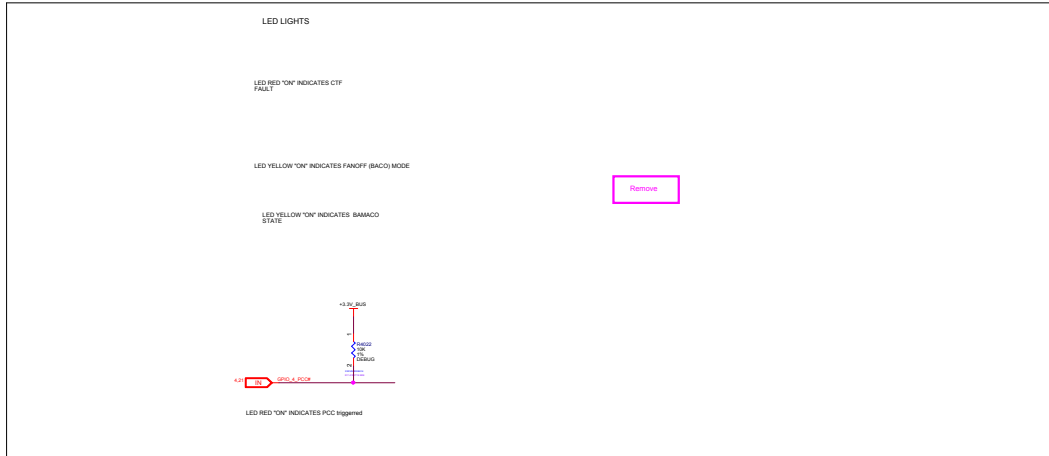
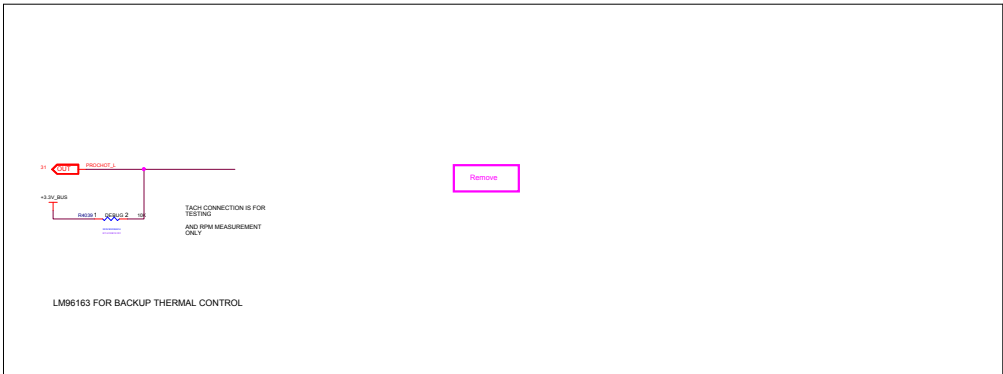
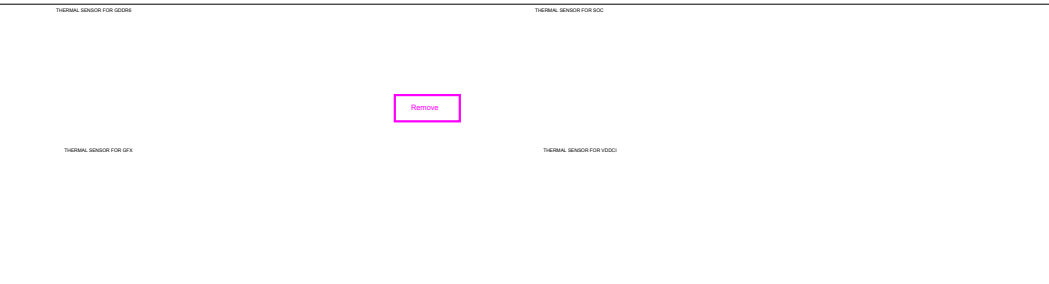
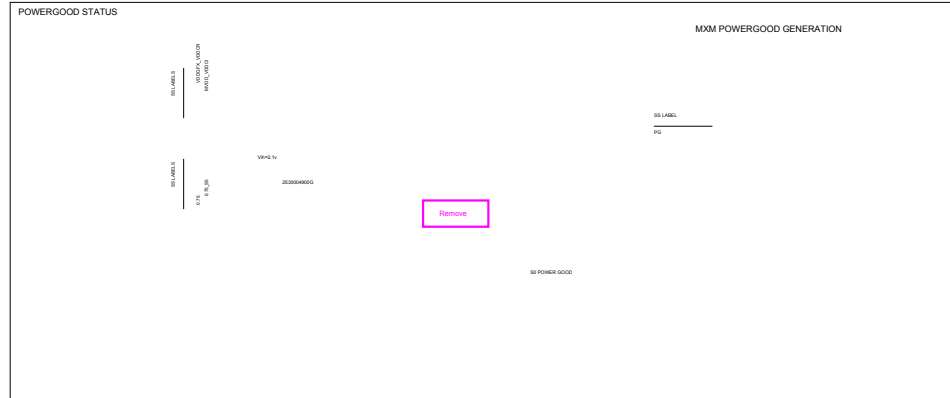
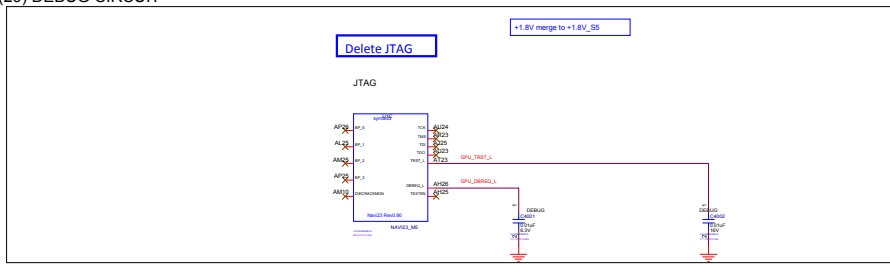
To Enable VDDCR_GFX
and VDDCR_S0C

To Enable VPP
VPP_PG to Enable
MVDDQ






(29) DEBUG CIRCUIT



Remove PI Debug

	MICRO-STAR INT'L CO.,LTD	
	MS-V502	
	Size Custom	Document Description 0035 MINI PI
Date: Wednesday, May 19, 2021		Sheet 35 of 37



TITLE:

NAVI23 DT XT GDDR6 x16 BOARD

DOCUMENT NUMBER:

105-D532cc-00

DATE:

Tue Jul 07 03:31:54 2020

SHEET NUMBER:

36 OF 36

REV: 00B

REVISION HISTORY

ENGINEER:

Yahyazadeh, Danial

NOTES:

NOTE

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REVISION DESCRIPTION

SCH Rev

PCB Rev

Date

00A 00A 05/19/2020 Initial schematic
00B 00B 06/30/2020 Change all ESD based on EM's new requirement Add Q1033 related circuit for VDDGFX_SOC_EN control to resolve the potential risk on SACO avx(P2)
07/06/2020 Change +3.3V_MDDR, +5V_MDDR, +5V_GATE_DRV circuit(P20,P21)



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Custom	0036 REVISION HISTORY	2.0

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