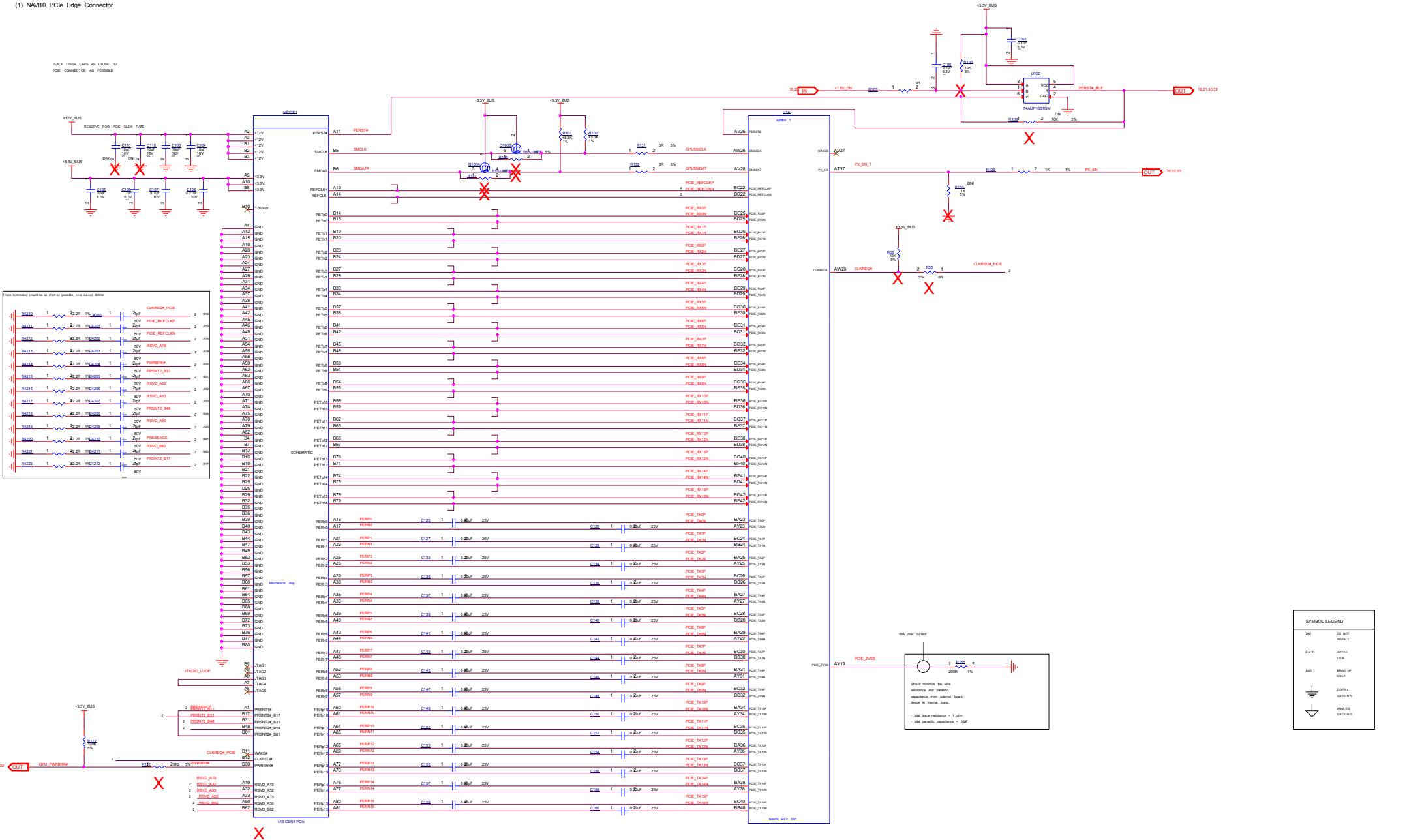


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22	REG MVDD		
23	REG VDDCI		
24	REG 0.75V		
25	REG 1.8V		

(1) NAV10 PCIe Edge Connector

PLACE THESE CAPS AS CLOSE TO  
PCI CONNECTOR AS POSSIBLE

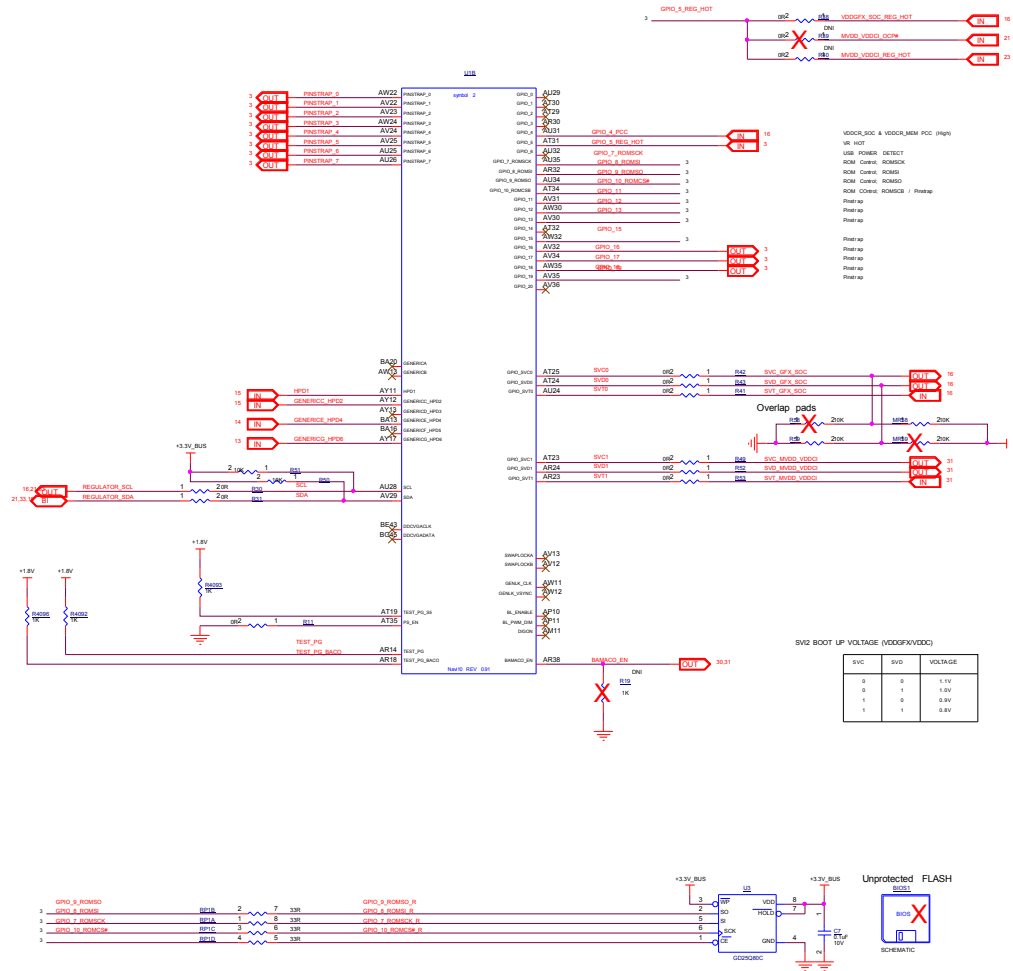


SYMBOL LEGEND

DNV	DO NOT INSTALL
5V #	ACTIVE LOW
BUVD	BRING UP ONLY
	DIGITAL GROUND/0
	ANALOG GROUND/0

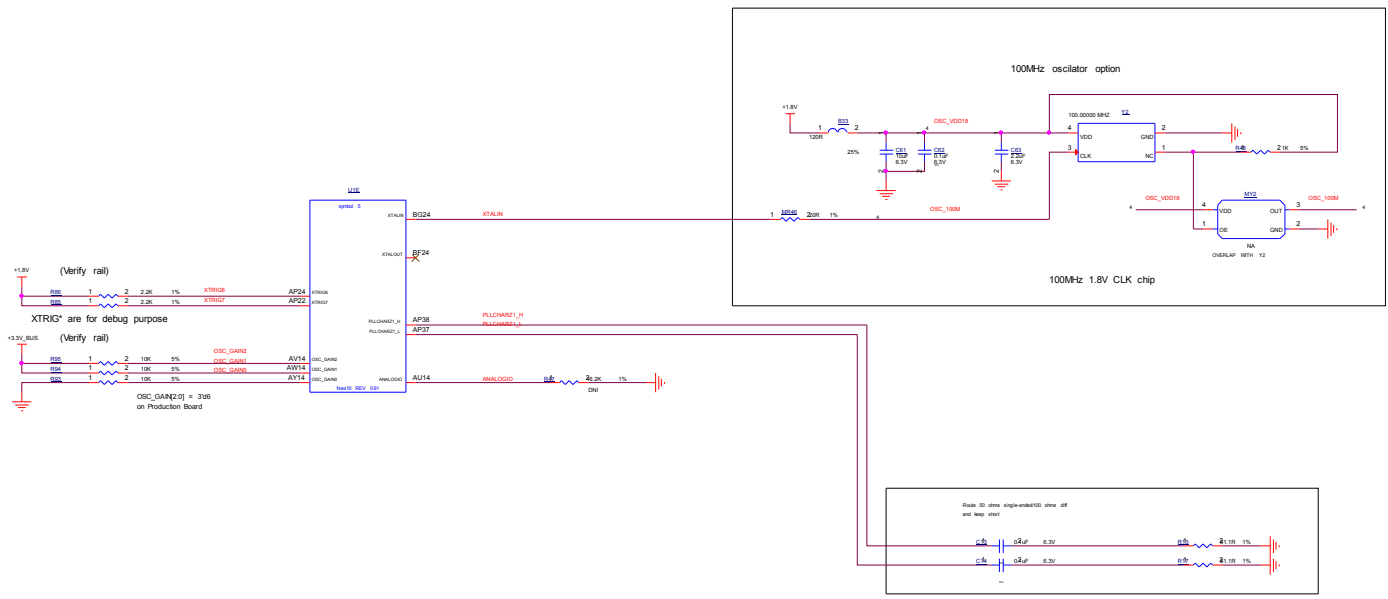
**MICRO-STAR INT'L CO., LTD**  
**MS-V381**

Size	Document	Description	NAV10 PCIe Interface	REV 5.0
Custom				
Date:	2019 11 07	Sheet	2	of 35

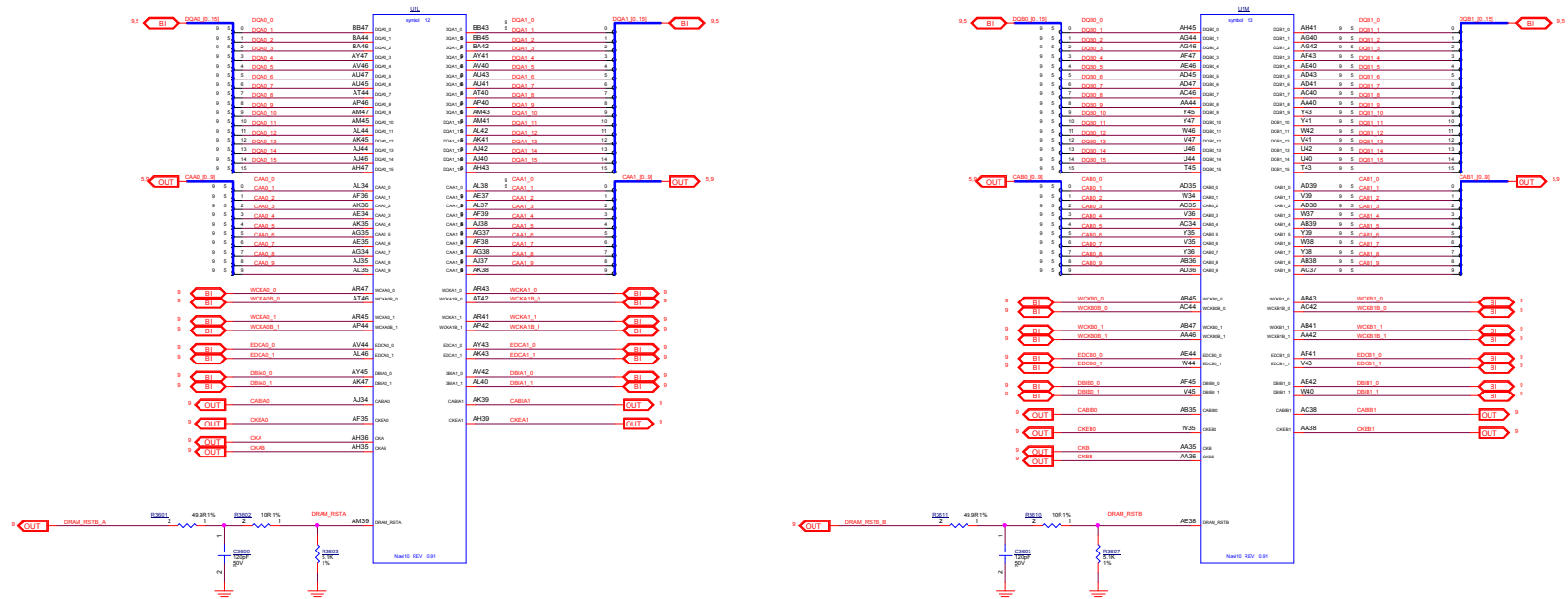


Note: Internal PUPD at GPIO pad is -40k strength in 14nm design spec.

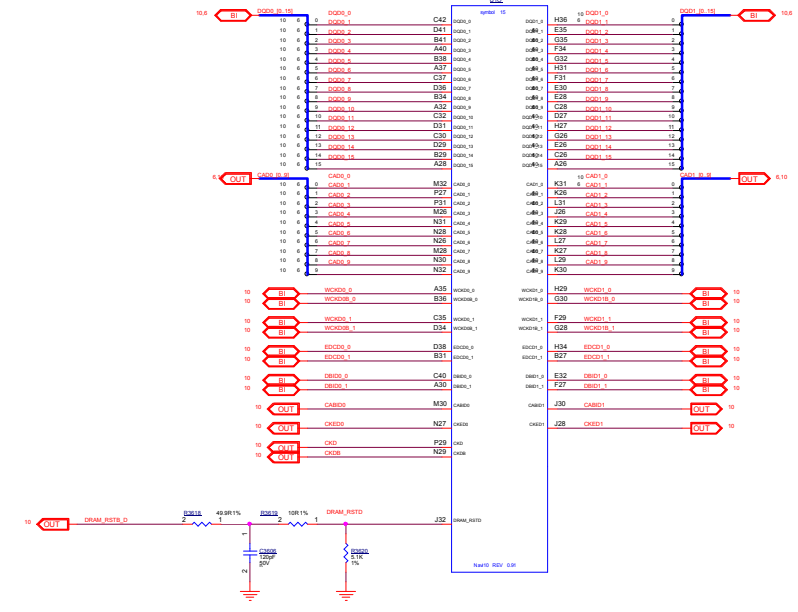
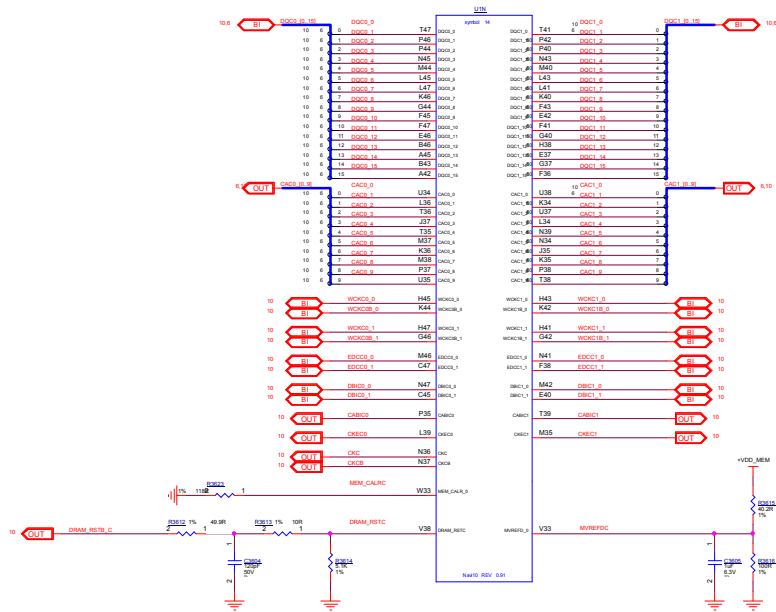
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: FCW GEN 4 not required 1: FCW GEN 4 not required
	0	PNSTRAP_BIF_CLK_PM_EN 0: CLKSTOP power management capability is disabled 1: CLKSTOP power management capability is enabled
	0	PNSTRAP_BIF_IC_TX_SWING 0: VCA controller polarity enabled 1: The signal will be deasserted as the system's VGA controller
DCE	0	PNSTRAP_BIF_VGA_DIS 0: VCA controller polarity enabled 1: The signal will be deasserted as the system's VGA controller
	0	PNSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: 0x enable connected 1: 1x enable connected 2: 2x enable connected 3: 3x enable connected 4: 3x enable connected 5: 2x enable connected 6: 1x enable connected 7: 0x enable connected
	0	PNSTRAP_AUD[1:0] 1: Audio by DisplayPort only 2: Audio by DisplayPort and HDMI if display is selected 3: Audio by DisplayPort and native HDMI
Platform	0	GPIO_18
	0	GPIO_17
	0	GPIO_16
SMU	1	PNSTRAP_2
	0	PNSTRAP_1
	1	PNSTRAP_0
	0	GPIO_18
	0	GPIO_16
	1	PNSTRAP_BIOS_ROM_EN 0: enable 1: disable the external BIOS ROM device



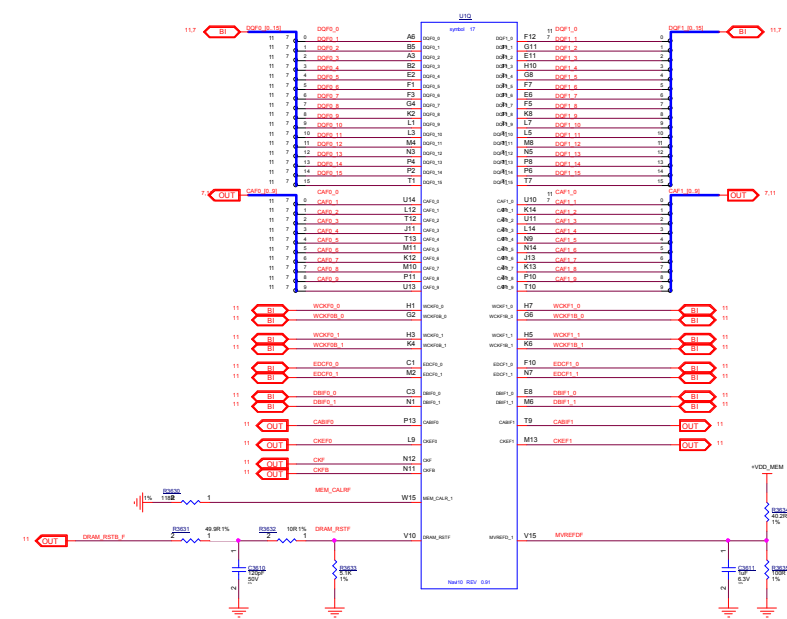
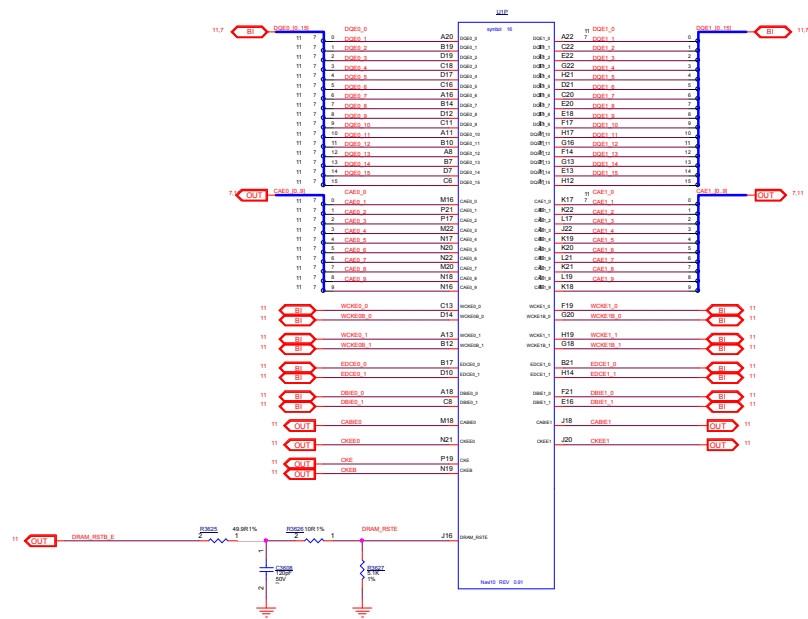
NAVI 10 MEM INTERFACE CH A/B



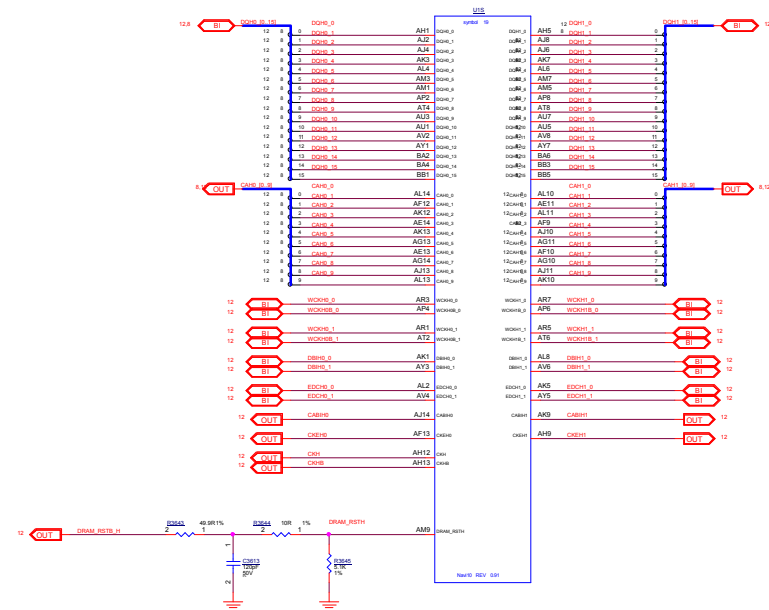
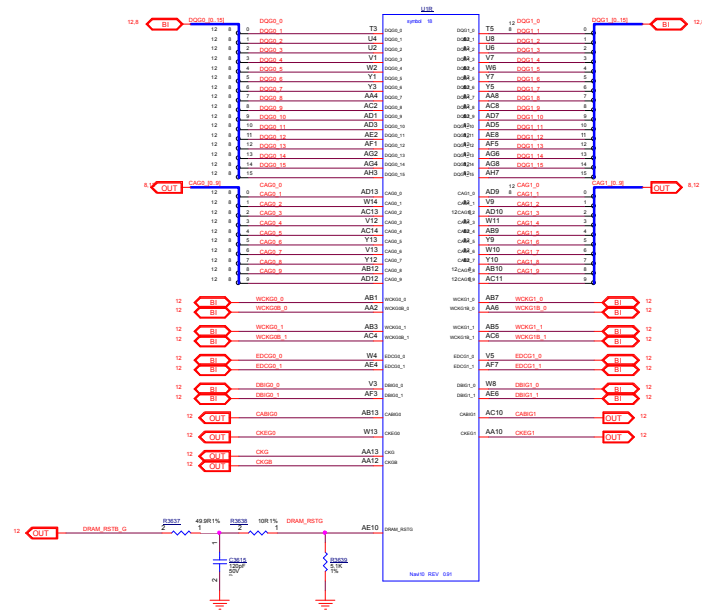
NAVI 10 MEM INTERFACE CH C/D



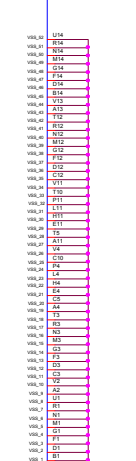
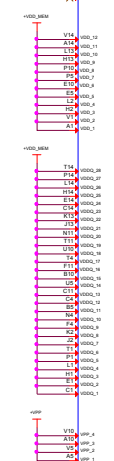
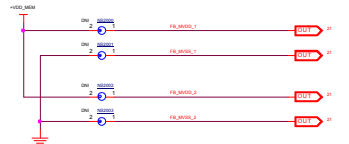
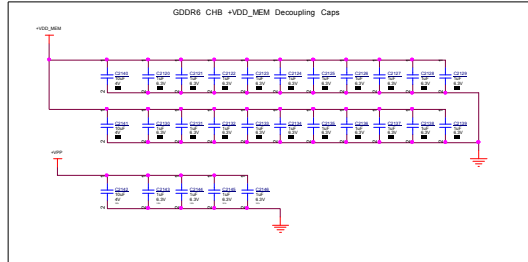
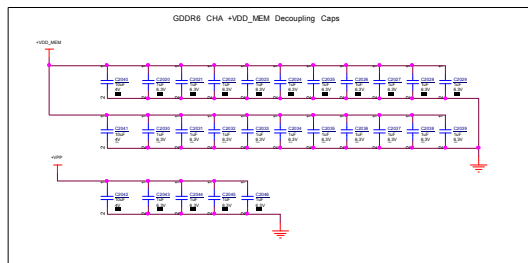
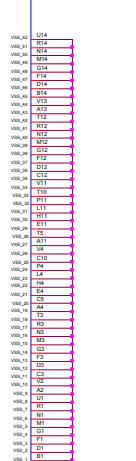
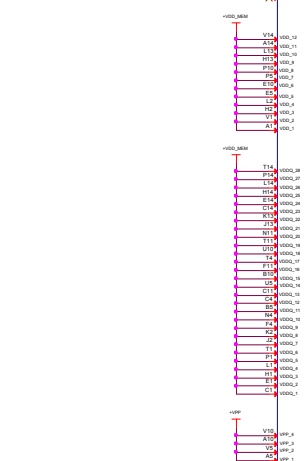
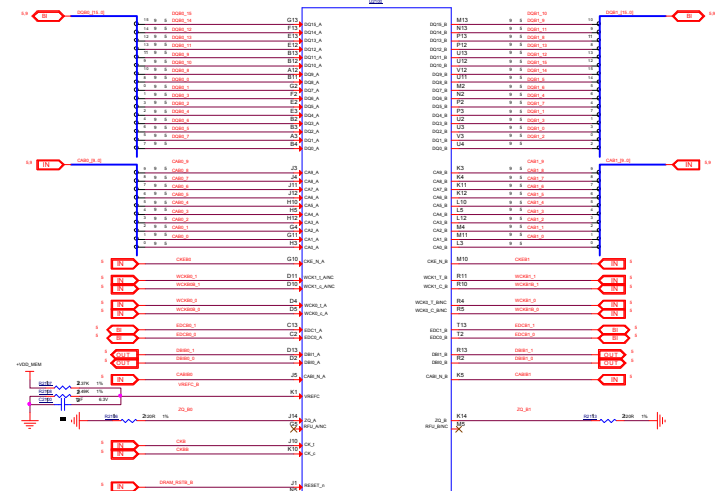
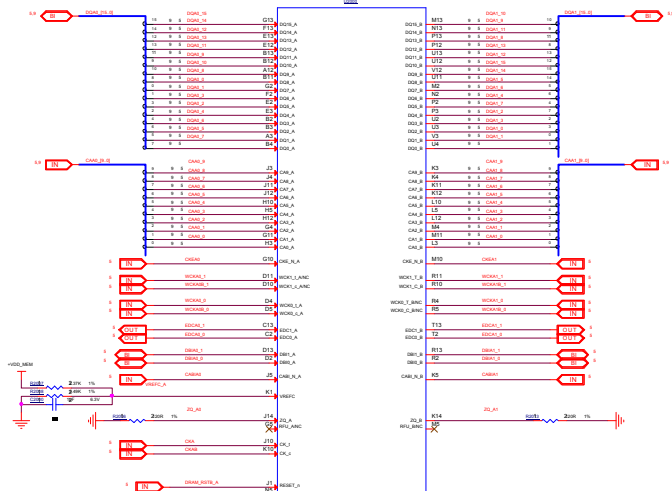
NAVI 10 MEM INTERFACE CH E/F

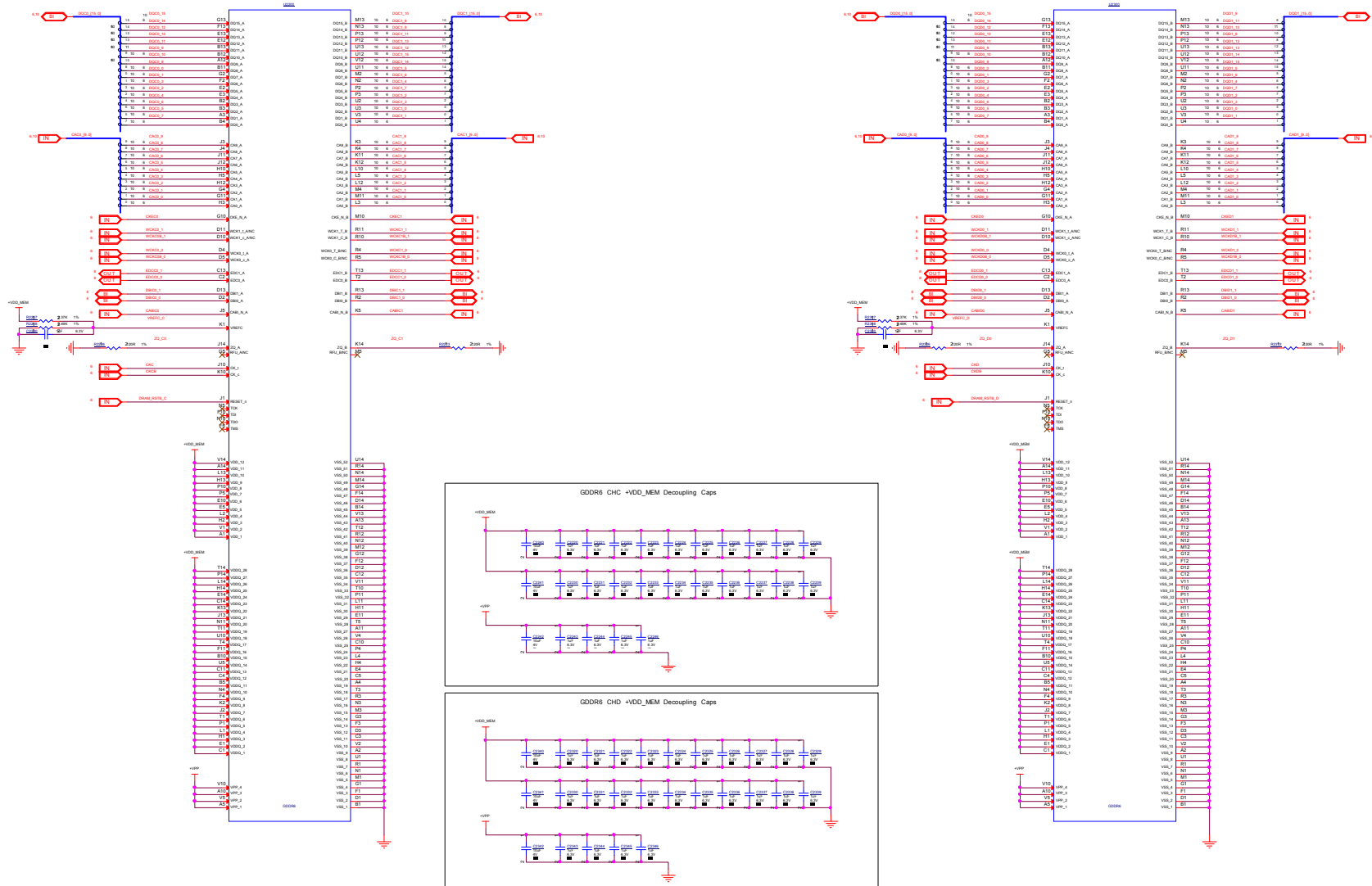


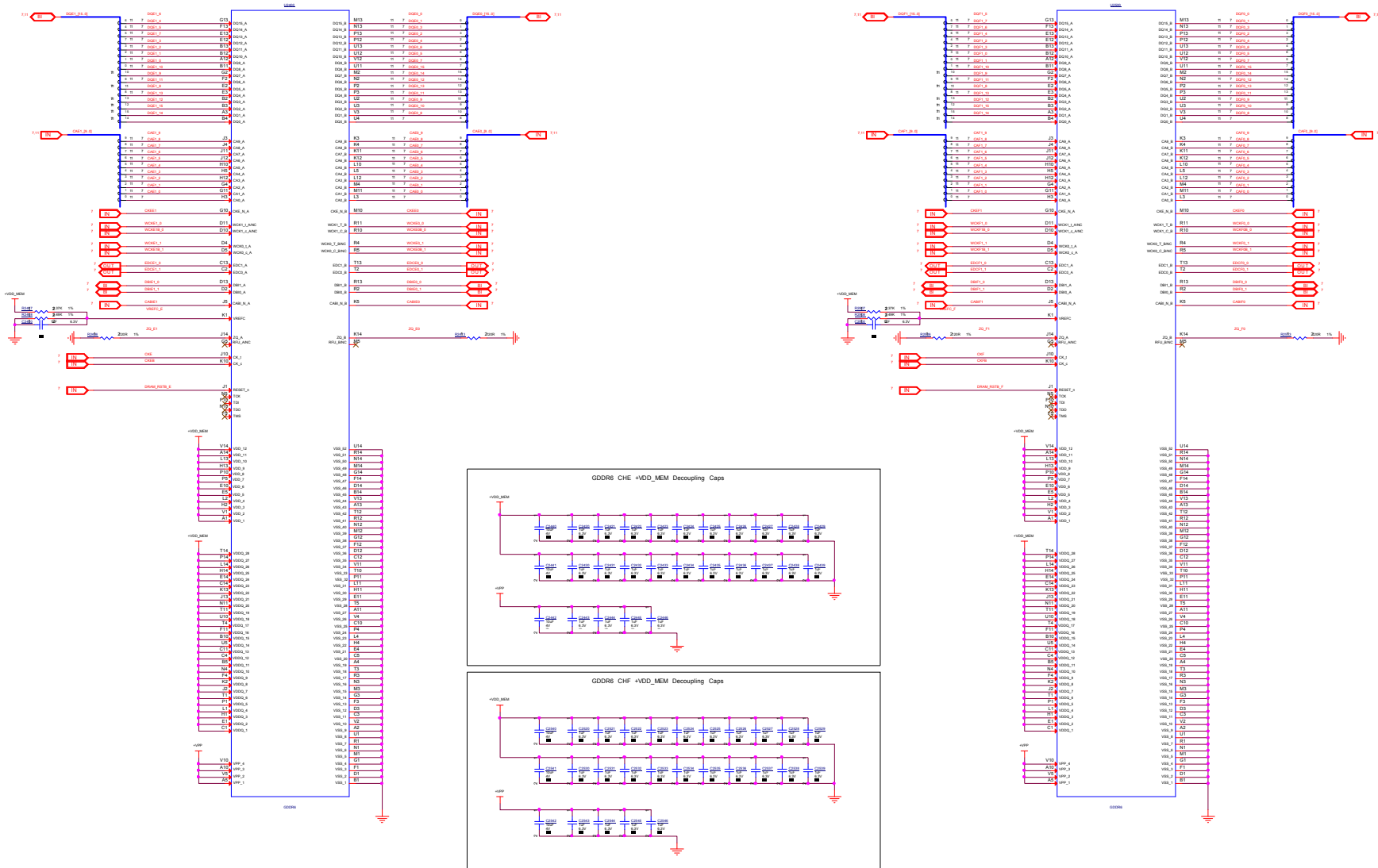
NAVI 10 MEM INTERFACE CH G/H

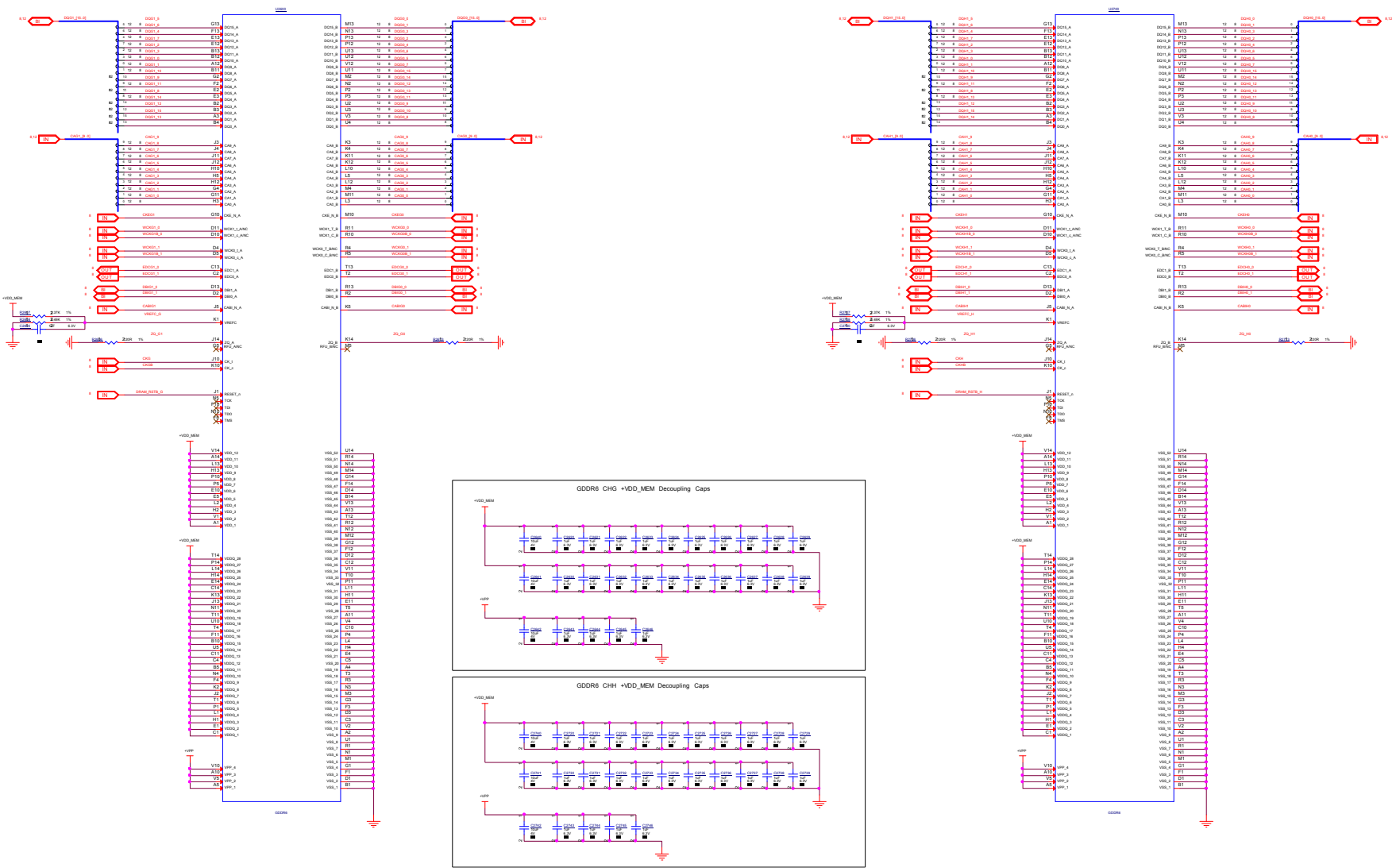


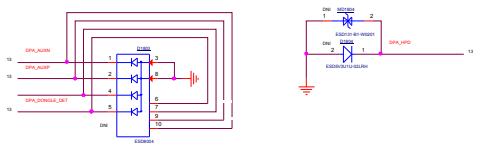
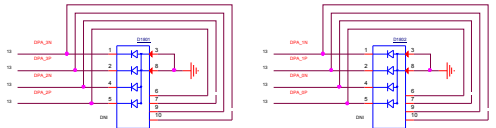
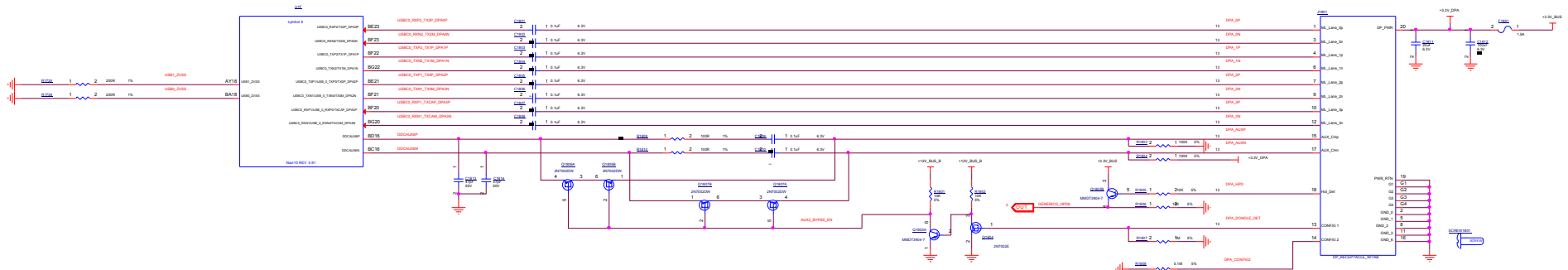
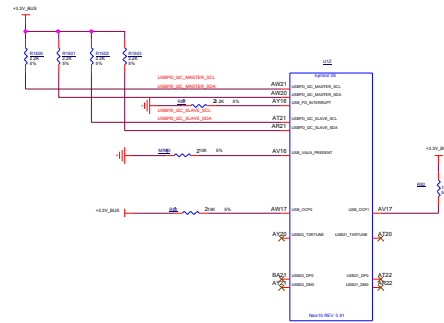
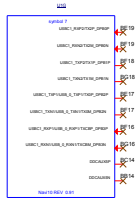




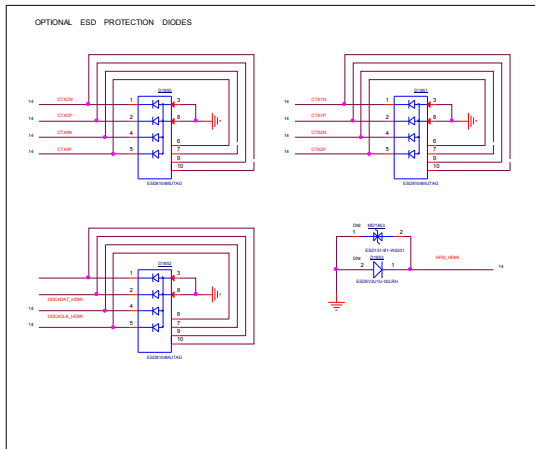
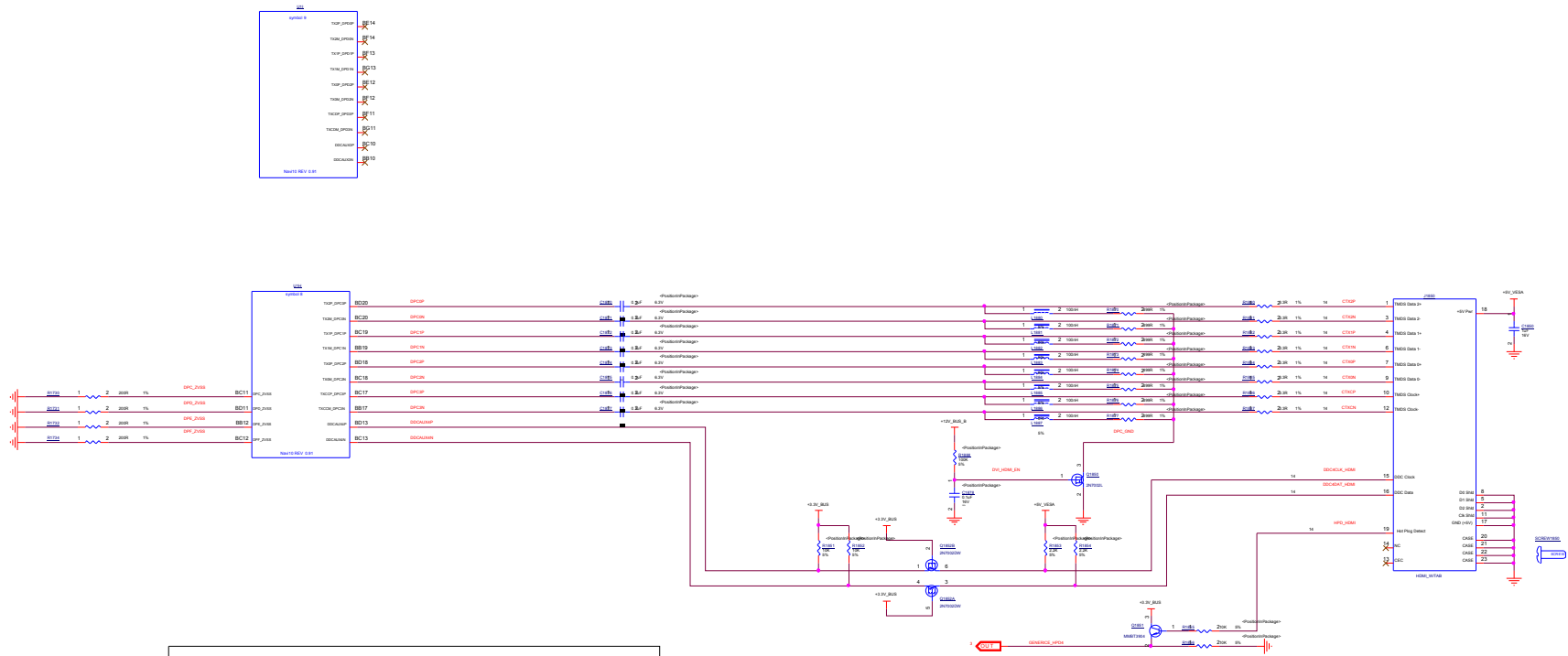




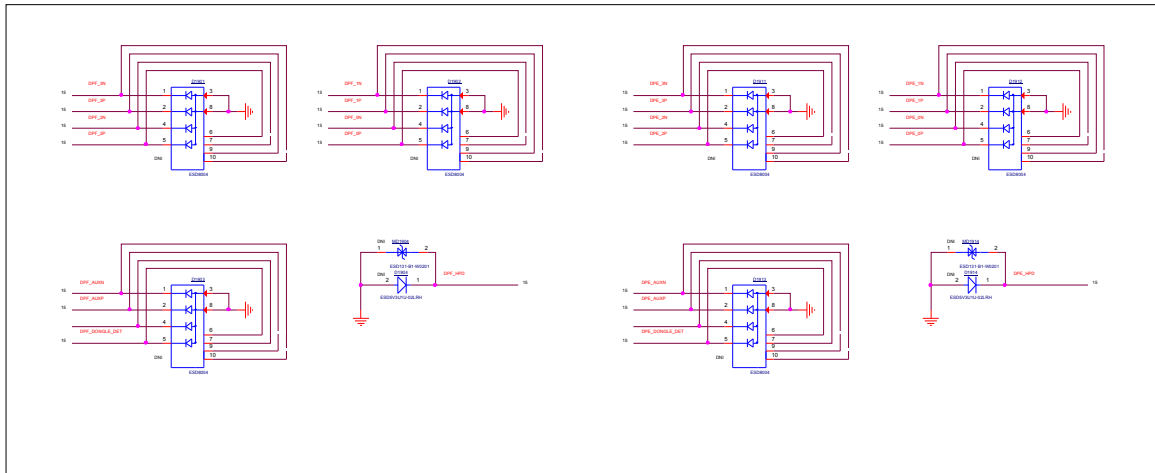
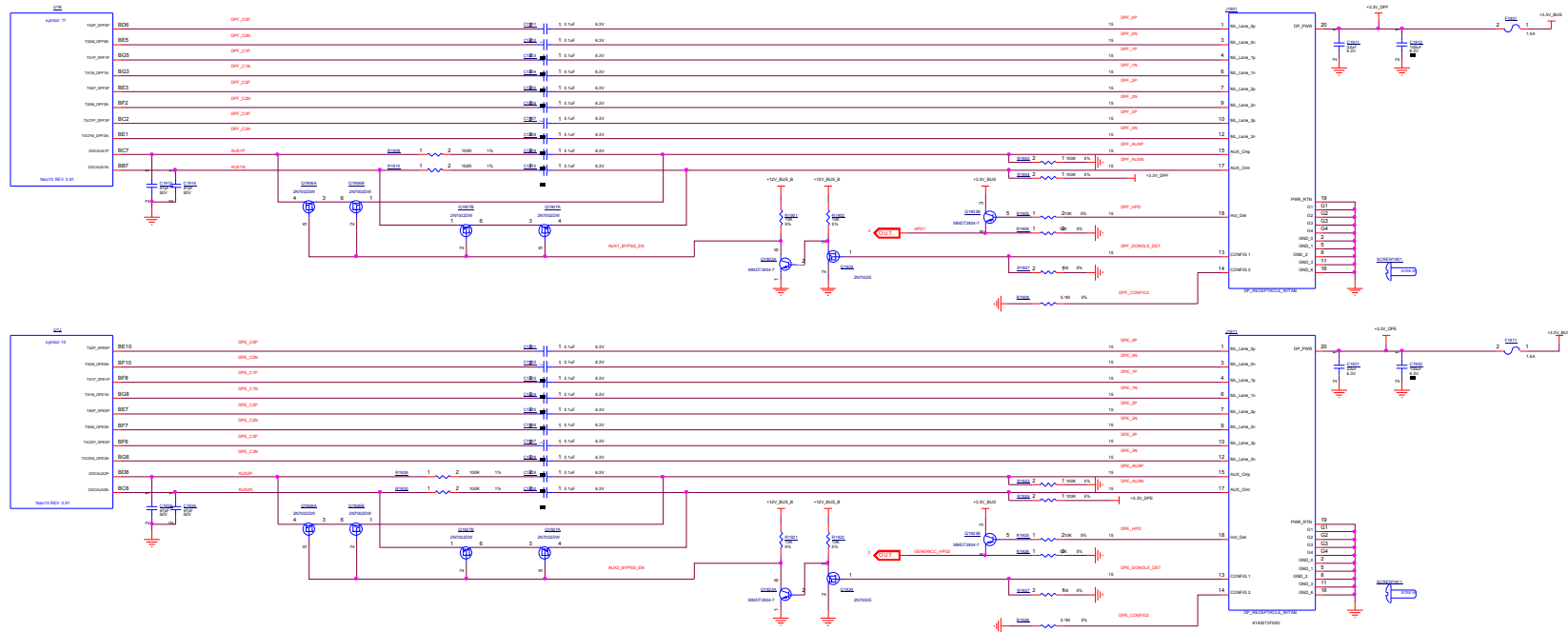


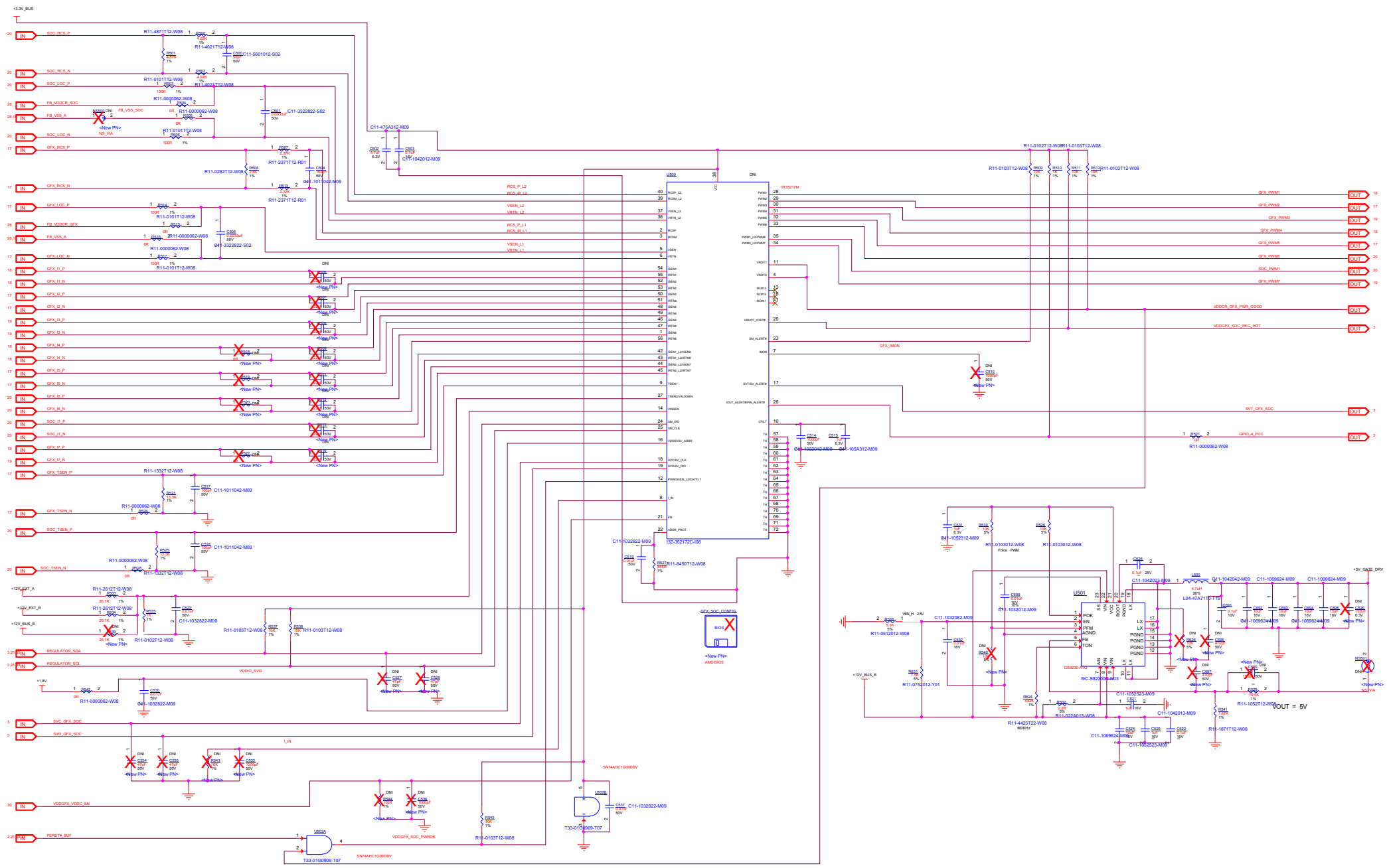


NAV110 TMDP C/D

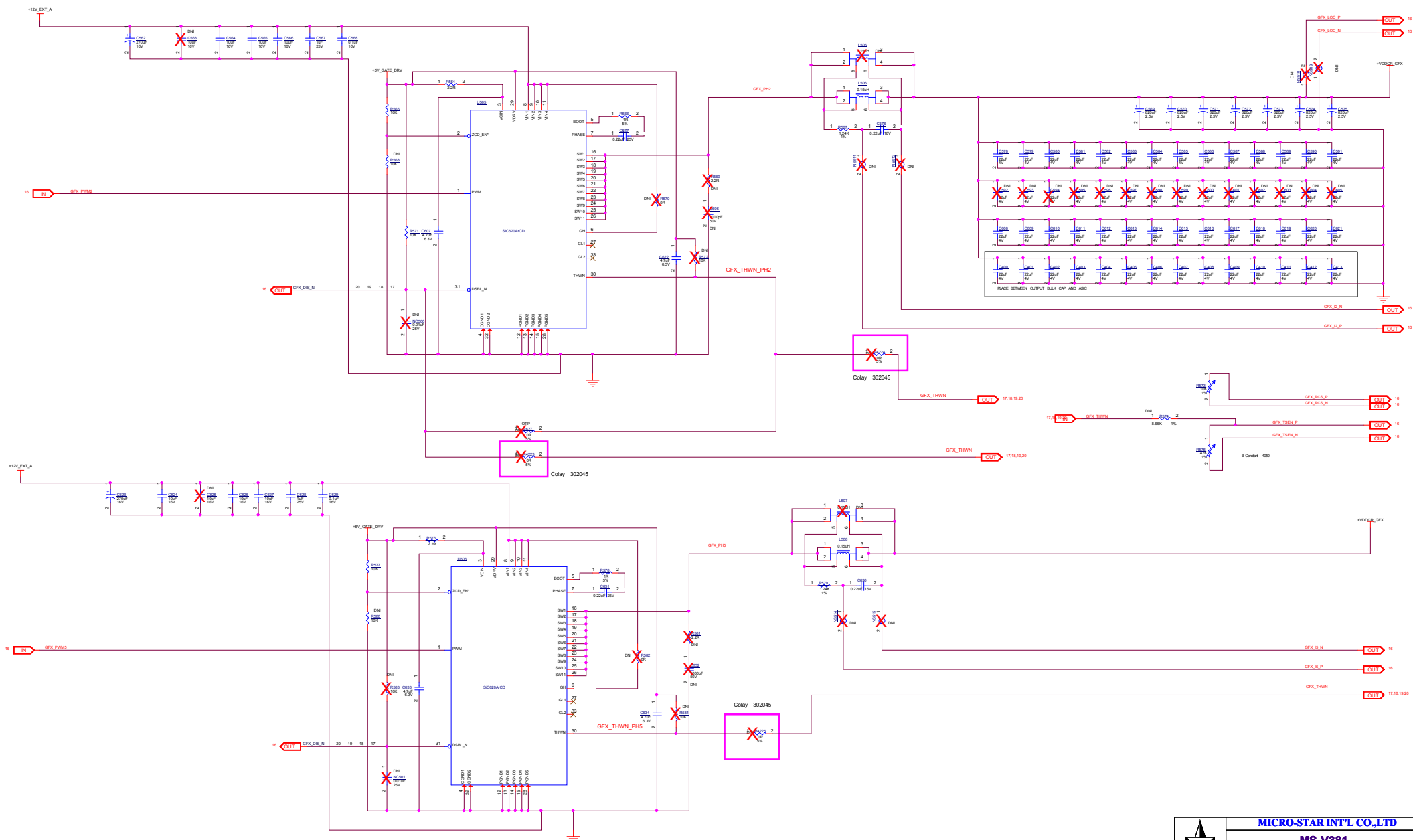


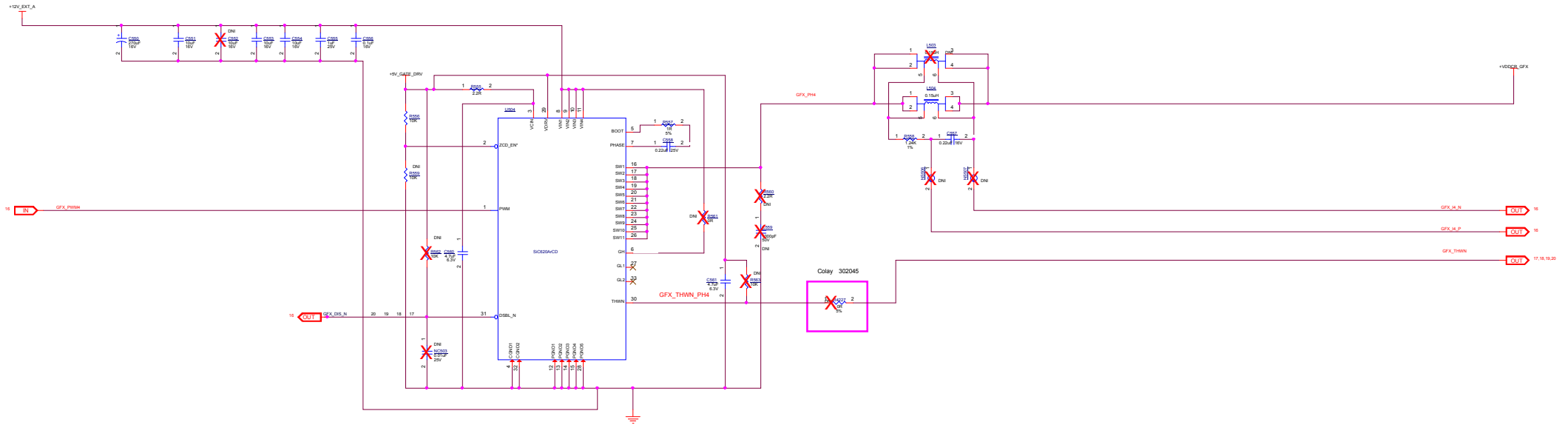
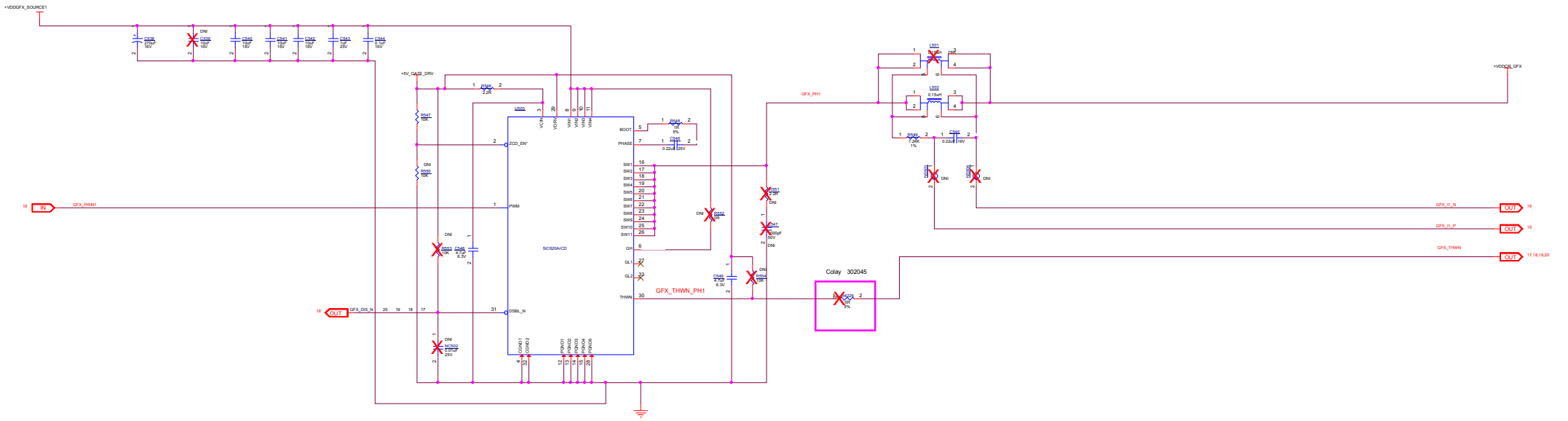
(9) NAVI10 TMDP E/F

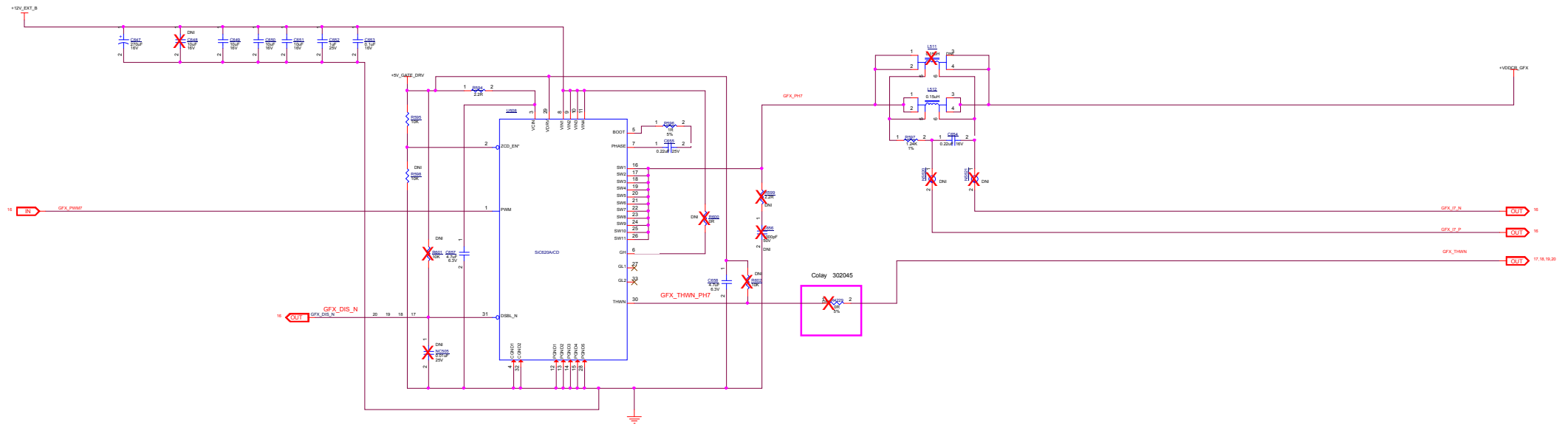
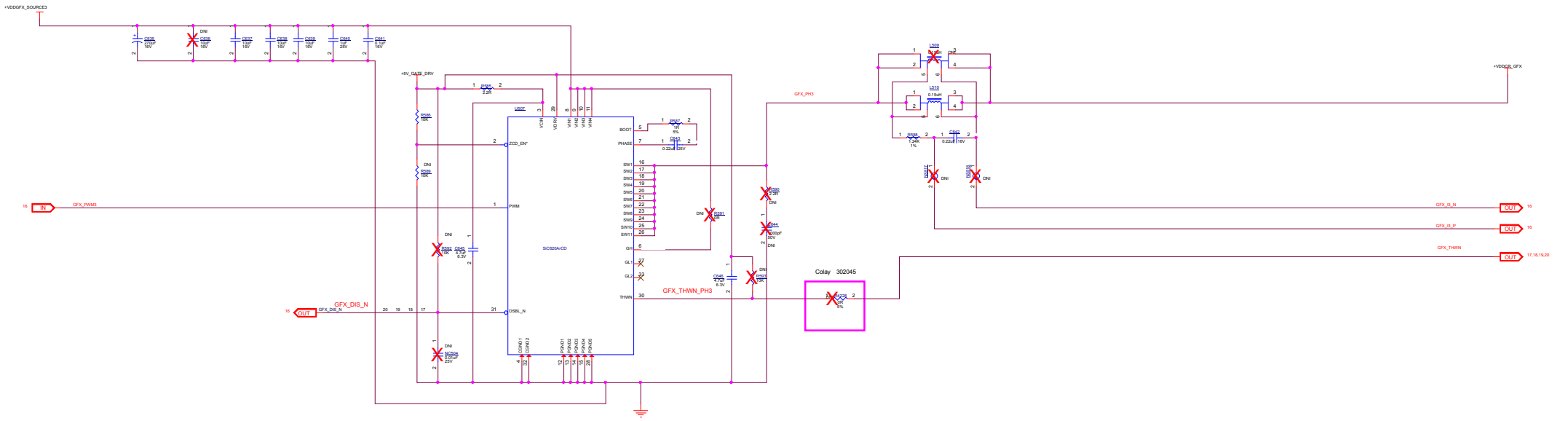


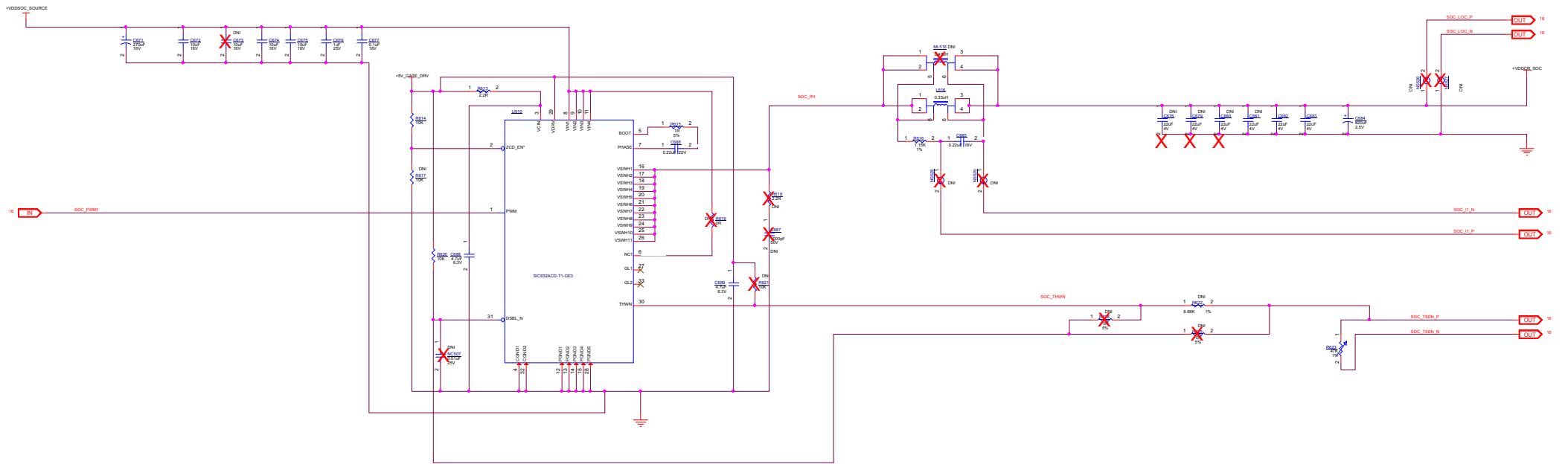
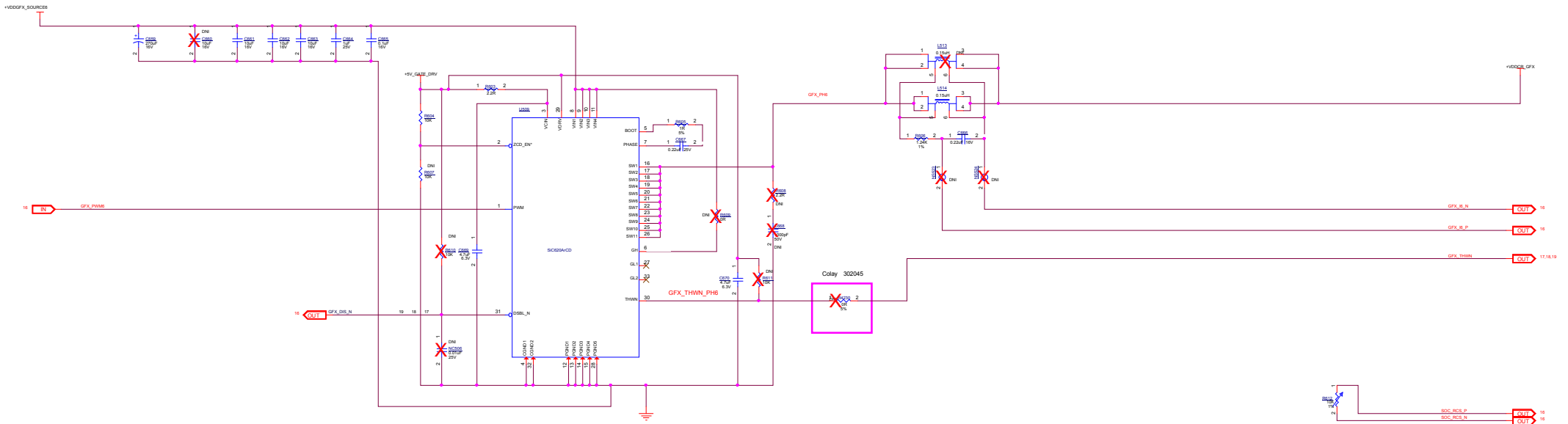


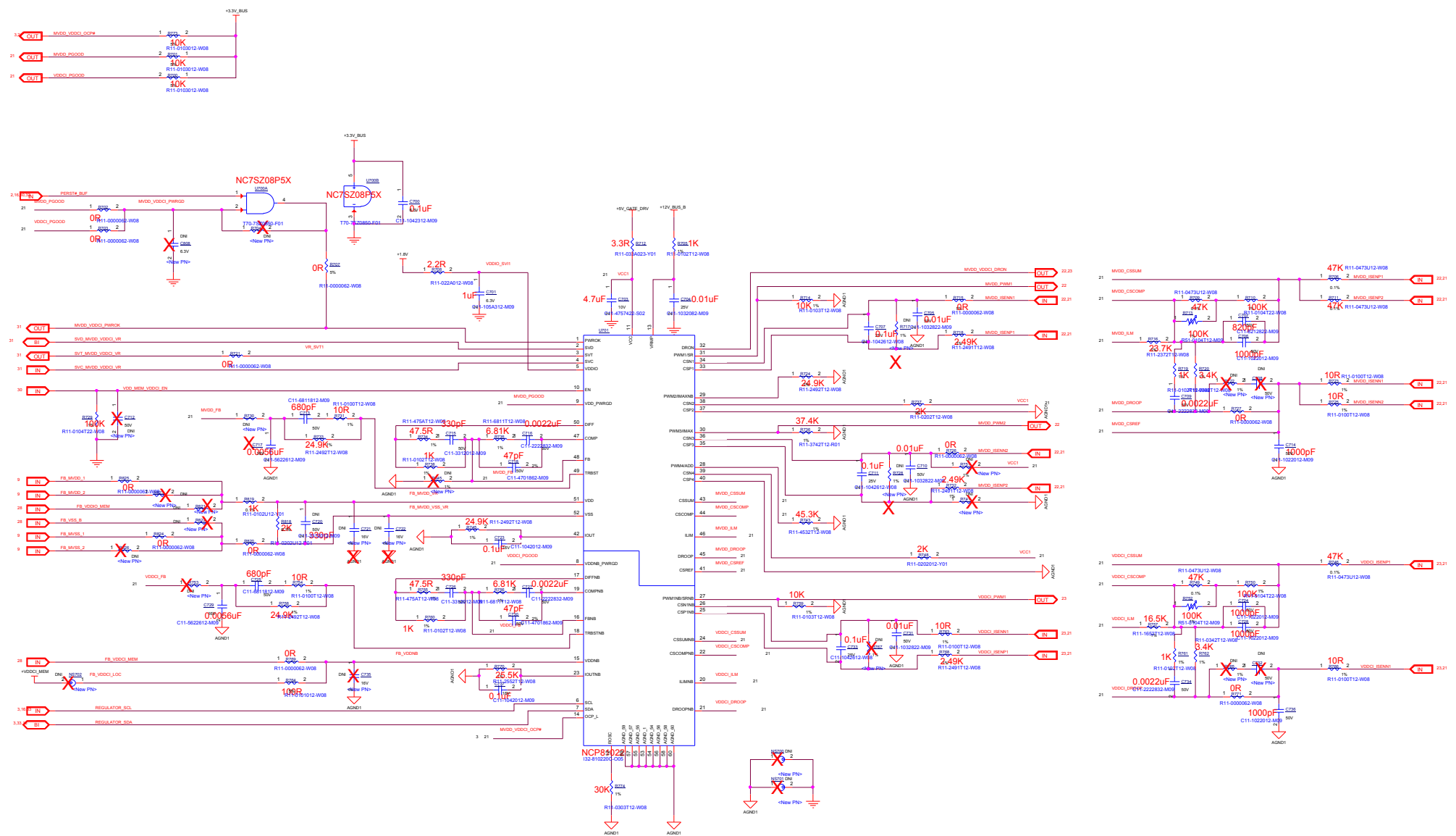


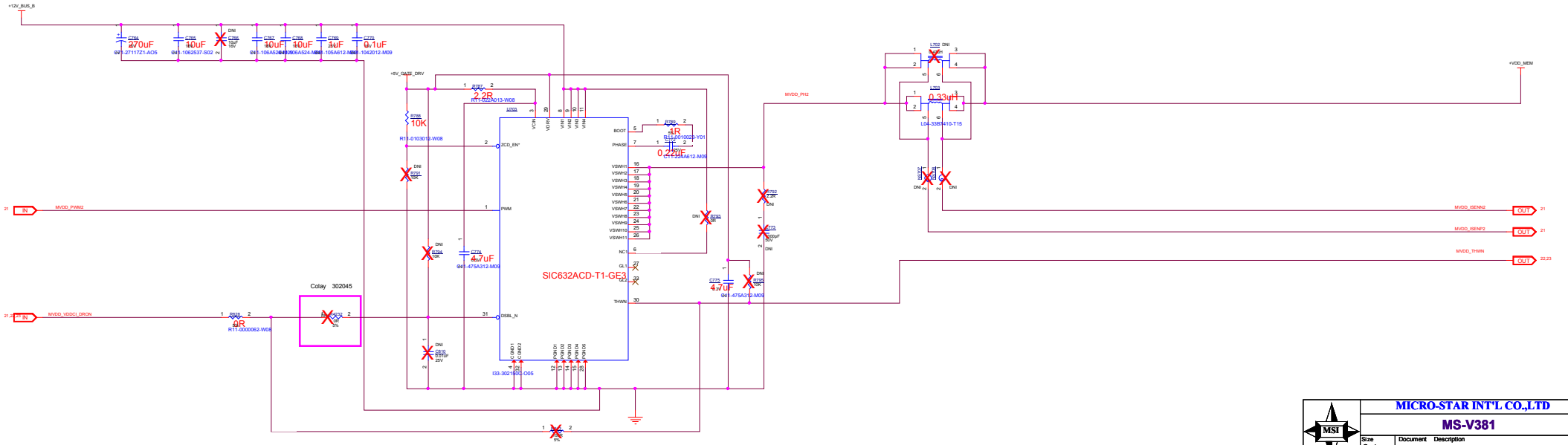
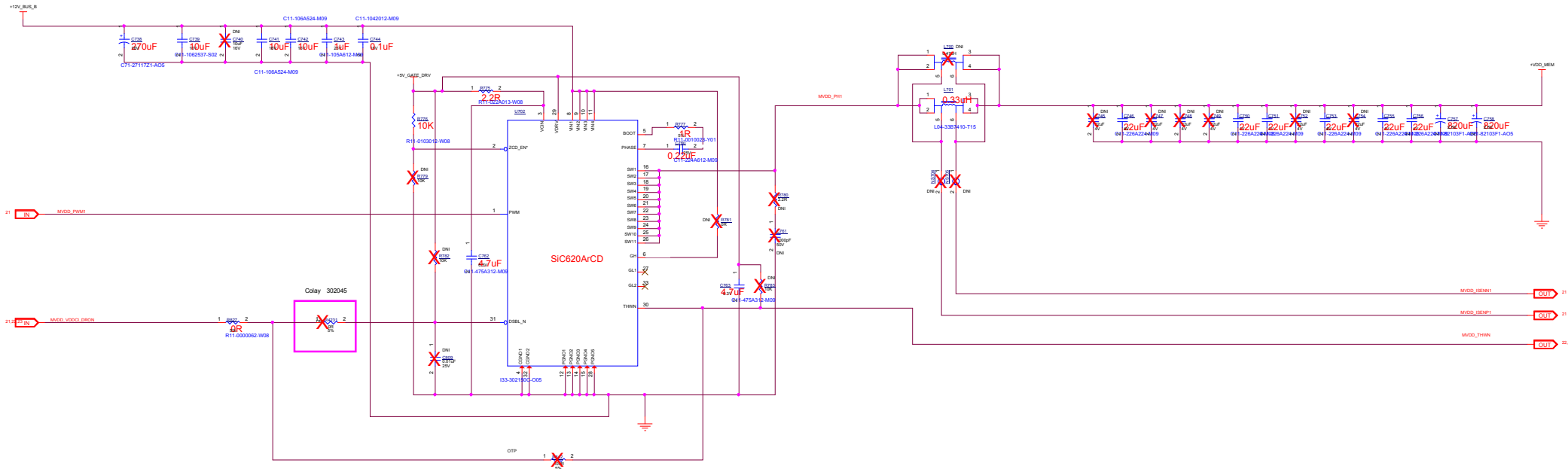


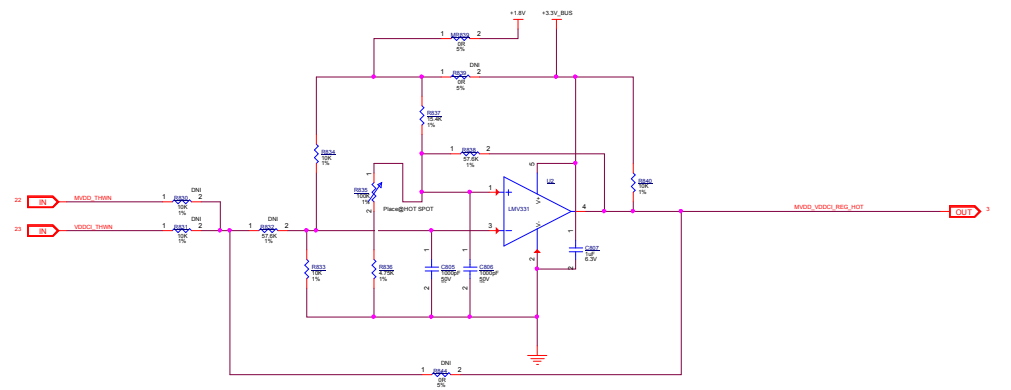
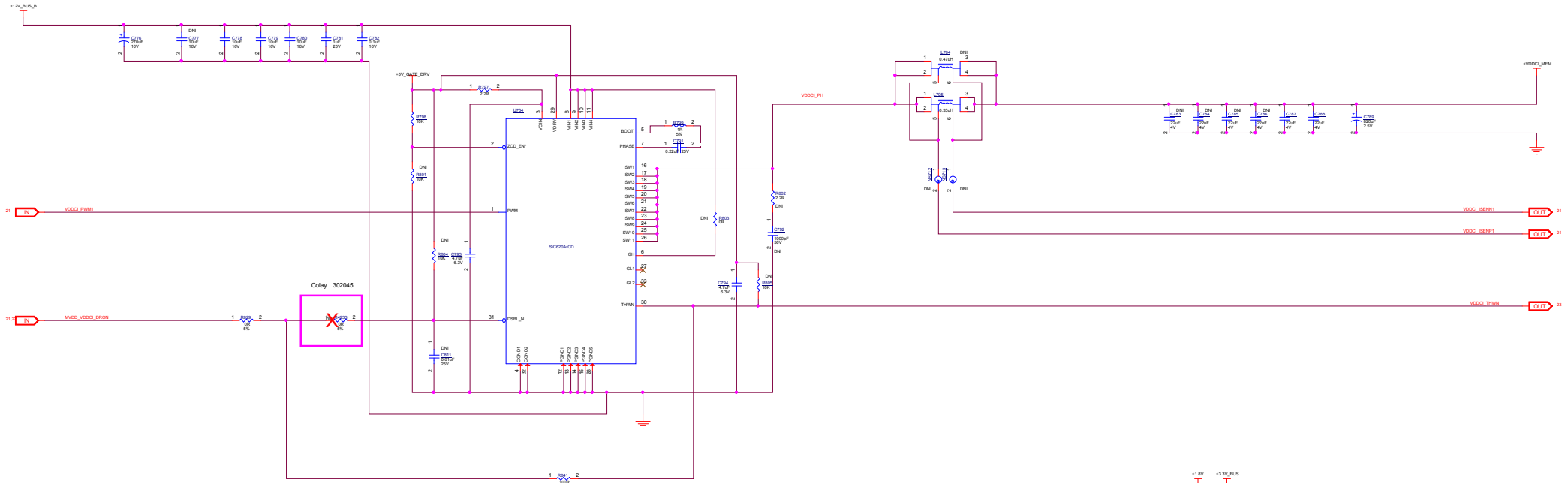


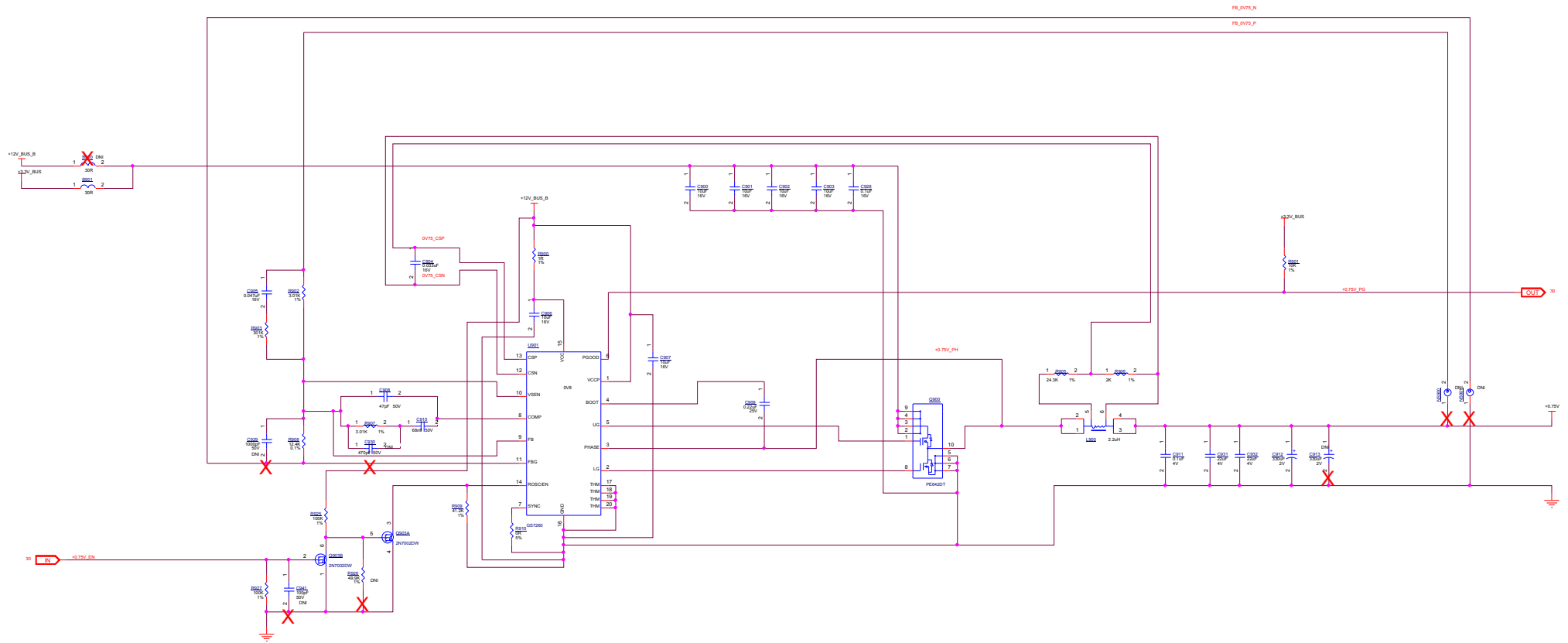




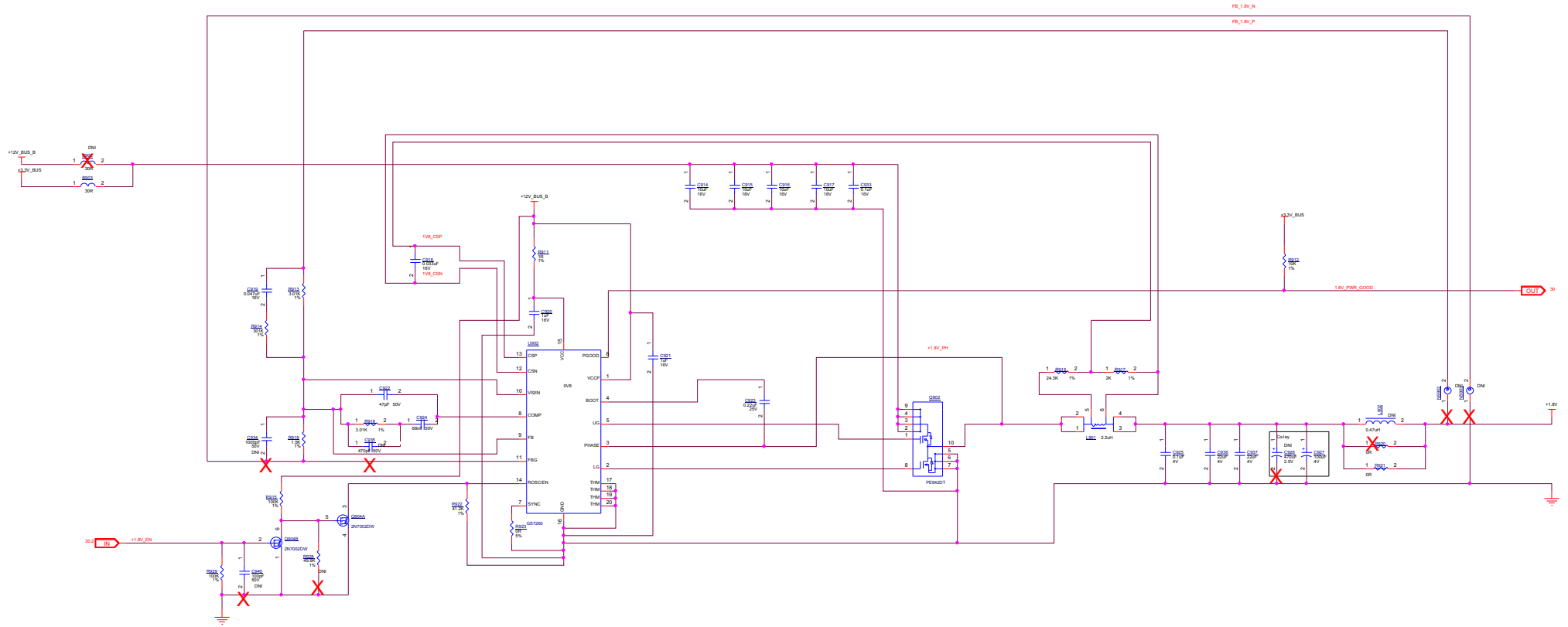




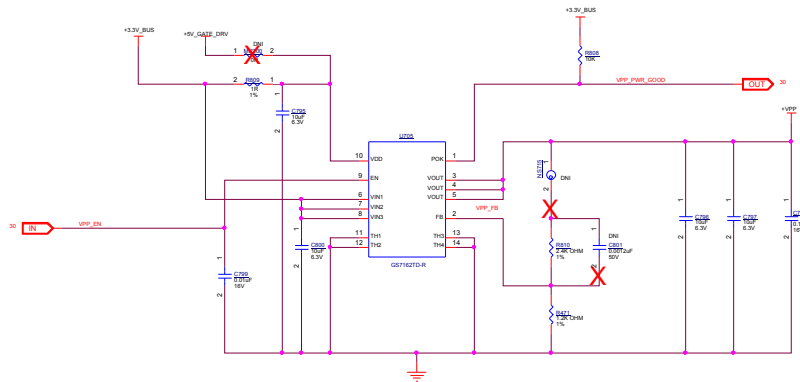
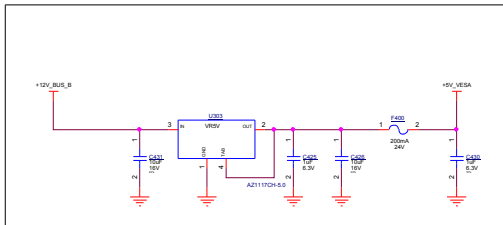


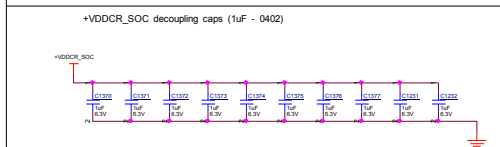
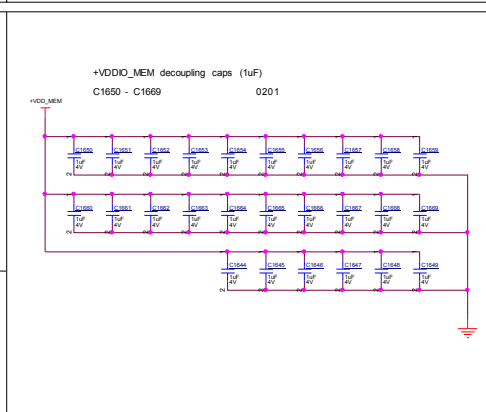
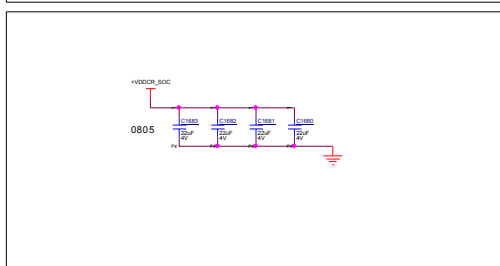
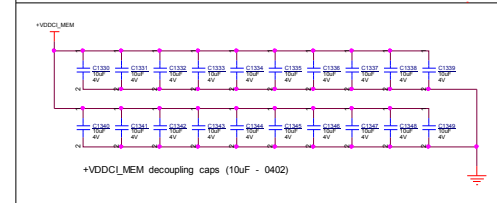
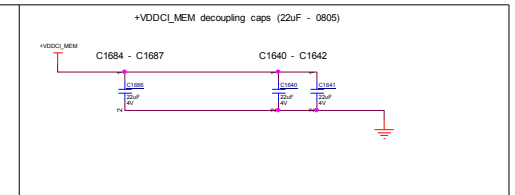
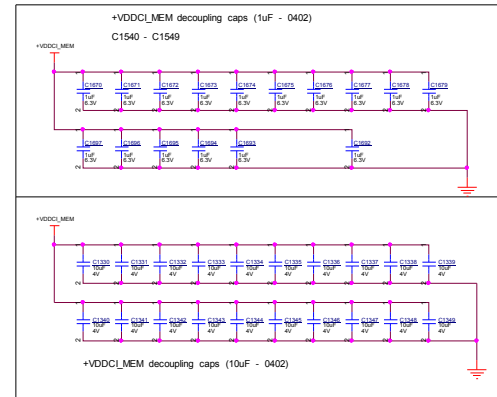
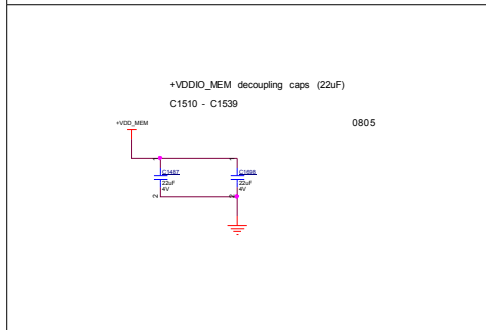
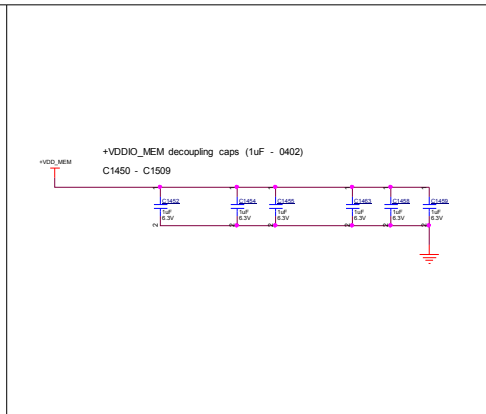
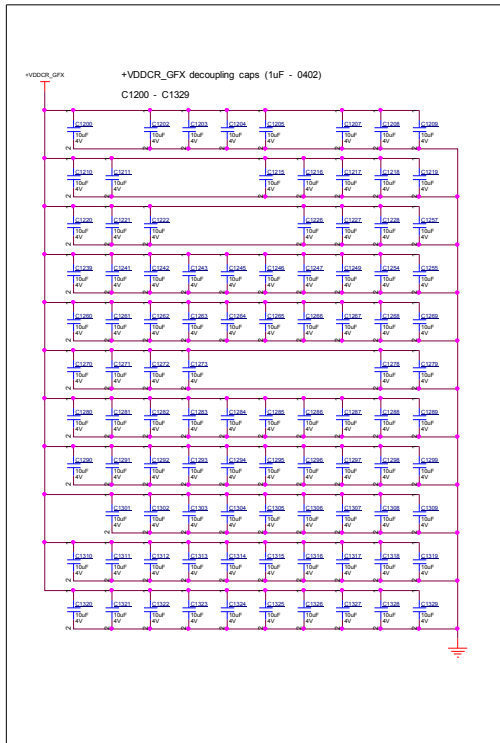


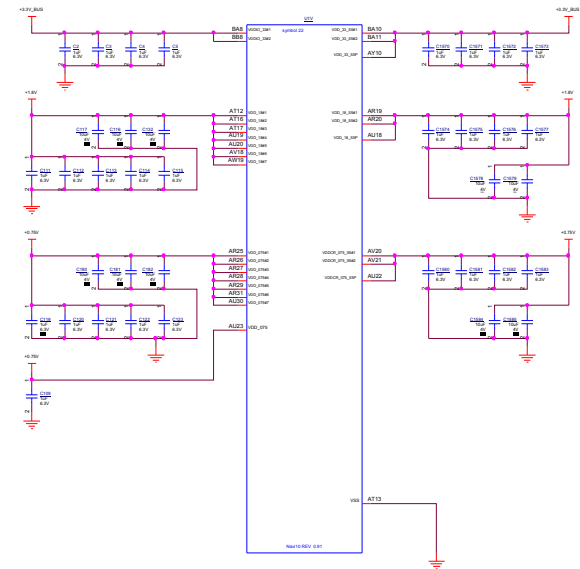
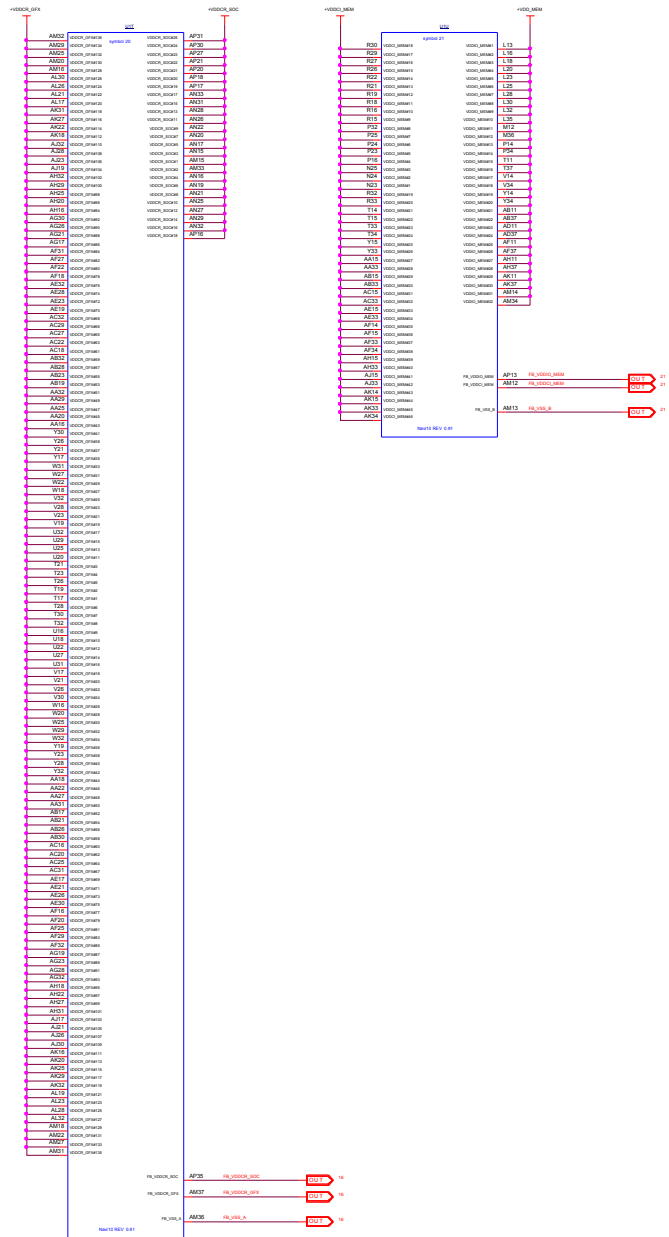


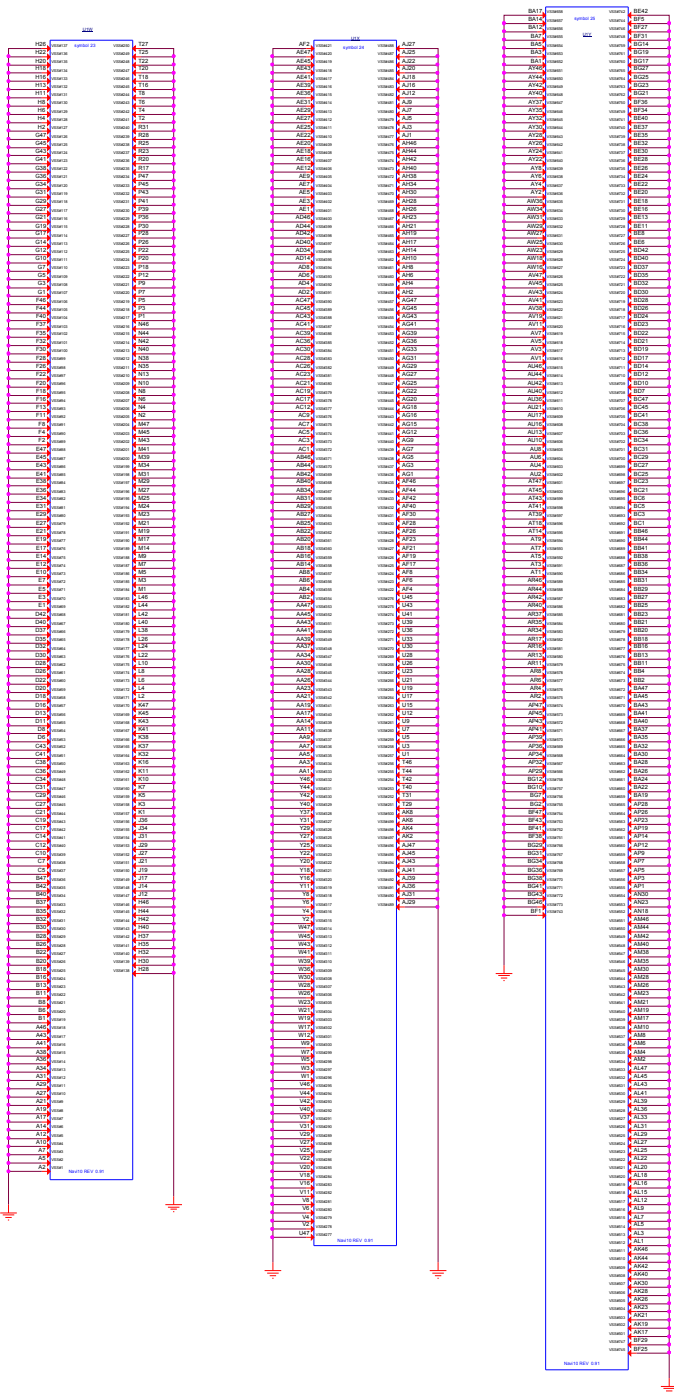


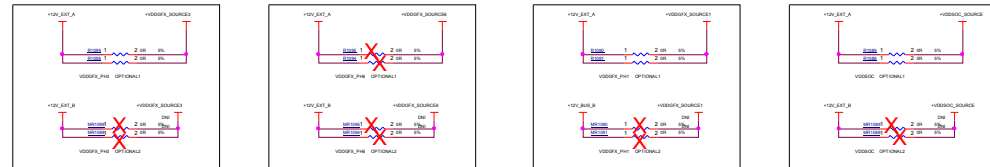
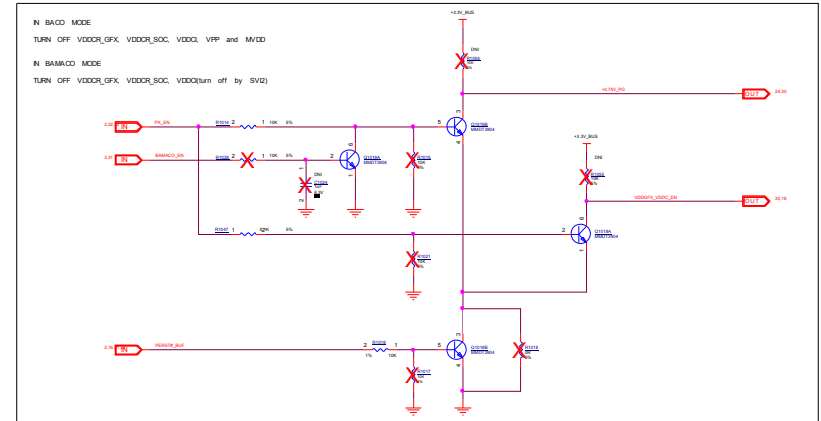
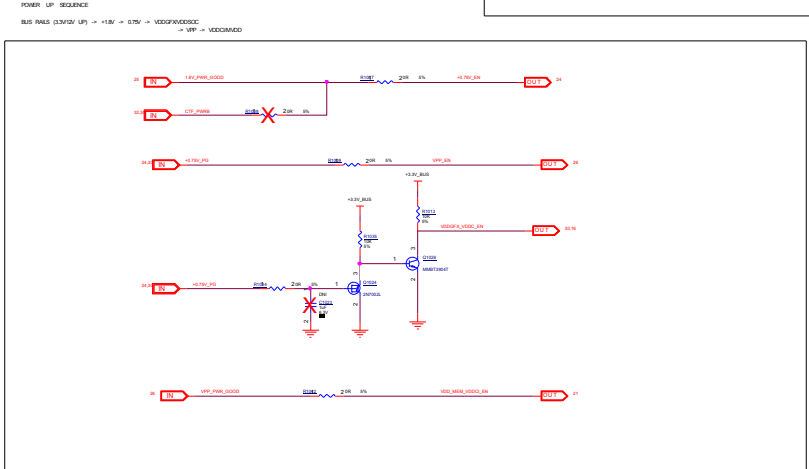
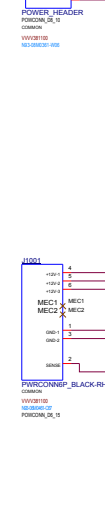
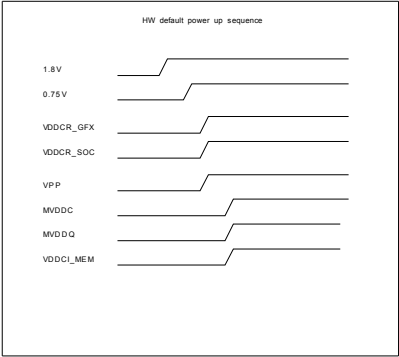
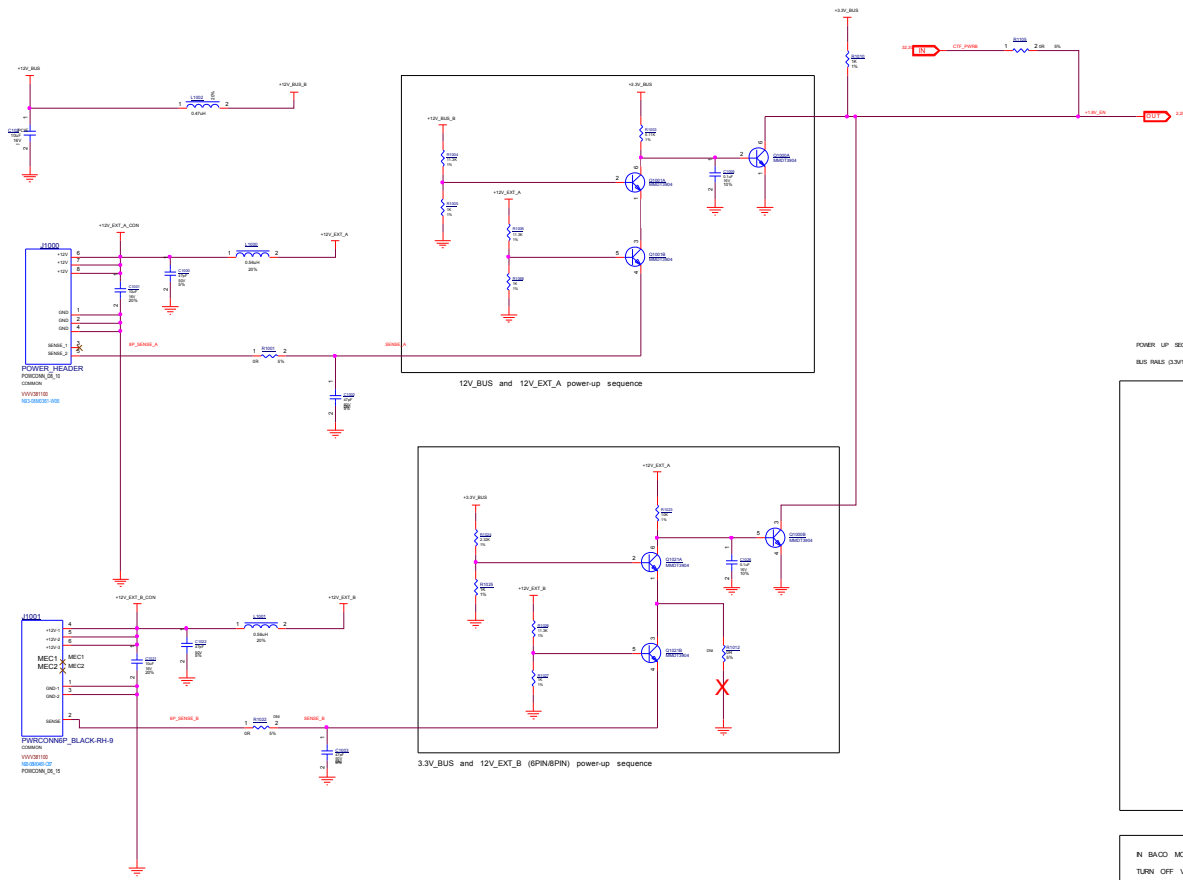
REGULATOR FOR +5V RALS  
 IOUT = 50mA

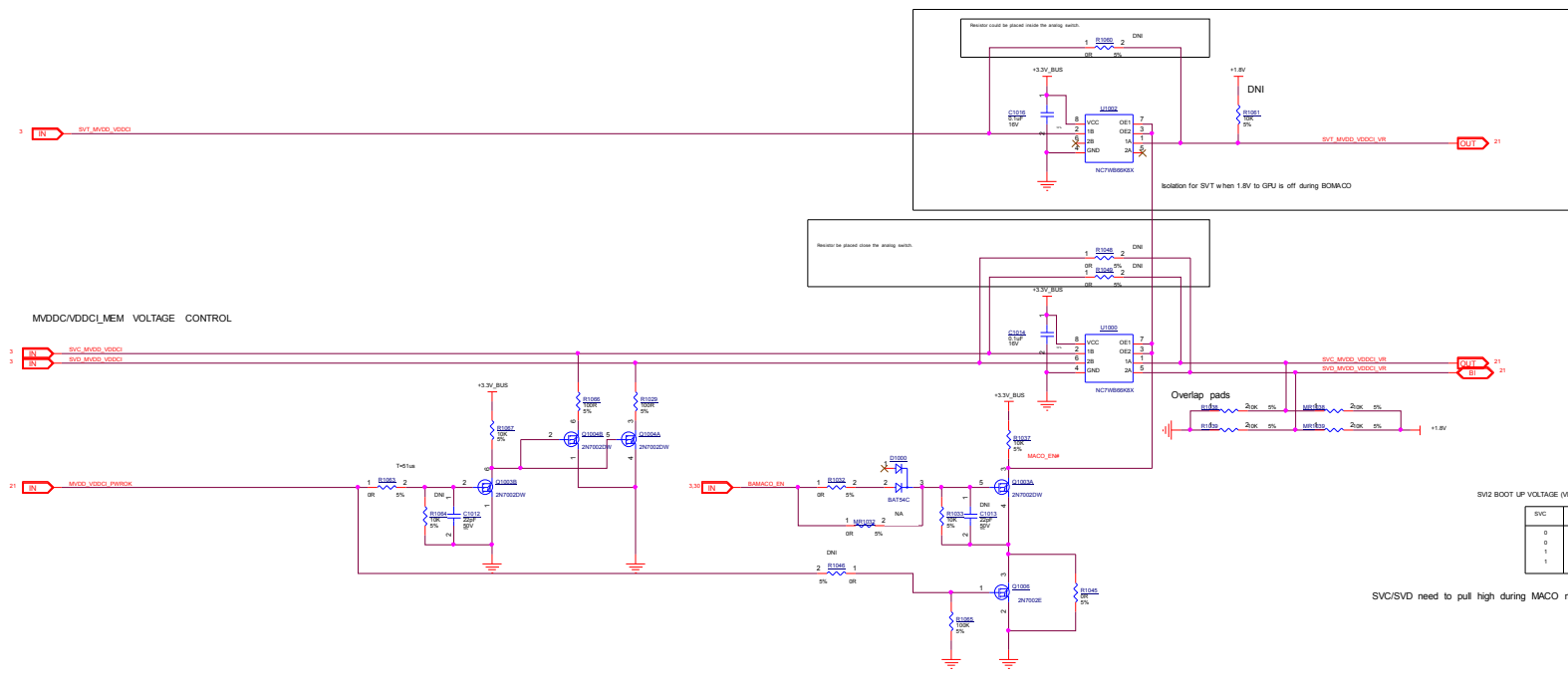












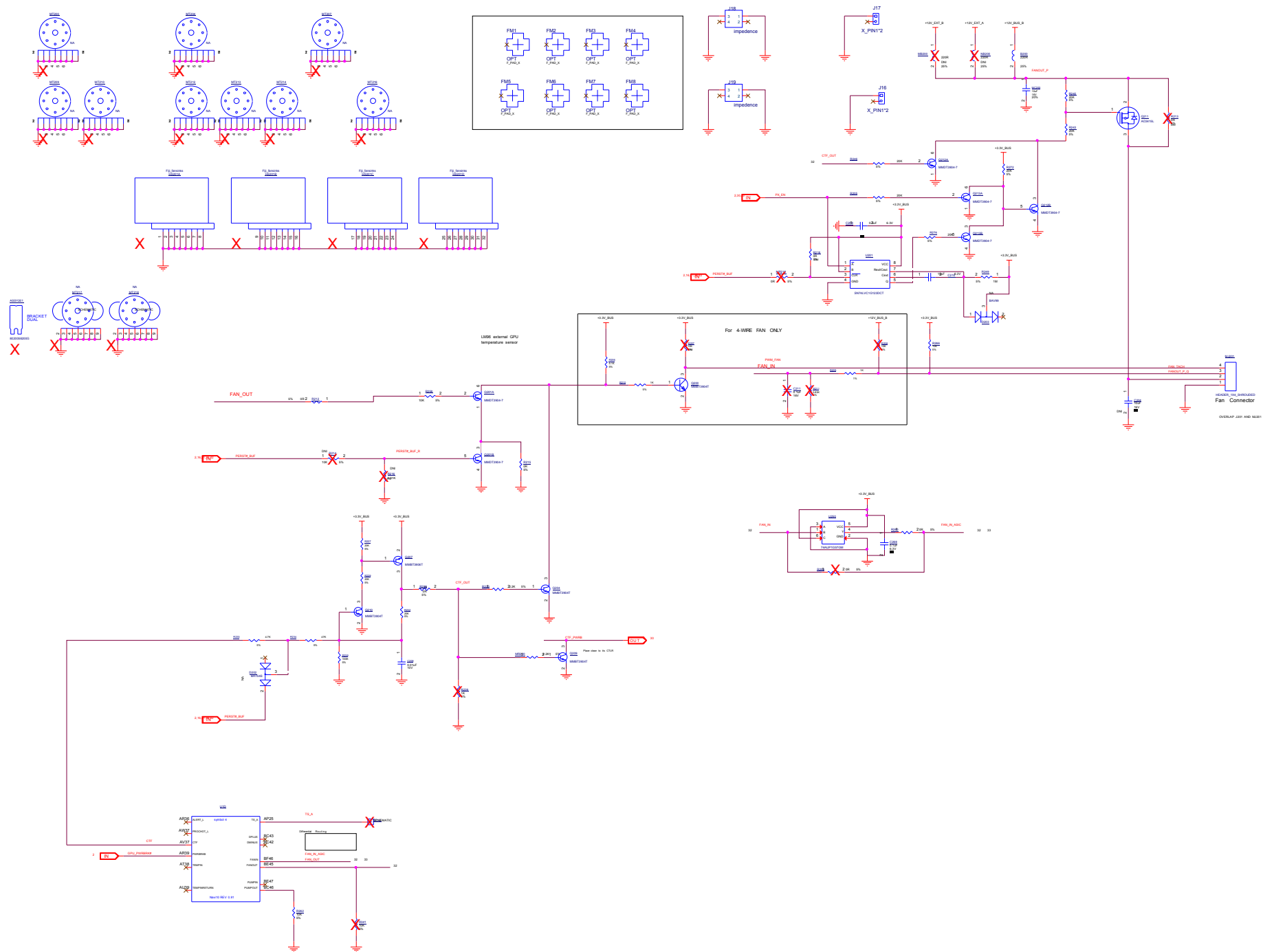
MDDC/VDDC\_MEM VOLTAGE CONTROL



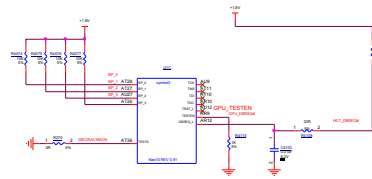
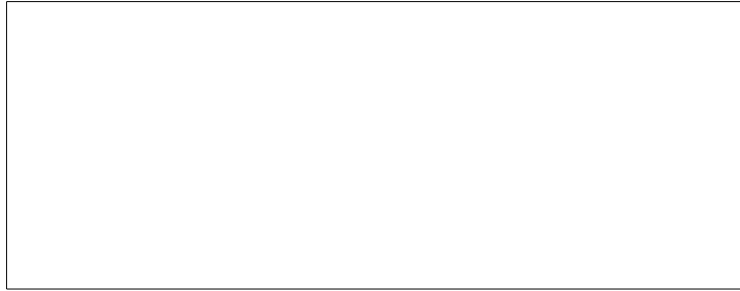
SV2 BOOT UP VOLTAGE (VDDQ\_MEM/MVDD)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

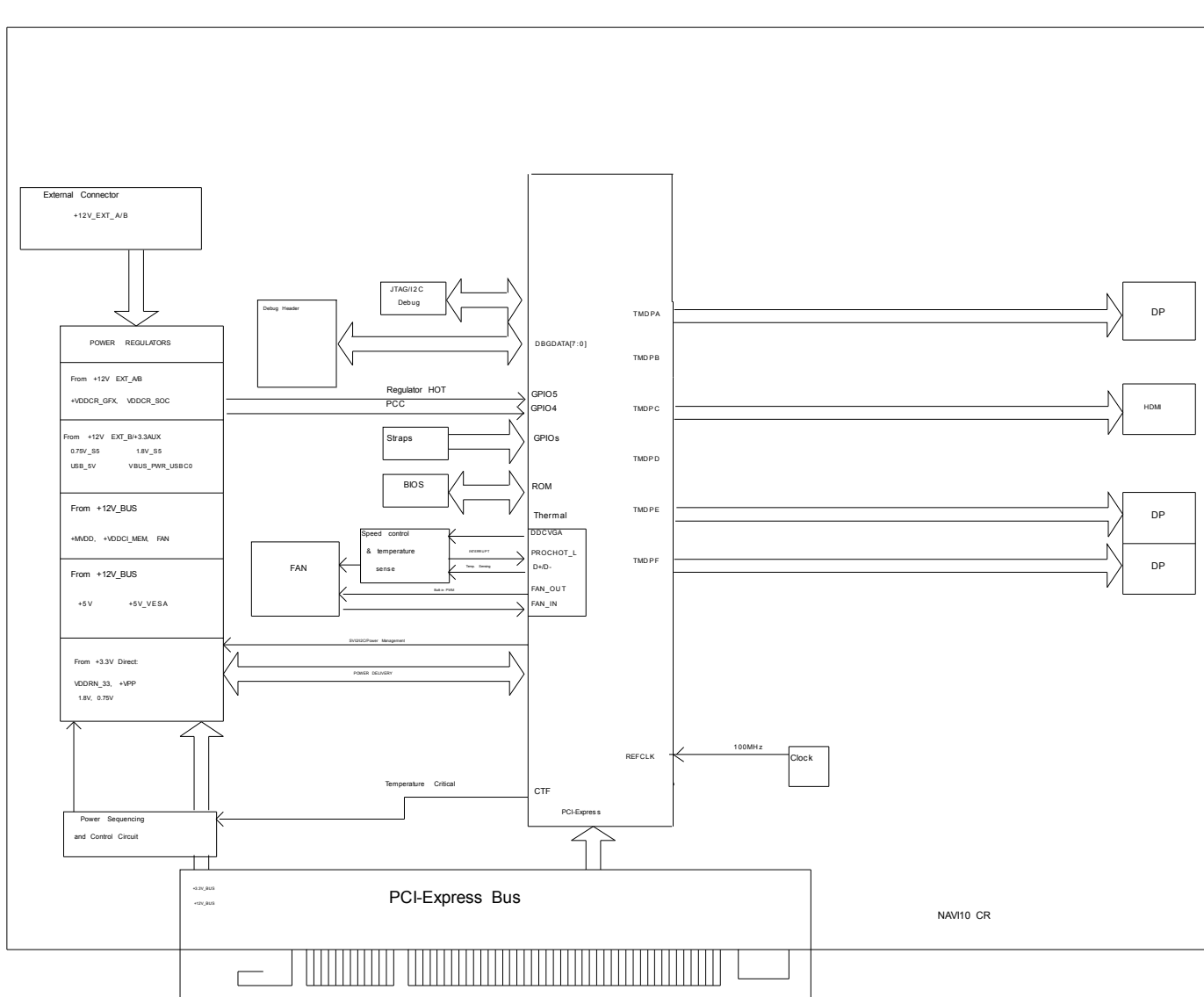
SVC/SVD need to pull high during MACO mode







RADEON Lightbar header





TITLE:

NAV110 GX16mode DP DP HDMI DP

DOCUMENT NUMBER:

105\_D199a\_00B

DATE:

Fri Jun 21 03:44:58 2019

SHEET NUMBER:

35

OF

35

REV: 1.00

## REVISION HISTORY

ENGINEER:

Peak, Dong

NOTES:

NOTE

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 AMD - PLATFORM HARDWARE ENG  
 No.669, HUANKE ROAD  
 SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
1	-00A	FEB 11 2019	-00A schematics
2	-00B	JUN 21 2019	ADD FULL HIGH ON THE PWB/RVB
<p>2019_11_07 GFX_MEM_SOC_VDDCI Co-Lay 302045 and Power PIN fix to 8+6 reverse type Only</p> <p>2019_11_11 Add Fan_IN output back Page 32, Change Footprint con_dp_astron_r6890020_tab &gt; con_tab , edgecon_pci_express_gen4_16 &gt; edgecon_16 , Remove MT203, MT 211, MT208 Screw Hole</p> <p>2019_11_14 add Cross Light point , Remove Page 2 TP detect point, Remove lightbar header, Remove CTF &amp; J4100 debug Pin</p>			