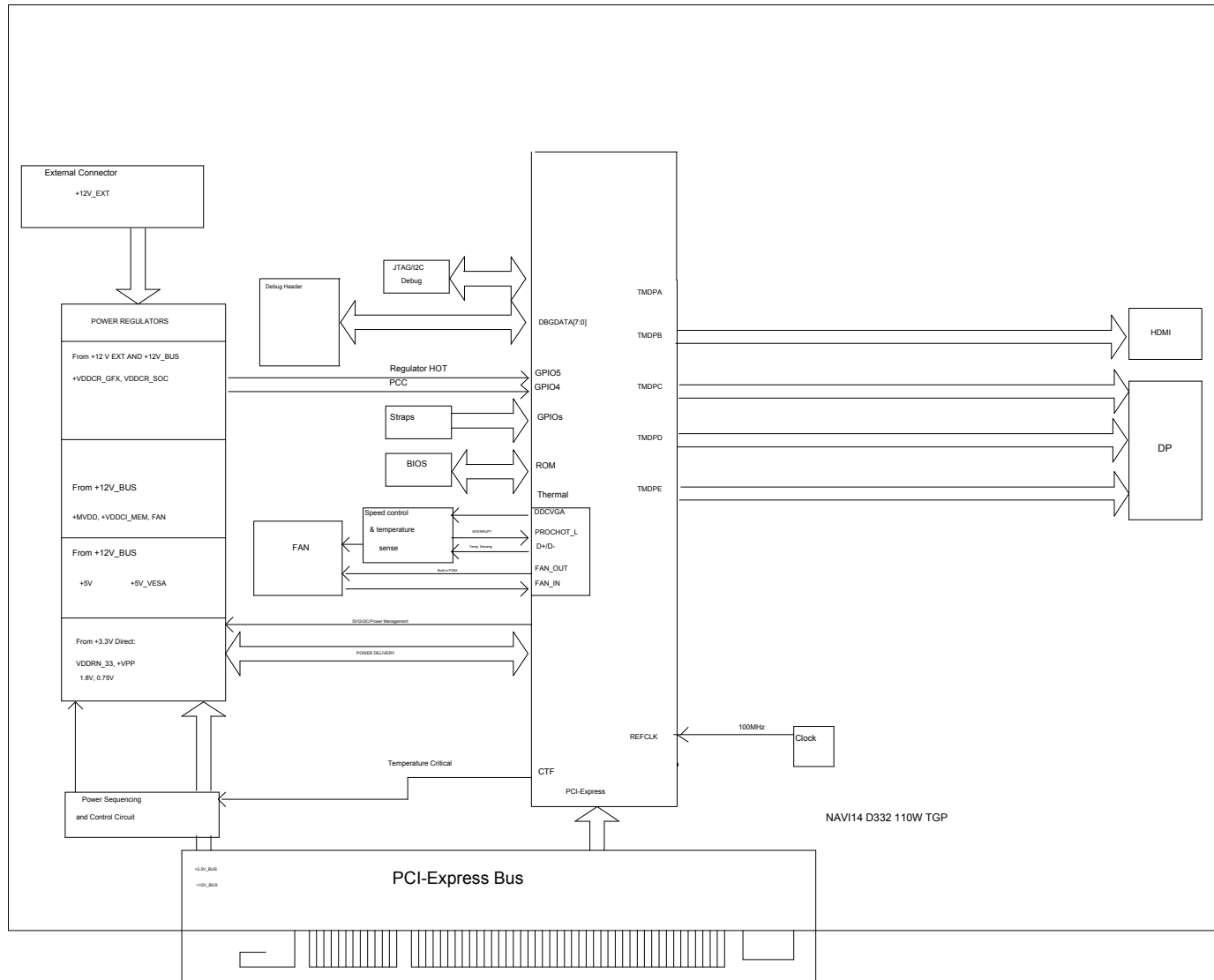


NAVI14 GDDR6 4PCS,8L 3xDPs +1xHDMI  
 105-D332xx-00B RevB Desktop board(110W TGP)

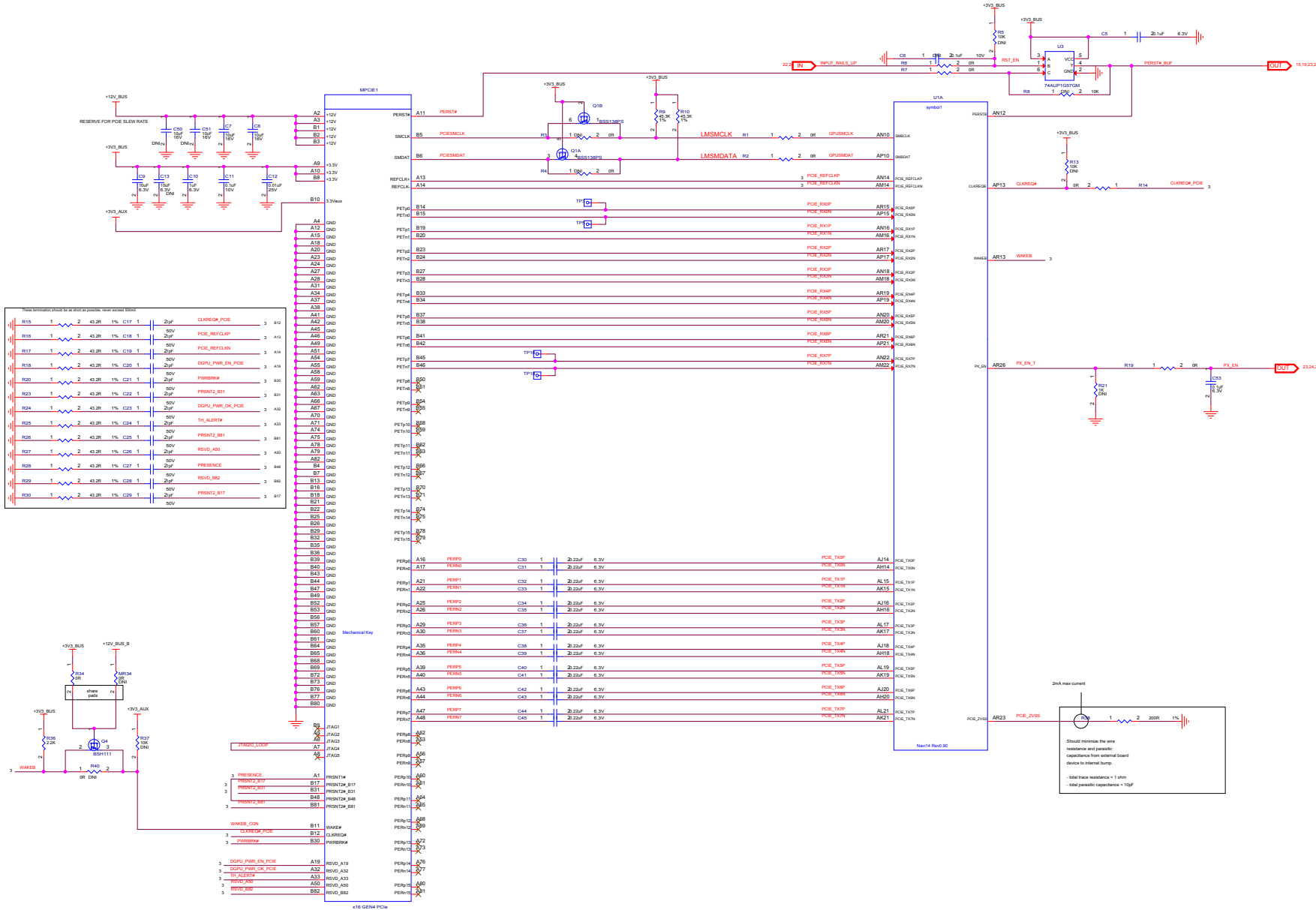
TABLE OF CONTENTS

SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	DEBUG CIRCUITS
2	BLOCK DIAGRAM	27	REVISION HISTORY
3	NAVI14 - PCIe Interface		
4	NAVI14 - GPIO, EXTRA		
5	NAVI14 - XTAL		
6	NAVI14 - POWER and GND		
7	NAVI14 - Decaps		
8	NAVI14 - MEM CH AB		
9	NAVI14 - MEM CH CD		
10	GDDR6 x16 - MEM CH AB		
11	GDDR6 x16 - MEM CH CD		
12	NAVI14 - TMDPAB - USB,HDMI		
13	NAVI14 - TMDPCD - DP,DP		
14	NAVI14 - TMDPE - DP		
15	REG VDDGFX/SOC CNTL		
16	REG VDDGFX		
17	REG VDDSOC		
18	REG PCC		
19	REG VDDCI/MVDD CNTL		
20	REG VDDCI/MVDD		
21	REG - 0V75		
22	LDO 1VB/PP1SV/SV_VESA		
23	MECHANICAL AND THERMAL		
24	POWER MANAGEMENT		
25	SVI2		



(3) NAV14 PCIe Edge Connector

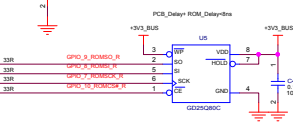
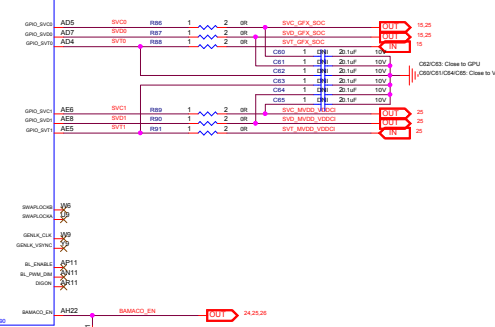
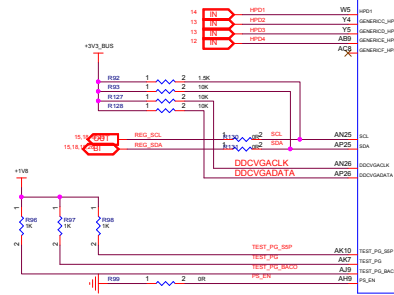
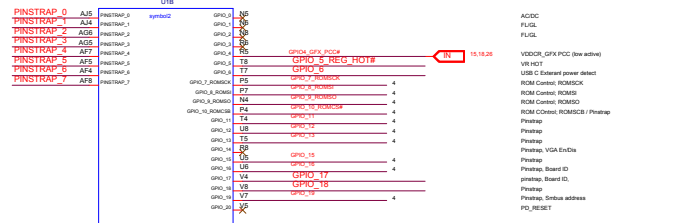
SYMBOL LEGEND	
DN	DO NOT INSTALL
1 +	ACTIVE LOW
BUD	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND



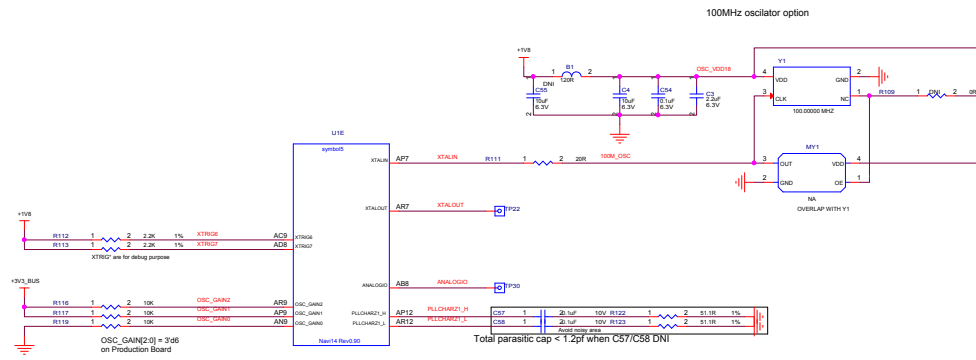
	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>MS-V382</b>	
Size	Custom	Rev
Document Description	NAV14 - PCIe Interface	
Date:	Thursday, September 12, 2019	Sheet 3 of 27

Note: Internal PUPD at GPIO pad is ~40k strength in 14nm design spec

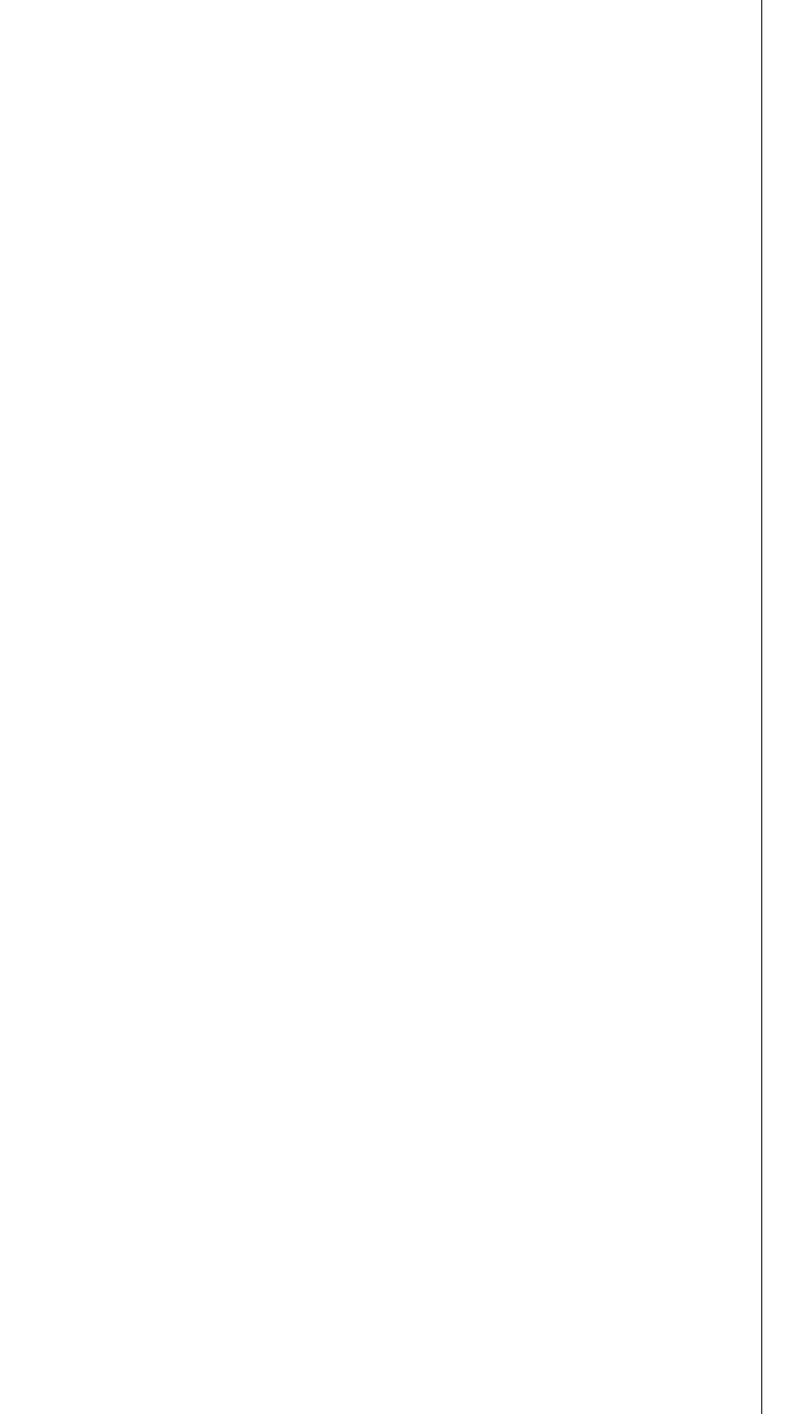
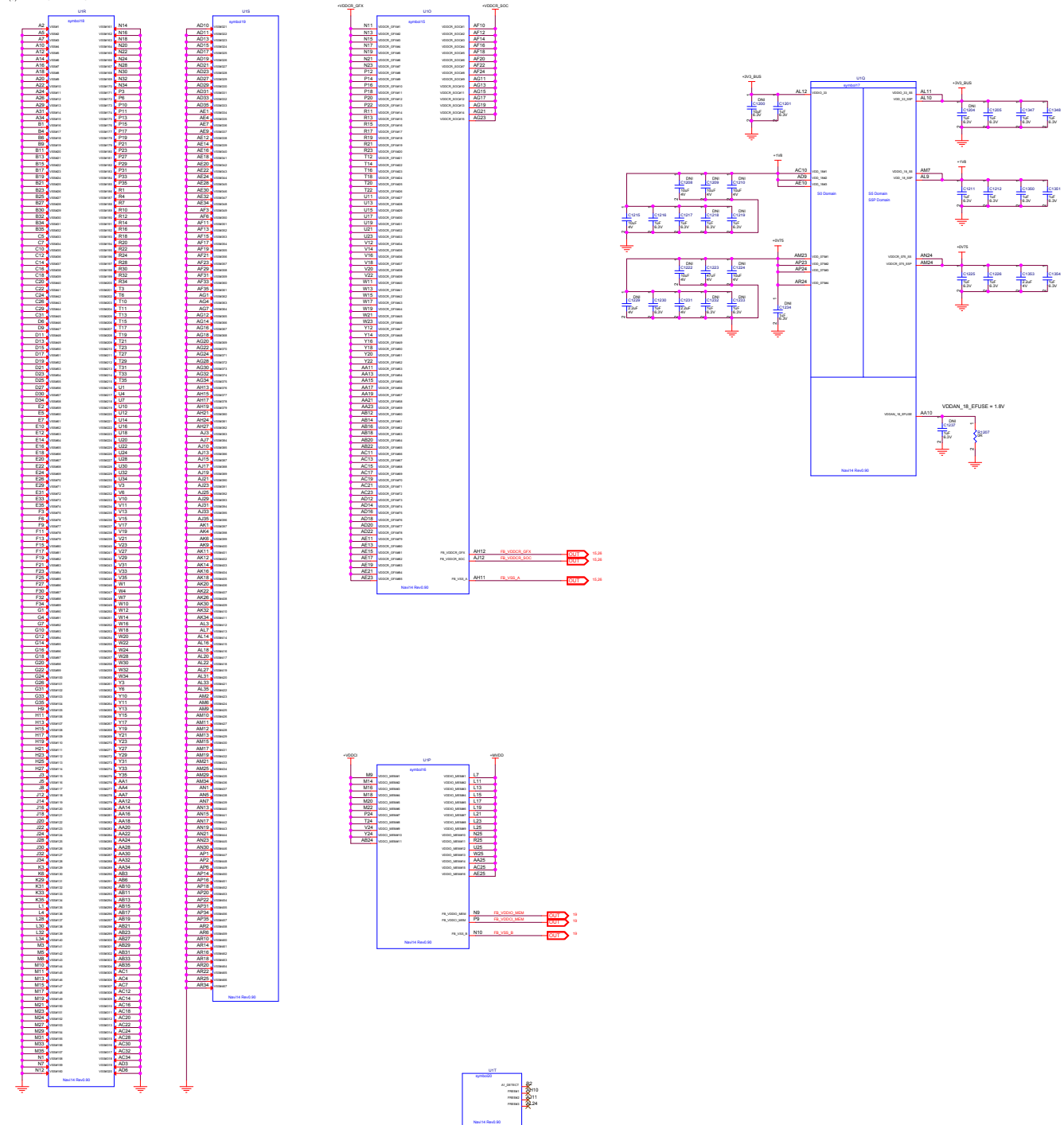
HW ID	HW ID	FUNCTION	IC BUS	DEVICE
0x00	0x60	VDDCR_GFX/S0C	SCL/SDA	U501R3S217
0x02	0x44	MVSD/VSDCI	SCL/SDA	U701NCR8102
0x03	0x4E	PC/presserved	SCL/SDA	U4801QSS801
0x48	0x50	GE Temperature	DDCVGACK/DATA	U4000TMP102A
0x4C	0x5B	EXT SENSOR	DDCVGACK/DATA	U4001LMB91B3

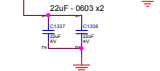
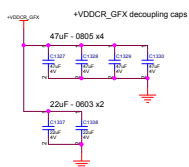
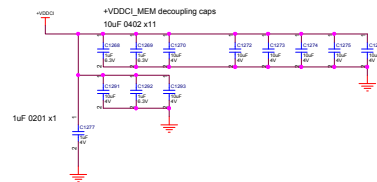
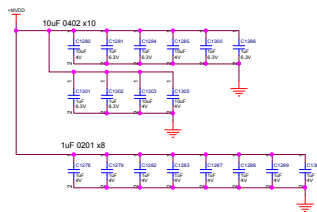
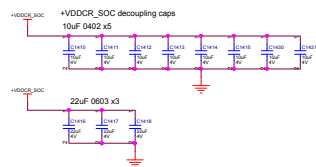
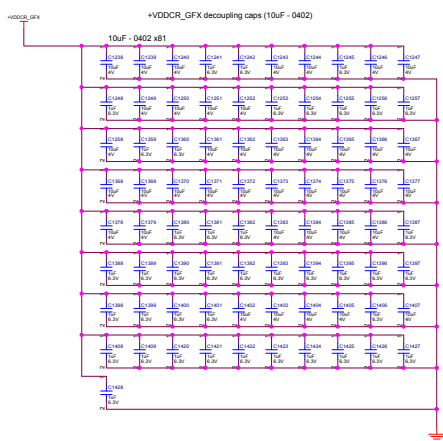


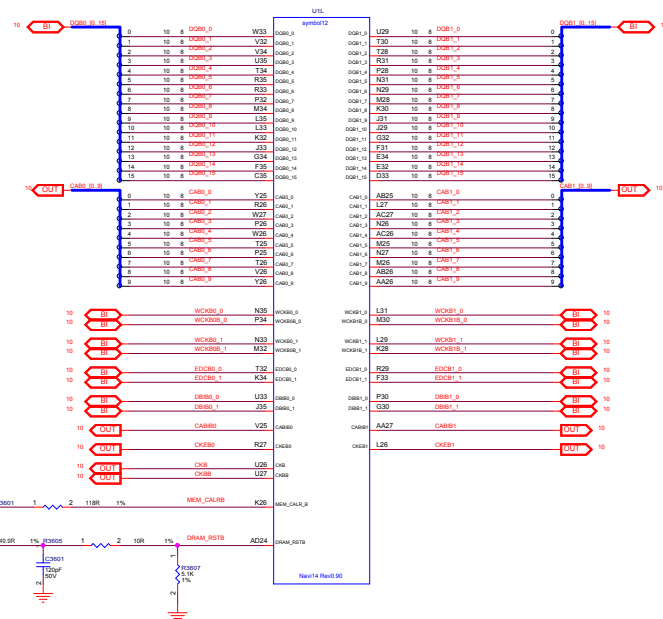
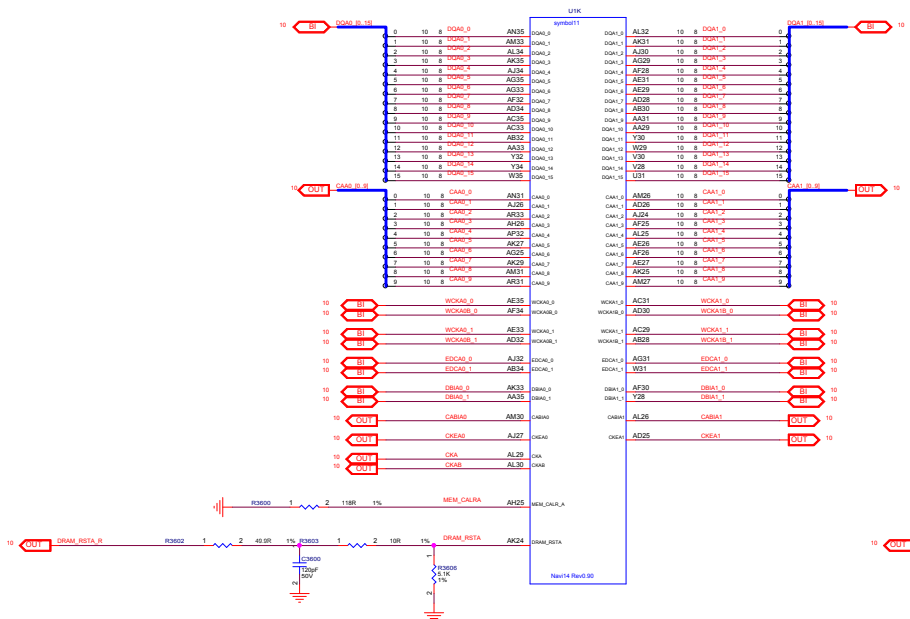
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GENA_DIS_A 0: PFCM GEN4 supported 1: PFCM GEN4 not supported
	0	PINSTRAP_BIF_CLK_PM_EN 0: CL3/PFCM4 power management capability is disabled 1: CL3/PFCM4 power management capability is enabled
	0	PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing mode(default setting)
	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capability is enabled 1: The device won't be recognized as the system's VGA controller
DCE	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 8 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected Default:[PINSTRAP5,PINSTRAP4,PINSTRAP3] = 000
	0	PINSTRAP_AUD[1:0] 1: Enable for DisplayPort only 2: Enable for DisplayPort and HDMI if dongle is detected 3: Enable for both DisplayPort and HDMI Default:[GPIO12,GPIO11] = 11
	0	PINSTRAP_FIG[1:0] - No definition on NV
Platform	0	PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
	1	PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100: 512KBIT (E1) M20P0A 101: 1MBIT (E1) M20P1A 110: 2MBIT (E1) M20P2A 111: 4MBIT (E1) M20P4A 100: 1MBIT (E1) M20P0A 101: 512KBIT (E1) M20P1A 110: 1MBIT (E1) M20P2A 111: 1MBIT (E1) M20P4A
SMU	0	PINSTRAP_SMBUS_ADDR 0: 0x47h 1: 0x49h
	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device



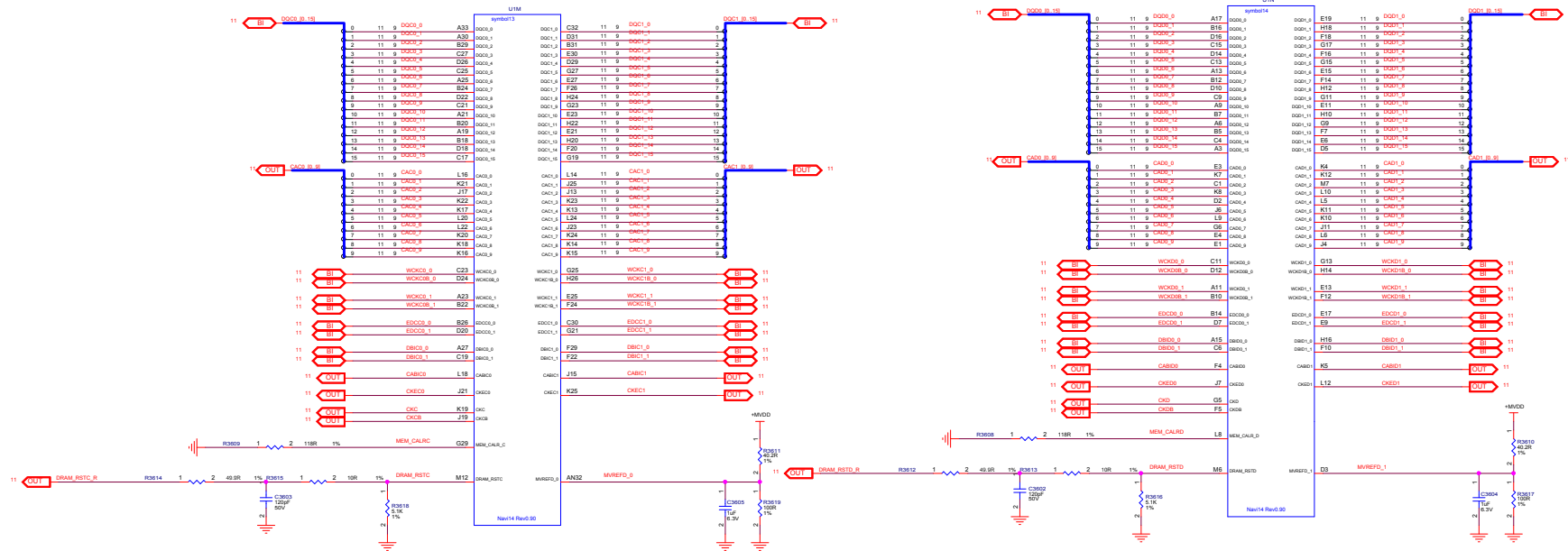
(6) NAV14 POWER AND GND

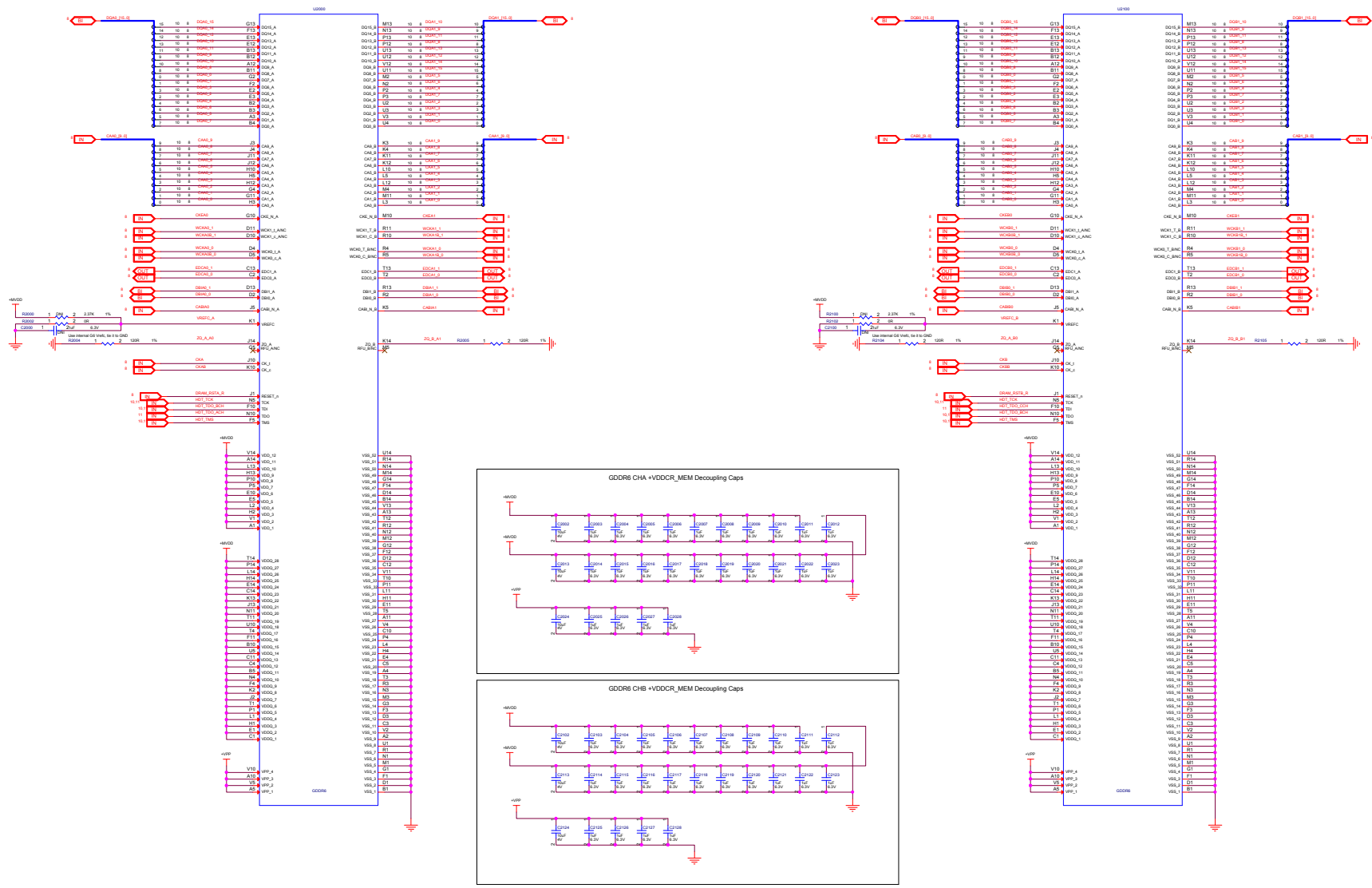


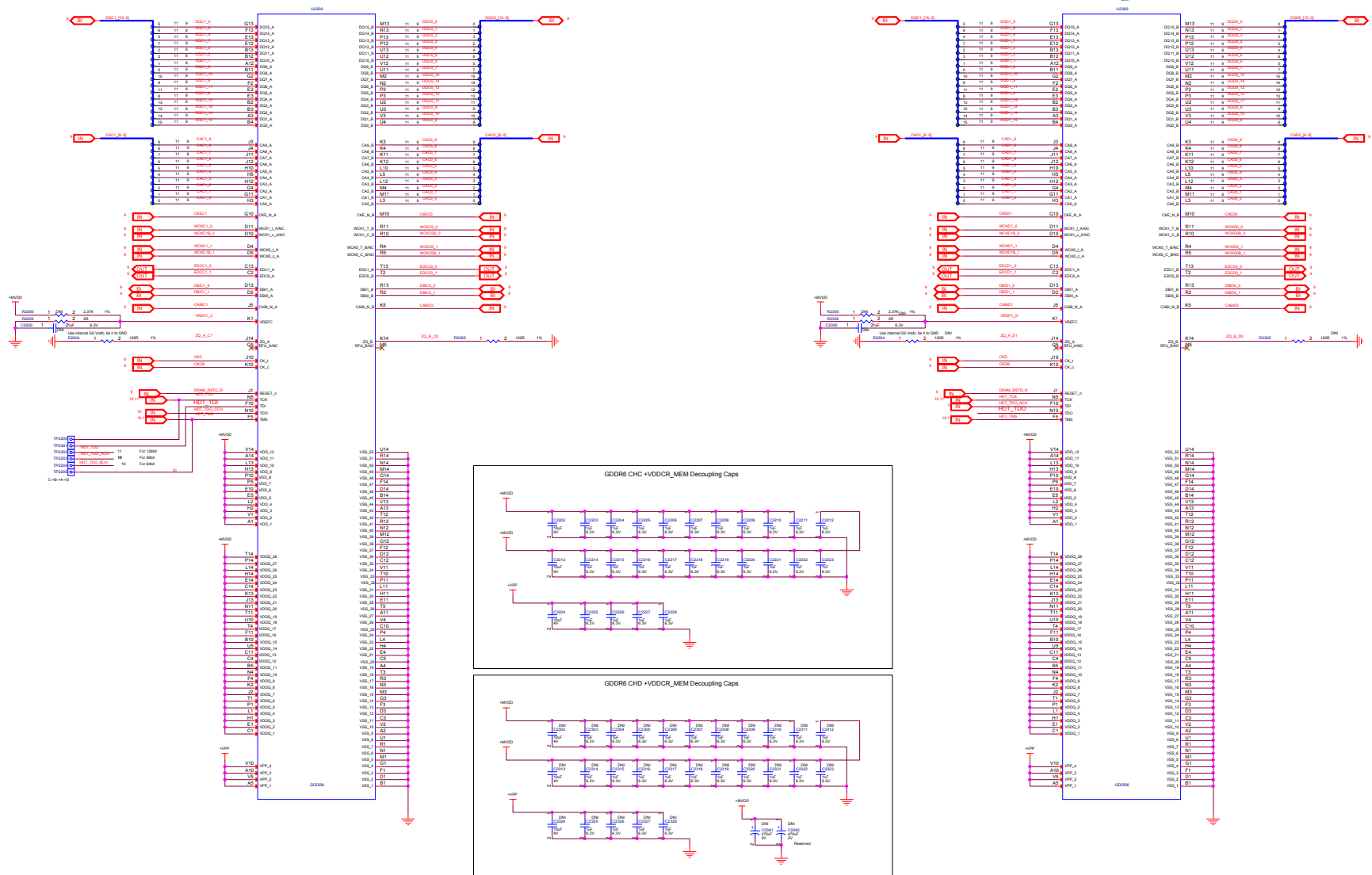


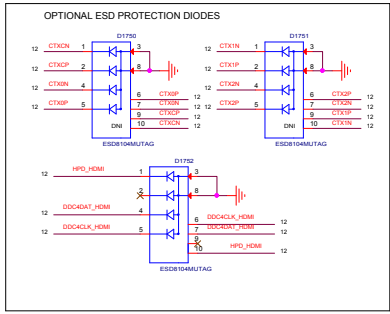
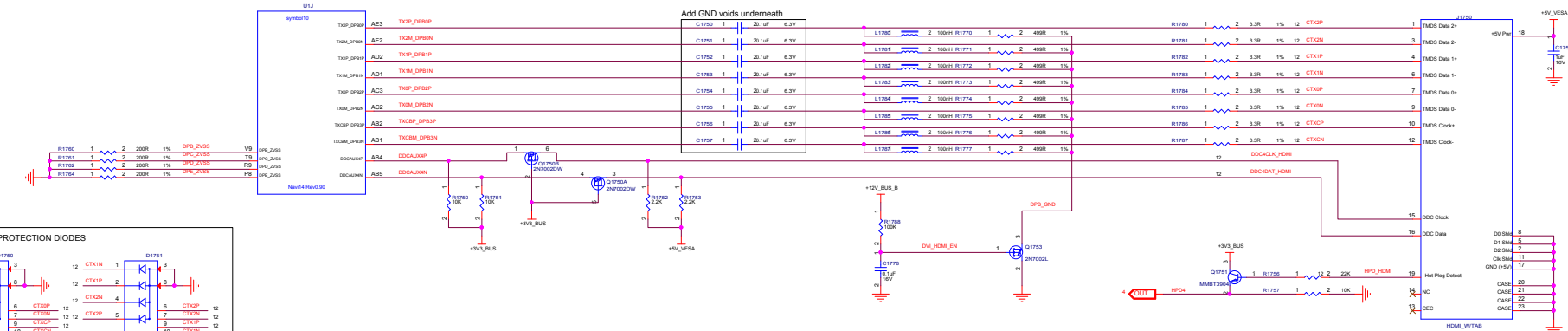
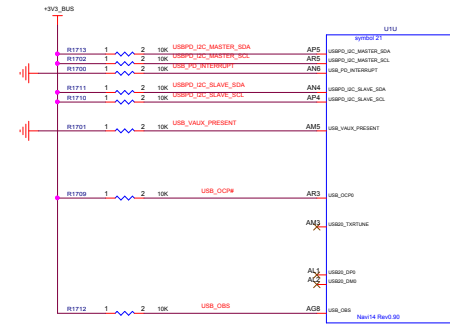
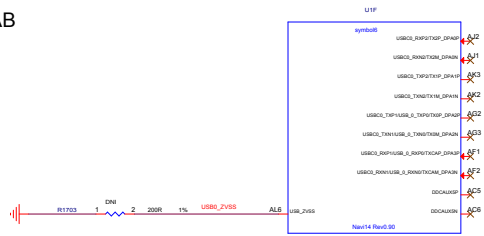


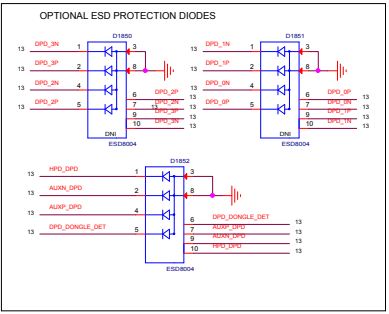
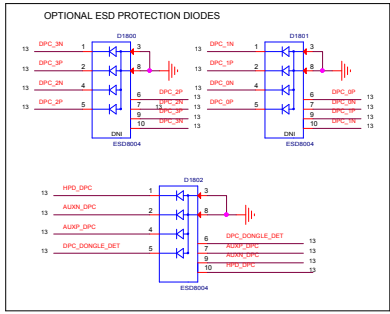
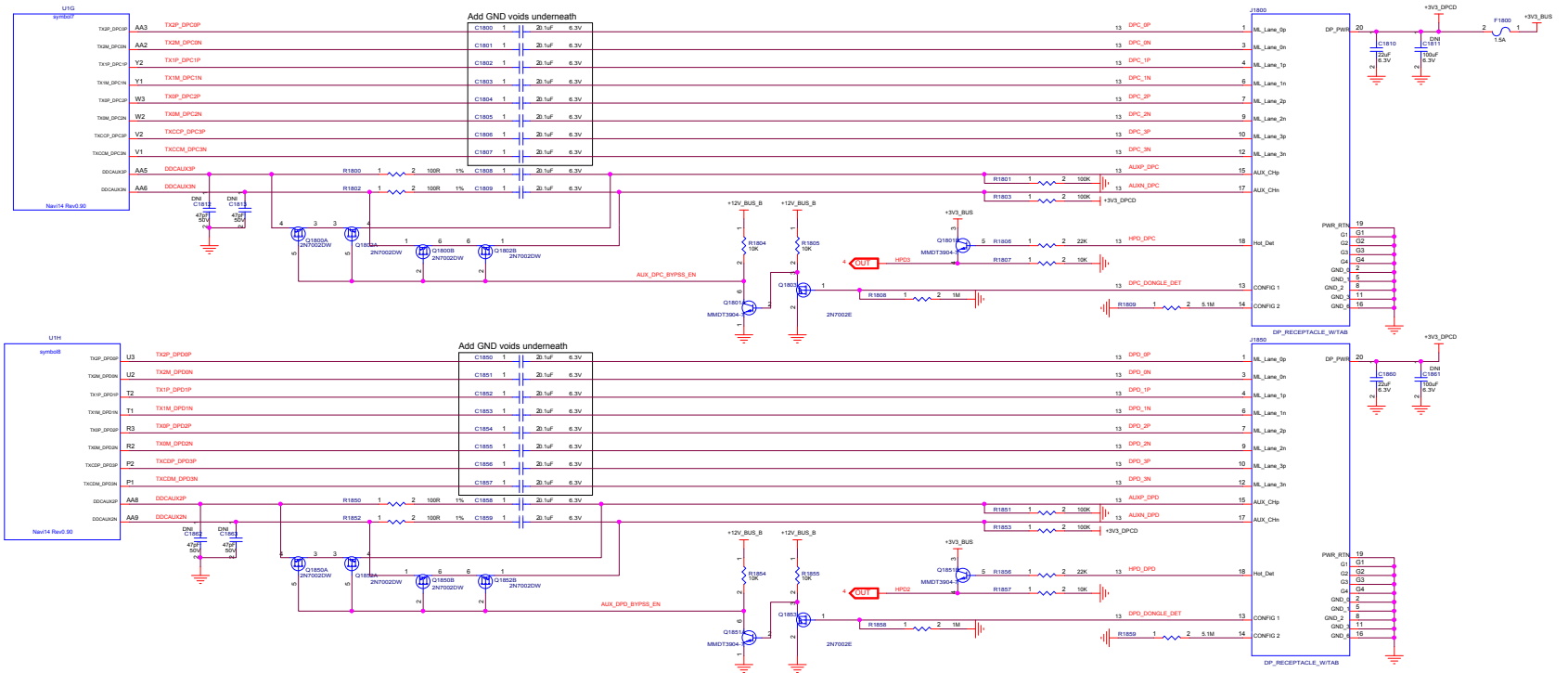


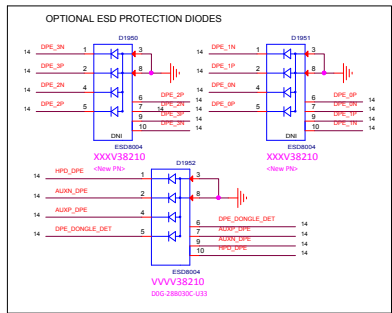
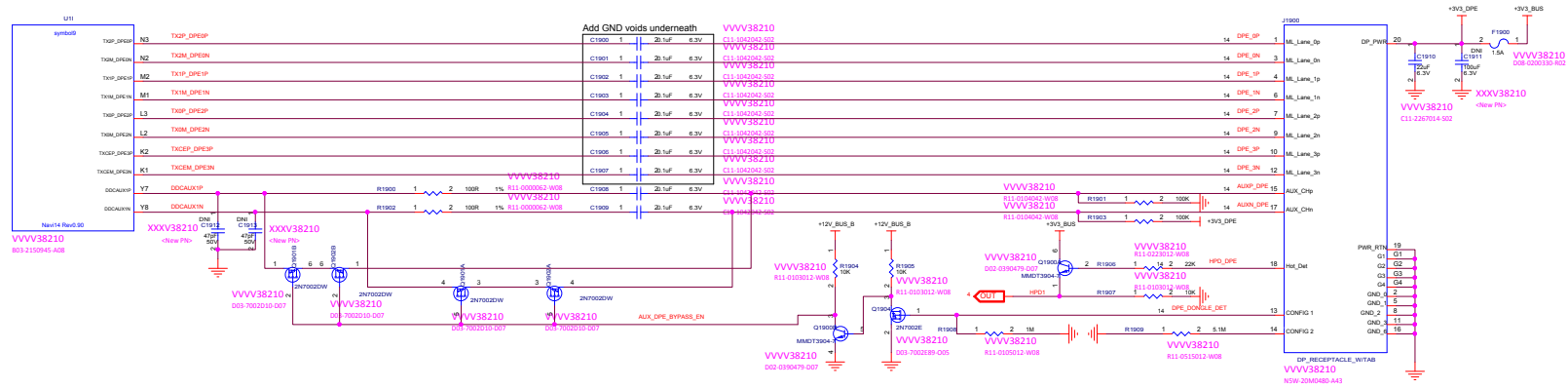




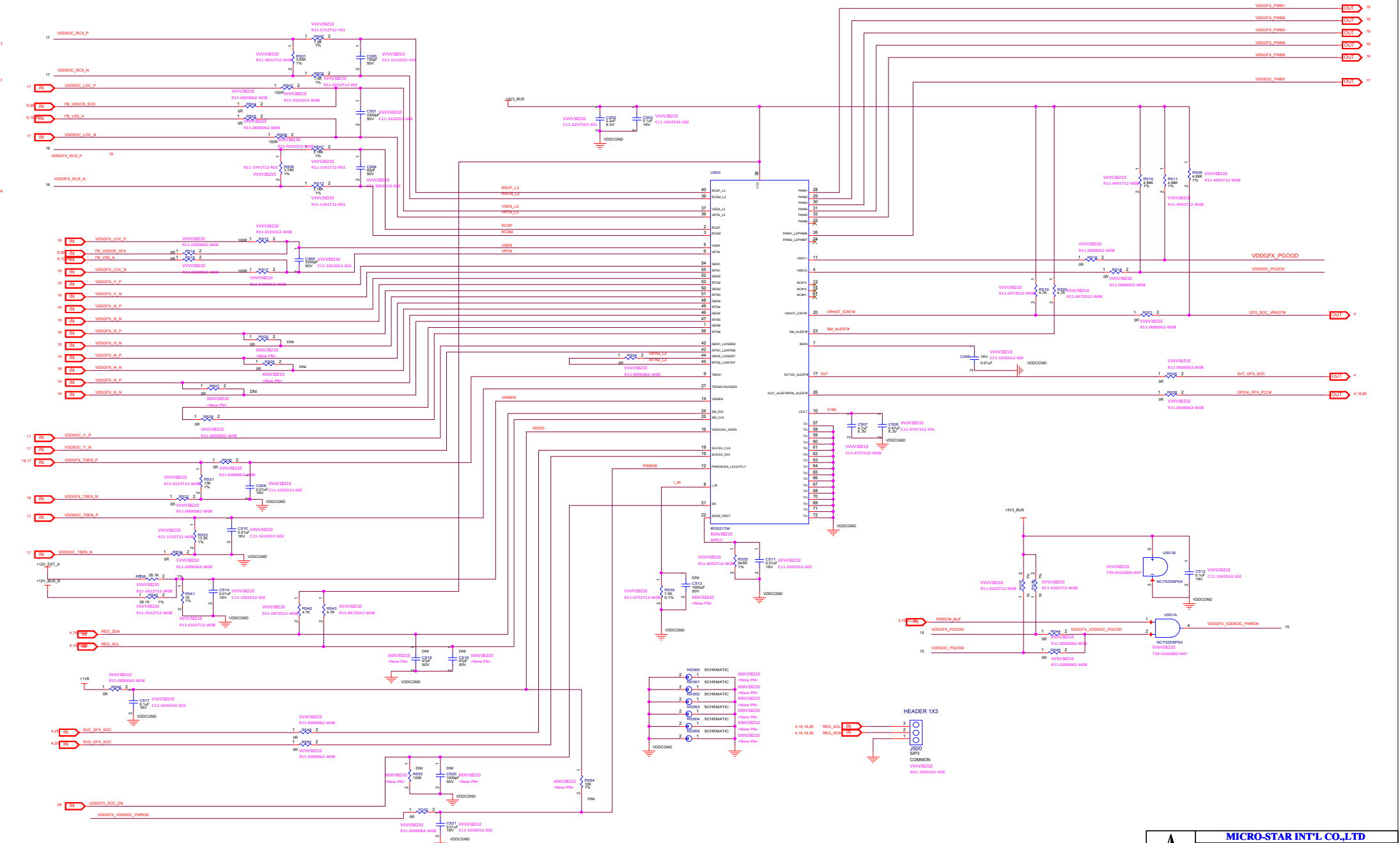


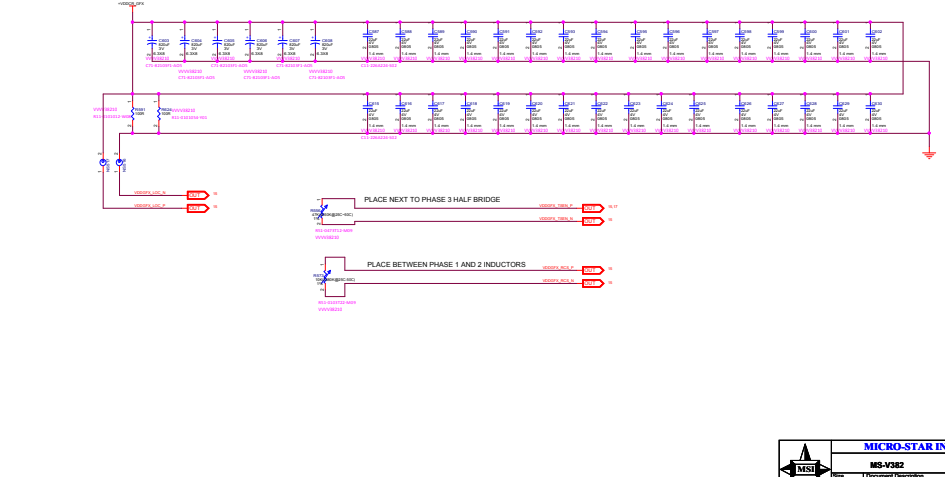
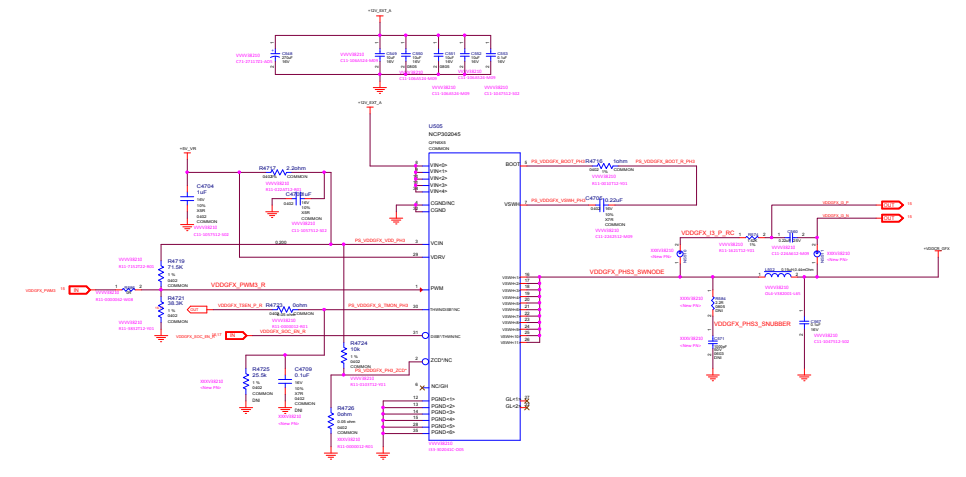
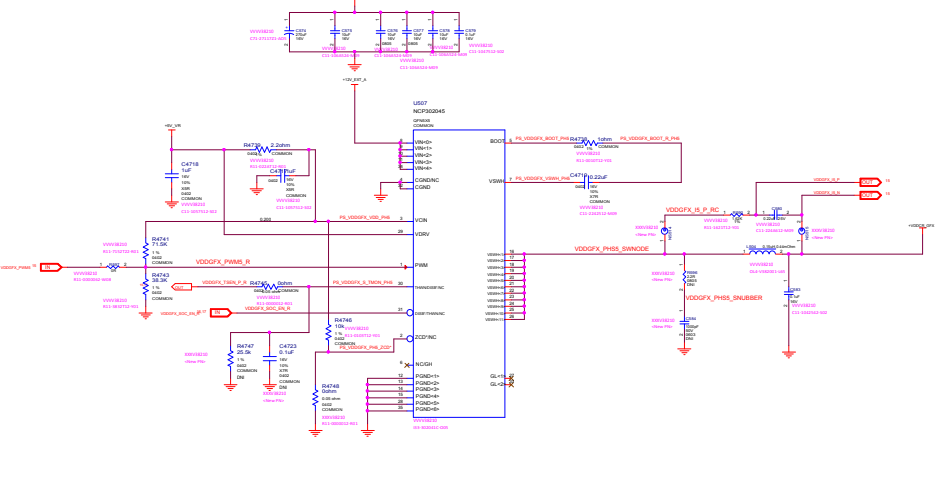
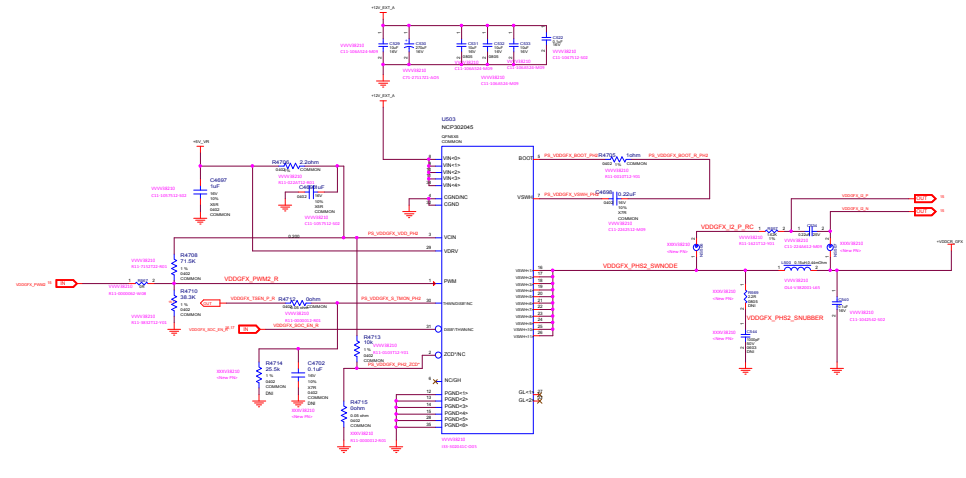
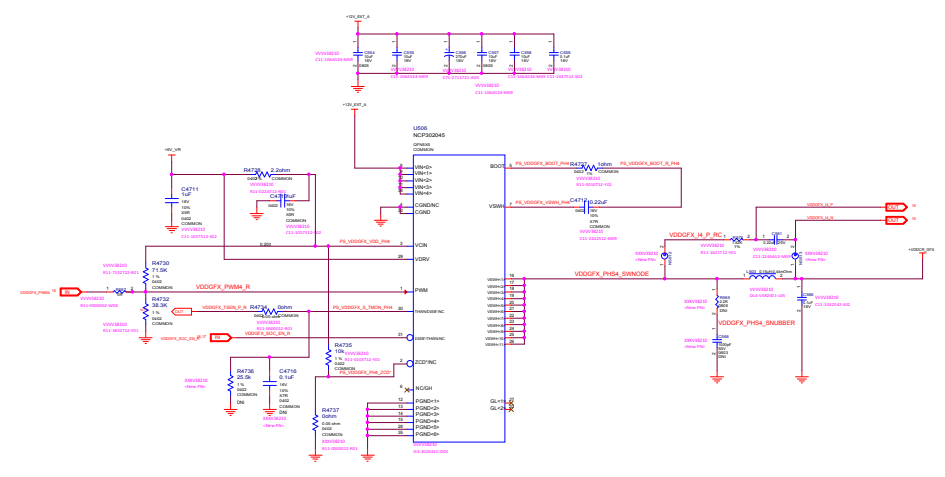
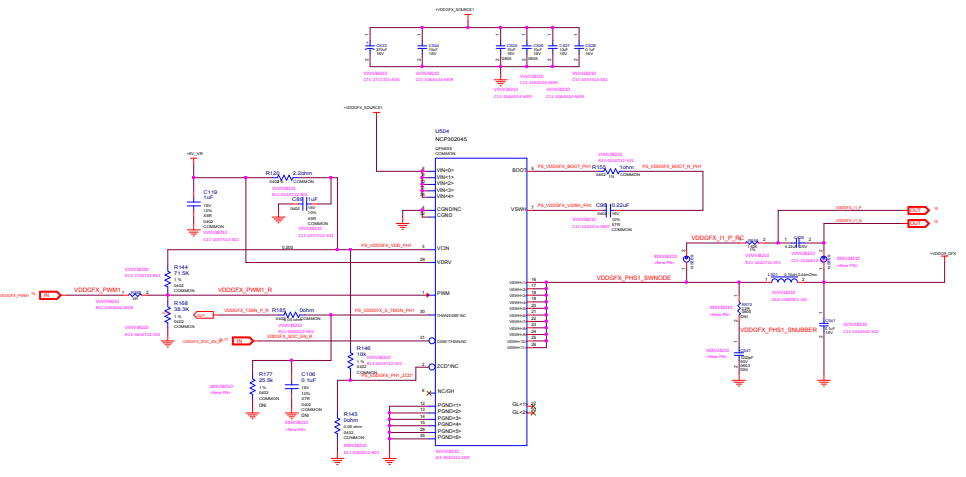




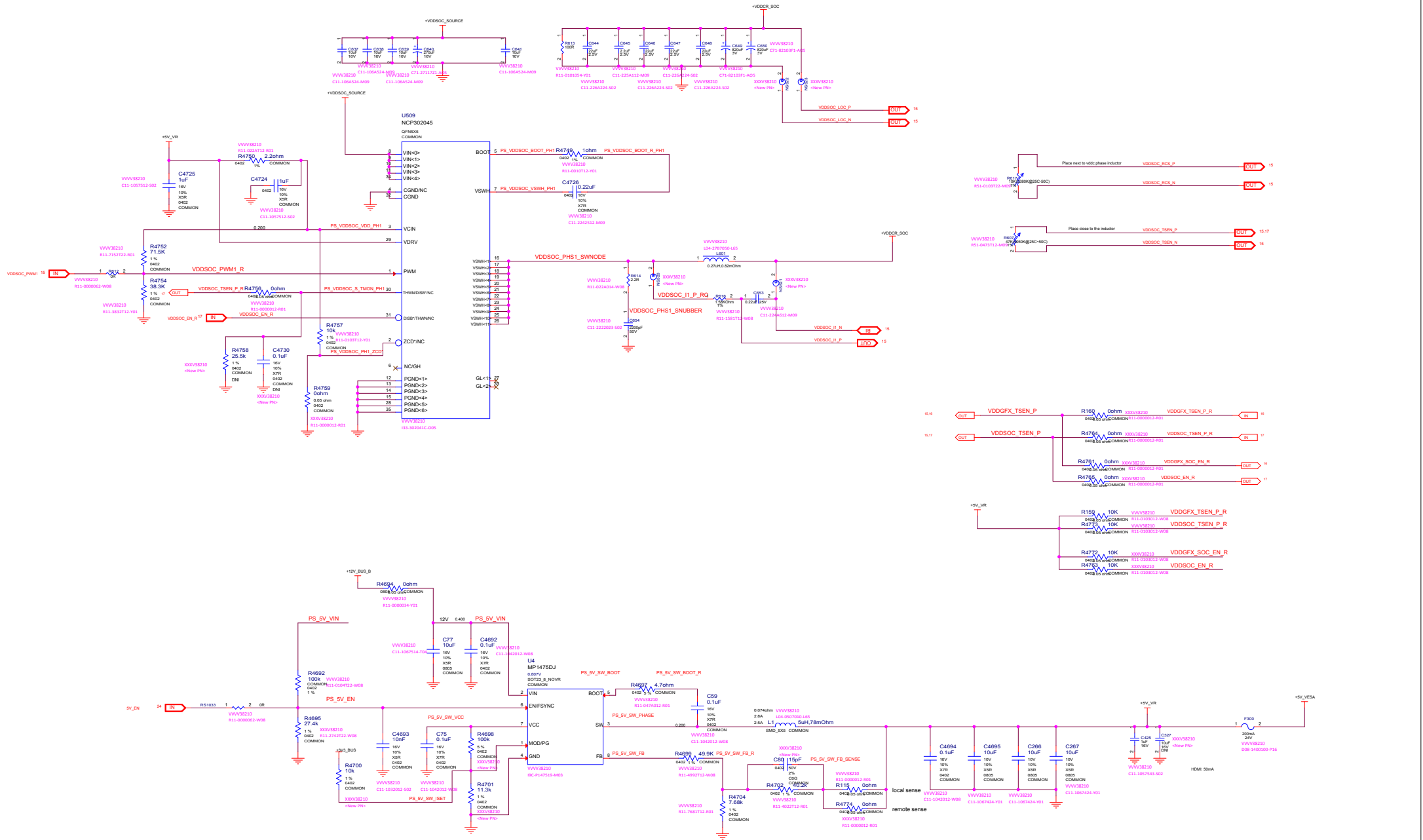


REG - VDDGFV/VDDSOC CTRL






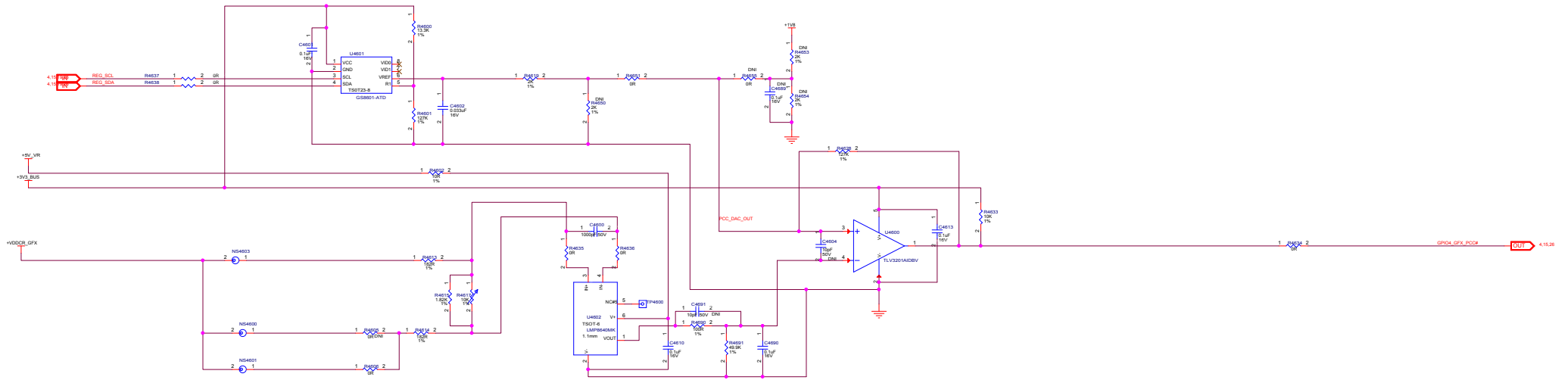


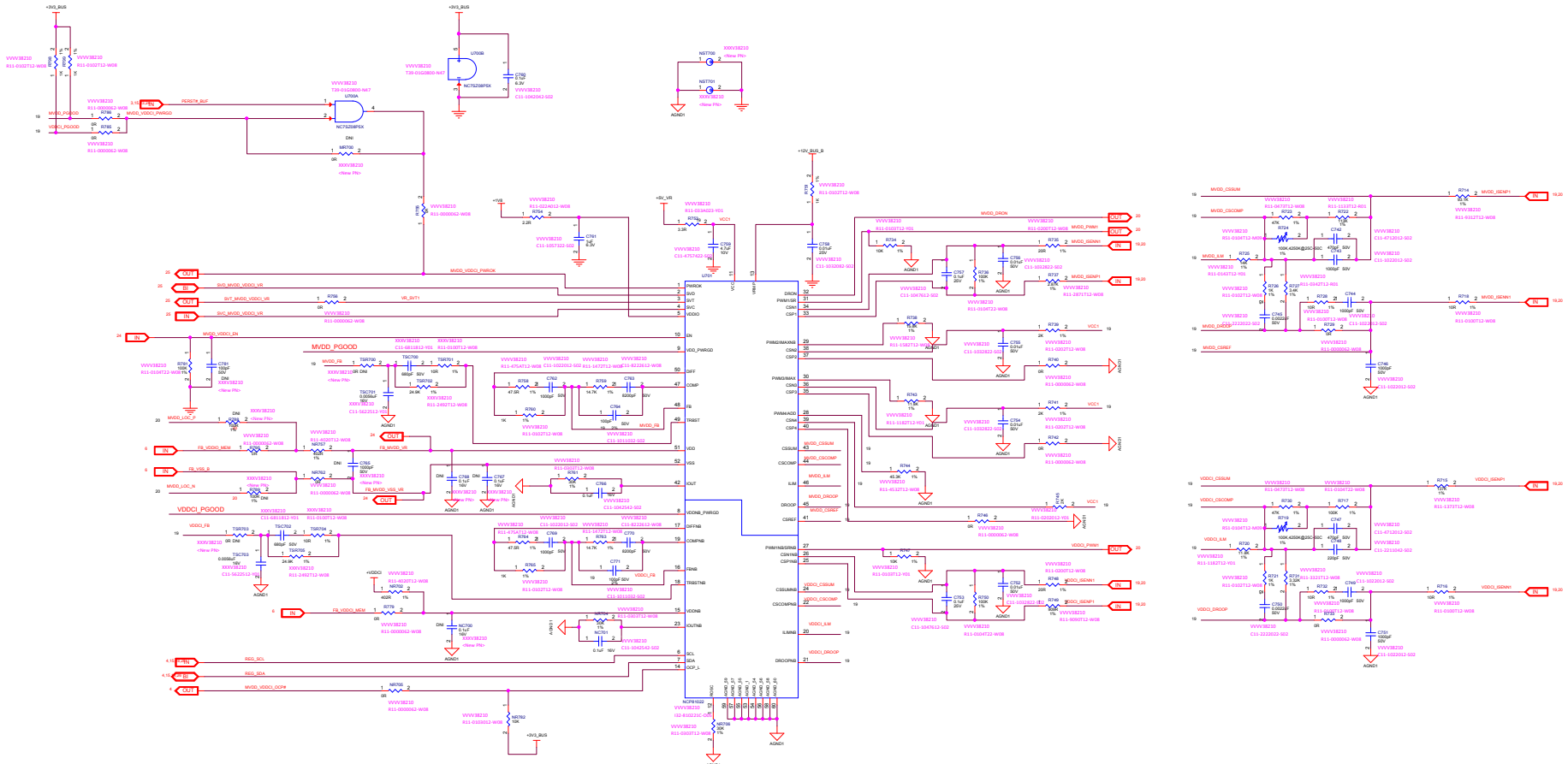


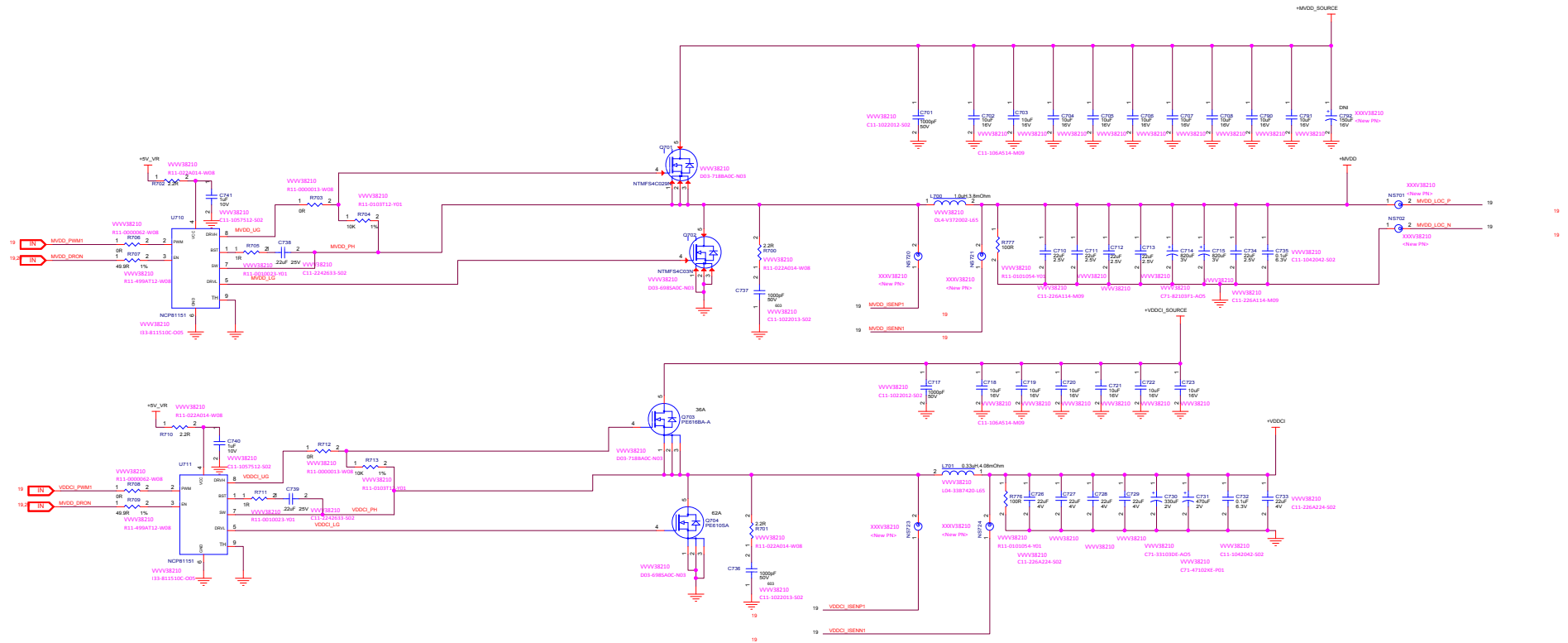
$$0.8V \cdot (1 + 40.2K / 7.68K) = 4.9875V$$

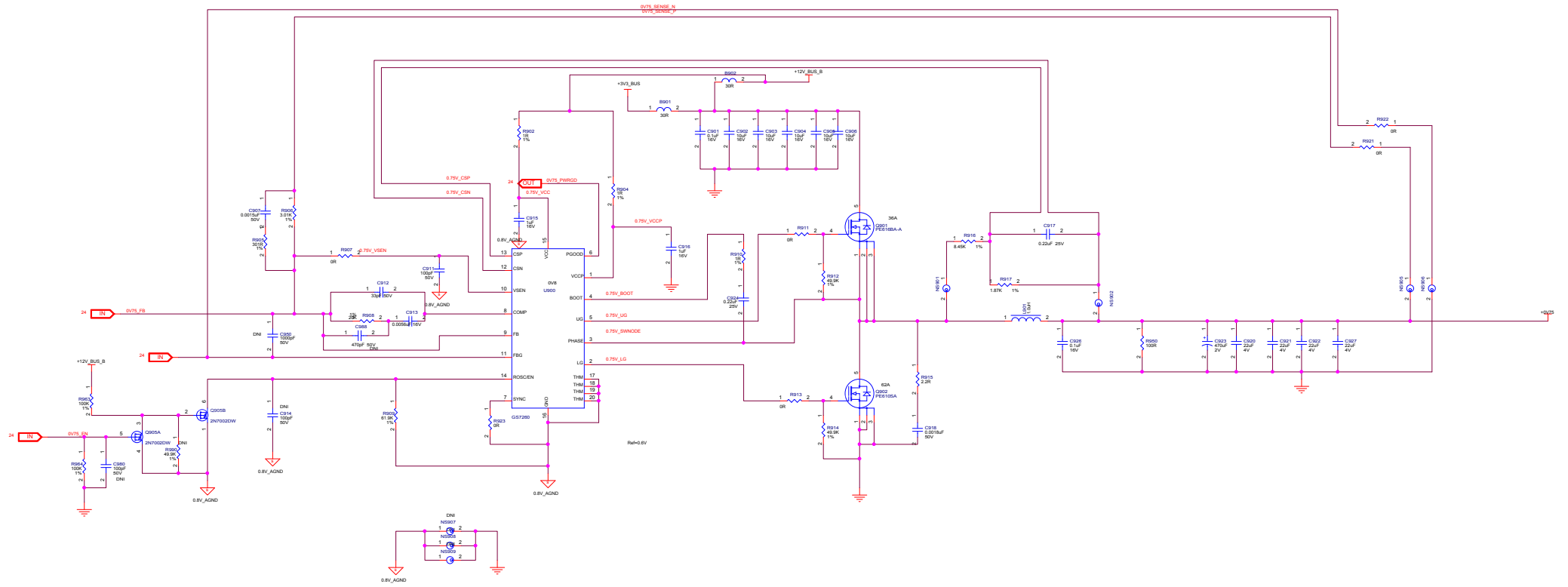
		<b>MICRO-STAR INT'L CO.,LTD</b>	
		<b>MS-V382</b>	
Size	Document Description	Rev 10	
Custom	REG VDDSOC	Date: Thursday, September 12, 2019   Sheet 17 of 27	

1.8V REFERENCE DAC  
 INITIAL VOLTAGE = 1.8V  
 I2C ADDRESS(7bit/8bit) 0x53/0xA6

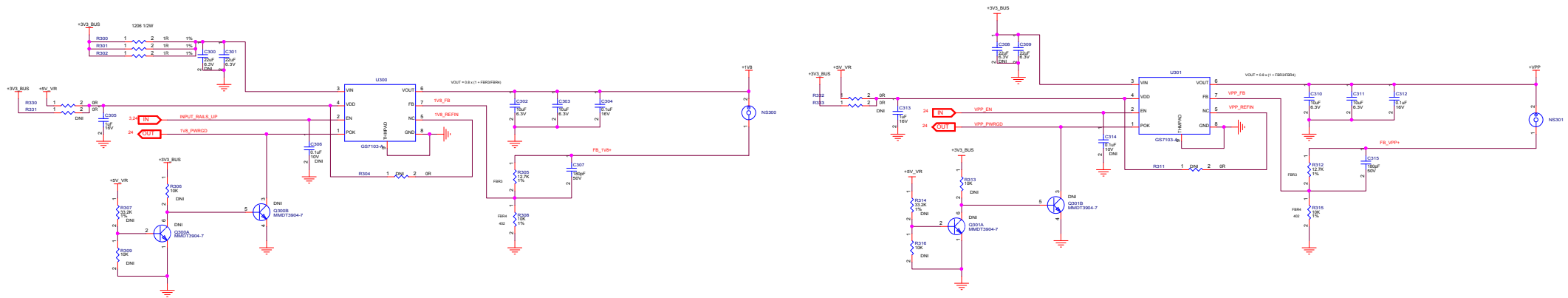


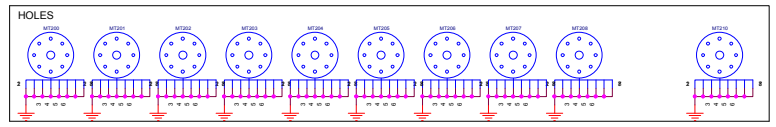
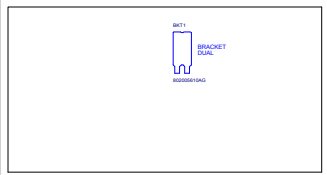
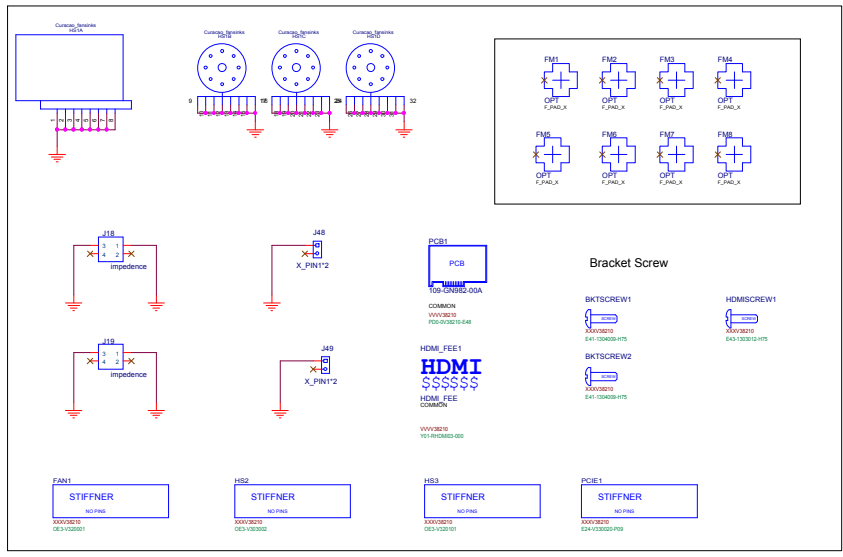
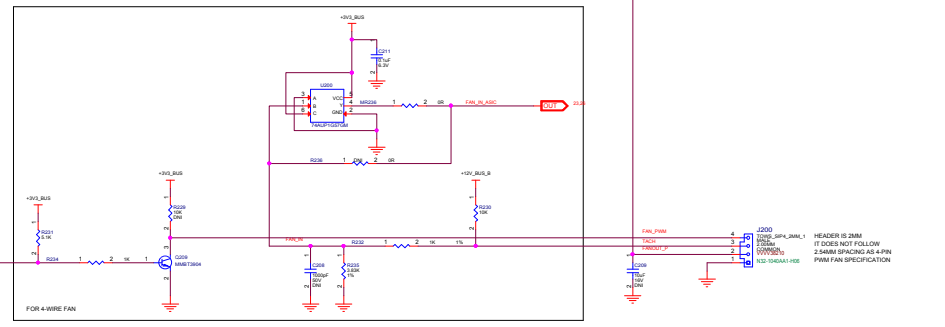
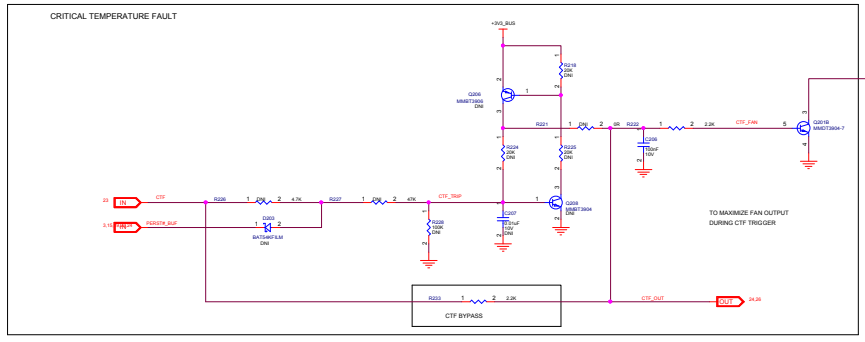
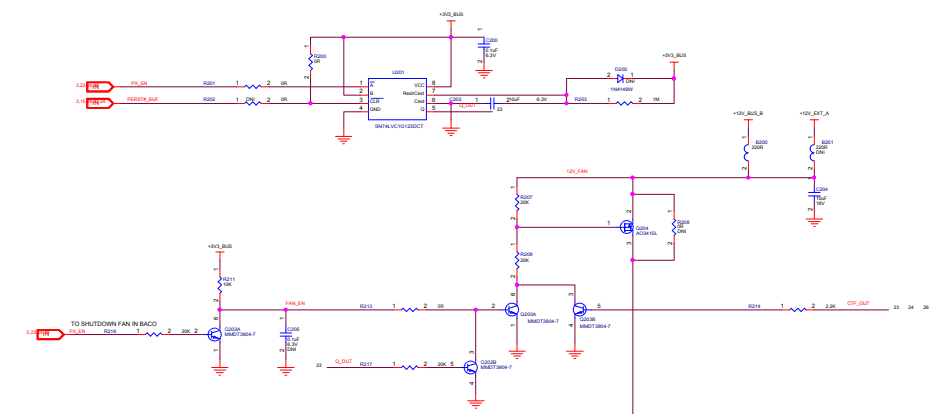
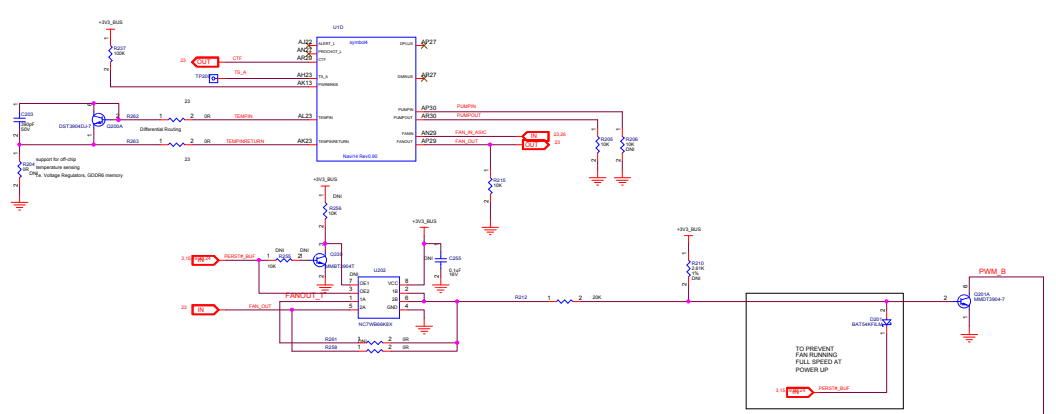


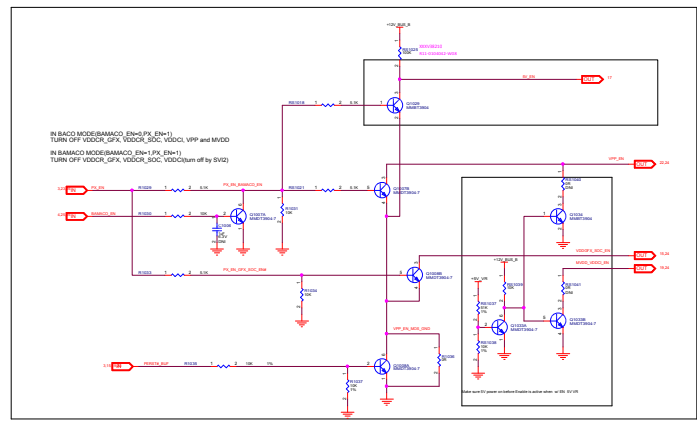
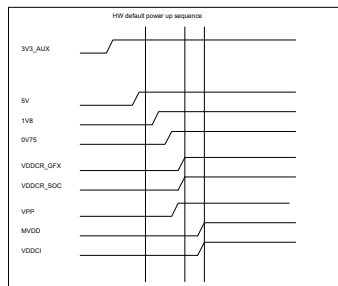
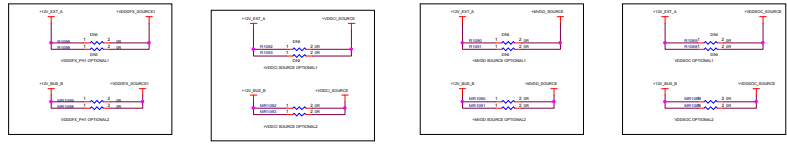
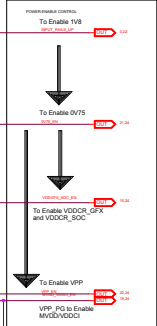
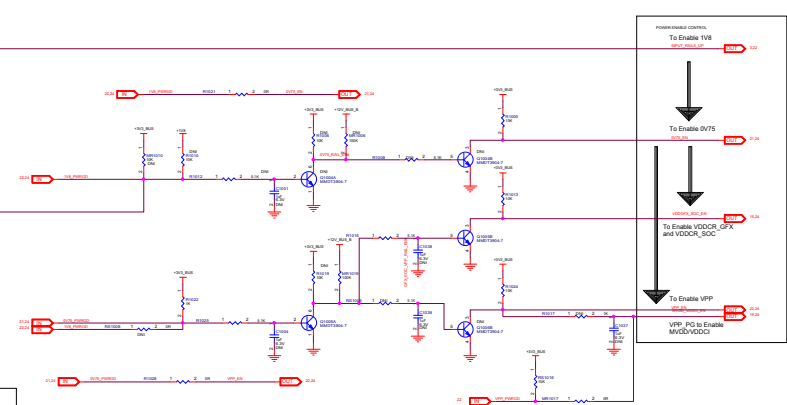
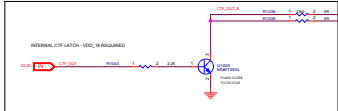
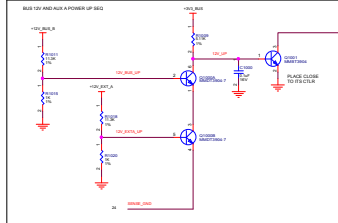
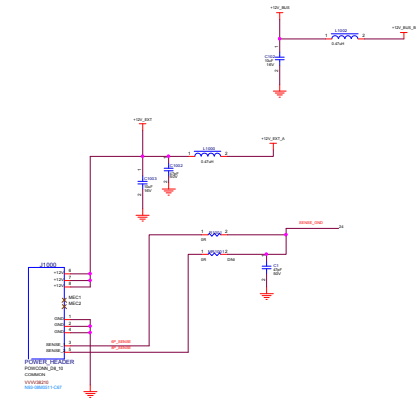




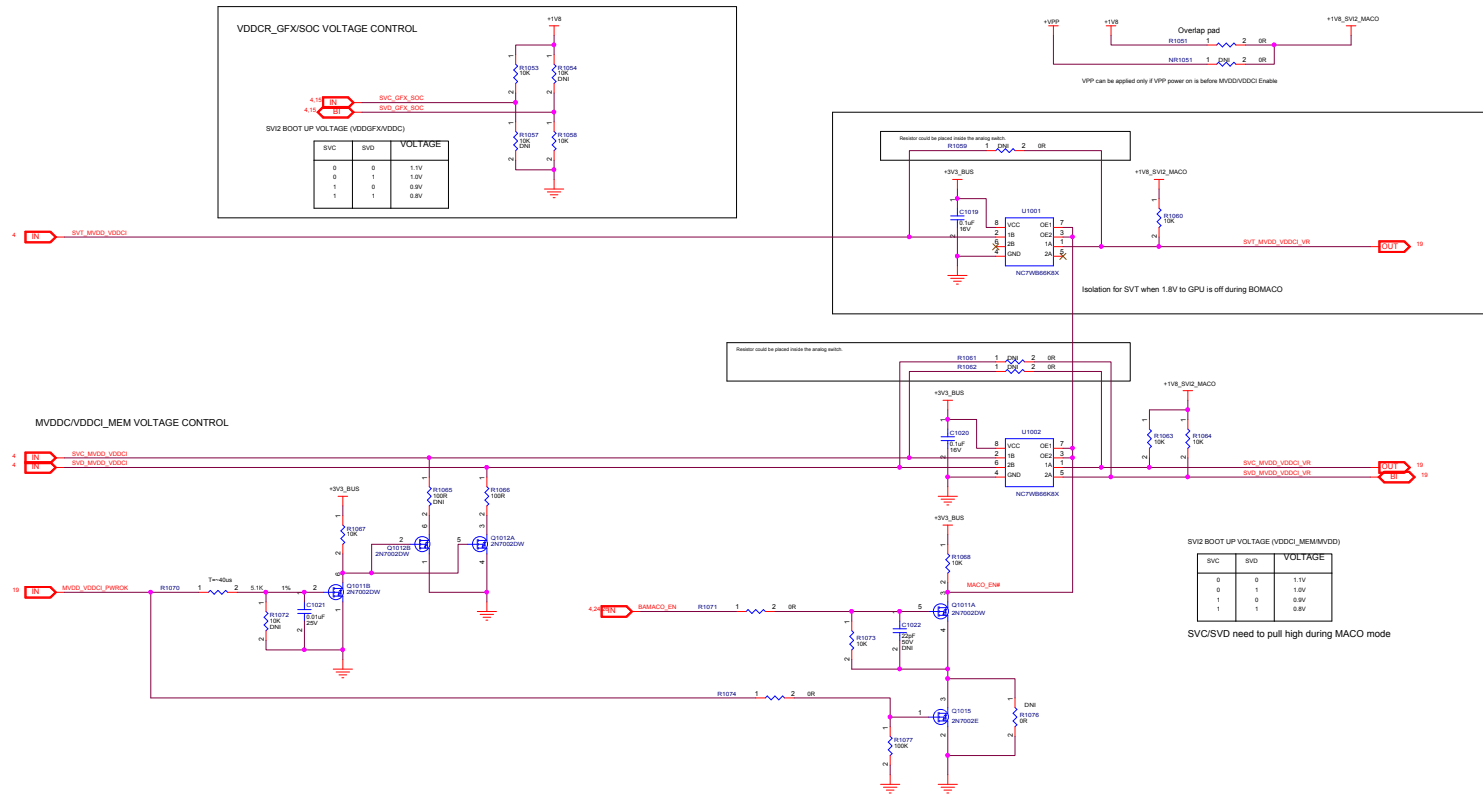
LDO - 1V8/VPP/5V



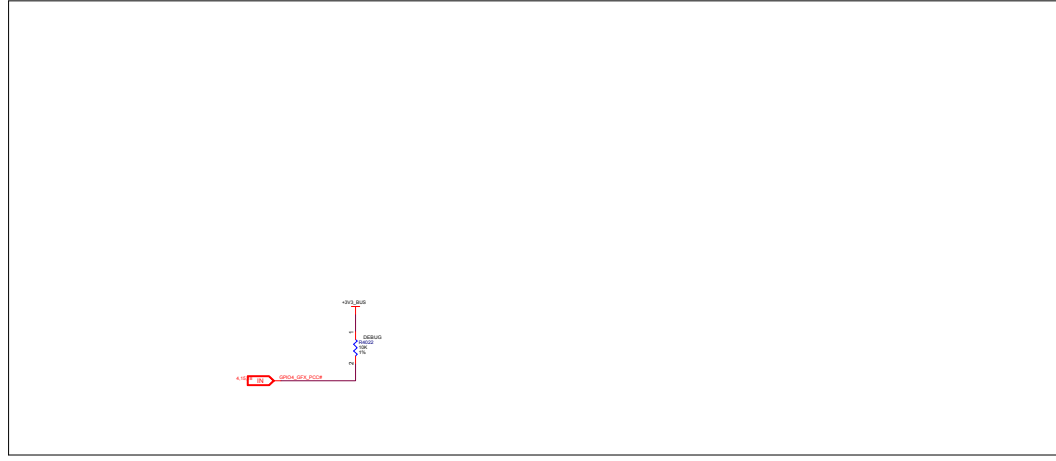
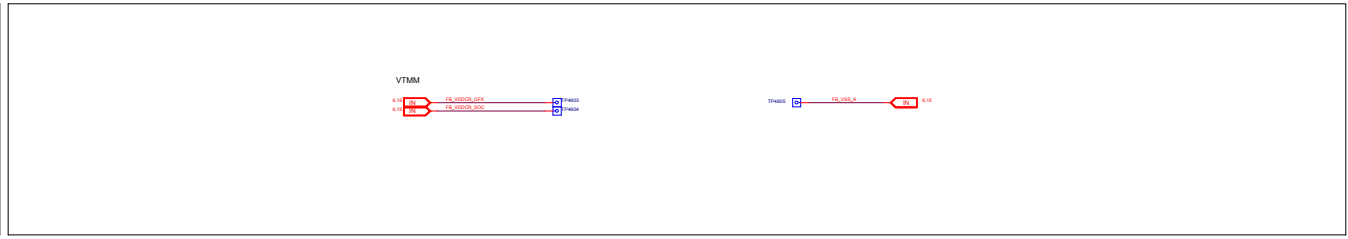
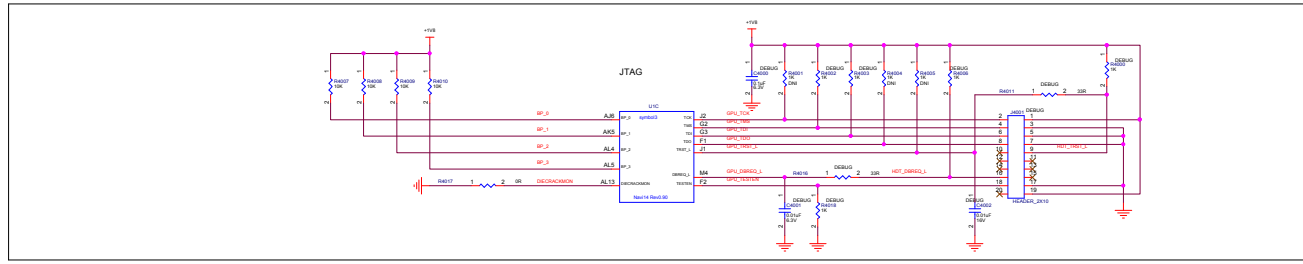








(29) DEBUG CIRCUIT





TITLE: NAVI14 XT GDDR6 x16 DT BOARD

DOCUMENT NUMBER: 105-D33200-00B

DATE: Mon Apr 22 08:33:14 2019

SHEET NUMBER: 27 OF 27

REV: B

REVISION HISTORY

ENGINEER: Billy Deng

NOTES: NOTE

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AMD-PLATFORM HARDWARE ENG  
 No.669,HUANKE ROAD  
 SHANGHAI,CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
1.00	00A	08/07/2018	Initial schematic
1.00	00B	12/29/2018	change all 4172010501G parts to 4172010500G
		04/16/2019	ADD D1152 D1162 D1182 D1192 ADD R1016 AND CHANGE INVOID LOCAL SENSE POINT ADD R1022 R1093 MR1092 MR1093 and reassign g1 phase1-3 input source ADD R4653 R4654 R4655 C4659 Change P51: 0.33uF4520118000G R749: 909R1316050000G NR704: 30K13160300200G R743: 18K13160180220G C747-470uF14170047500G C748:220uF14170022100G



MICRO-STAR INT'L CO.,LTD  
 MS-V382  
 Document Description  
 REVISION HISTORY  
 Date: Monday, September 09, 2019 Sheet 27 of 27