

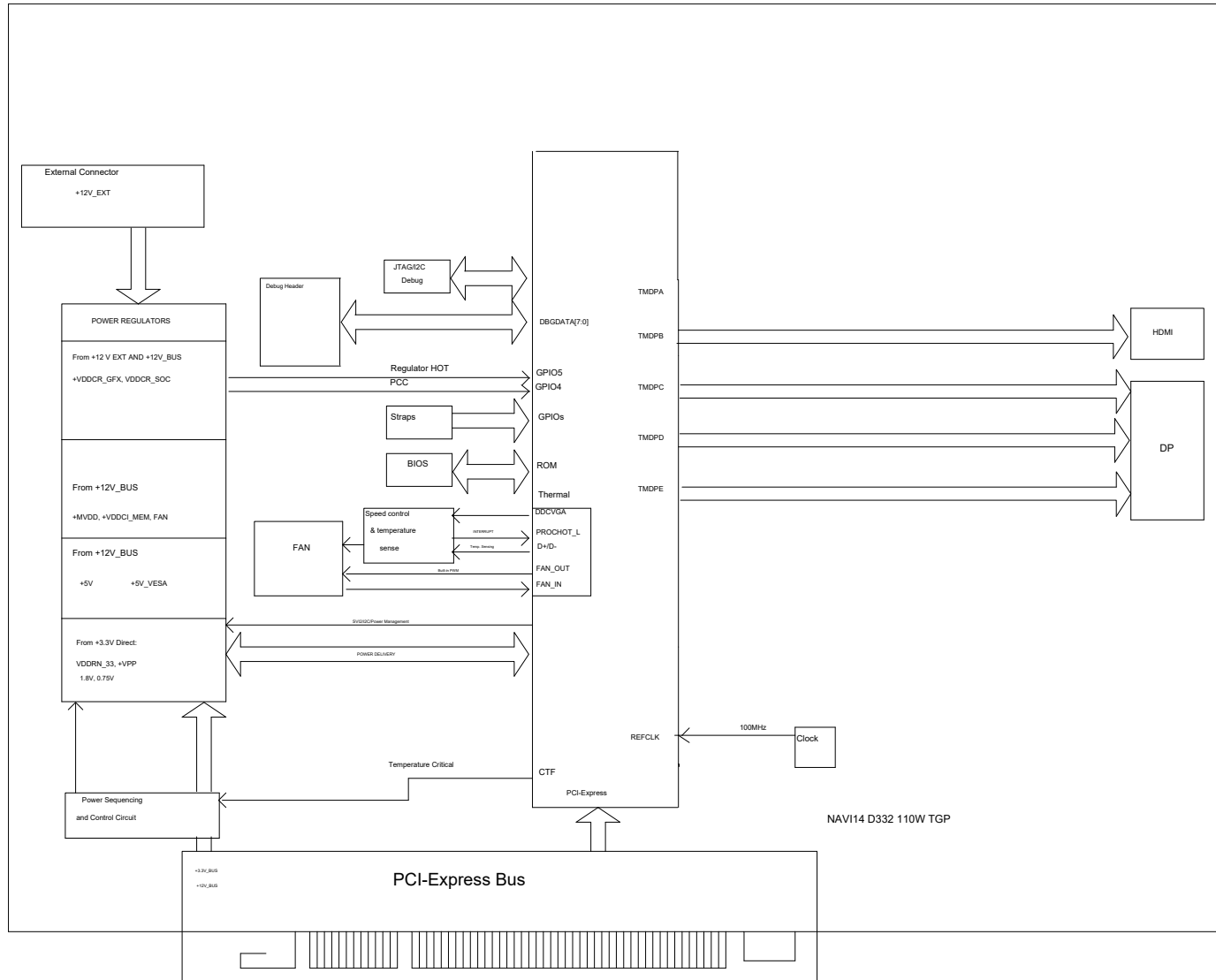
2019/08/28:

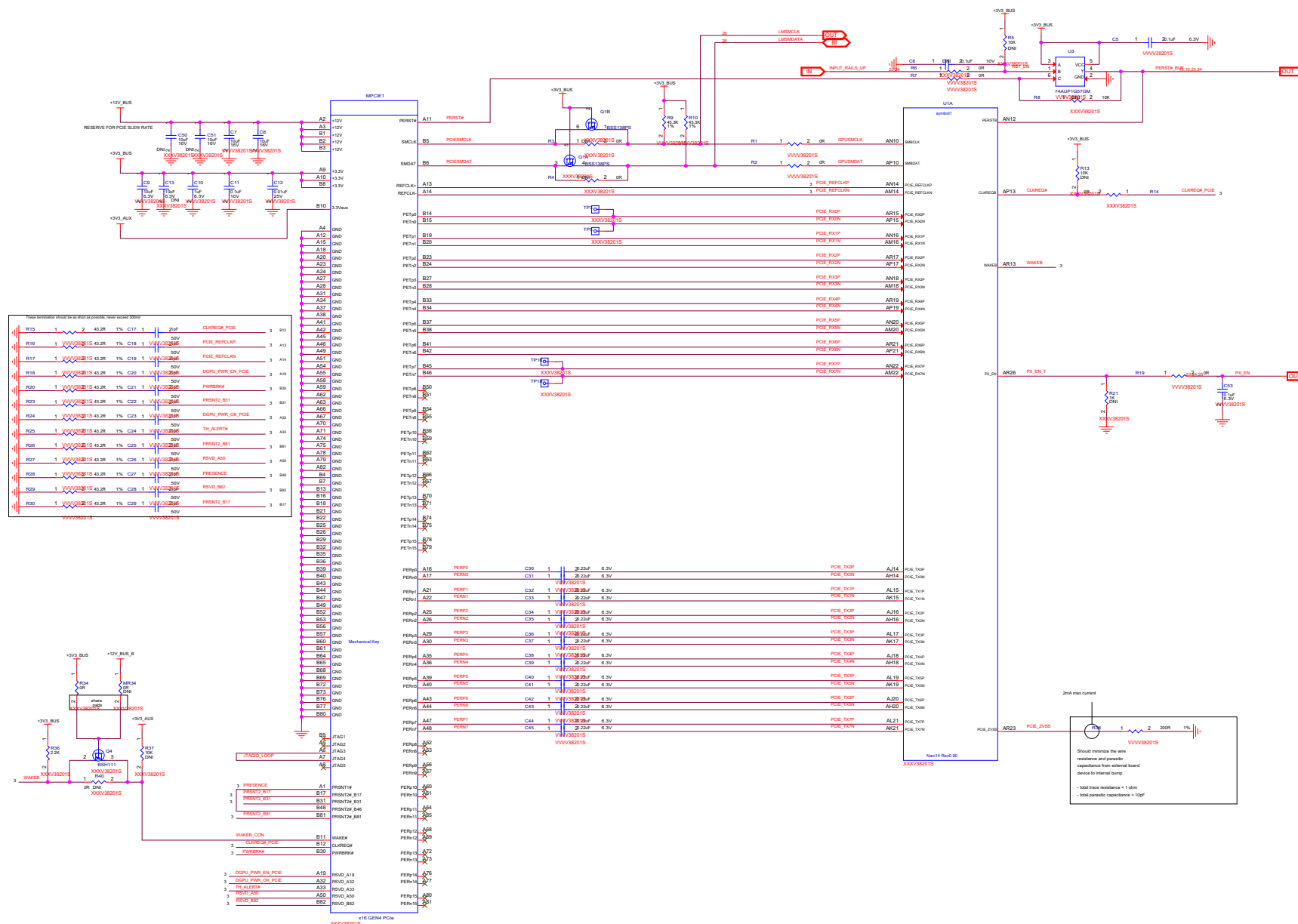
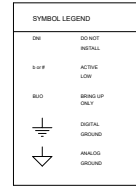
PAGE14: 上件DP
 PAGE24: 改反向6 & 8 PIN COLAY
 ADD FUSE
 PAGE27: ADD MCU

NAVI14 GDDR6 4PCS,8L 3xDPs +1xHDMI
 105-D332xx-00B RevB Desktop board(110W TGP)

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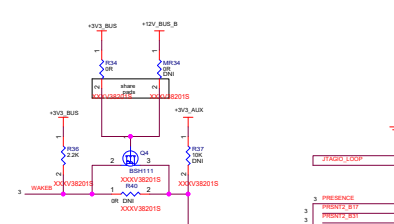
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	DEBUG CIRCUITS
2	BLOCK DIAGRAM	27	REVISION HISTORY
3	NAVI14 - PCIe Interface		
4	NAVI14 - GPIO_EXTRA		
5	NAVI14 - XTAL		
6	NAVI14 - POWER and GND		
7	NAVI14 - Decaps		
8	NAVI14 - MEM CH AB		
9	NAVI14 - MEM CH CD		
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16	REG VDDGFX		
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20	REG VDDCIMVDD		
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22	LDO 1V8/PPIS/SV_VESA		
23	MECHANICAL AND THERMAL		
24	POWER MANAGEMENT		
25	SVI2		





Resistor tolerances should be as tight as possible, unless stated otherwise

R15	1	43.2k	1%	C17	1	22pF	CLRREQ_P0E	3	810
R16	1	43.2k	1%	C18	1	22pF	P0E_REFCLKP	3	810
R17	1	43.2k	1%	C19	1	22pF	P0E_REFCLKN	3	810
R18	1	43.2k	1%	C20	1	22pF	DGPU_PWR_EN_P0E	3	810
R20	1	43.2k	1%	C21	1	22pF	PWRB9M4	3	810
R23	1	43.2k	1%	C22	1	22pF	PRINT2_B01	3	810
R24	1	43.2k	1%	C23	1	22pF	DGPU_PWR_OK_P0E	3	810
R25	1	43.2k	1%	C24	1	22pF	TH_ALERTA	3	810
R26	1	43.2k	1%	C25	1	22pF	PRINT2_B01	3	810
R27	1	43.2k	1%	C26	1	22pF	REV0_A00	3	810
R28	1	43.2k	1%	C27	1	22pF	PRESSENCE	3	810
R29	1	43.2k	1%	C28	1	22pF	REV0_B02	3	810
R30	1	43.2k	1%	C29	1	22pF	PRINT2_B17	3	810



Mechanical Key

1	PRESENCE	A1	PRINTM4
3	PRINT2_B17	B17	PRINTM7_B17
3	PRINT2_B01	B01	PRINTM7_B01
3	PRINT2_B04	B04	PRINTM7_B04
3	PRINT2_B01	B01	PRINTM7_B01
3	WAKEB_CON	B11	WAKEB
3	CLRREQ_P0E	B12	CLRREQ_P0E
3	PWRB9M4	B30	PWRB9M4
3	DGPU_PWR_EN_P0E	A19	REV0_A19
3	DGPU_PWR_OK_P0E	A32	REV0_A32
3	TH_ALERTA	A33	REV0_A33
3	REV0_Z00	A50	REV0_A50
3	REV0_B02	B02	REV0_B02

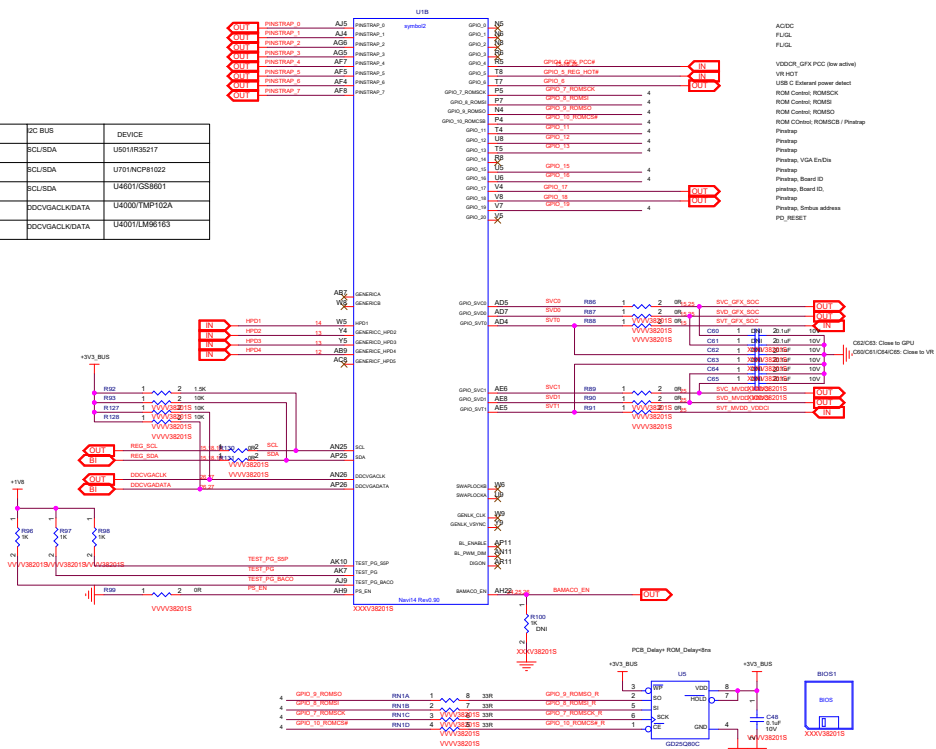
20mA max current

Should minimize the wire resistance and parasitic capacitance from external board device to internal bump.

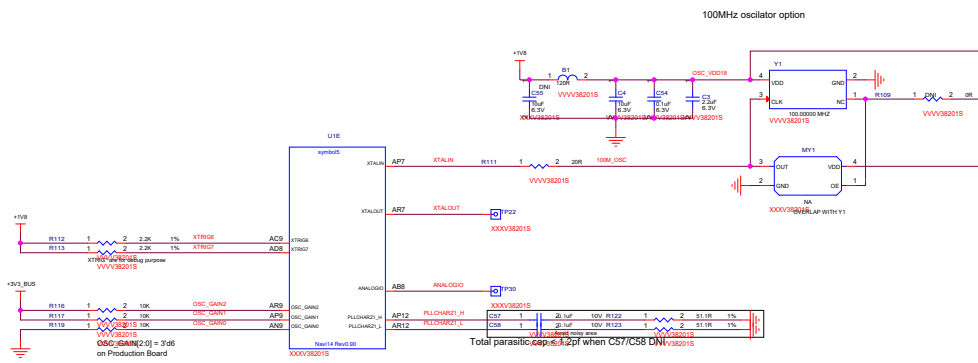
- Total trace resistance = 1 ohm
- Total parasitic capacitance = 10pF

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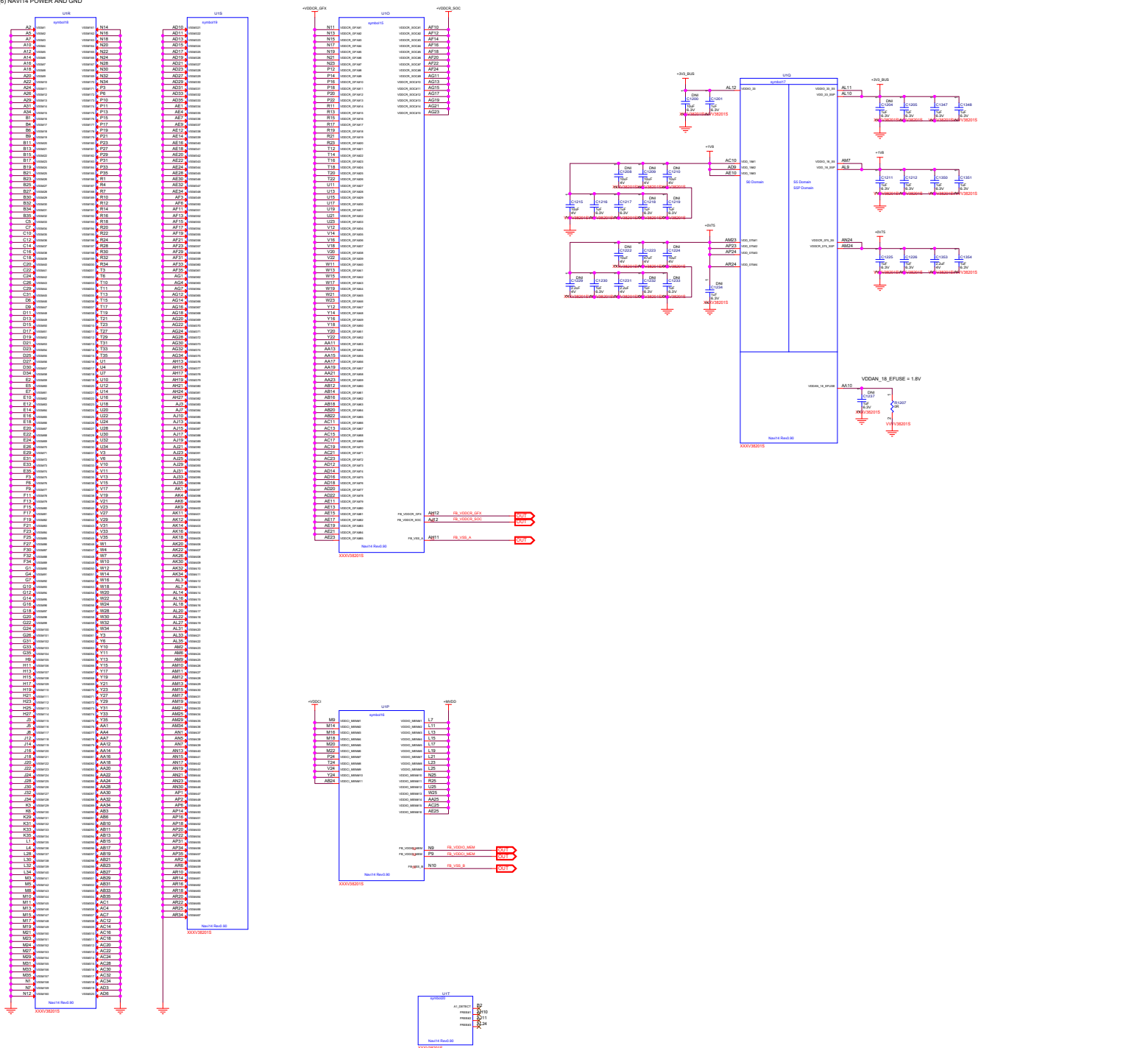
HW ID	HW ID	FUNCTION	I2C BUS	DEVICE
0x00	0x60	VDDCR GFX/IOC	SCL/SDA	U601R38217
0x02	0x44	MVDD/VDDCI	SCL/SDA	U701NCR9102
0x03	0x46	PCC/Preserved	SCL/SDA	U4001/CS8801
0x48	0x50	G6 Temperature	DDCVGACLKDATA	U4000/TMP102A
0x4c	0x68	EXT SENSOR	DDCVGACLKDATA	U4001/LM86183

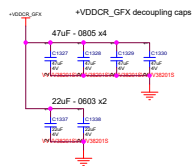
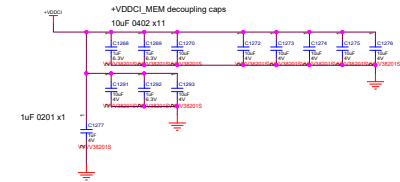
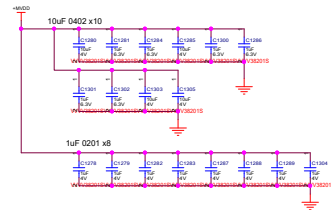
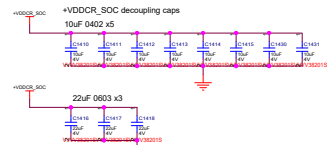
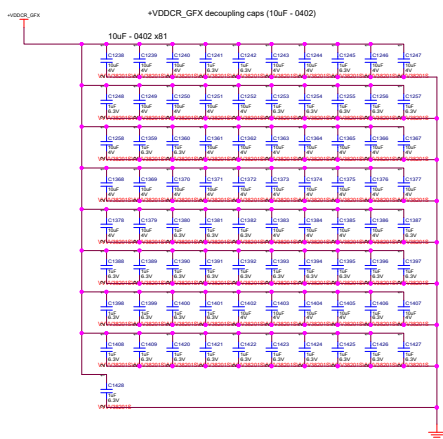


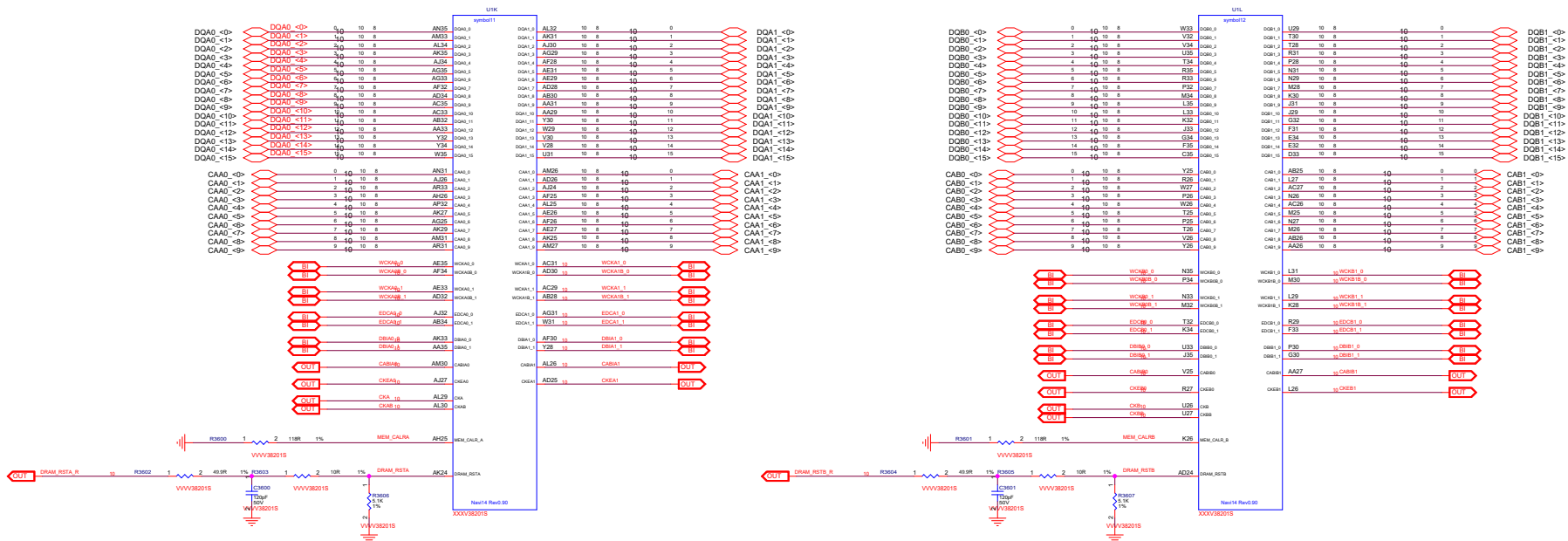
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: PCH GEN 4 supported 1: PCH GEN 4 not supported
	0	PINSTRAP_BIF_CLK_PM_EN 0: CLK/PWRD power management capability is disabled 1: CLK/PWRD power management capability is enabled
DCE	0	PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing (only for ramp)
	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity is enabled 1: The device won't be recognized as the system's VGA controller
Platform	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1-5: endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
	0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for both DisplayPort and HDMI Default: (GPIO12/GPIO11) = 11
SMU	1	PINSTRAP_FIG[1:0] - No definition on NV
	1	PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
SMU	1	PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100 - 512KBIT (BT) M25P04A 101 - 1MBIT (BT) M25P04A 101 - 504KBIT (BT) M25P04 101 - 4MBIT (BT) M25P04 101 - 1MBIT (BT) M25P04 101 - 512KBIT (CHNMG) M25LV512 101 - 1MBIT (CHNMG) M25LV512 Default: (PINSTRAP_PINSTRAP/PINSTRAP) = 101
	0	PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
SMU	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device
	0	GPIO_0



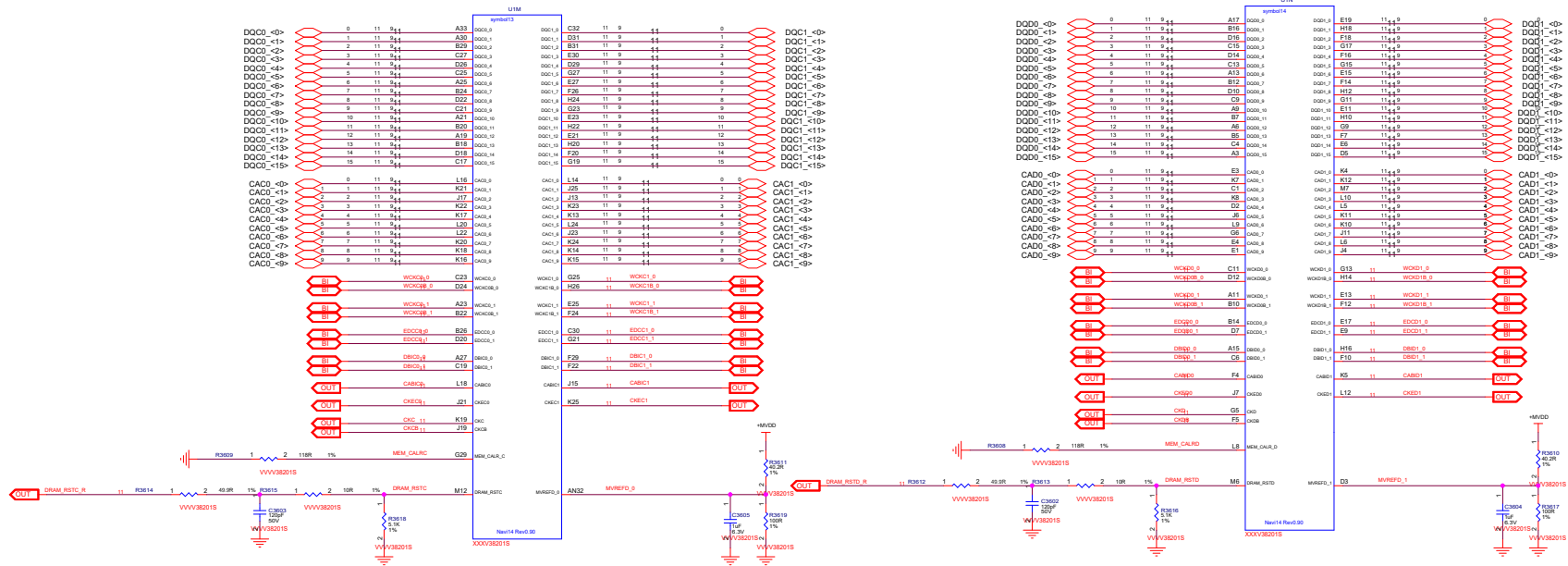
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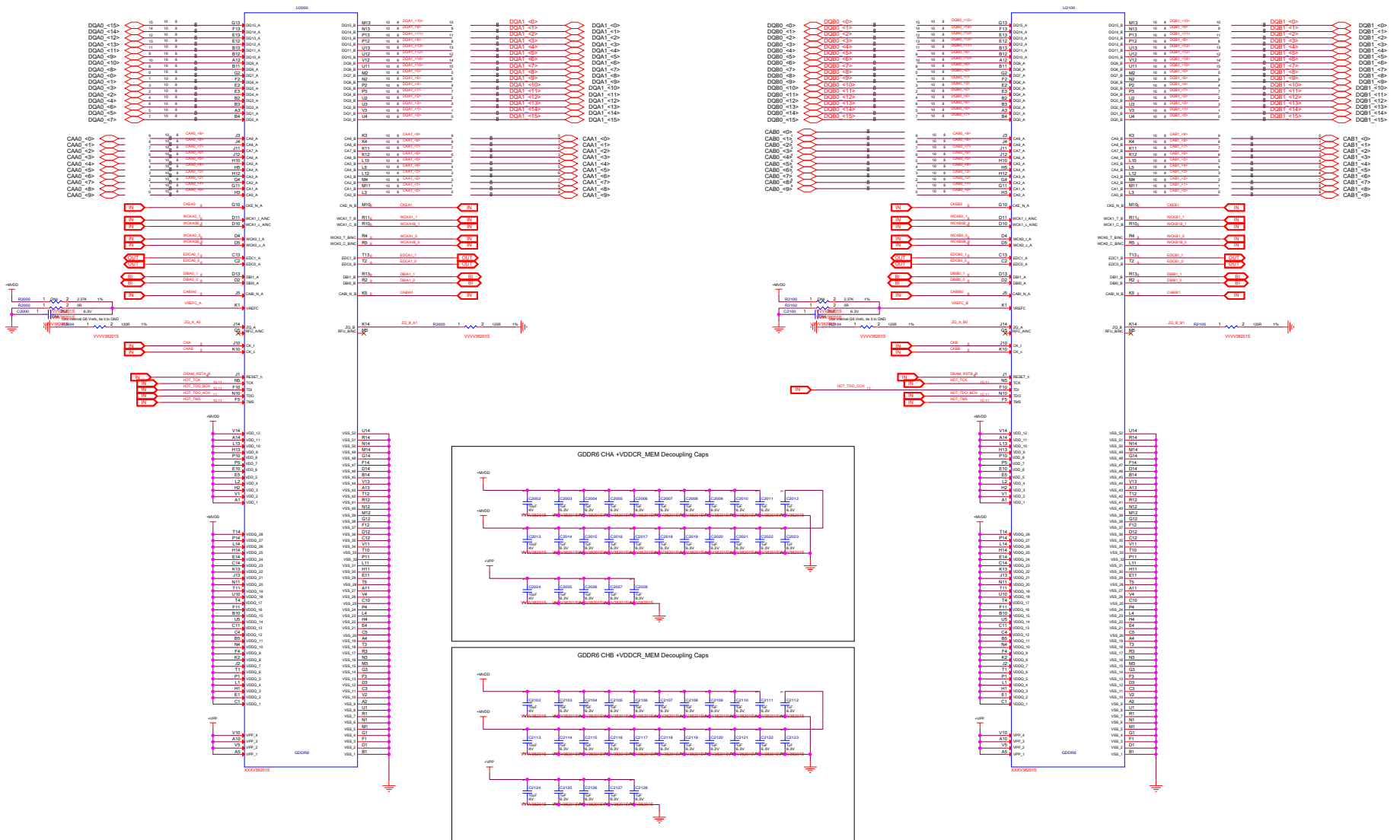


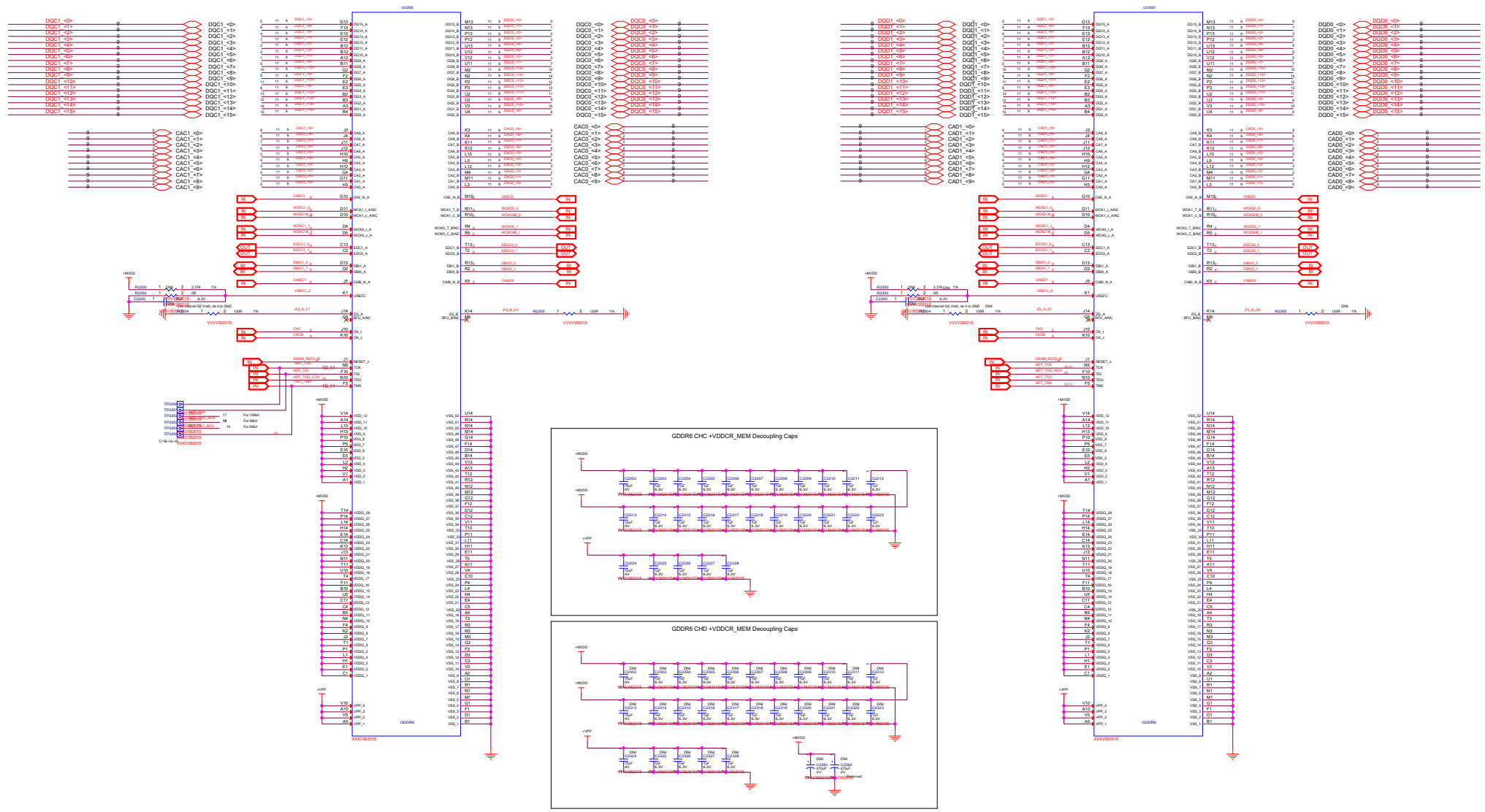




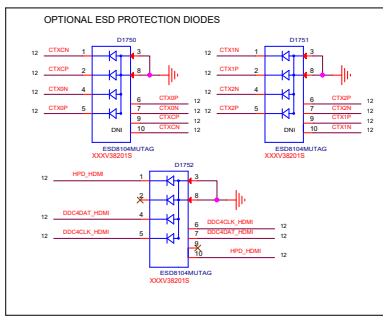
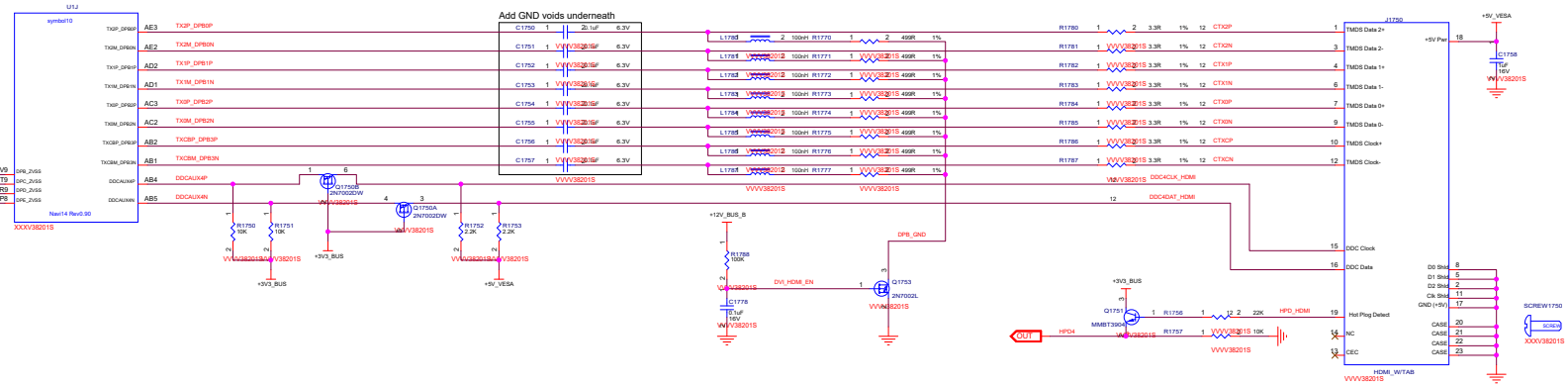
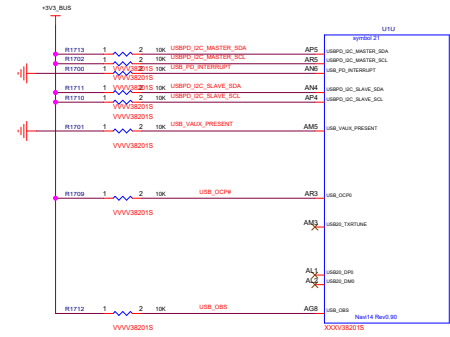
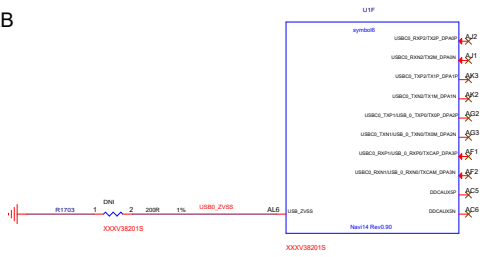
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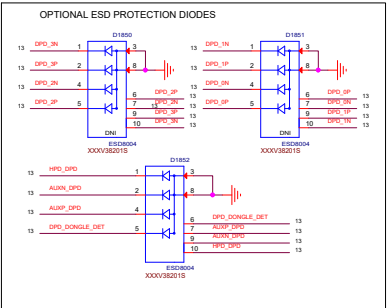
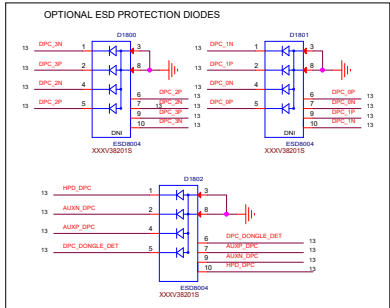
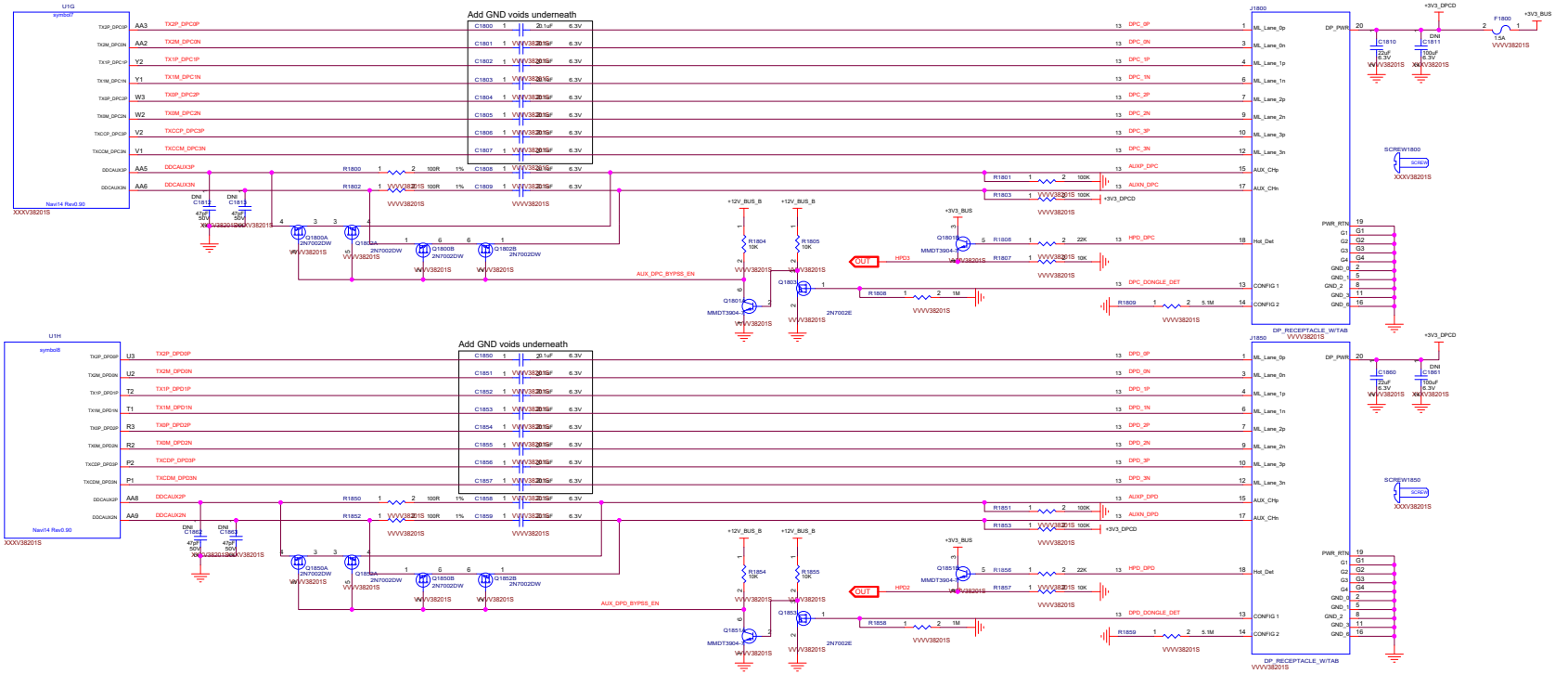




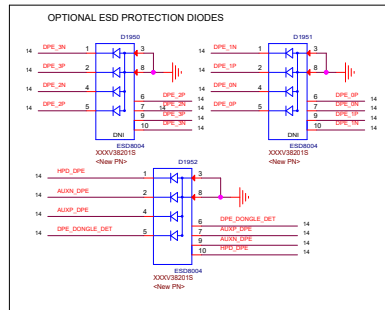
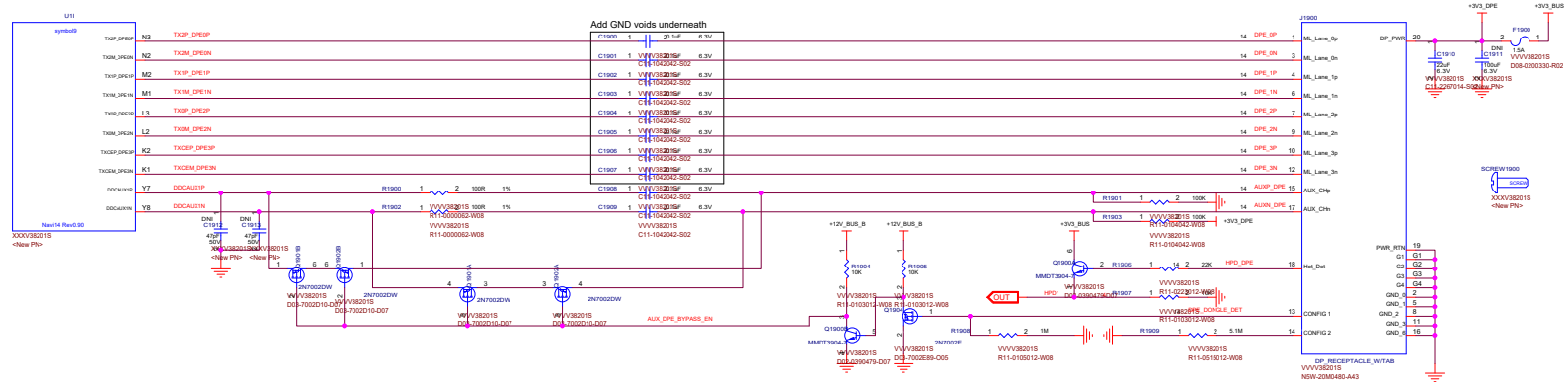
(12) TMDP AB



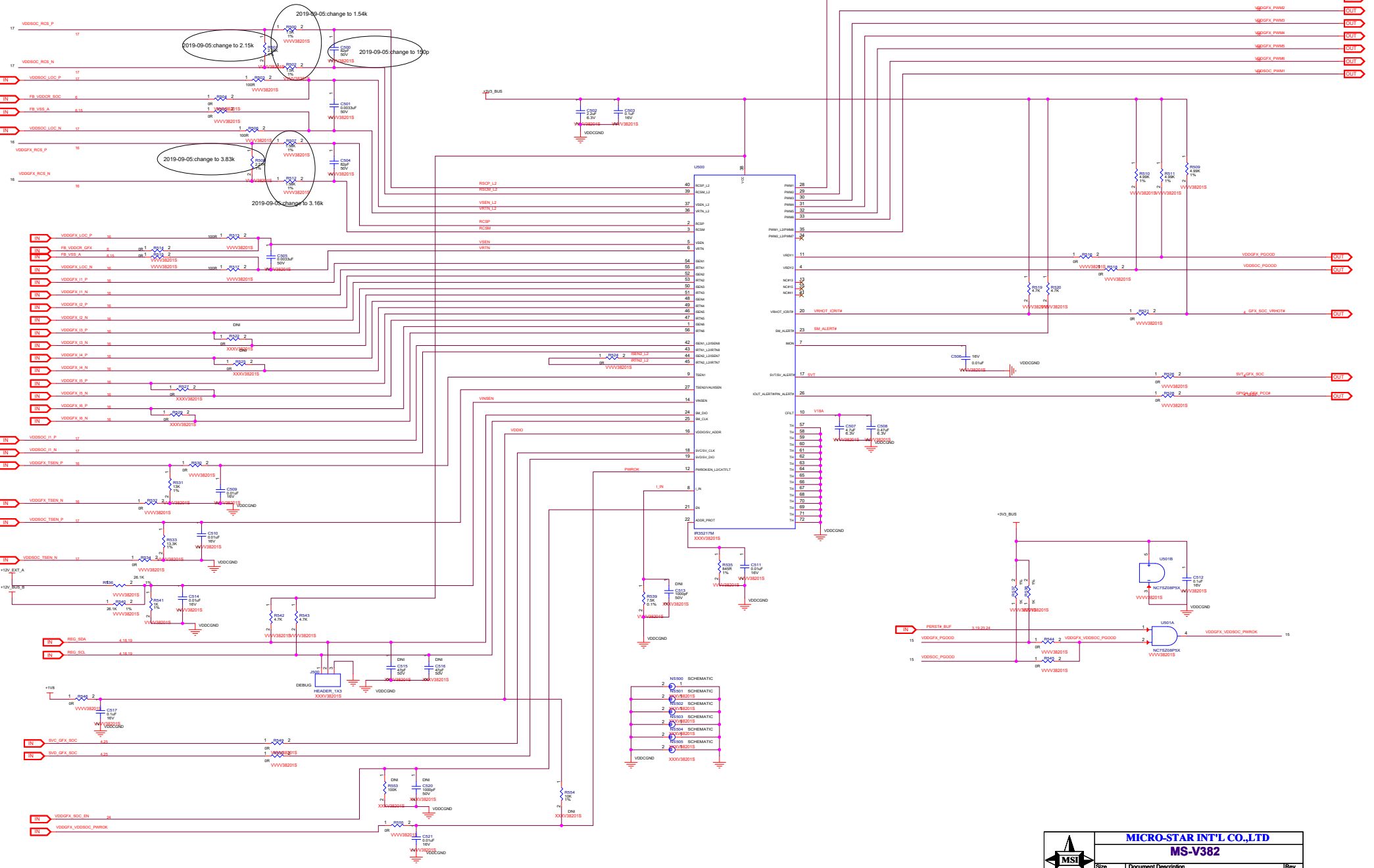
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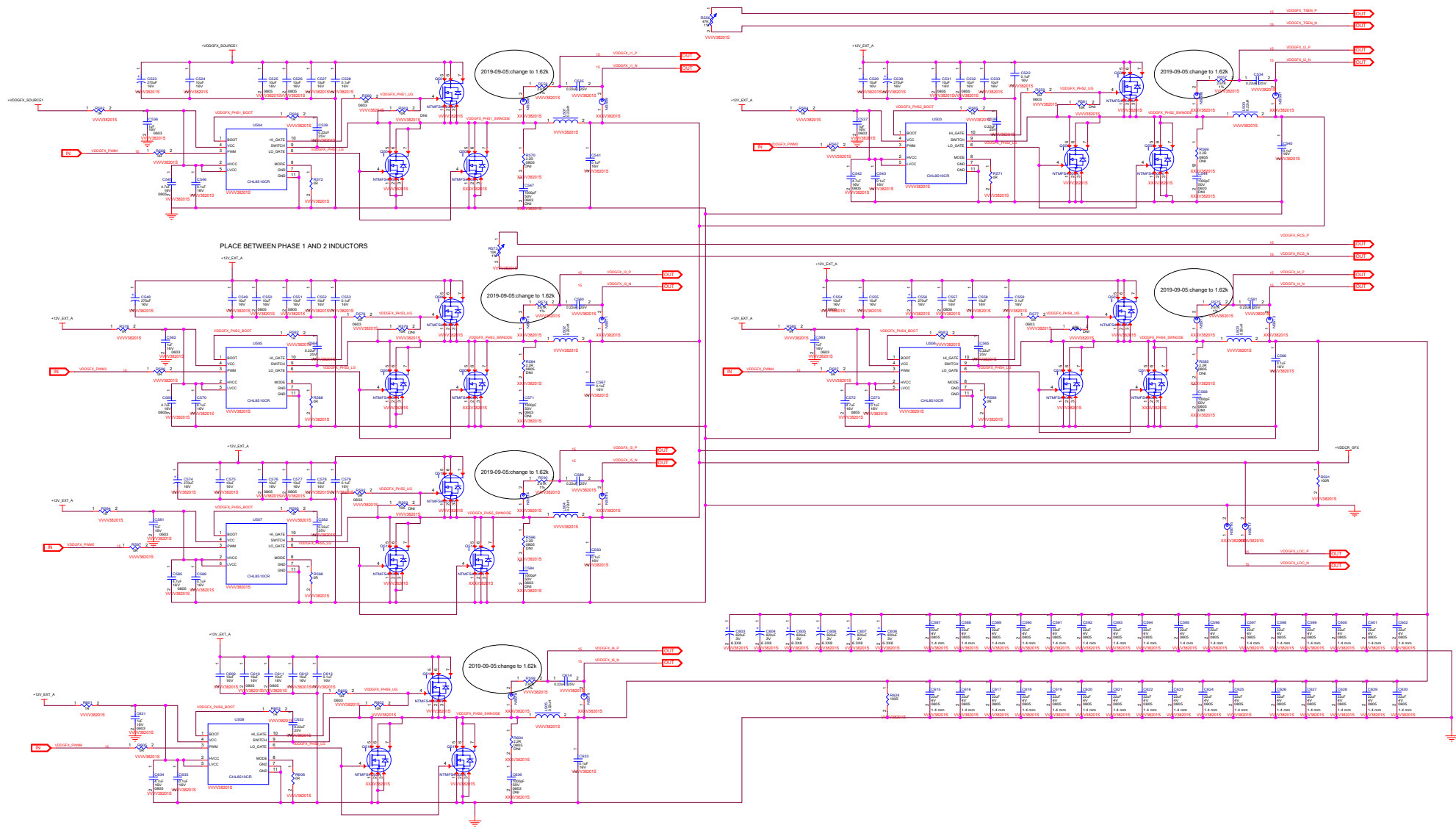
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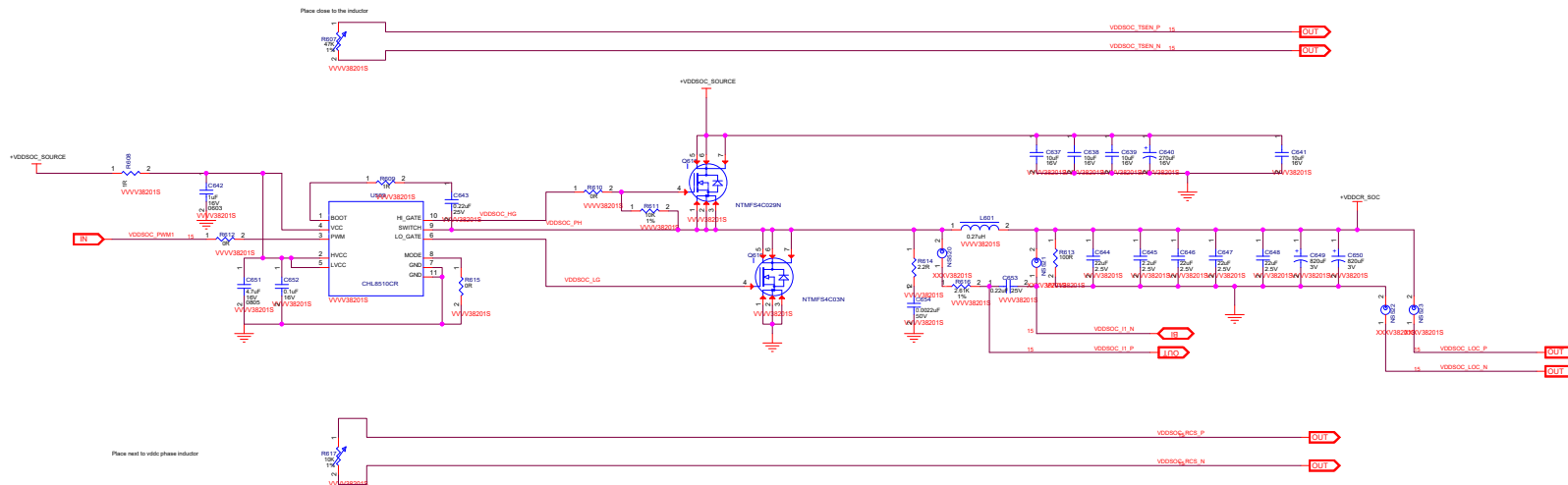


REG - VDDGF/VDDSOC CTRL



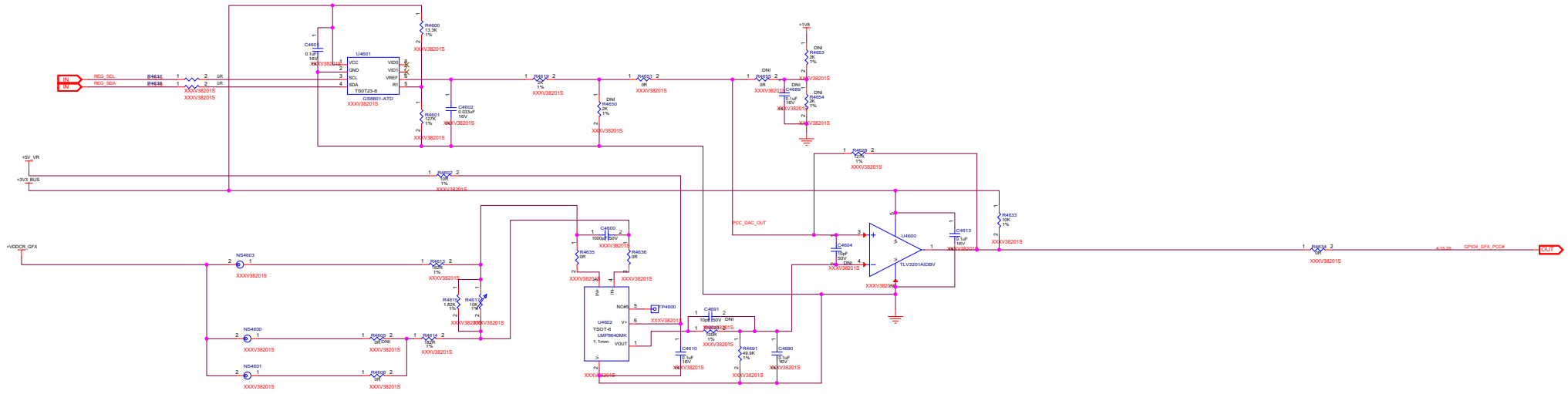
PLACE NEXT TO PHASE 3 HALF BRIDGE




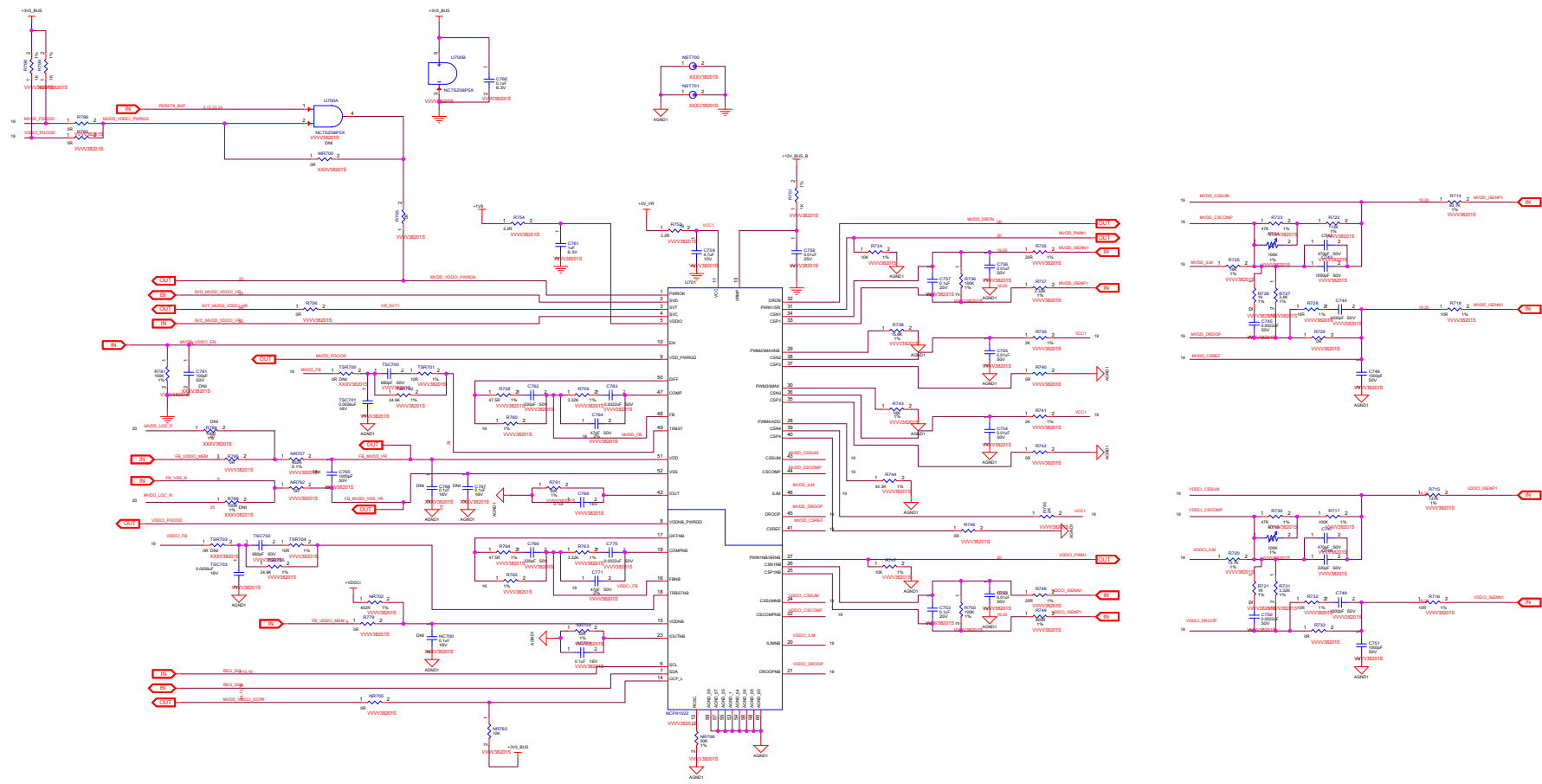


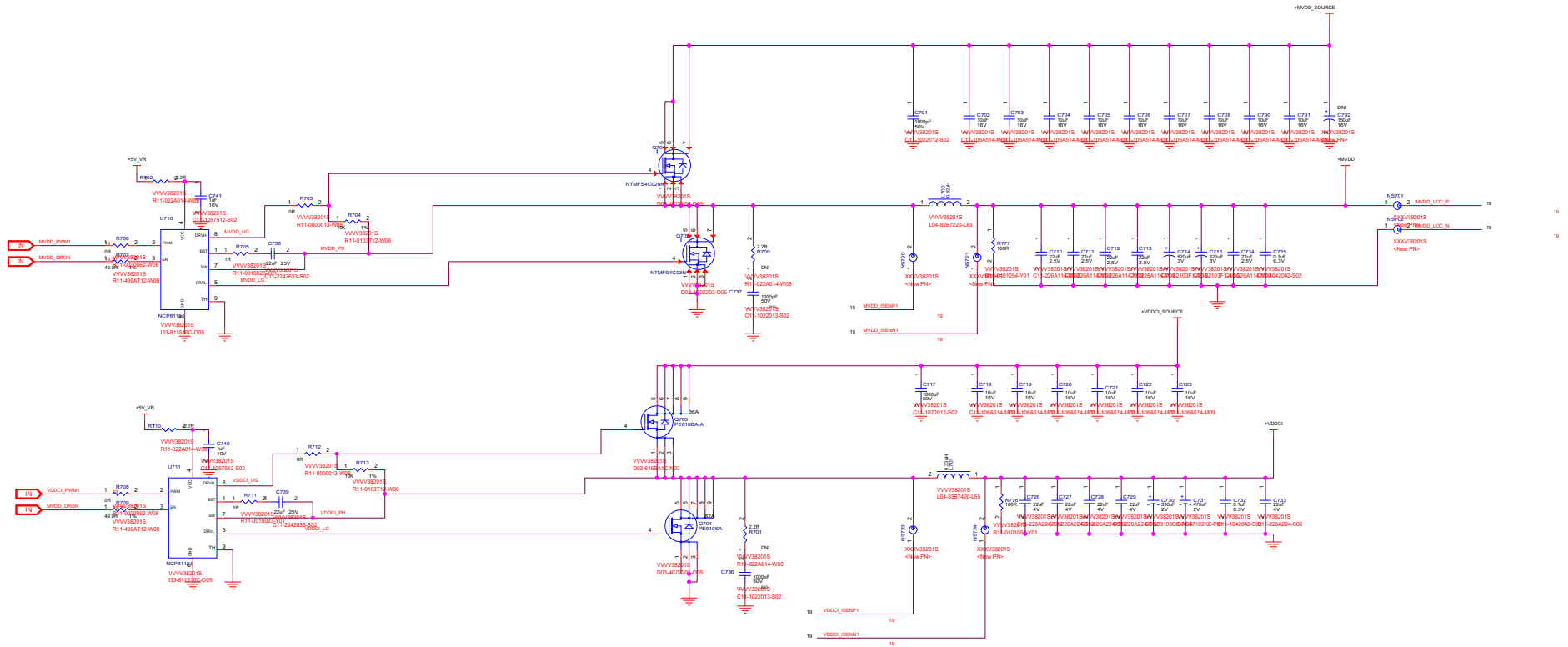
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1.8V REFERENCE DAC
 INITIAL VOLTAGE = 1.8V
 I2C ADDRESS(7bit/8bit) 0x53/0xA6

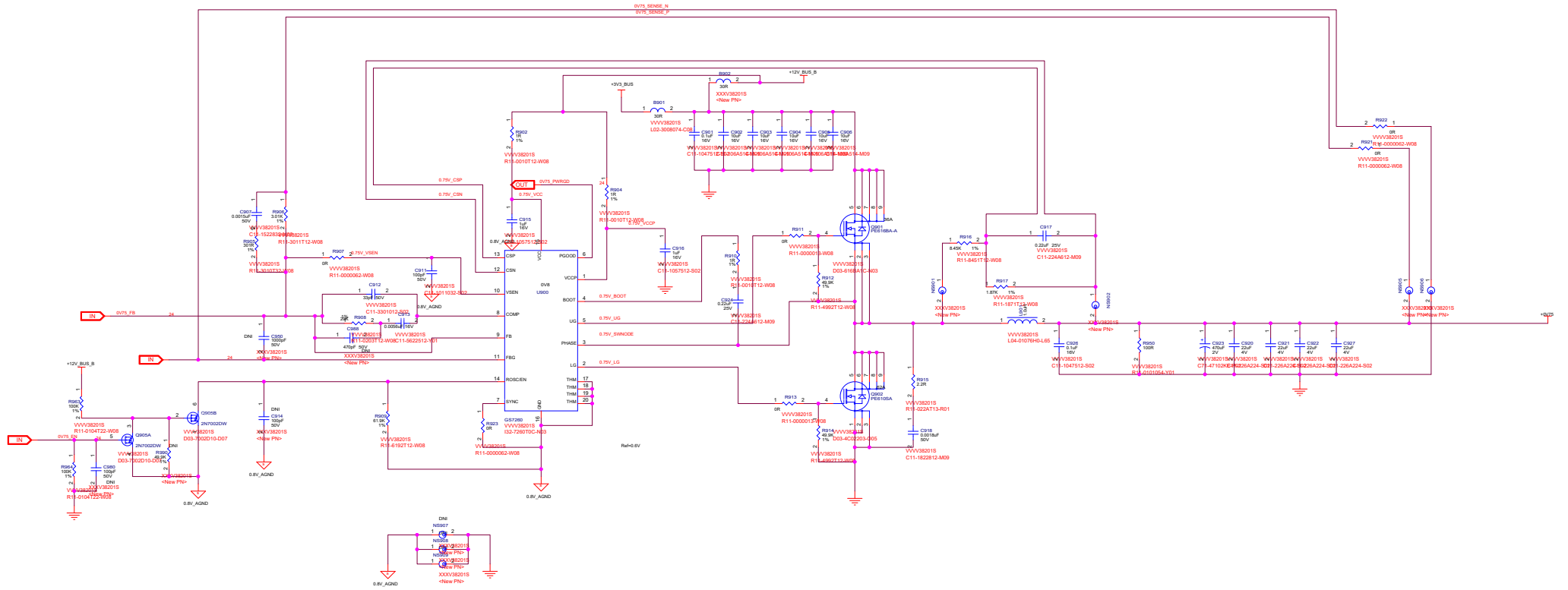


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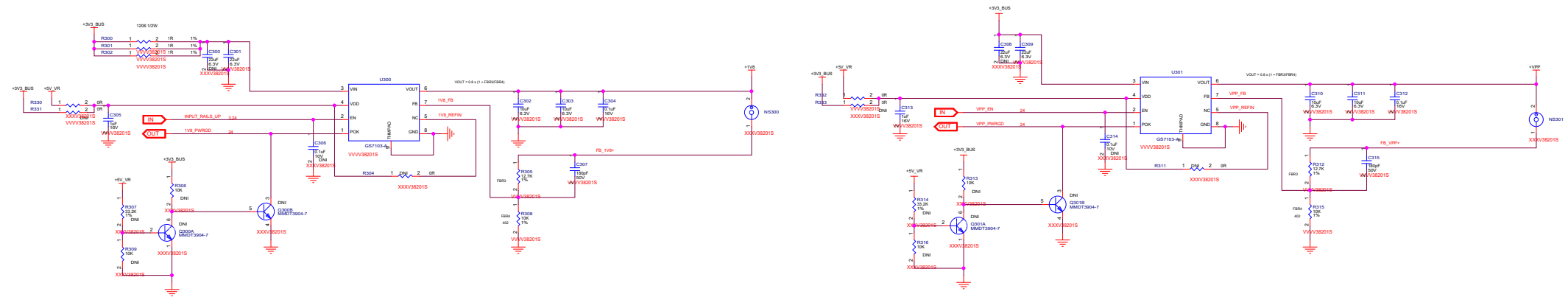




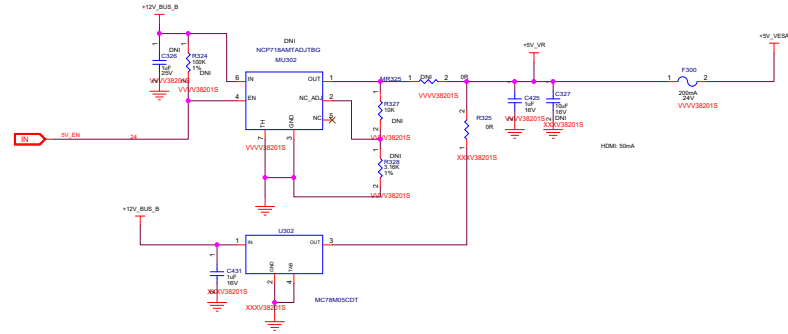
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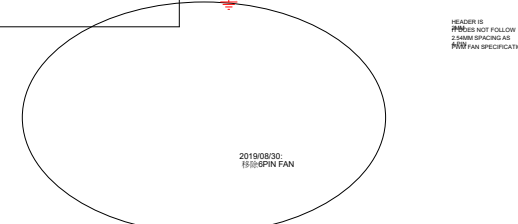
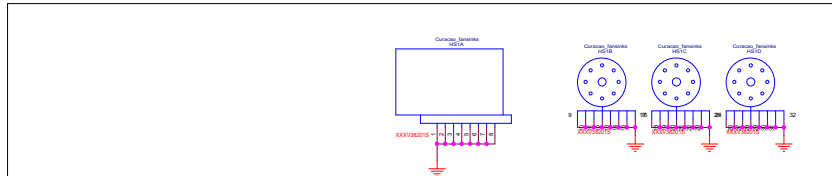
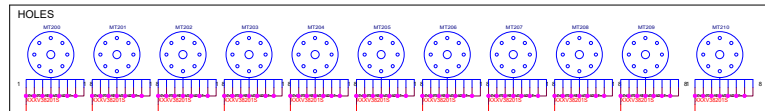
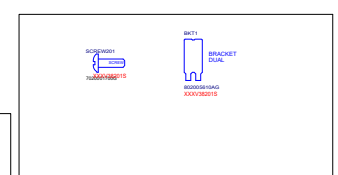
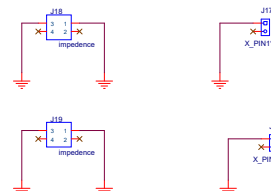
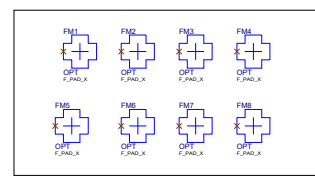
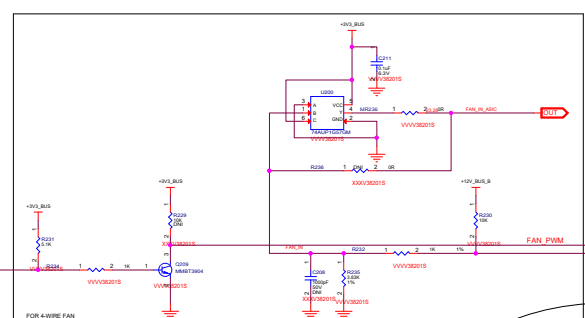
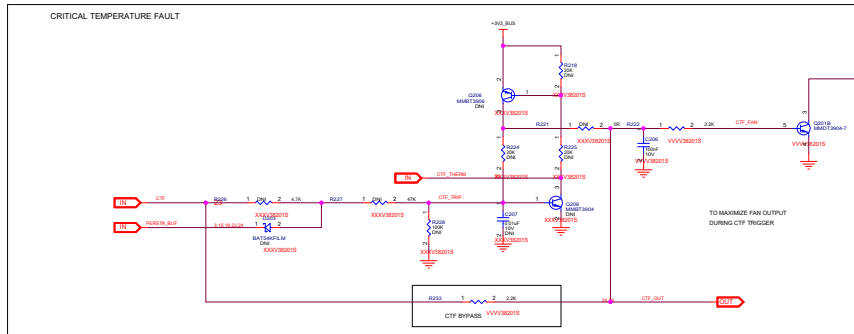
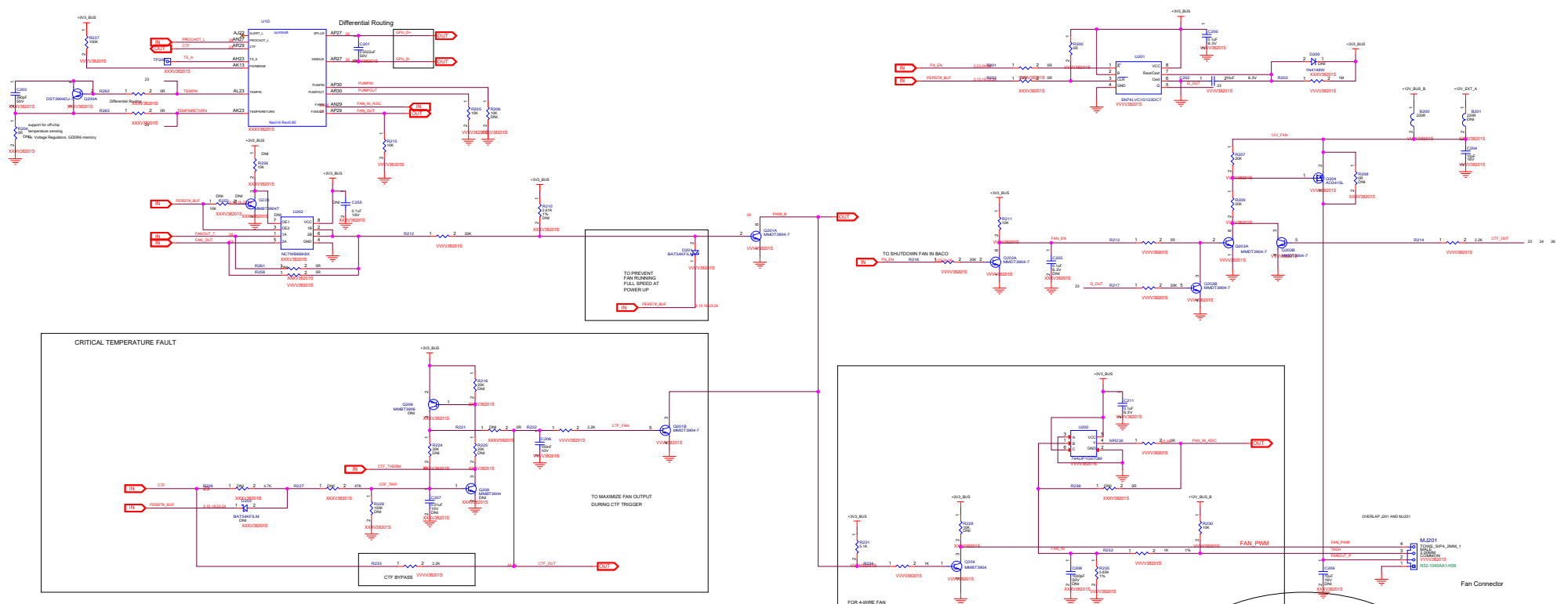
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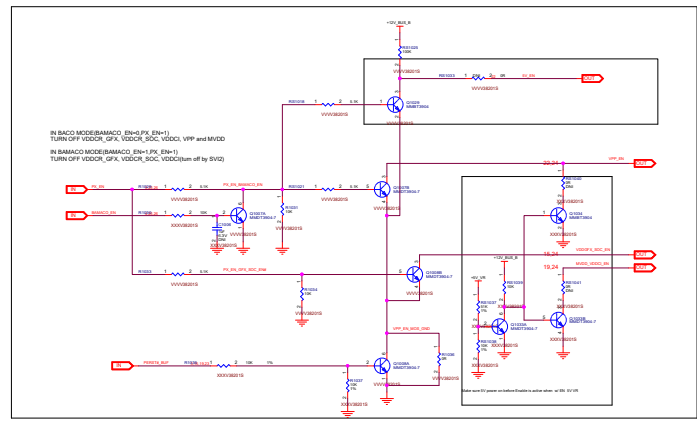
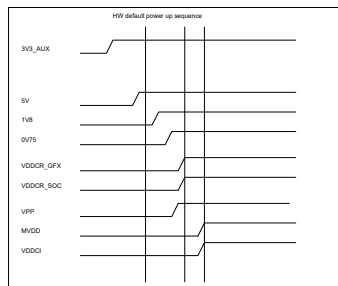
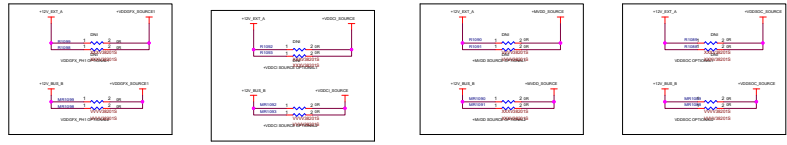
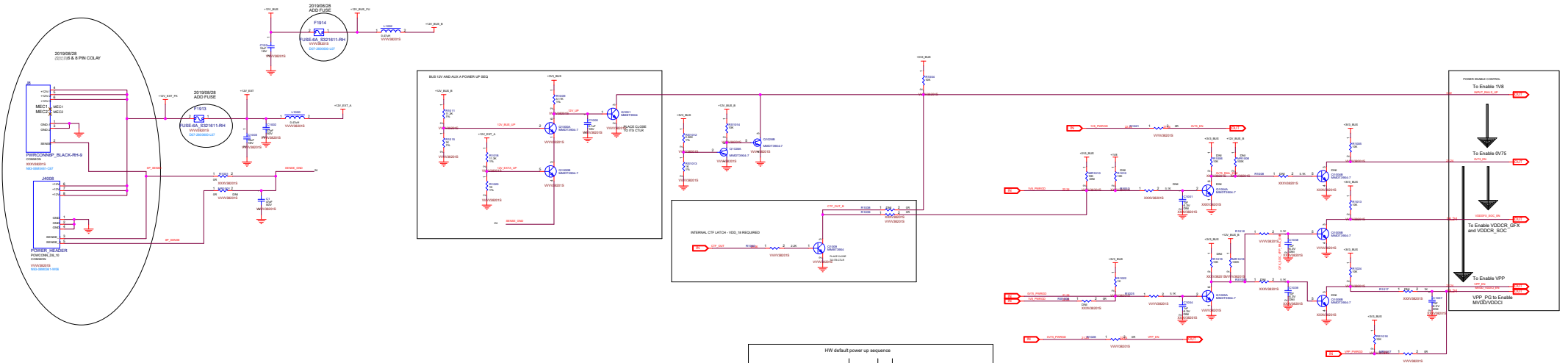
5V REGULATOR

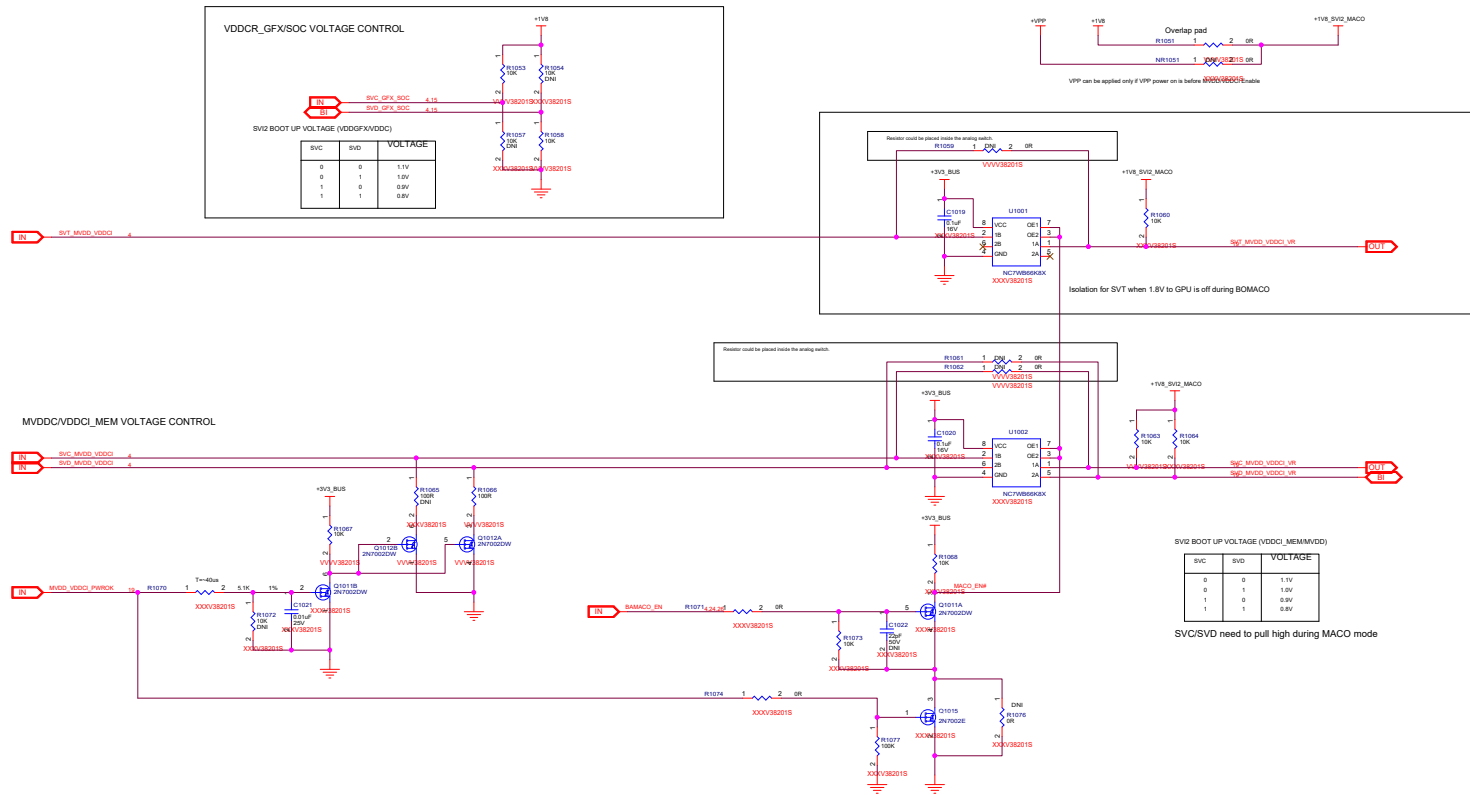


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Fan Connector
 HEADER IS
 #PINS NOT FOLLOW
 2.54MM SPACING AS
 #PIN SPECIFICATION





(29) DEBUG CIRCUIT

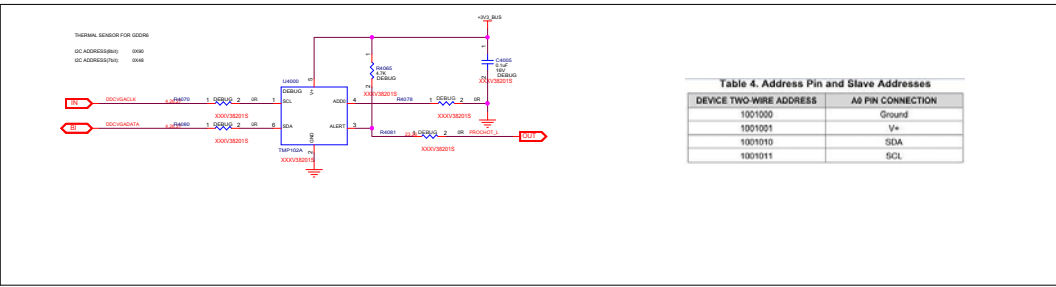
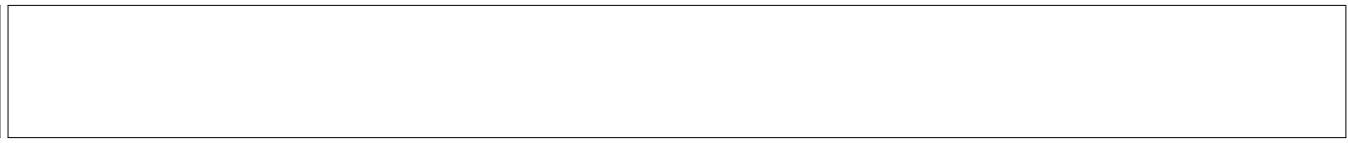
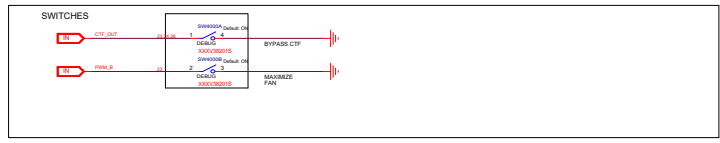
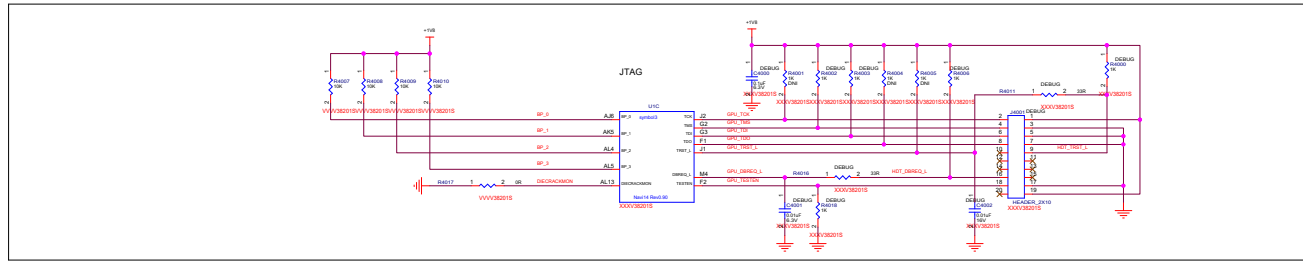


Table 4. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

