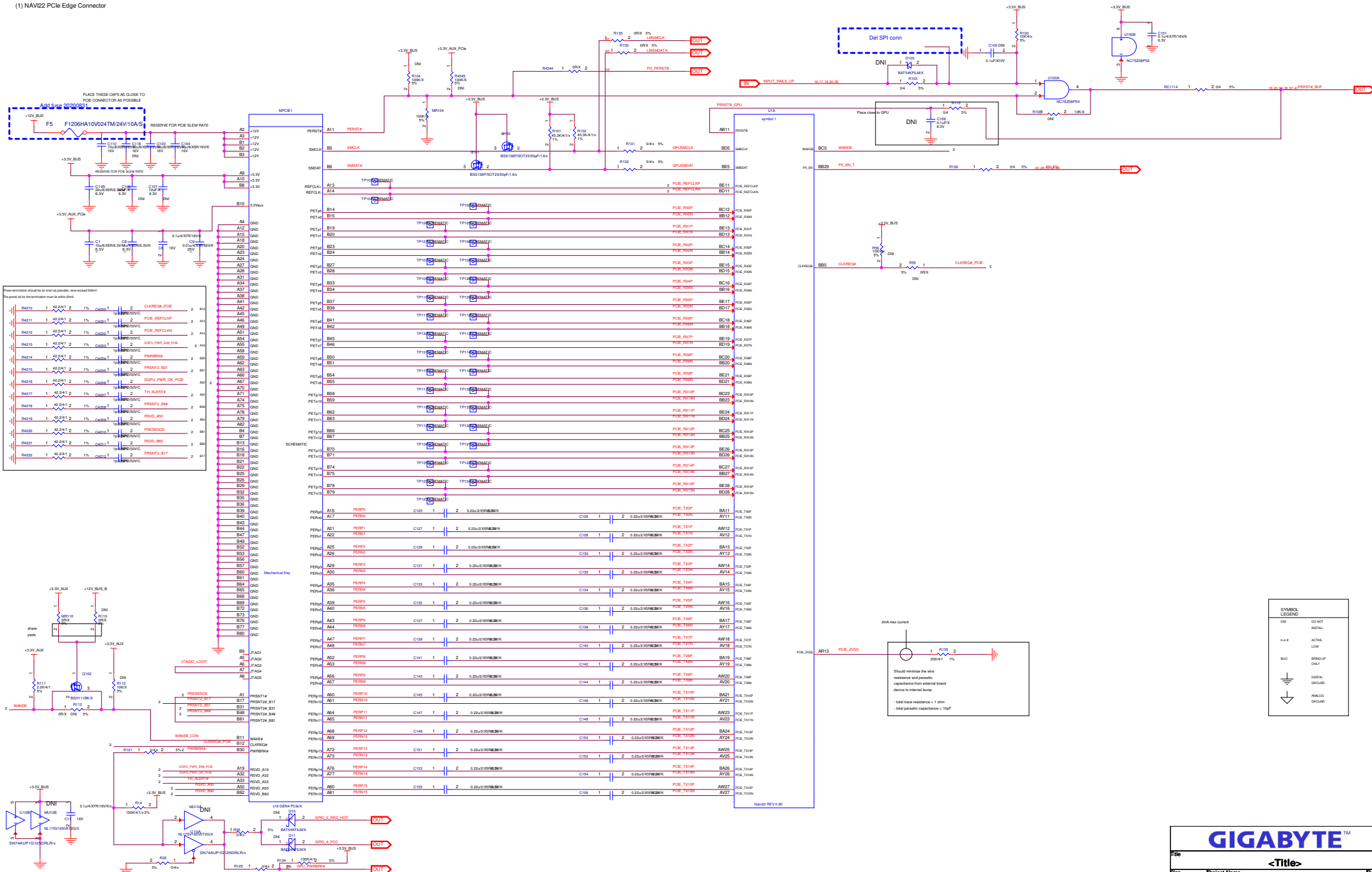


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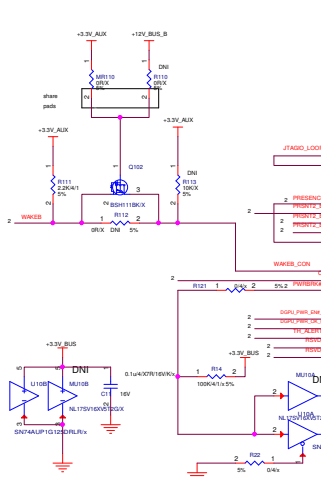
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	VDDCR_GFX PHASES 6
2	NAVI22 PCIe Interface	27	VDDCR_SOC_PHASE 1 and 2
3	NAVI22 GPIOs	28	MVDD_VDDCI CONTROLLER
4	NAVI22 XTAL	29	REG MVDD
5	NAVI22 MEM CHAB	30	REG VDDCI
6	NAVI22 MEM CHCD	31	SMALL RAIL LDO
7	NAVI22 MEM CHEF	32	NAVI22 DECAPS
8	GDDR6 MEM CHAB	33	NAVI22 POWER
9	GDDR6 MEM CHCD	34	NAVI22 GND
10	GDDR6 MEM CHEF	35	POWER MANAGEMENT
11	NAVI22 TMDPAB - USB-C/DP	36	SVi2 & BAMACO
12	NAVI22 TMDPCD- HDMI	37	MECHANICAL & THERMAL
13	NAVI22 TMDPEF - DP/DP	38	RADEON Lightbar
14	NAVI22 TMDPA	39	PI Debug
15	NAVI22 USB	40	DEBUG
16	PD Controller	41	BLOCK DIAGRAM
17	USB-C PORT 1& DP	42	REVISION HISTORY
18	3.3V_AUX		
19	USB_5V_1.8V_0.75V		
20	MODS CONTROL & POWER		
21	REG_5V_BUCK		
22	VDDGFX_SOC CONTROLLER		
23	VDDCR_GFX PHASES 2 and 5		
24	VDDCR_GFX PHASES 1 and 4		
25	VDDCR_GFX PHASES 3 and 7		



These termination should be as short as possible, then nearest 0805

Be good via for the termination must be within 0.5mm

RA210	1	A2-24V1	2	1%	CH02-1	2	CLAMPK_PCIE	2	80
RA211	1	A2-24V1	2	1%	CH02-1	2	PCIE_REFCLKP	2	81
RA212	1	A2-24V1	2	1%	CH02-1	2	PCIE_REFCLKN	2	82
RA213	1	A2-24V1	2	1%	CH02-1	2	GPU_PWR_SML_PCIE	2	83
RA214	1	A2-24V1	2	1%	CH02-1	2	PRESENCE	2	84
RA215	1	A2-24V1	2	1%	CH02-1	2	PRINT2_B01	2	85
RA216	1	A2-24V1	2	1%	CH02-1	2	GPU_PWR_OK_PCIE	2	86
RA217	1	A2-24V1	2	1%	CH02-1	2	TH_ALERT#	2	87
RA218	1	A2-24V1	2	1%	CH02-1	2	PRINT2_B02	2	88
RA219	1	A2-24V1	2	1%	CH02-1	2	PCIE_A00	2	89
RA220	1	A2-24V1	2	1%	CH02-1	2	PRESENCE	2	90
RA221	1	A2-24V1	2	1%	CH02-1	2	PRINT2_B01	2	91
RA222	1	A2-24V1	2	1%	CH02-1	2	PRINT2_B02	2	92

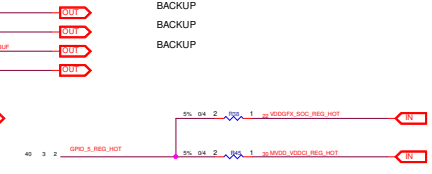
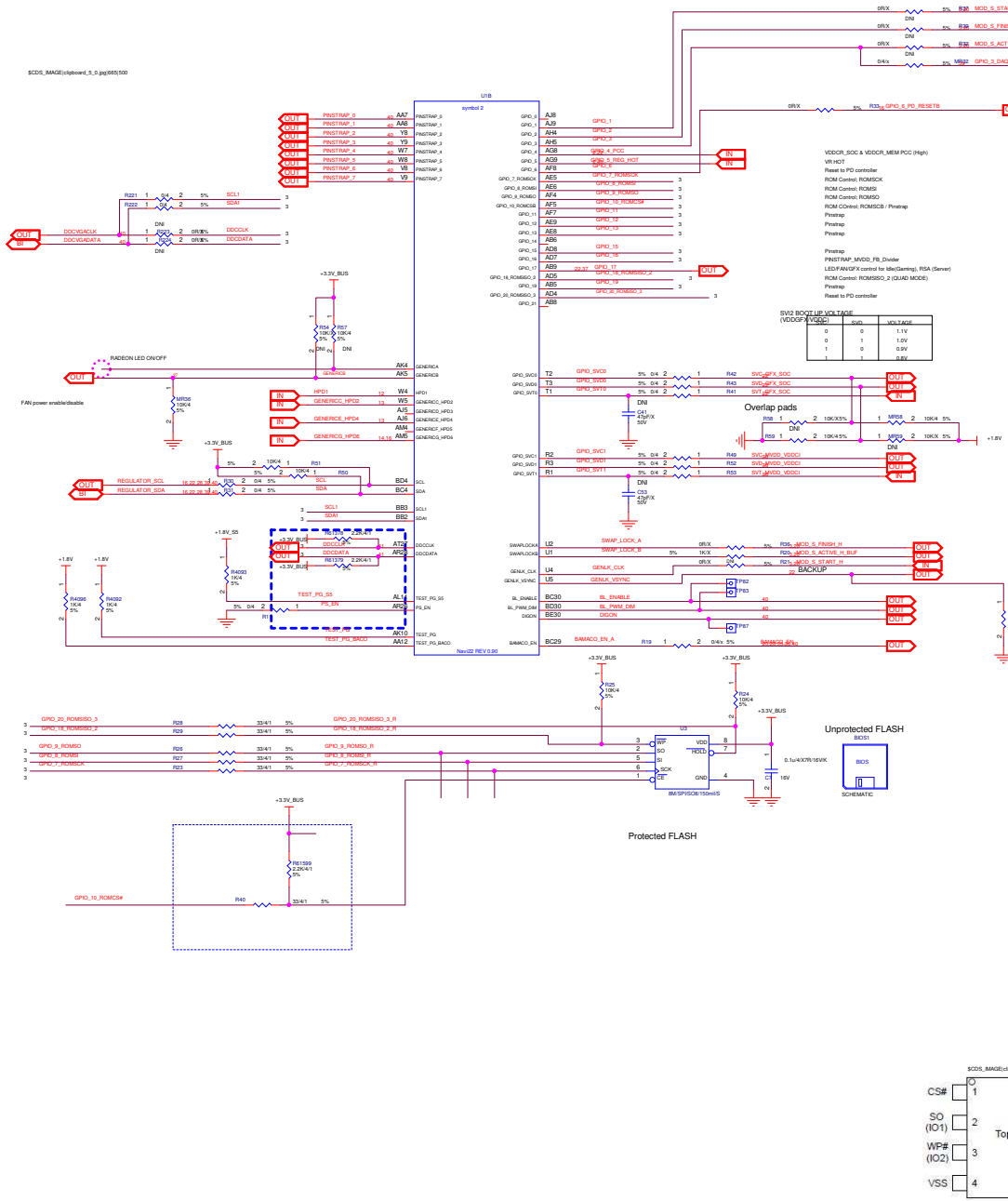


SYMBOL LEGEND	
DNI	DONT
METAL	METAL
100#	ACTIVE
LOW	LOW
BUD	BINGUP ONLY
	DATIN
	GROUND
	GROUND
	GROUND

20A max current

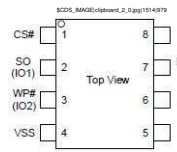
Should minimize the wire resistance and parasitic capacitance from external board device to internal bump.

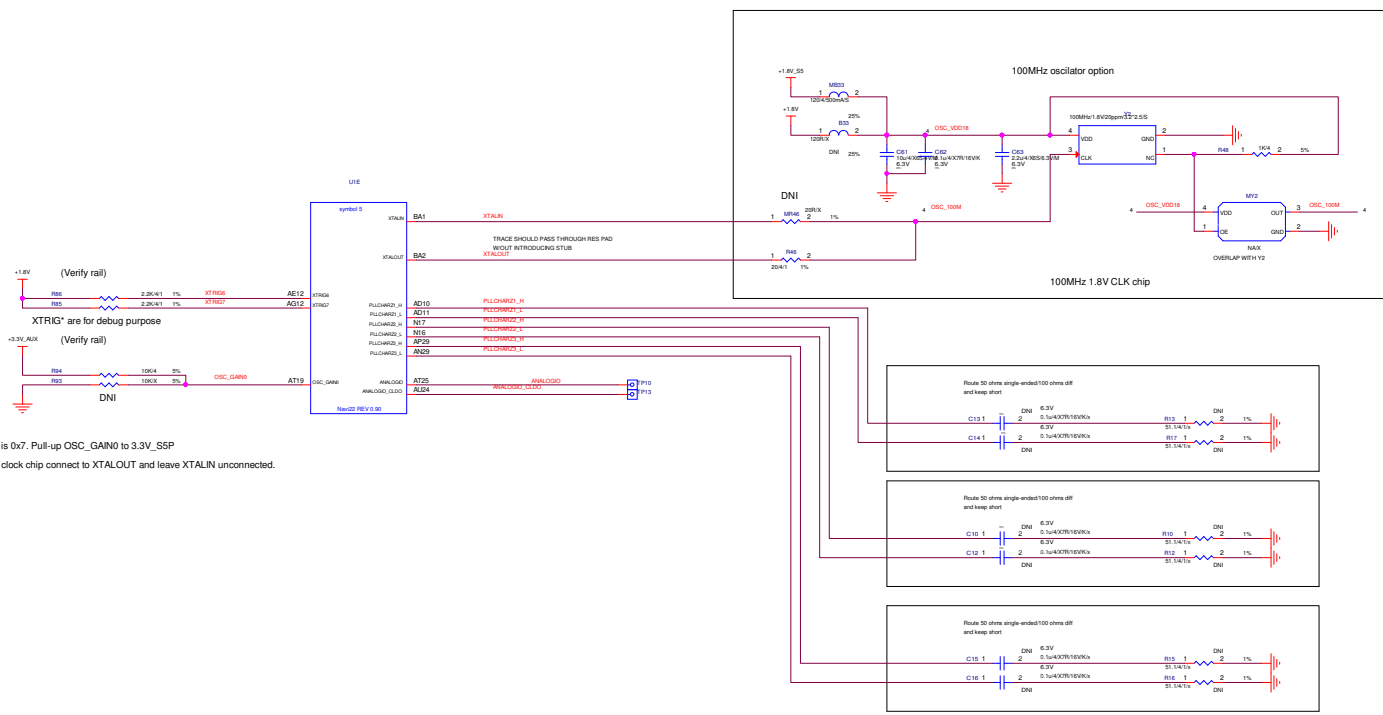
- total trace resistance < 1 ohm
- total parasitic capacitance < 10pF



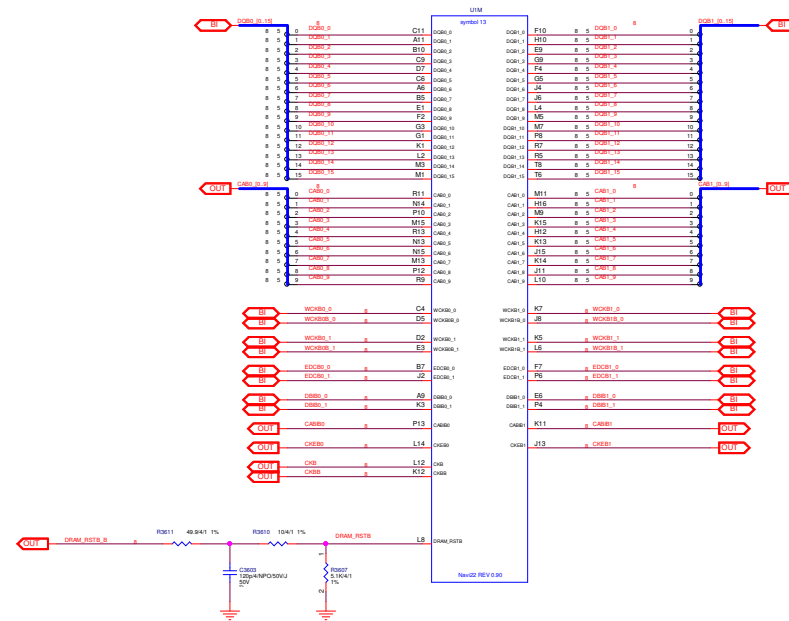
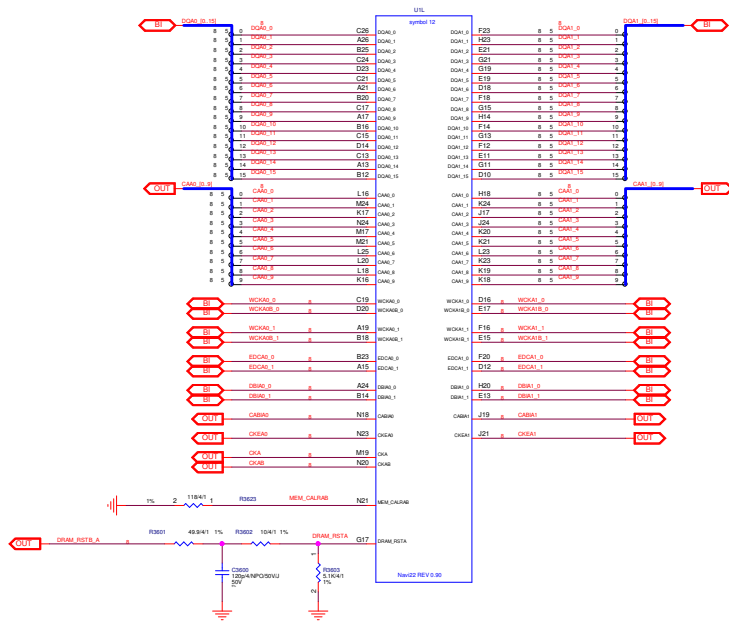
Note: Internal PU/PD at GPIO pad is 20kOhm in 14nm design spec

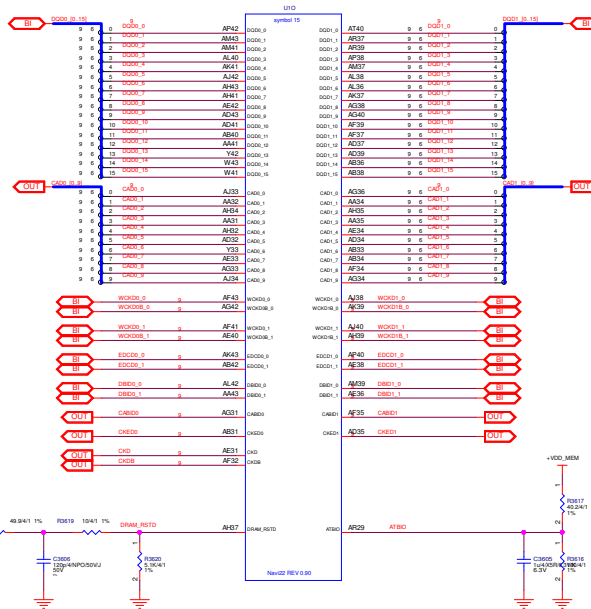
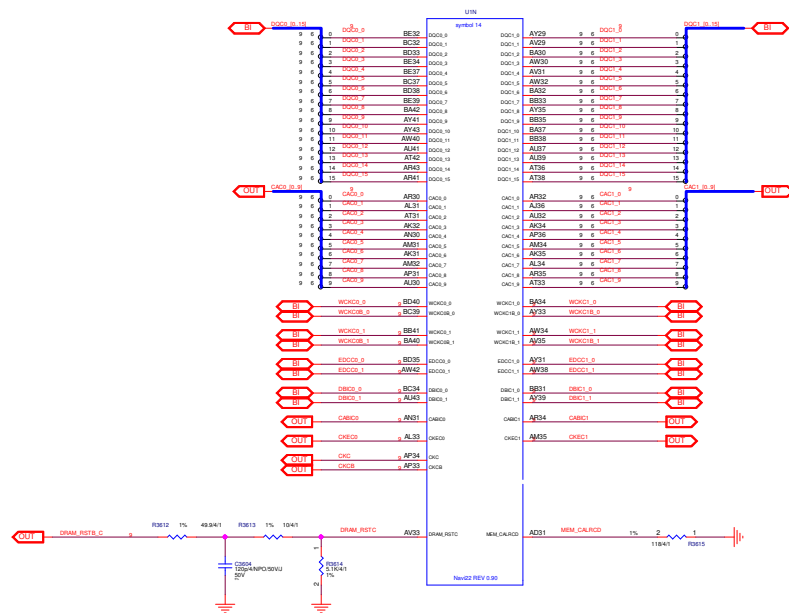
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN4 supported 1: PCIe GEN4 not supported
	0	PNSTRAP_BIF_CLK_PM_EN 0: CLARESPD power management capability is disabled 1: CLARESPD power management capability is enabled
	0	PNSTRAP_BIF_LC_TX_SWING 0: MDA controller capability is enabled 1: The device won't be recognized as the system's VGA controller
DCE	0	PNSTRAP_BIF_VGA_DIS 0: MDA controller capability is enabled 1: The device won't be recognized as the system's VGA controller
	0	PNSTRAP_AUD_PORT_CONW[2:0] Number of audio-capable display outputs
	0	PNSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if display is detected 3: Audio for DisplayPort and native HDMI
	0	PNSTRAP_BOARD_CONFIG[2:0] LED Fan/GFX control for idle power
Platform	0	PNSTRAP_MVDD_BOOT_VID_CONFIG 0: Pullup-1 without feedback divider 1: Pullup-1 with feedback divider enabled
	0	PNSTRAP_SMBUS_ADDR 0: 0x40 1: 0x48
SMU	0	PNSTRAP_ROM_CONFIG[2:0] 101
	1	PNSTRAP_ROM_CONFIG[2:0] 101
	1	PNSTRAP_ROM_CONFIG[2:0] 101
DNI	0	PNSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device
	1	PNSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

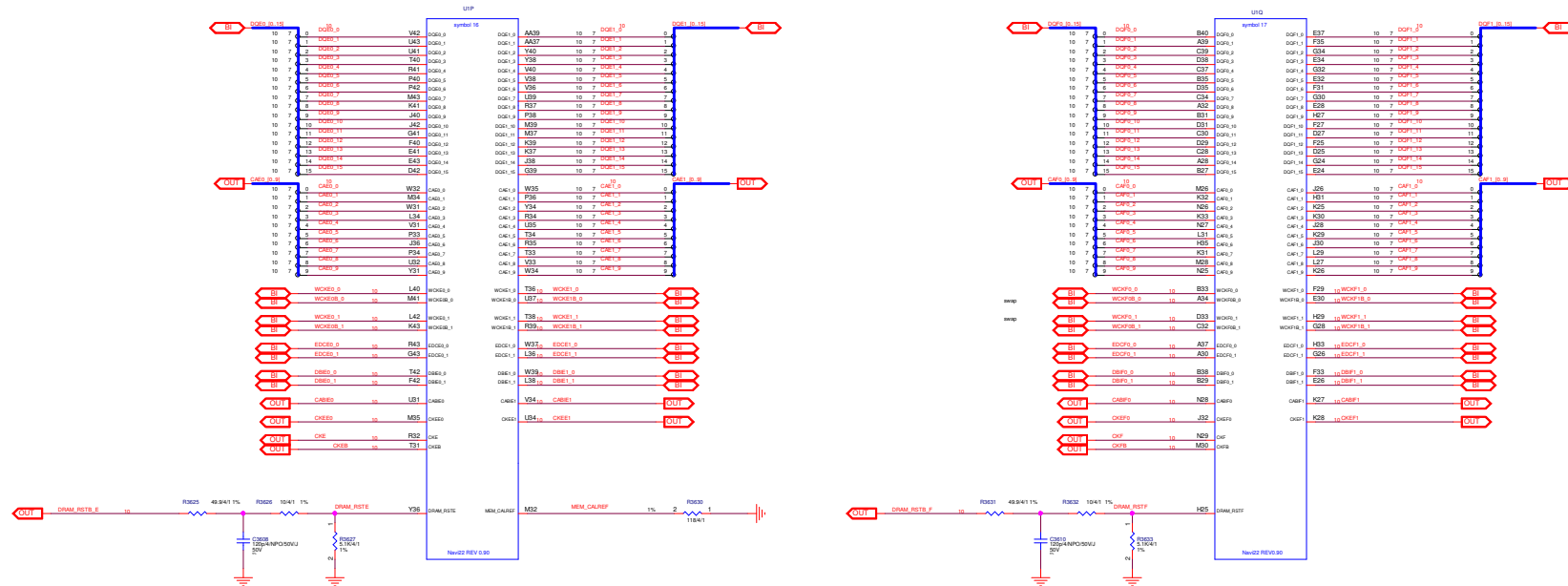


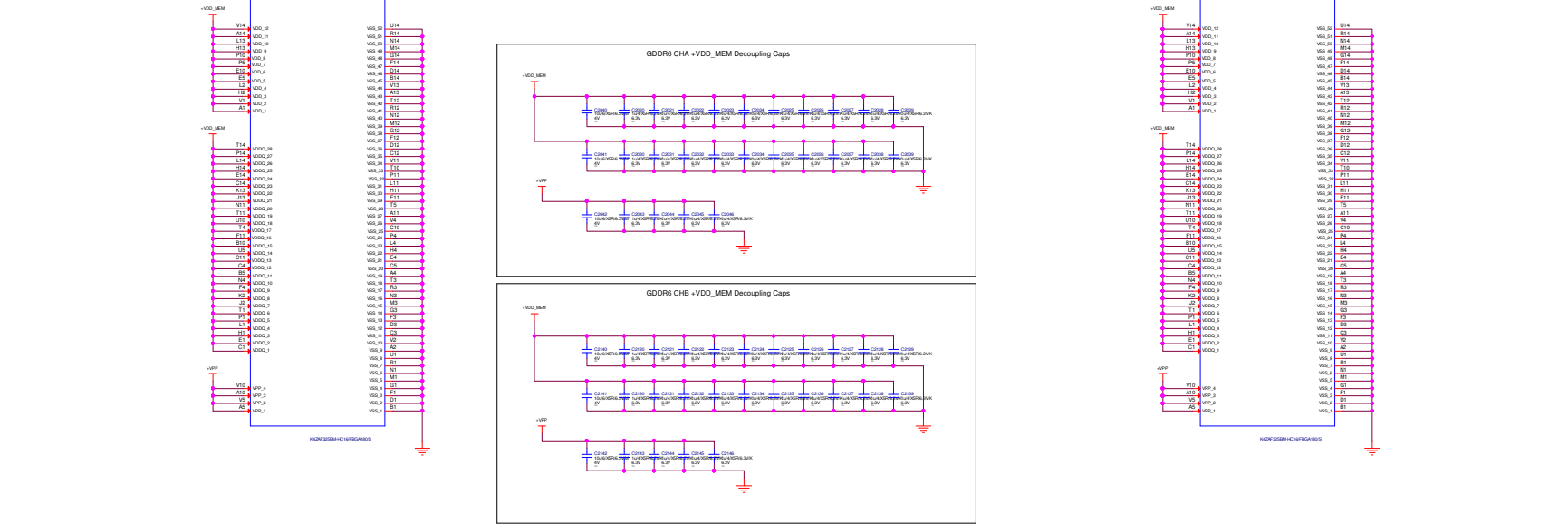
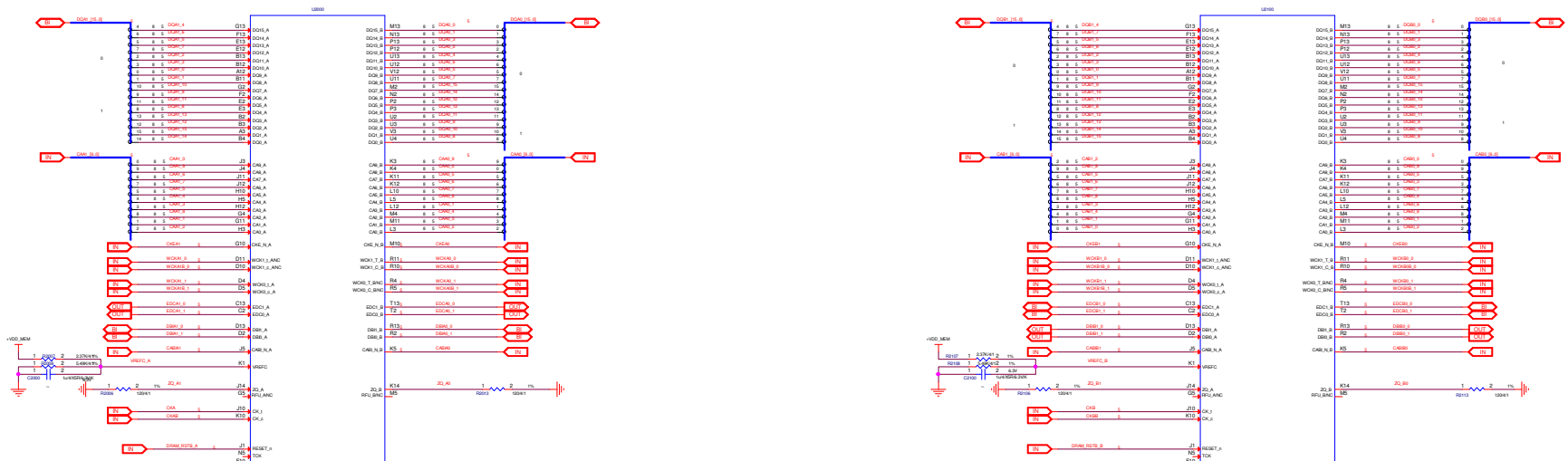


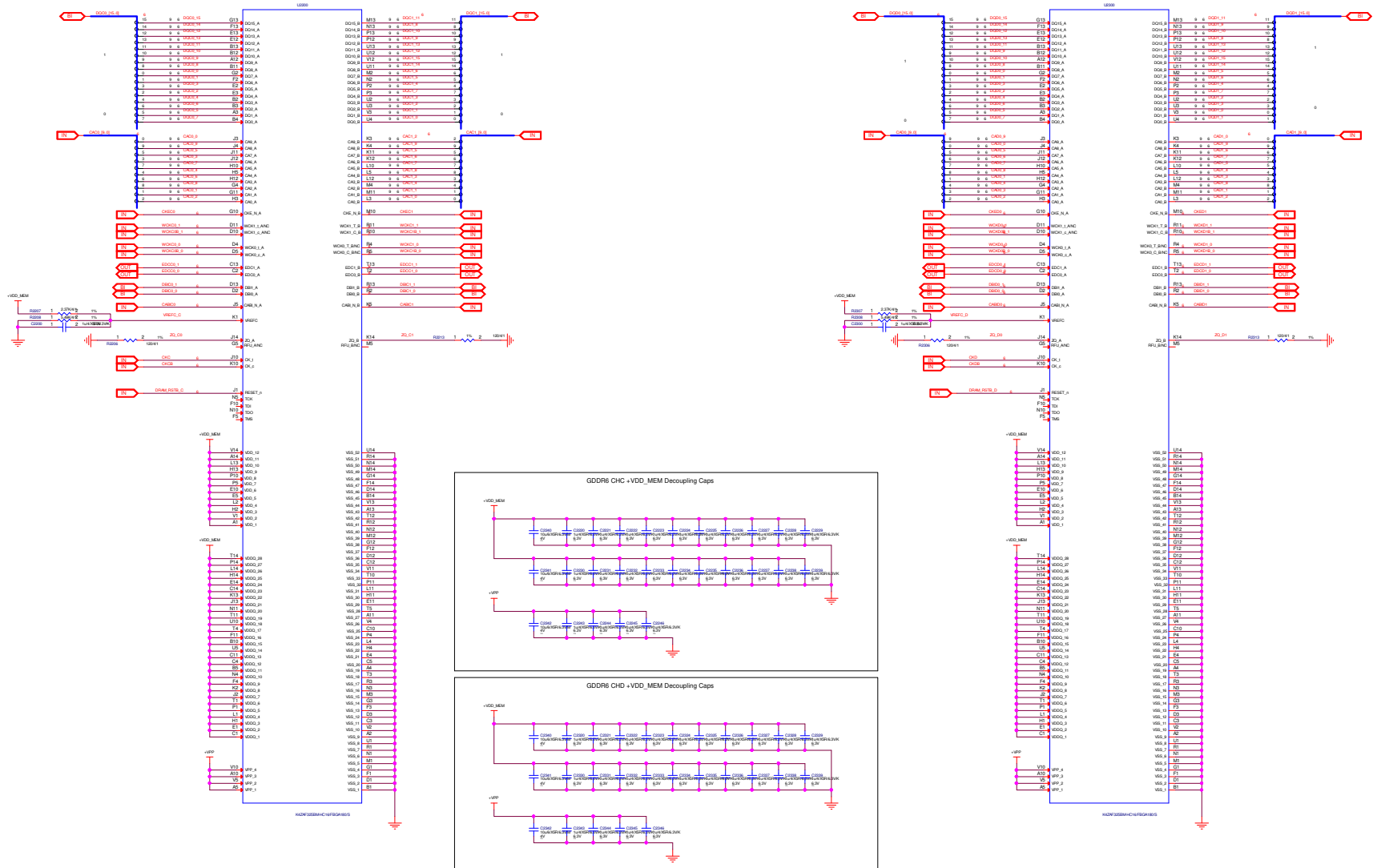
Default OSC_GAIN is 0x7. Pull-up OSC_GAIN0 to 3.3V_SSP
 When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

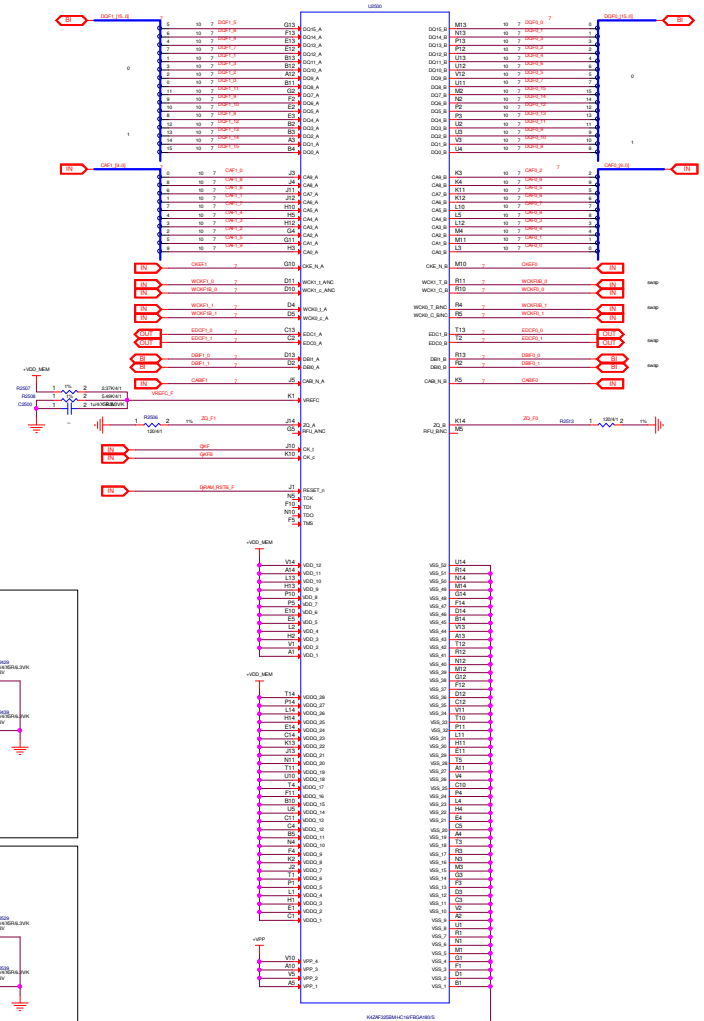
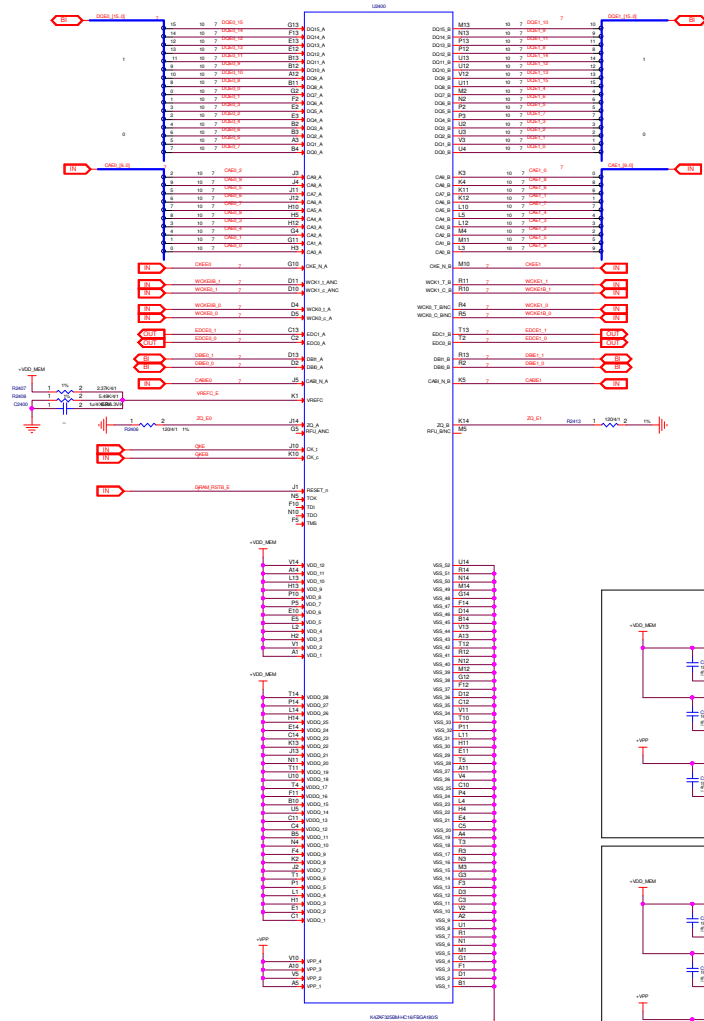


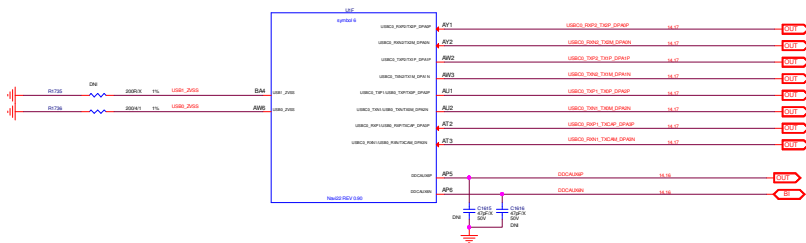
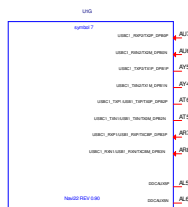






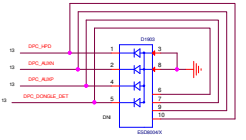
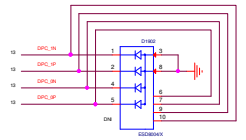
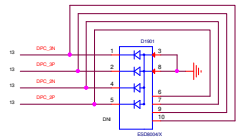
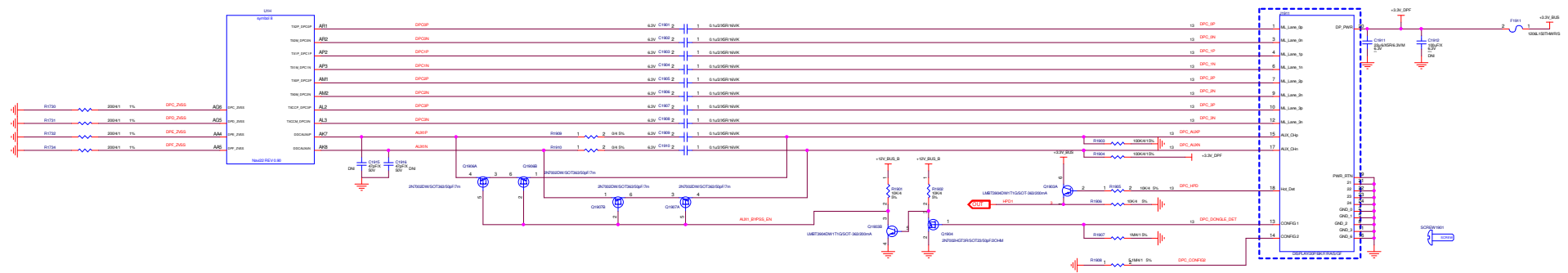


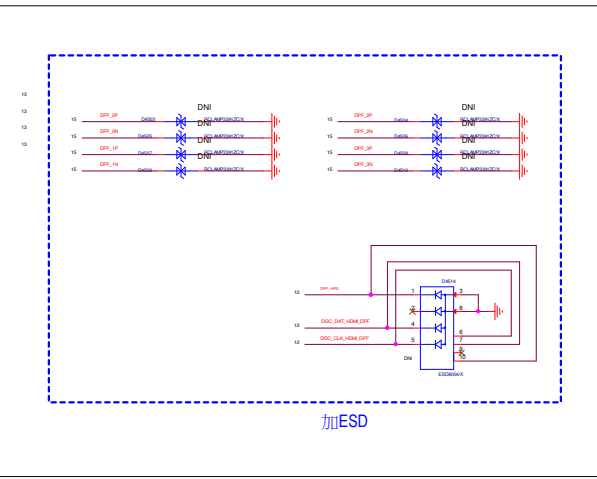
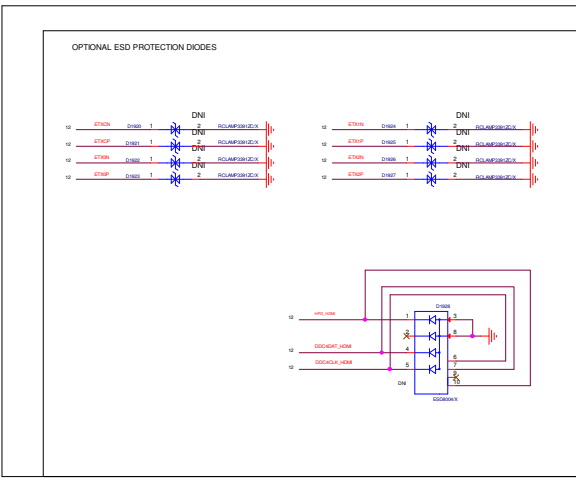
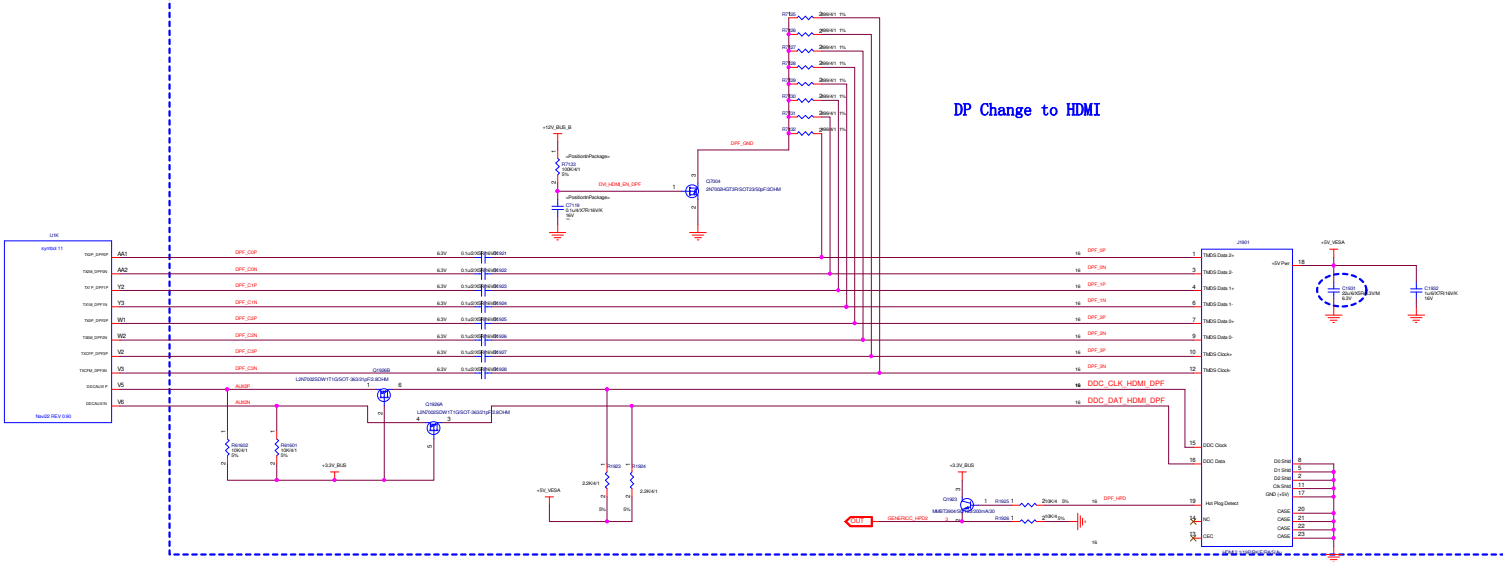
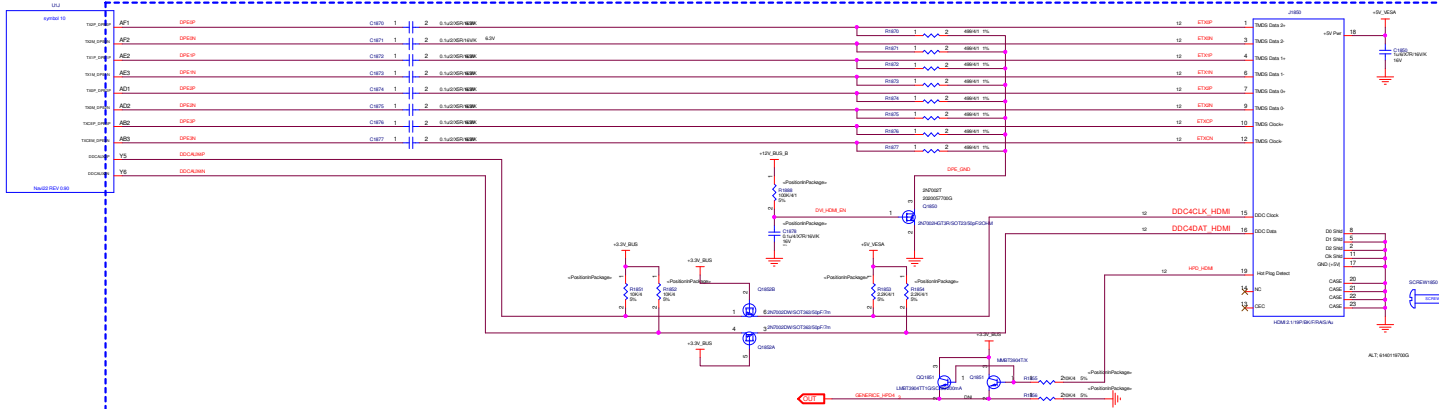


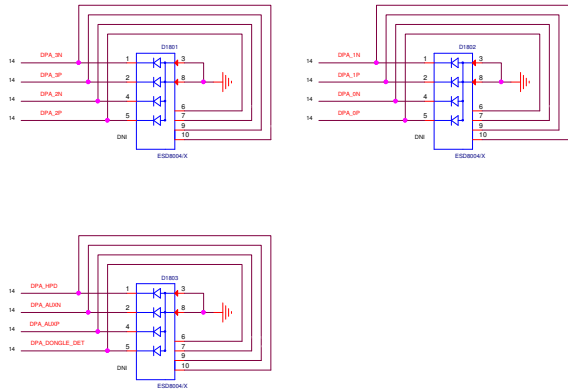
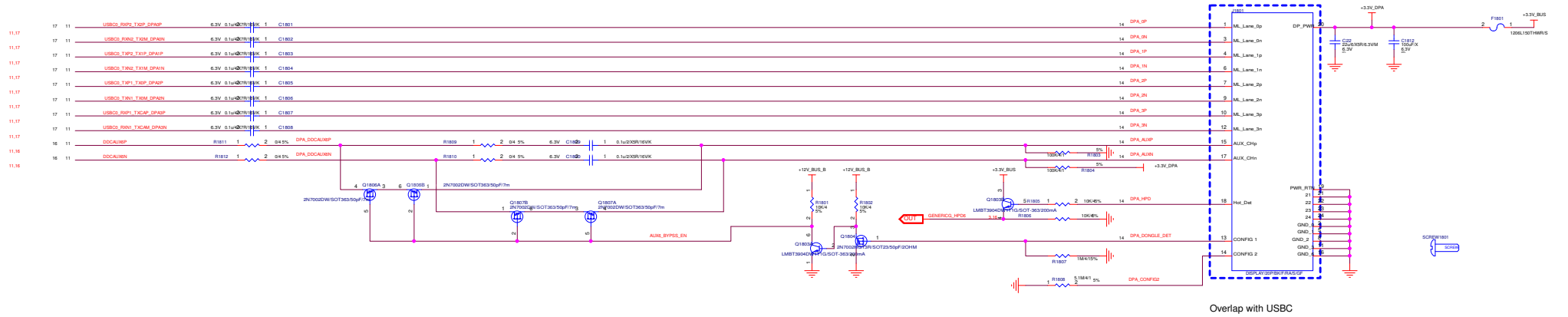


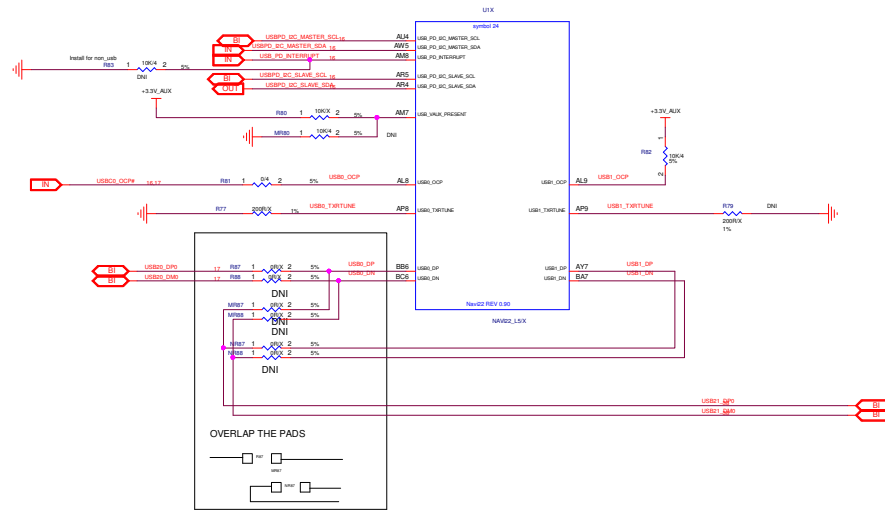
NAVI22 TMDP C/D

REF	VALUE	DESCRIPTION
APR003	20K	TEMP_SENSOR
APR004	20K	TEMP_SENSOR
APR005	20K	TEMP_SENSOR
APR006	20K	TEMP_SENSOR
APR007	20K	TEMP_SENSOR
APR008	20K	TEMP_SENSOR
APR009	20K	TEMP_SENSOR
APR010	20K	TEMP_SENSOR
APR011	20K	TEMP_SENSOR
APR012	20K	TEMP_SENSOR
APR013	20K	TEMP_SENSOR
APR014	20K	TEMP_SENSOR
APR015	20K	TEMP_SENSOR
APR016	20K	TEMP_SENSOR
APR017	20K	TEMP_SENSOR
APR018	20K	TEMP_SENSOR
APR019	20K	TEMP_SENSOR
APR020	20K	TEMP_SENSOR

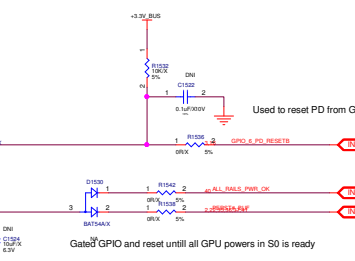
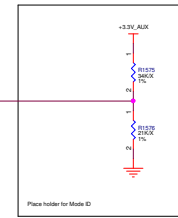
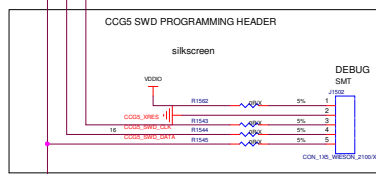
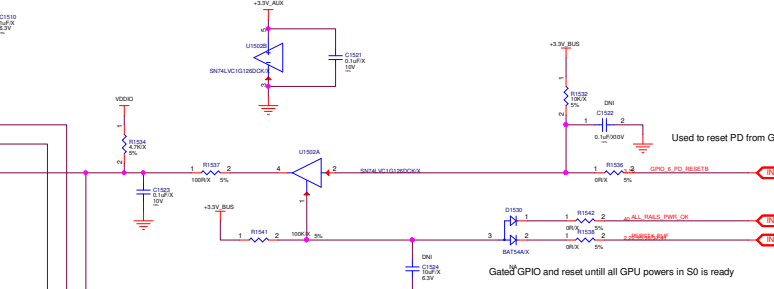
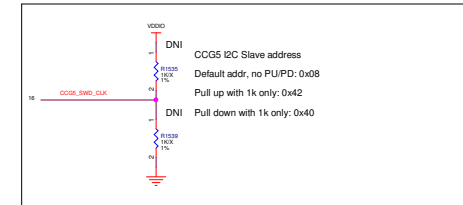
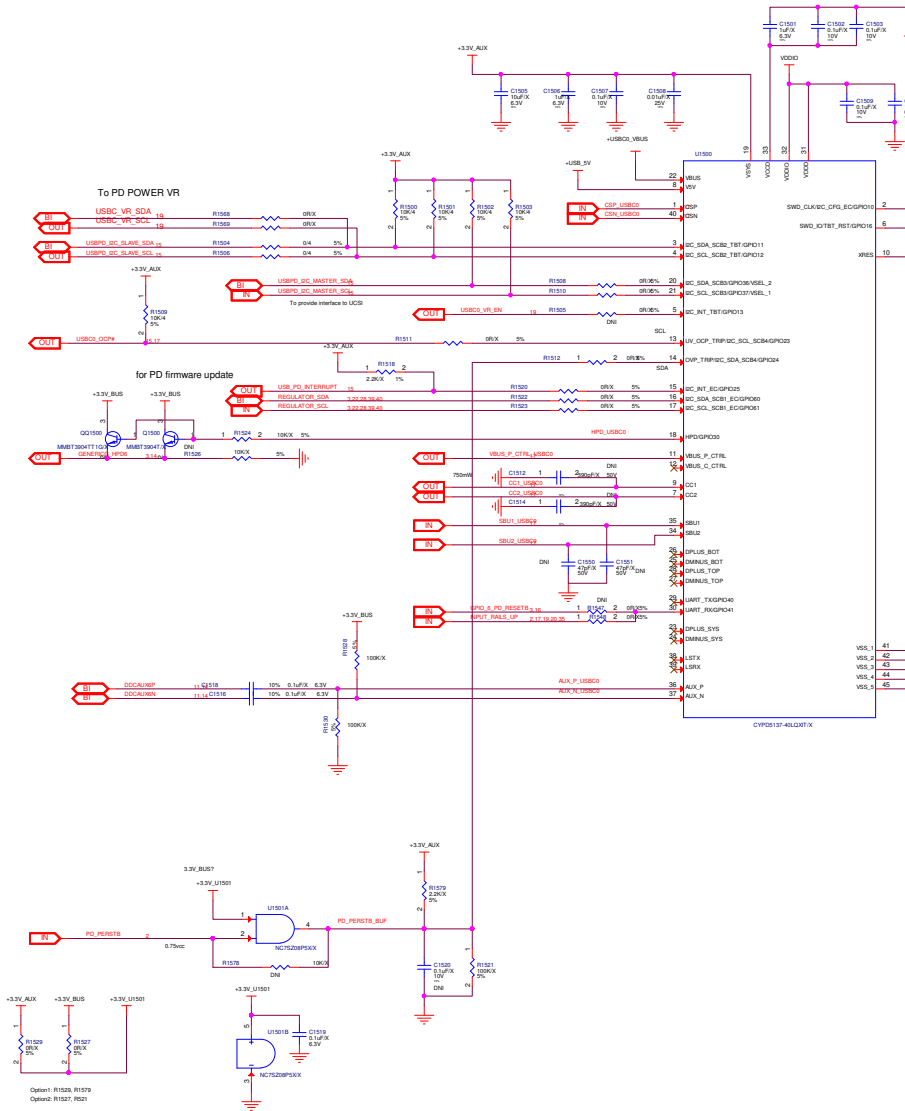




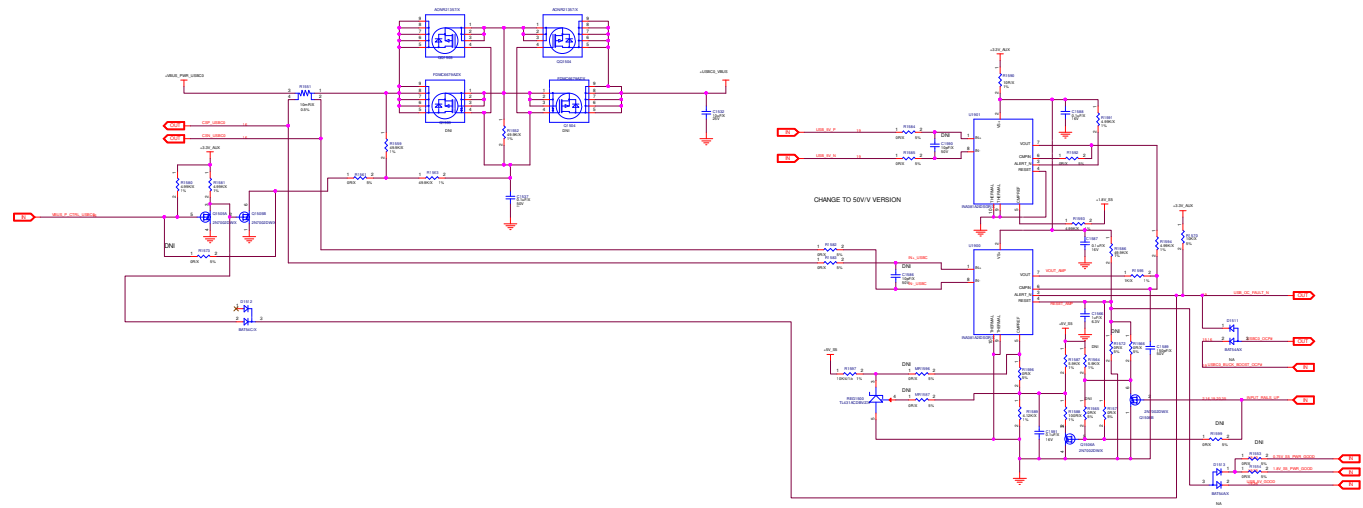




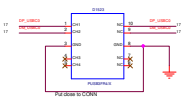
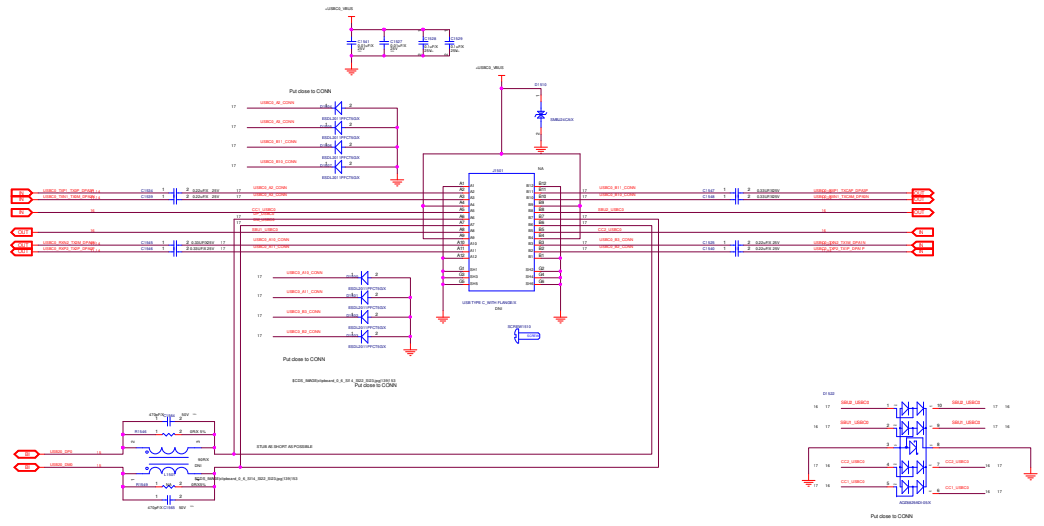
for GPU DP/USB COMBY PHY

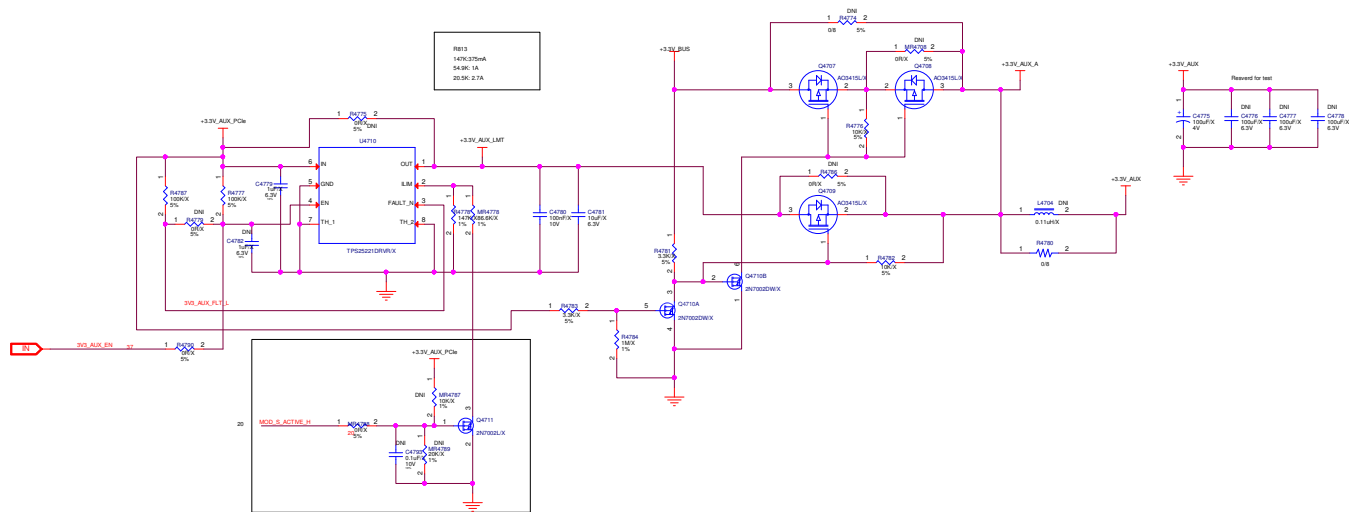


CCG5	Nav10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBDP_I2C_SLAVE_SDA/SCL	Nav10 MUX/PD_Regulator/re-driver
SCB3	USBDP_I2C_MASTER_SDA/SCL	

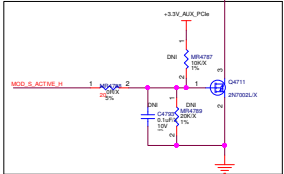


INPUT RAILS UP = 1 → 4.93A
 INPUT RAILS LP = 0 → 0.15A

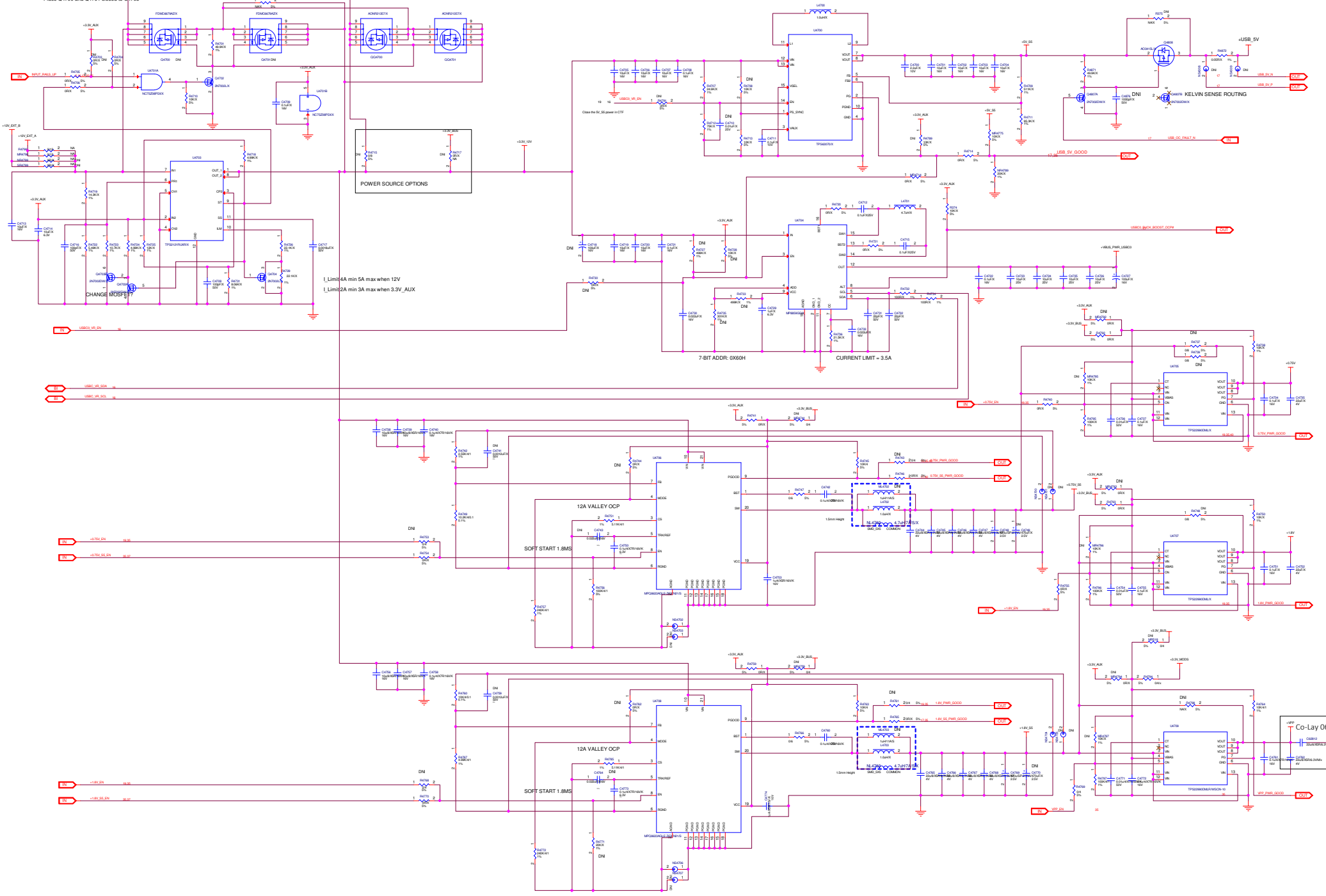




R13
147K:3750A
54.9K:1A
20.5K:27A

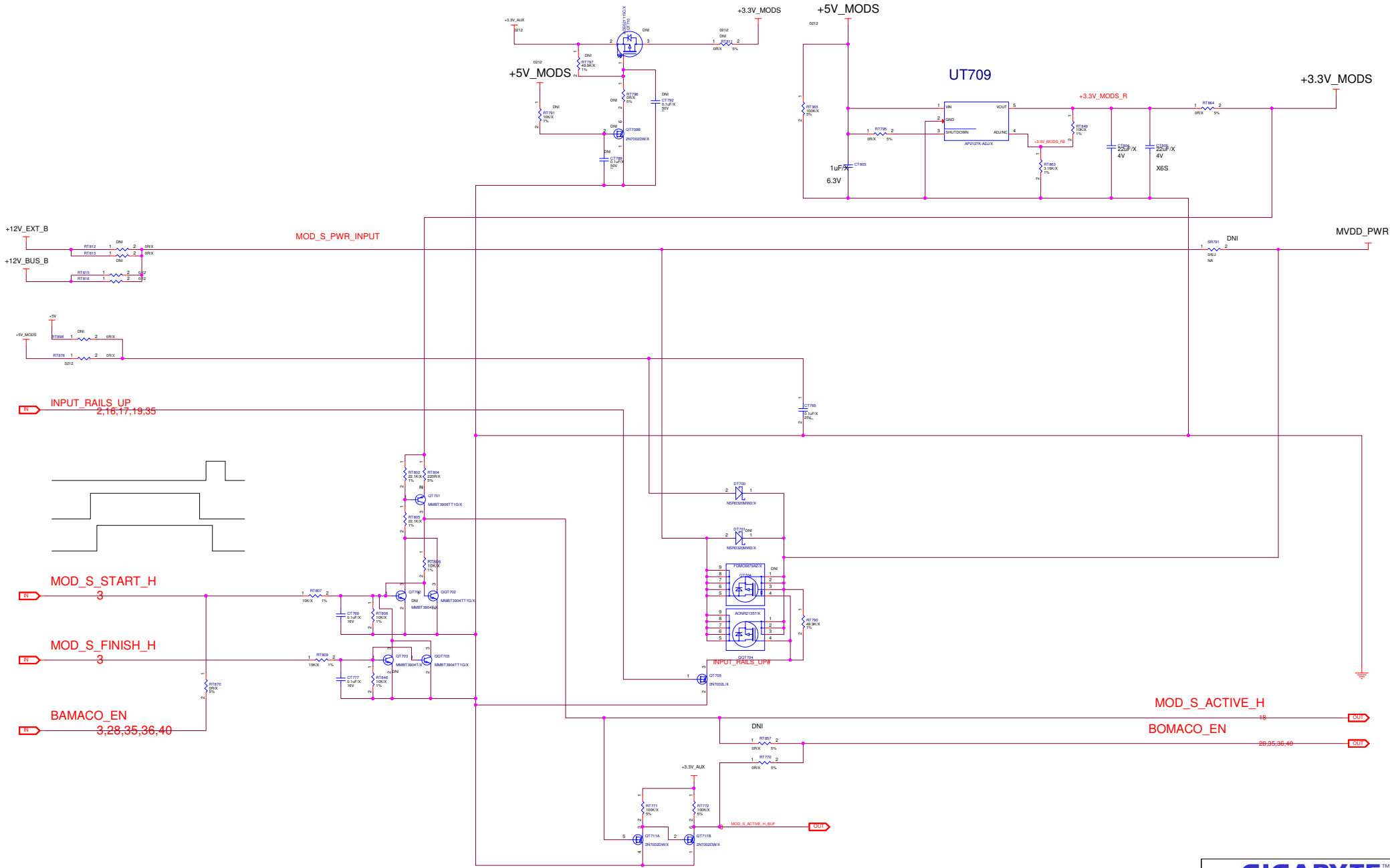


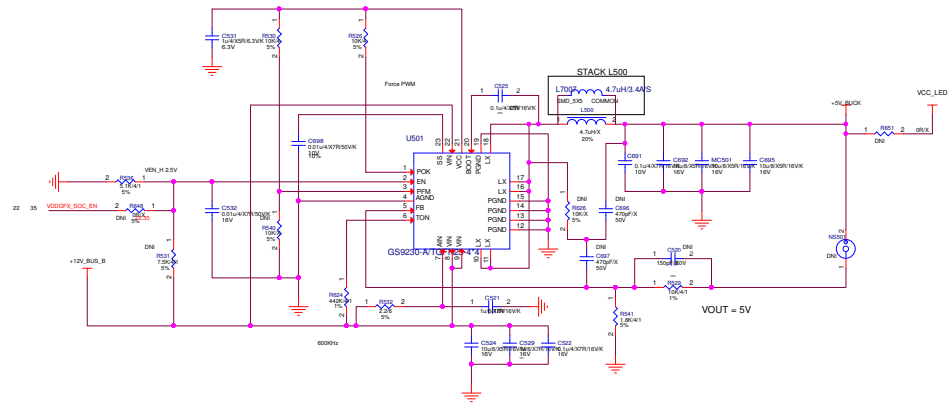
Place Q4700 and Q4701 closed to U1703

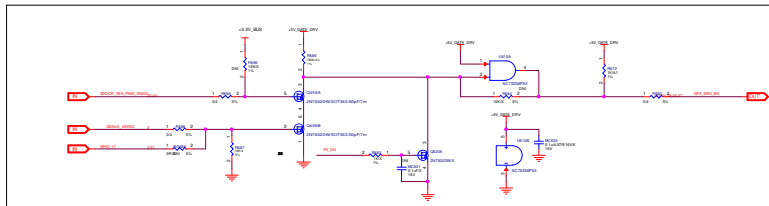
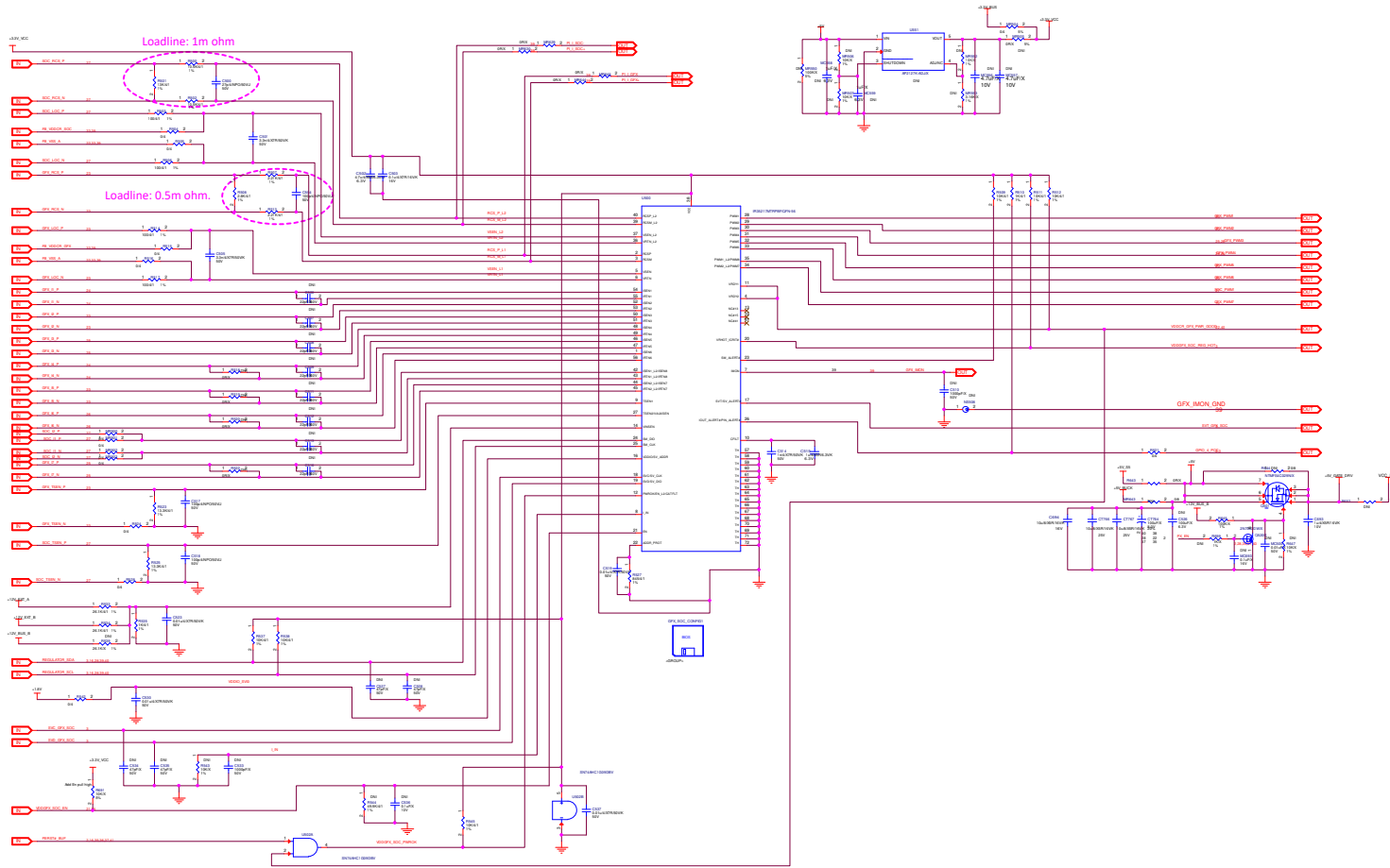


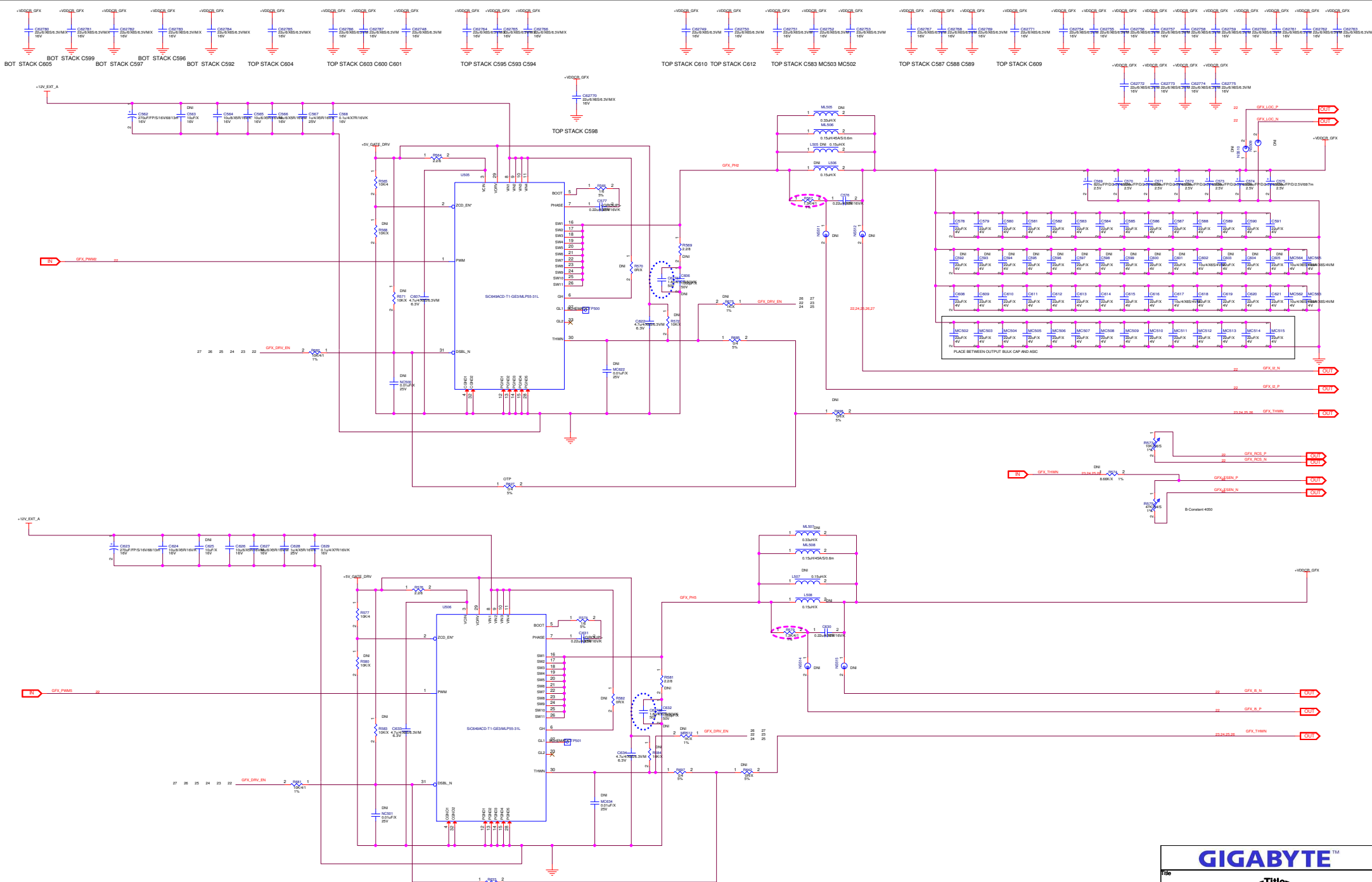
I_{Limit} 4A min 5A max when 12V
I_{Limit} 2A min 3A max when 3.3V_AUX

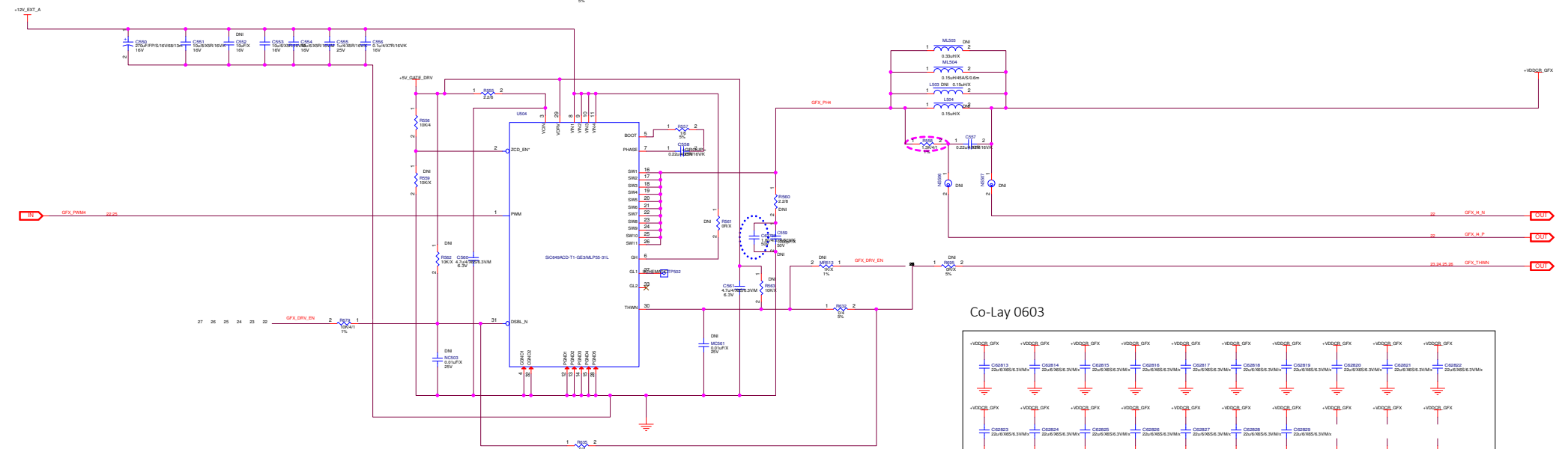
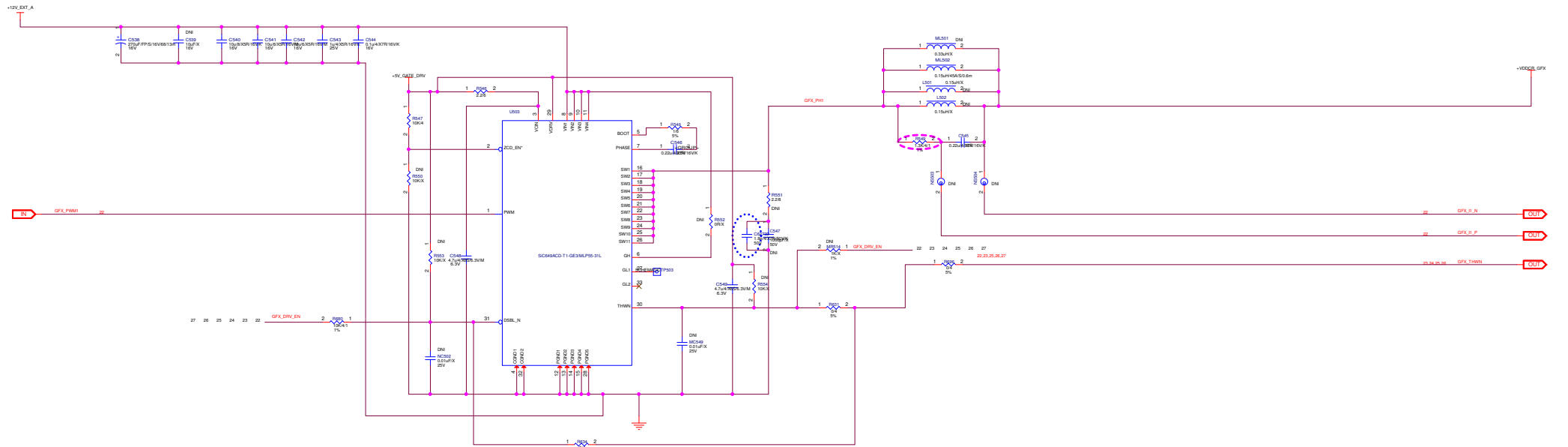
Co-Lay 0603



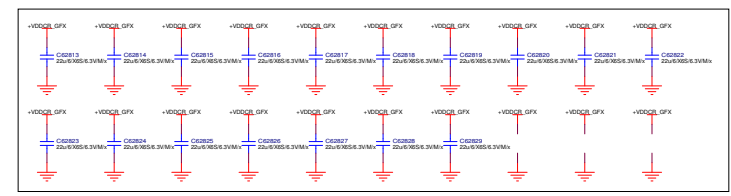


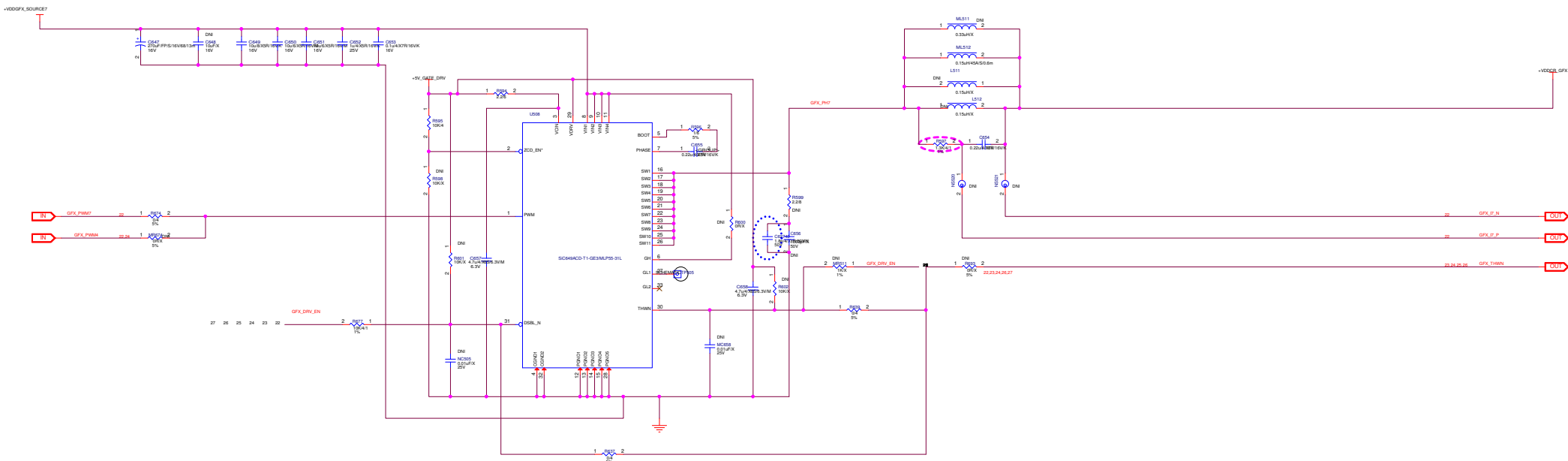
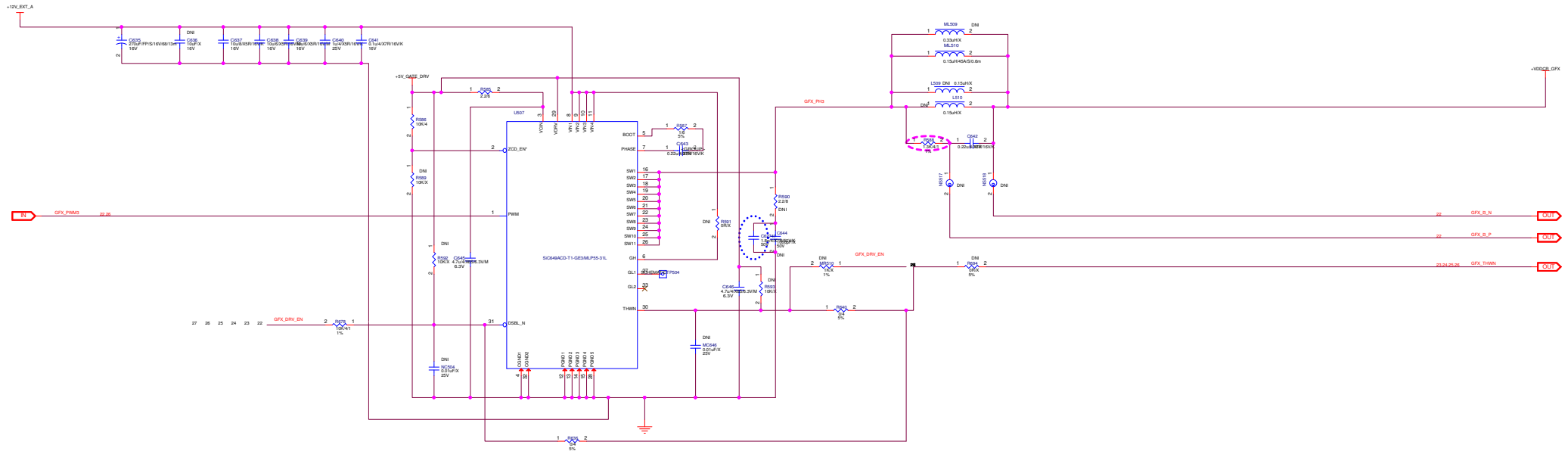






Co-Lay 0603

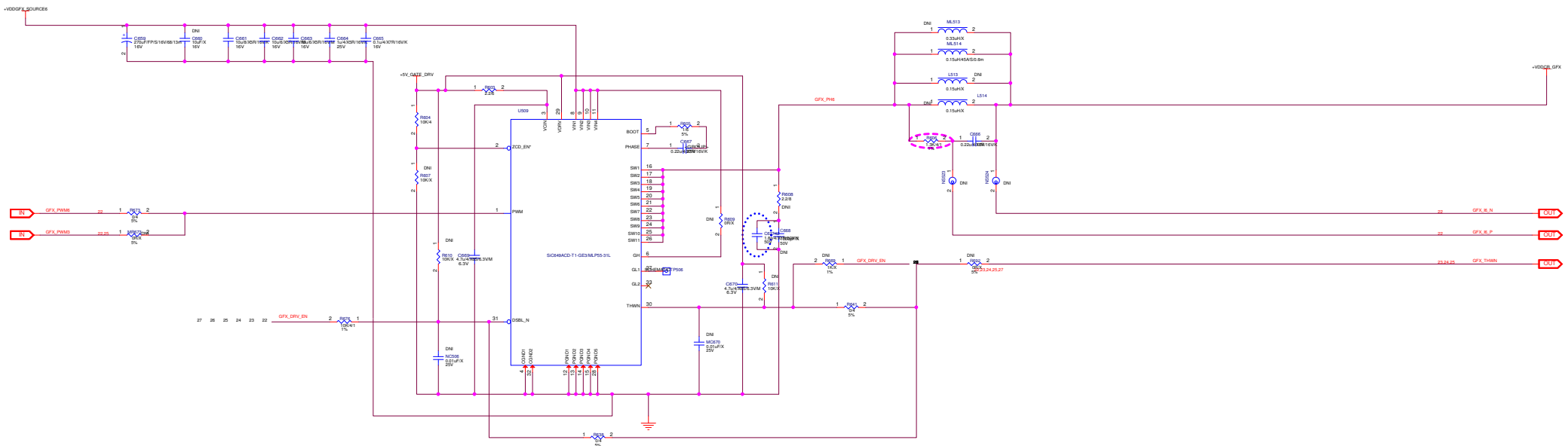


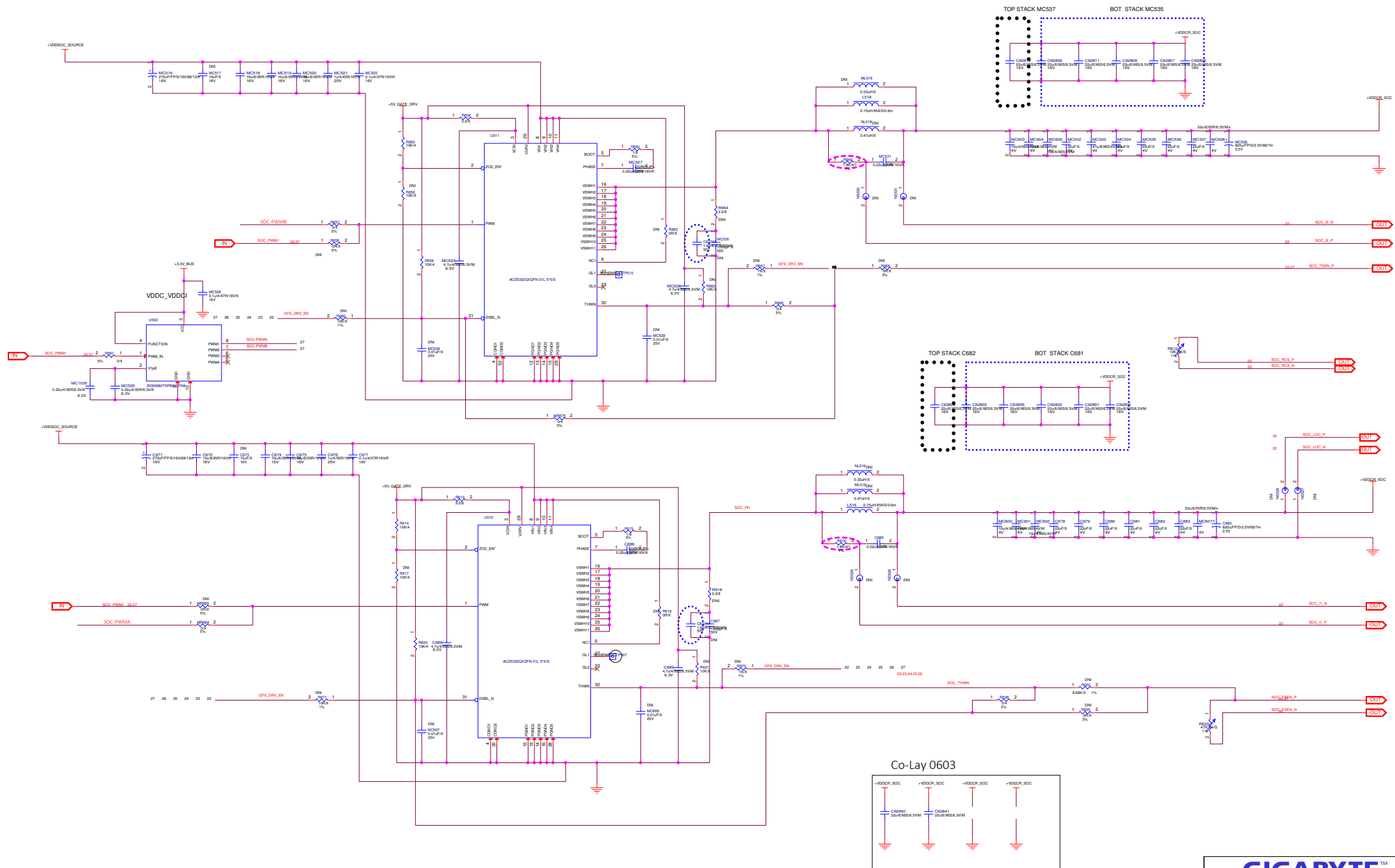


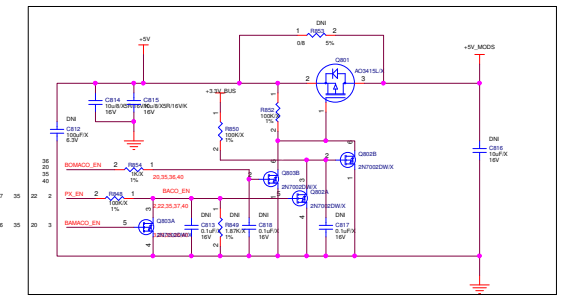
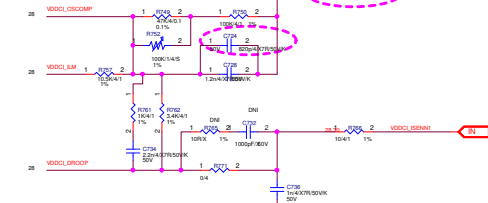
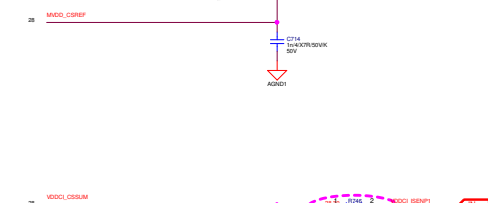
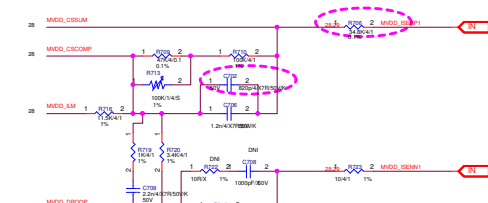
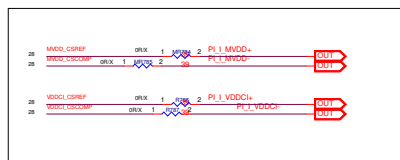
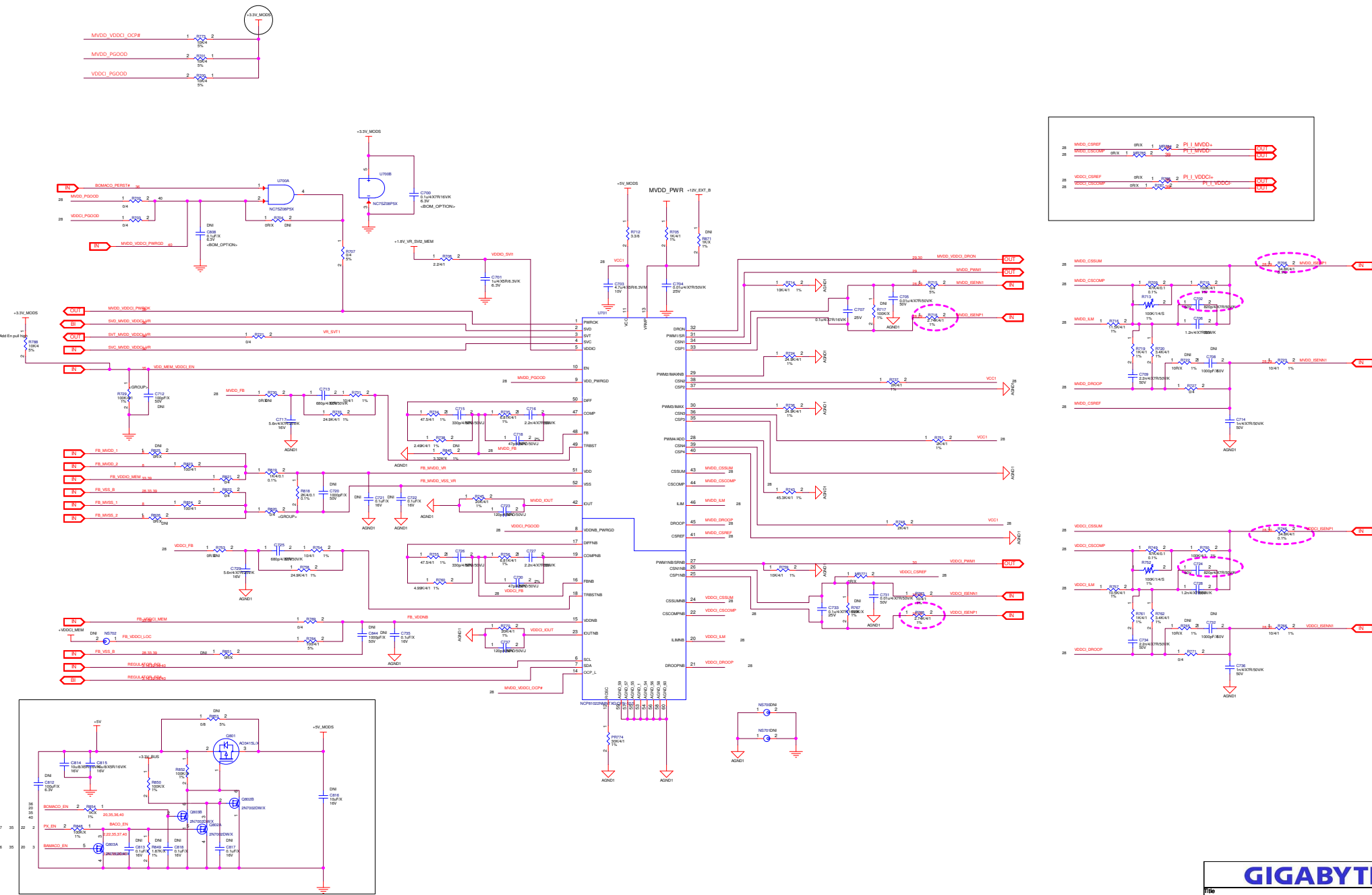
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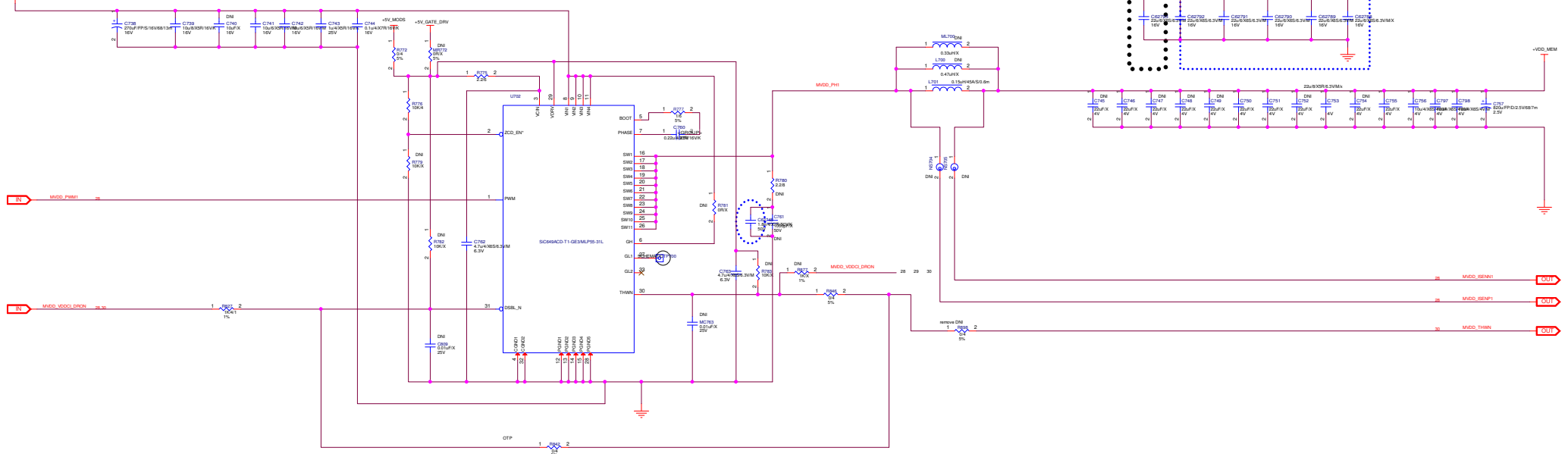
Date: Wednesday, January 06, 2021 Sheet 26 of 42



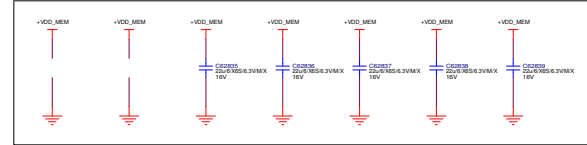




MVDD_PWR

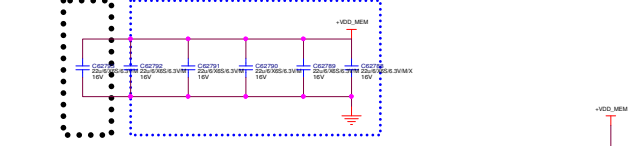


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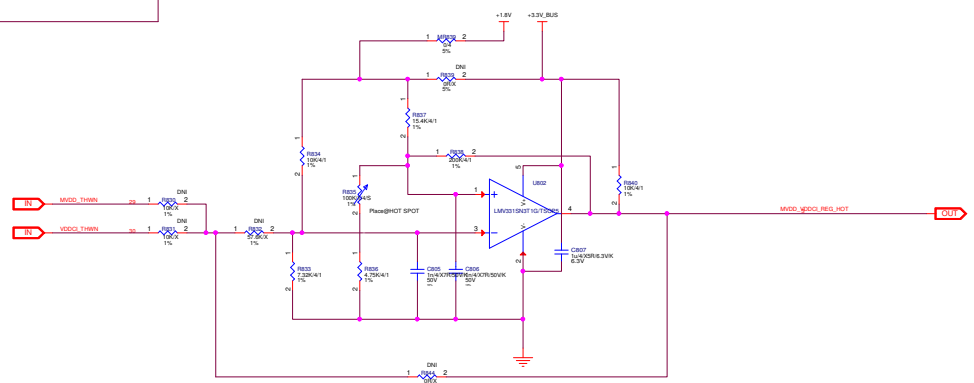
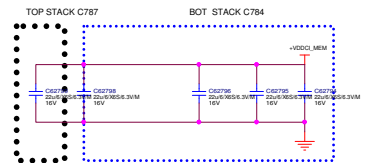
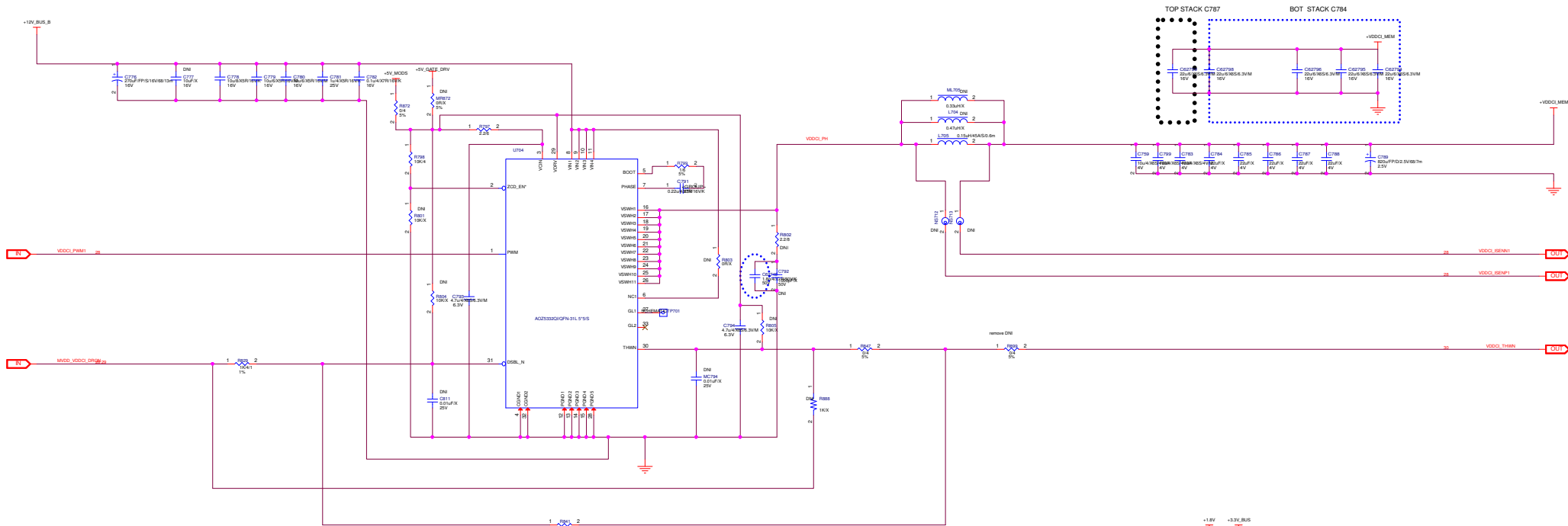


TOP STACK C753

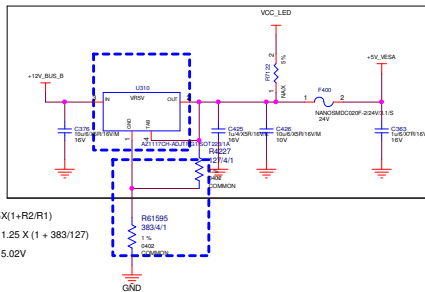
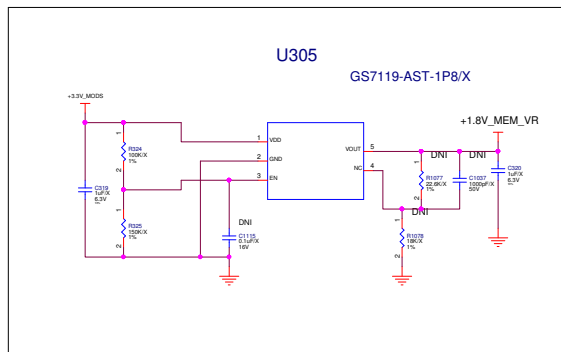
BOT STACK C754



GIGABYTE™



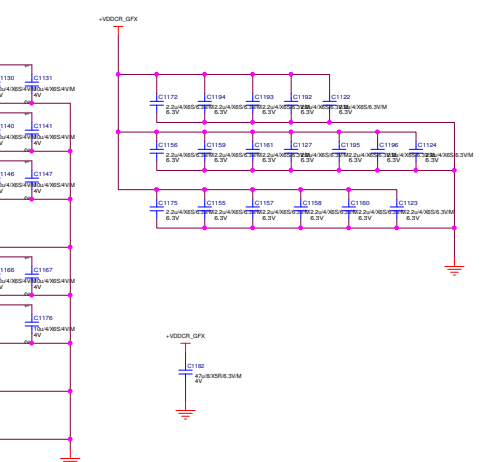
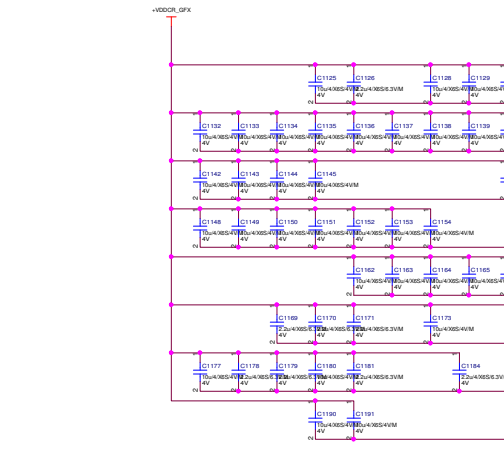
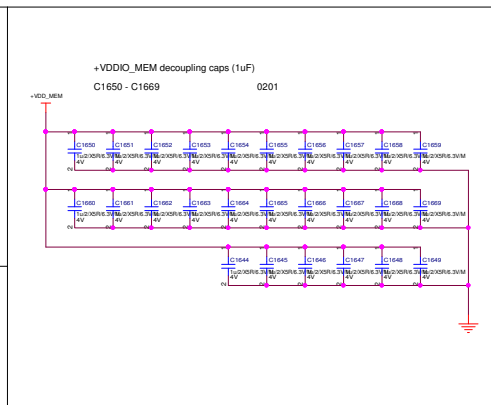
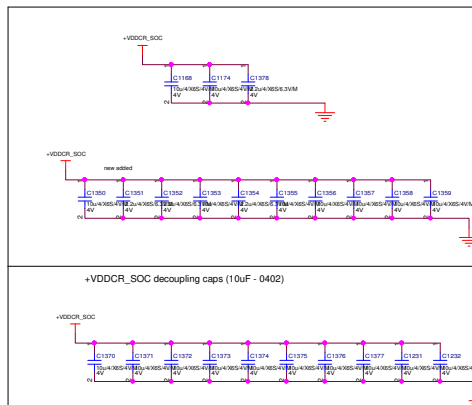
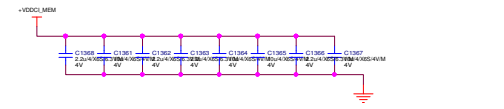
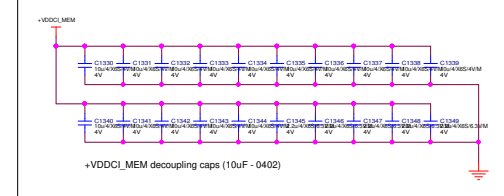
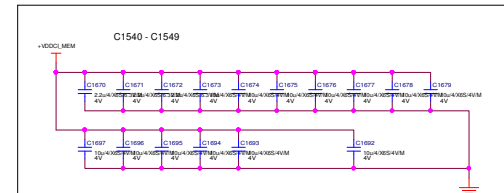
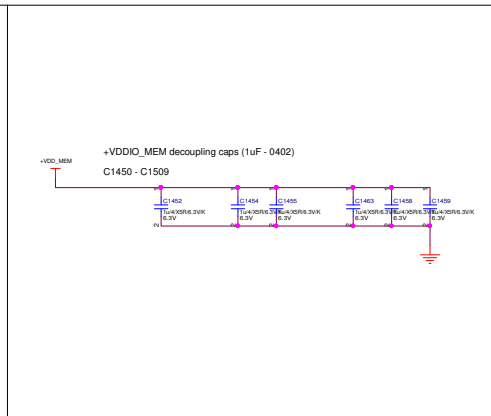
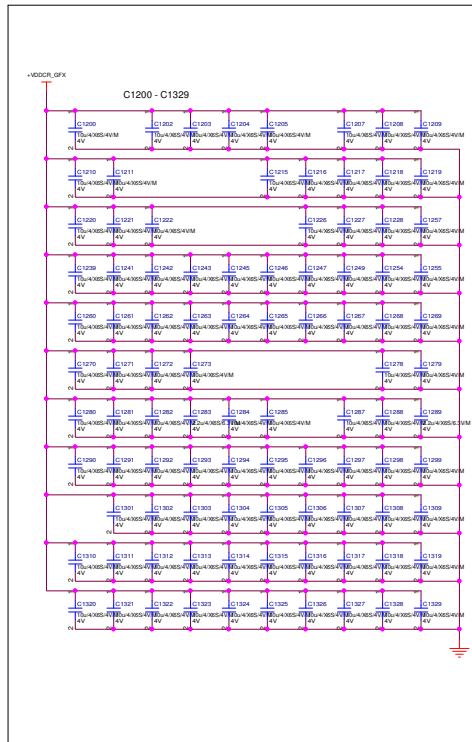
+1.8V FOR BOMACO

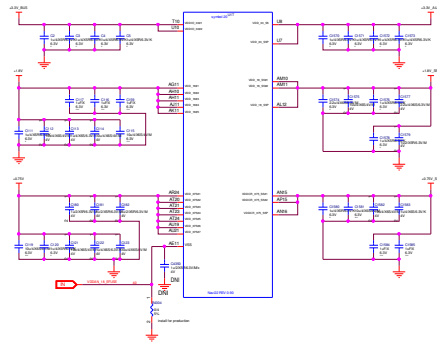
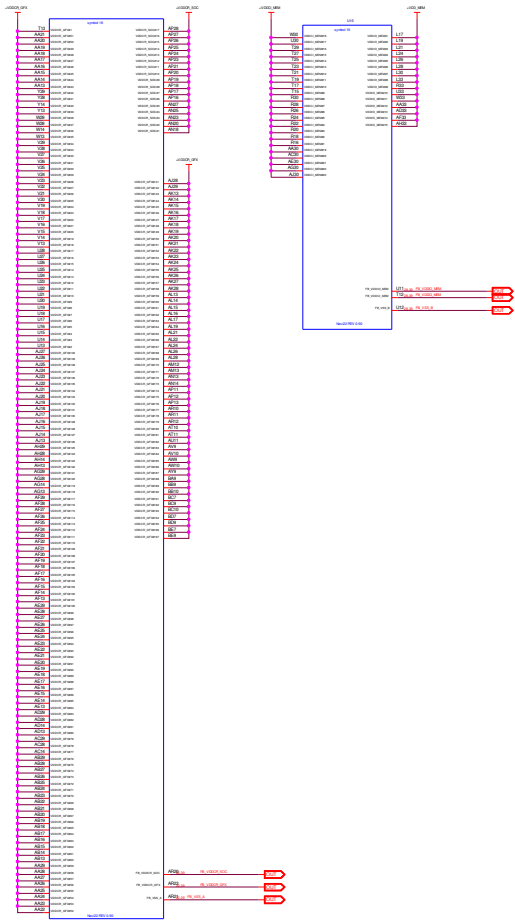


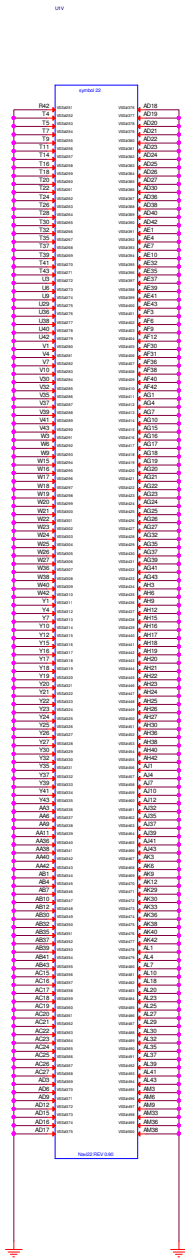
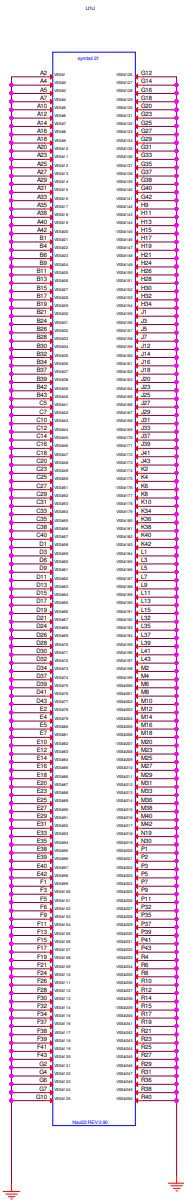
$$V_{OUT} = 1.25 \times (1 + R_2/R_1)$$

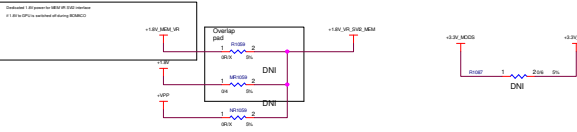
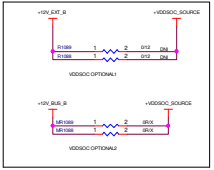
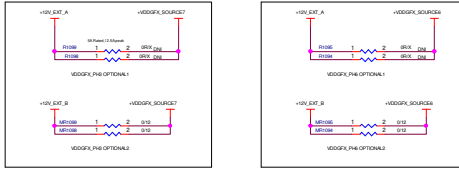
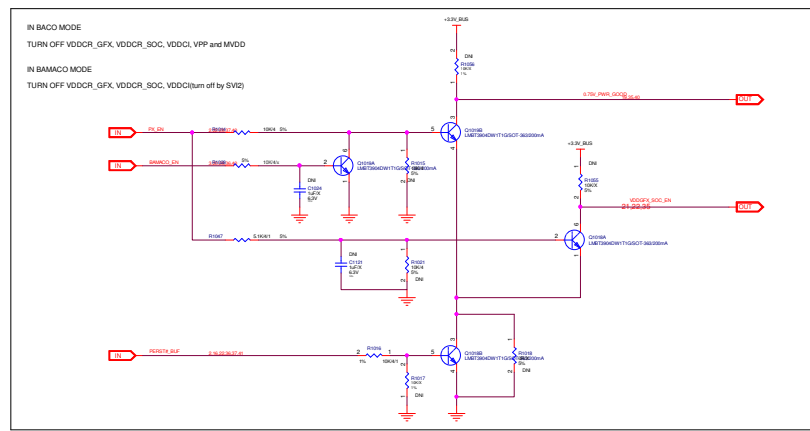
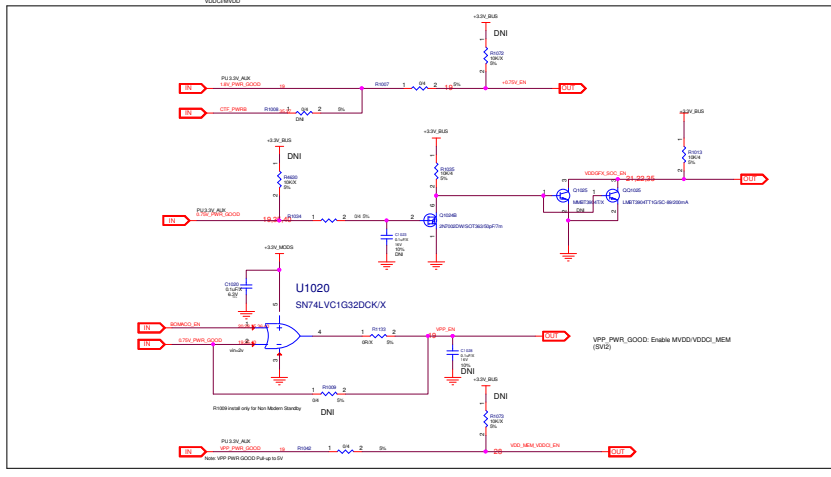
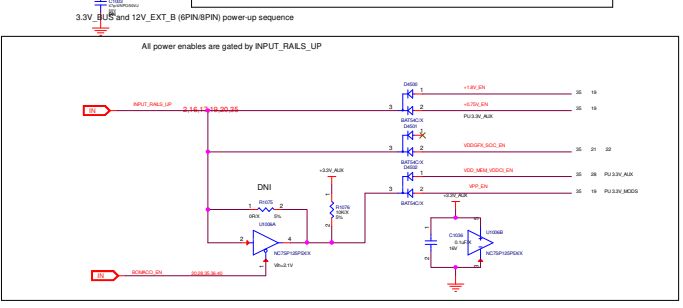
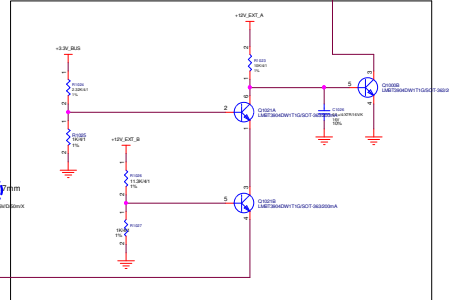
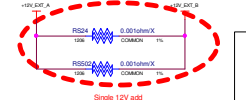
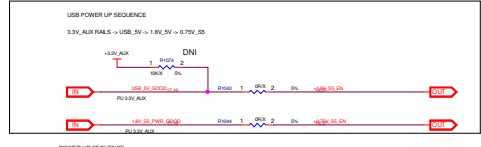
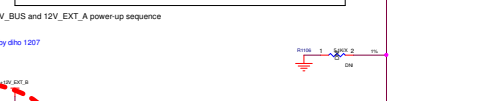
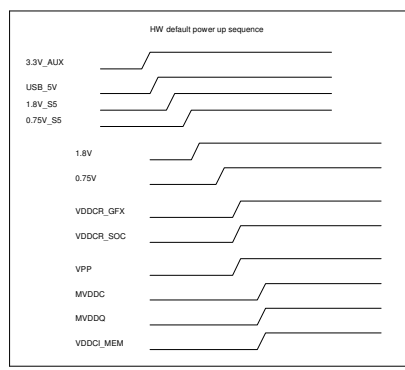
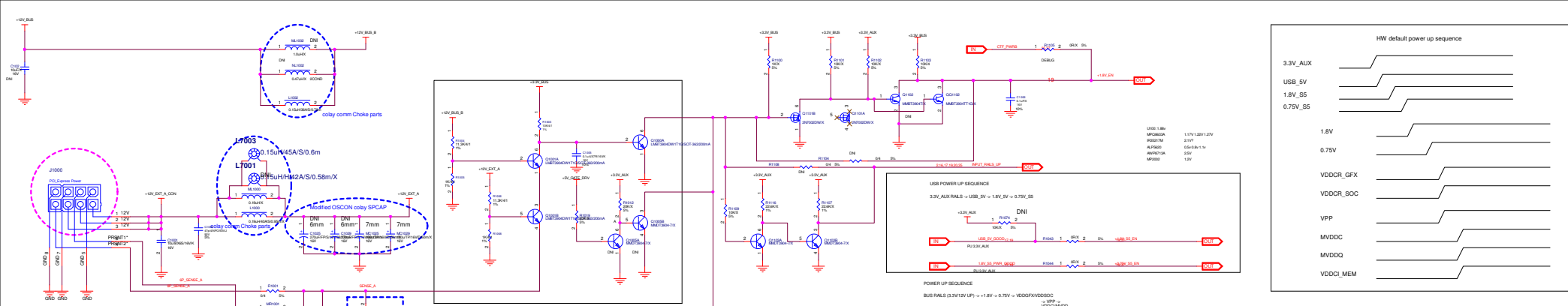
$$= 1.25 \times (1 + 383/127)$$

$$= 5.02V$$









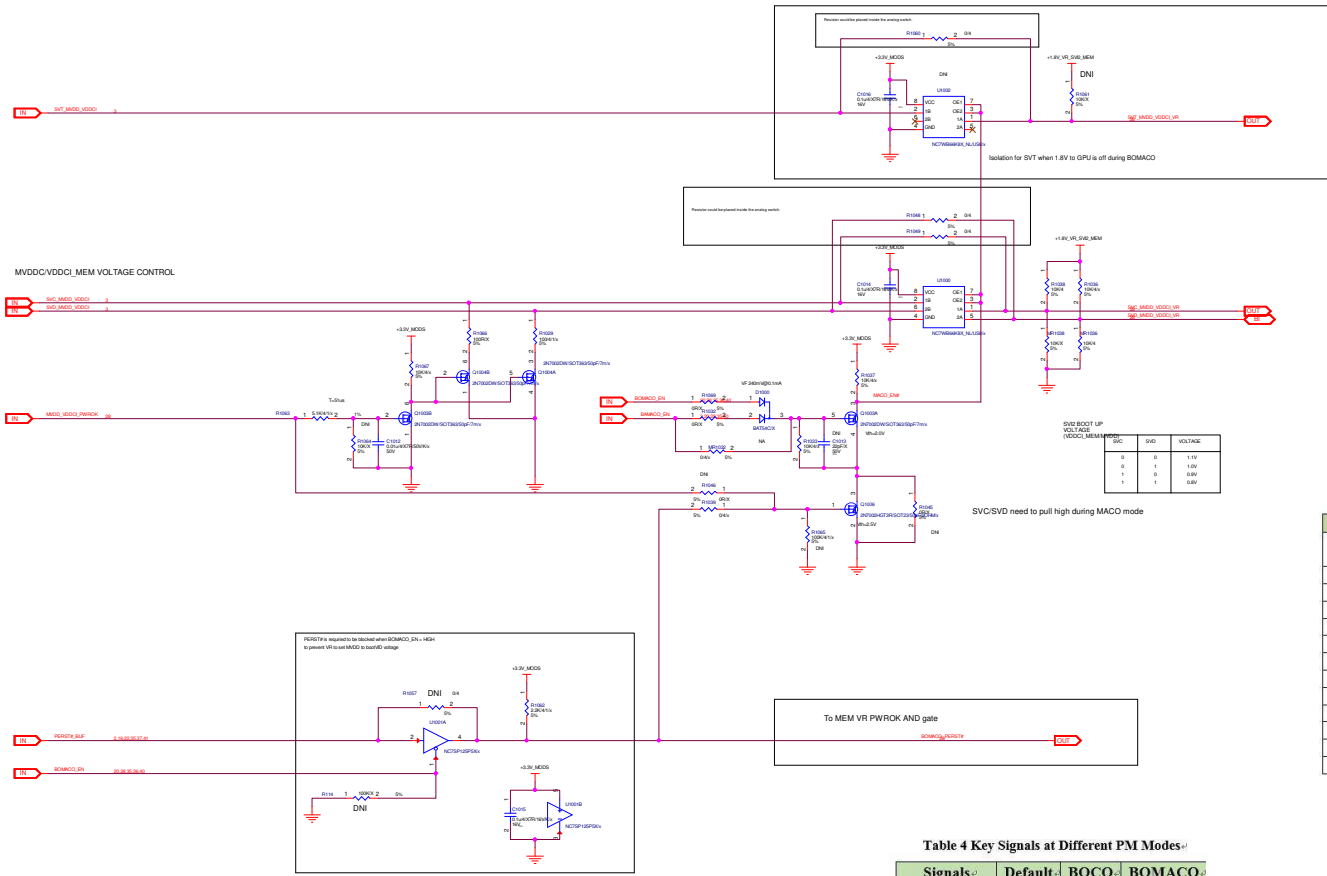


Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IP	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN * EFUSE	EFUSE	ON
VDDCR_S5	USB	ON

Table 3 Power Rails Status at BOMACO Mode

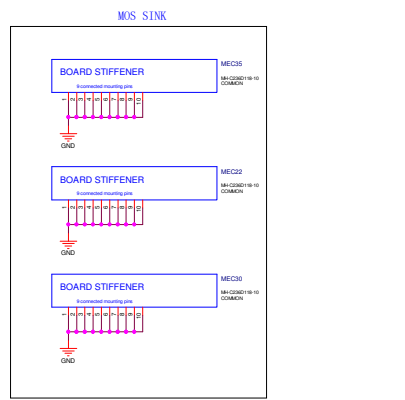
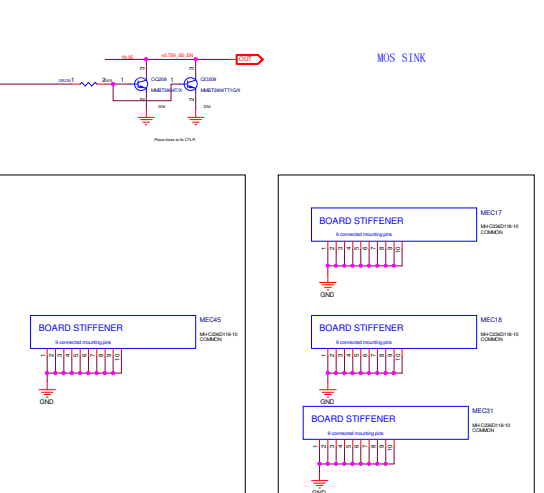
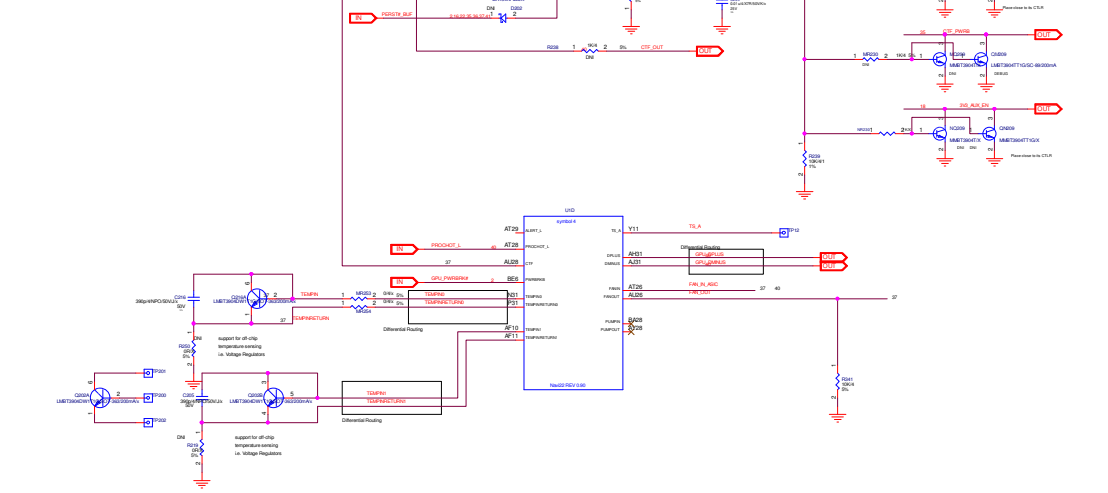
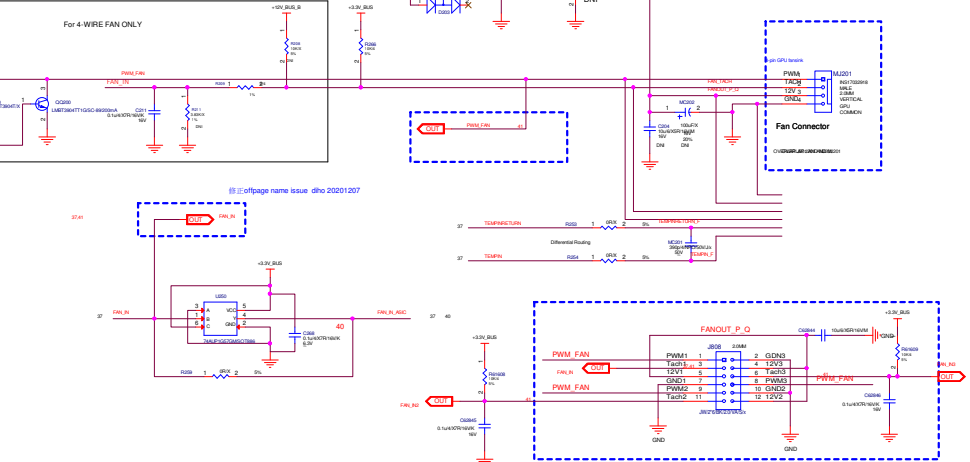
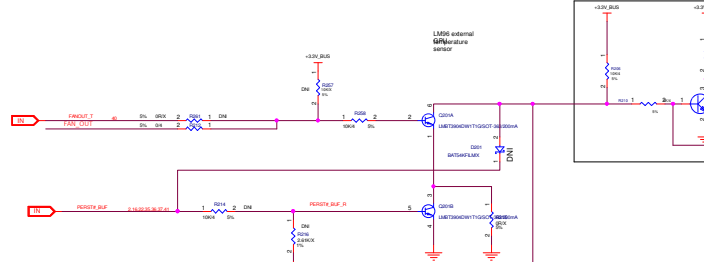
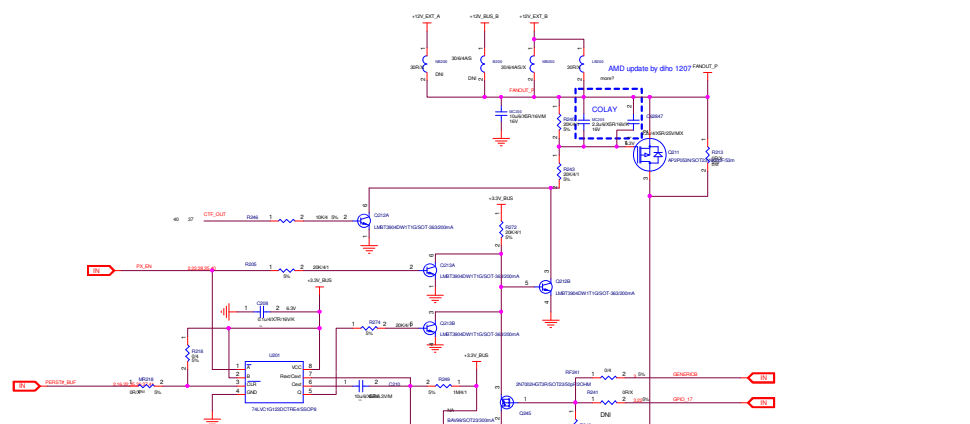
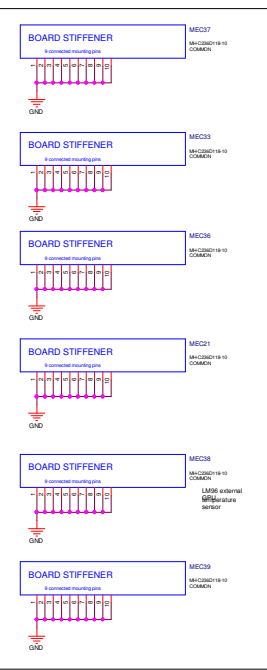
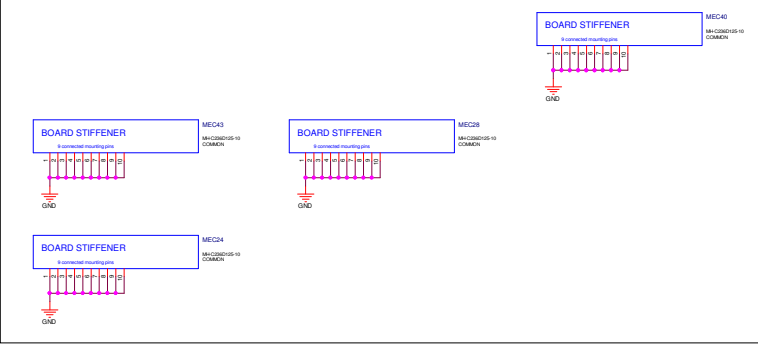
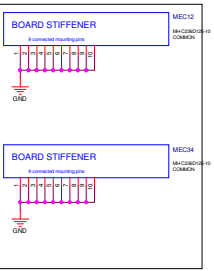
Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IP	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN * EFUSE	EFUSE	OFF
VDDCR_S5	USB	ON

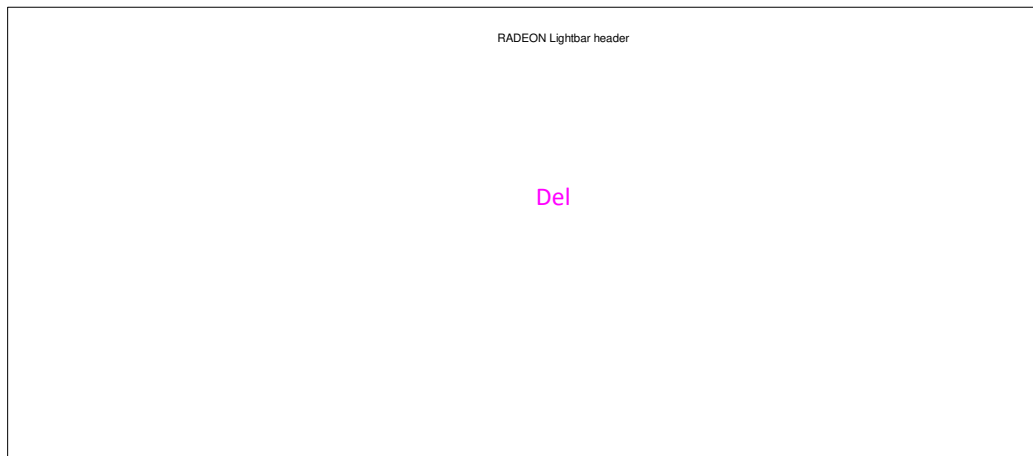
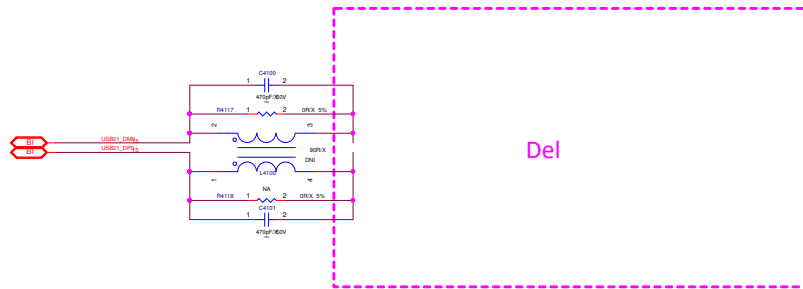
Table 4 Key Signals at Different PM Modes

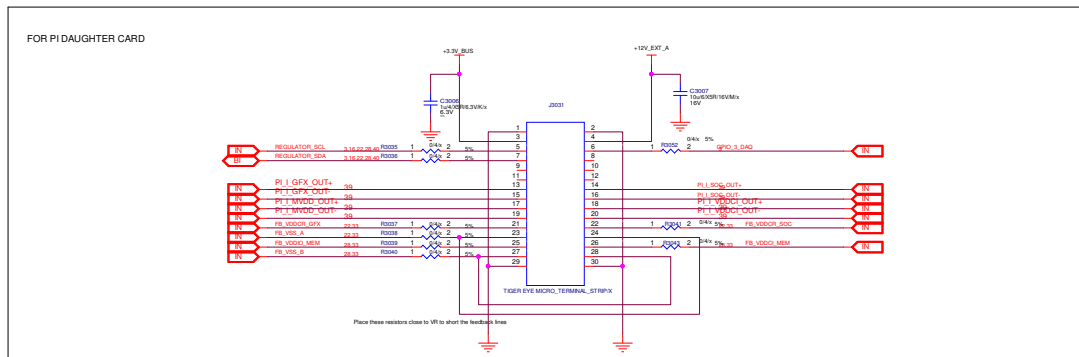
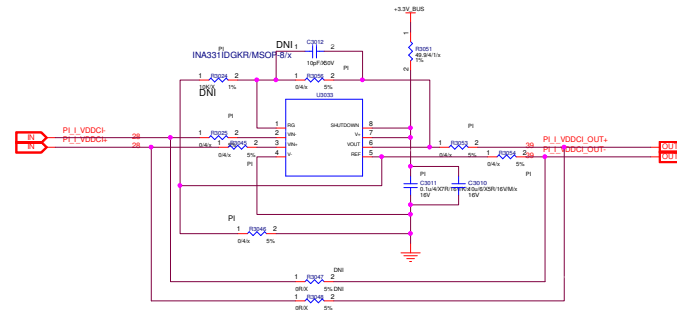
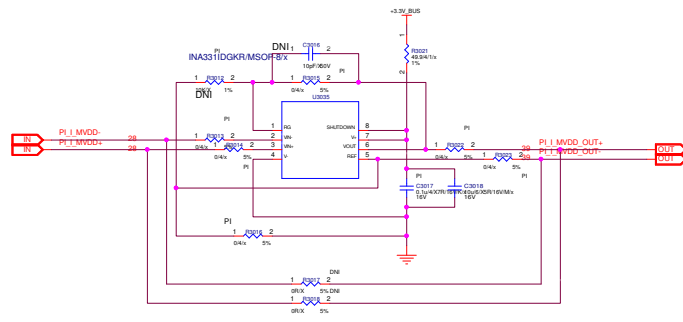
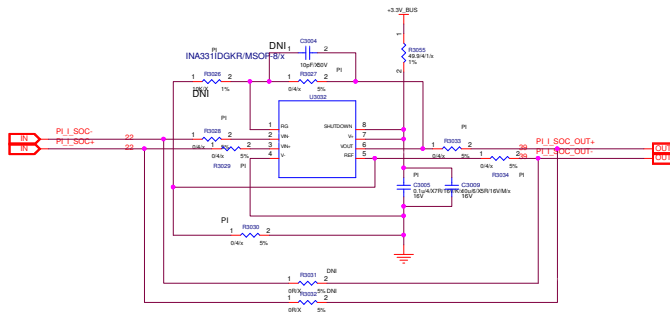
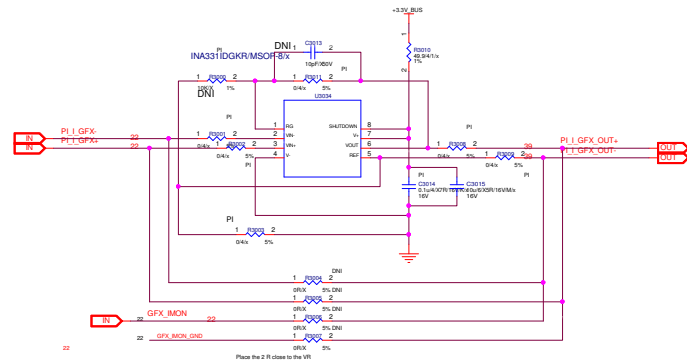
Signals	Default	BOCO	BOMACO
PX EN	LOW	N/A	N/A
MACO EN	N/A	N/A	N/A
PERSTb	HIGH	1->0->1	1->0->1
PWR EN	HIGH	LOW	LOW
BOMACO EN	LOW	LOW	HIGH

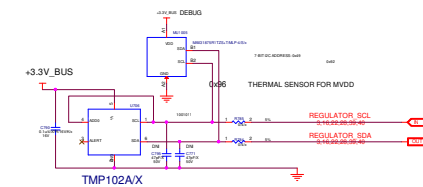
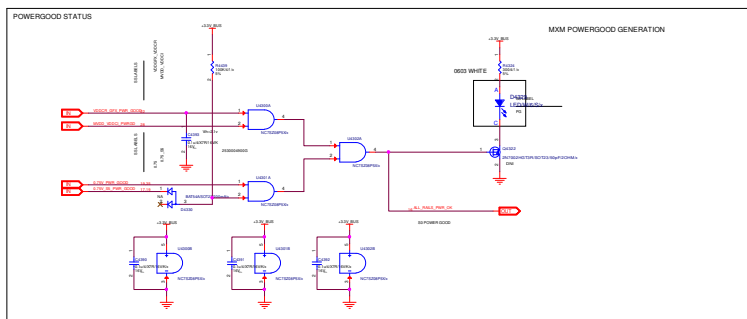
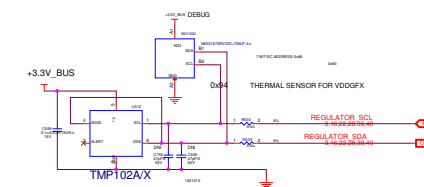
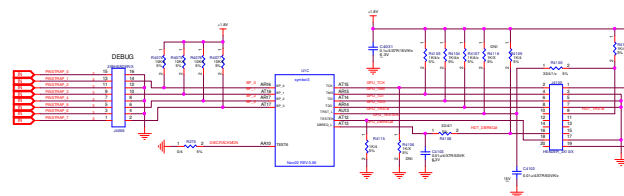
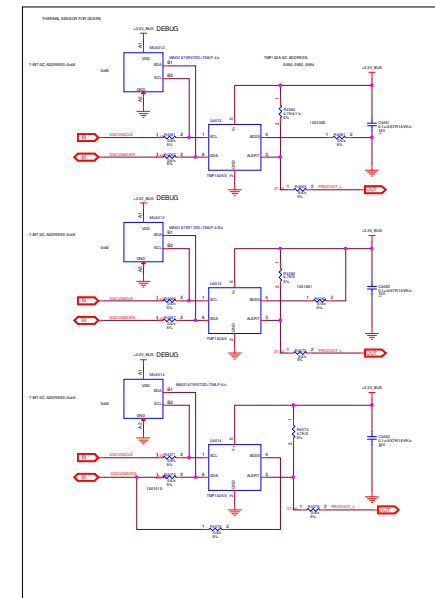
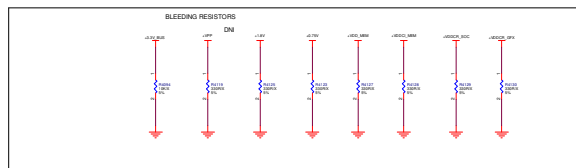
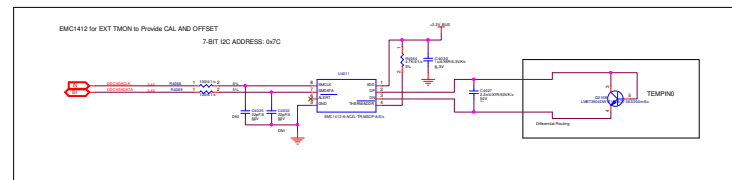
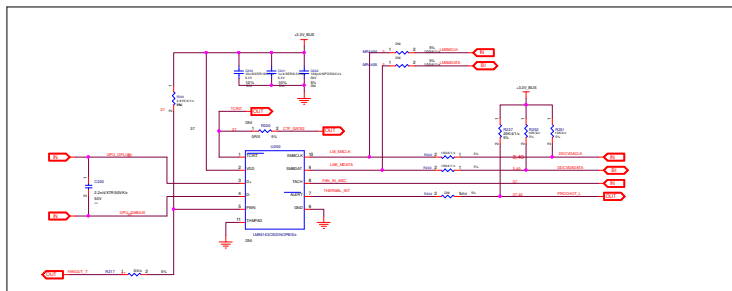
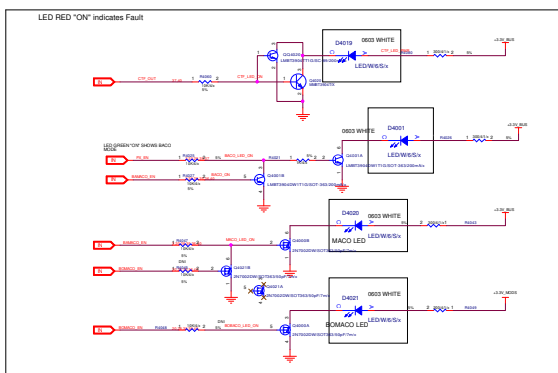
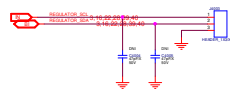
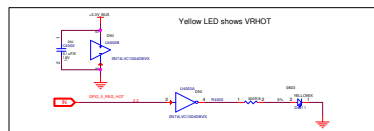
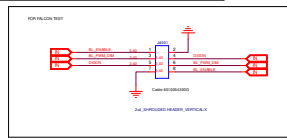
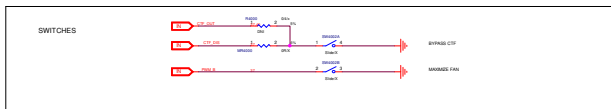
Table 5 Platform to Support BOMACO

BOMACO EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID





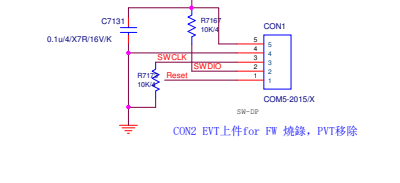
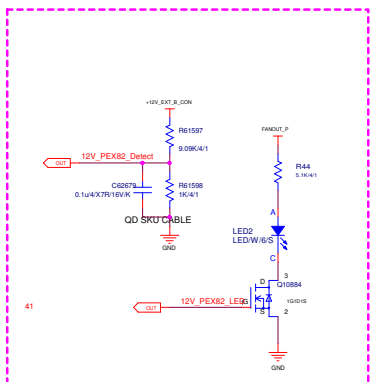
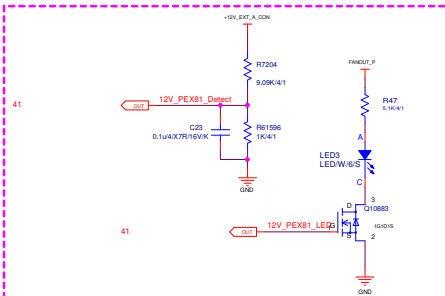
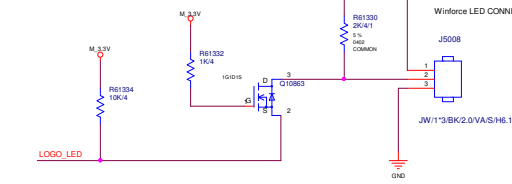
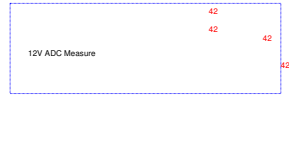
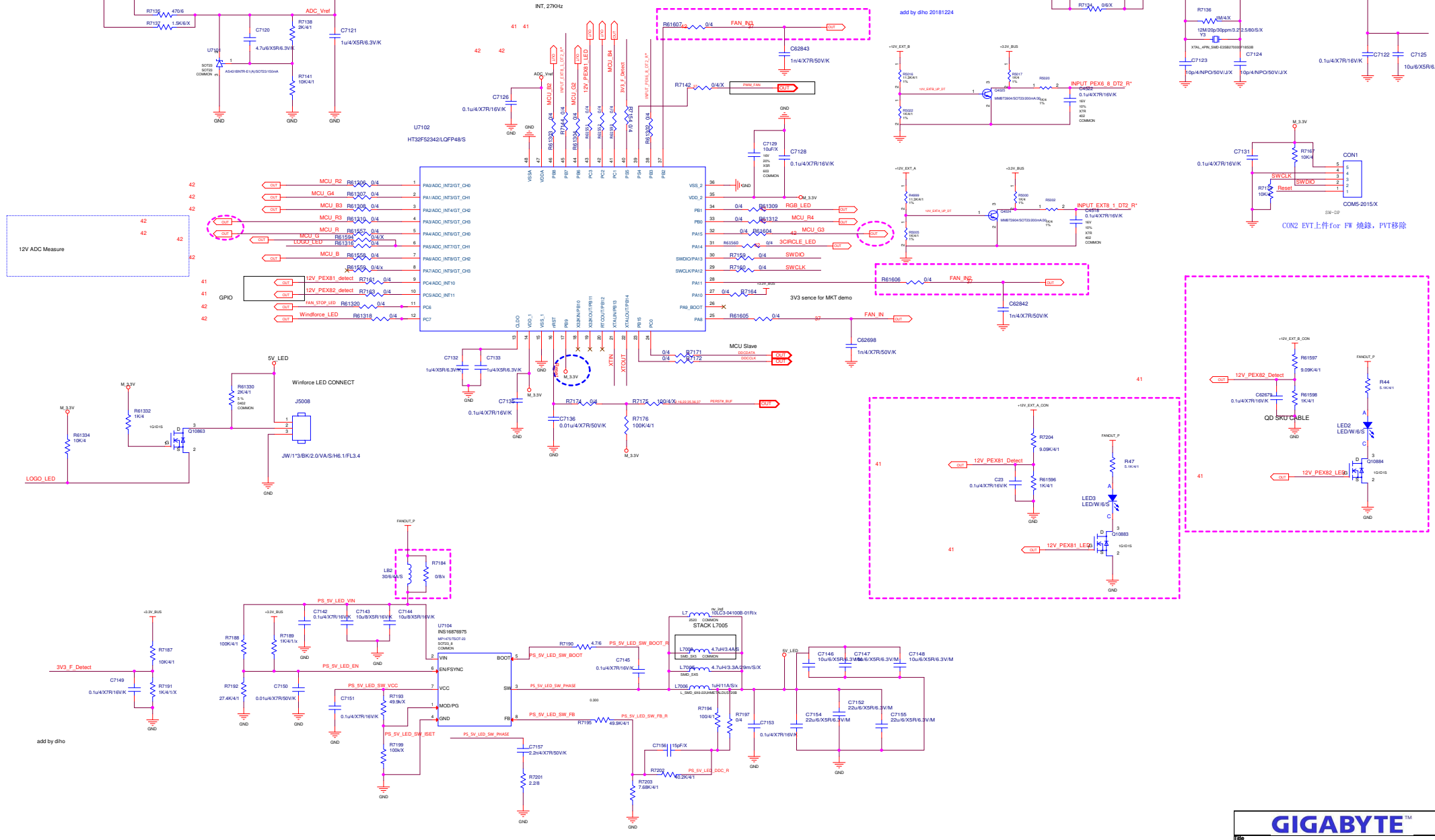




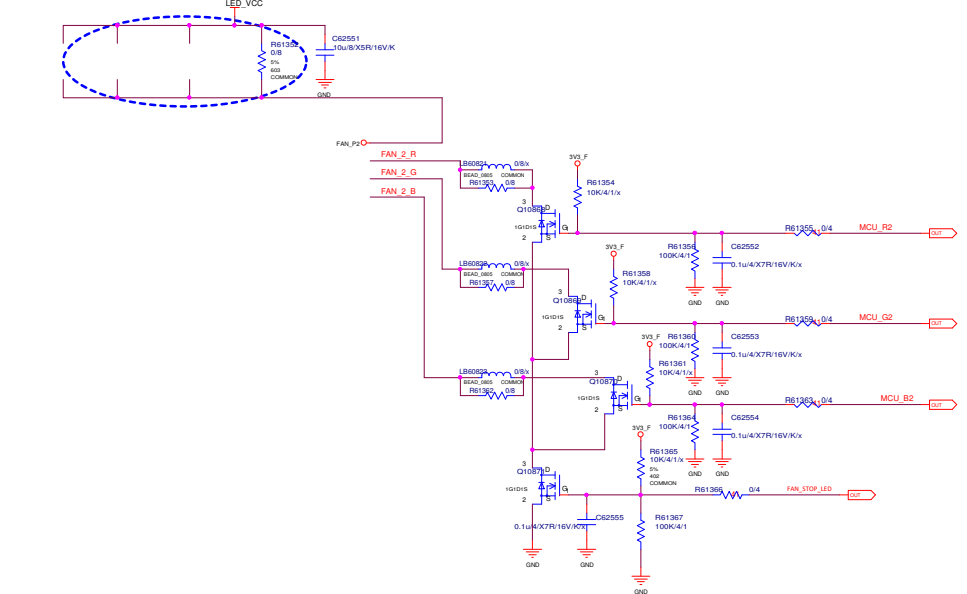
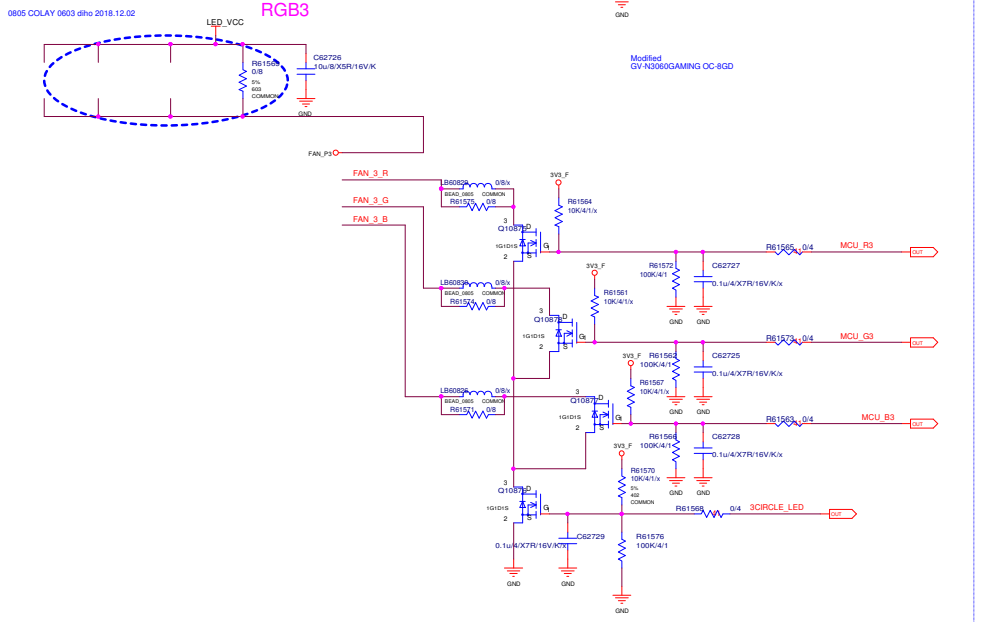
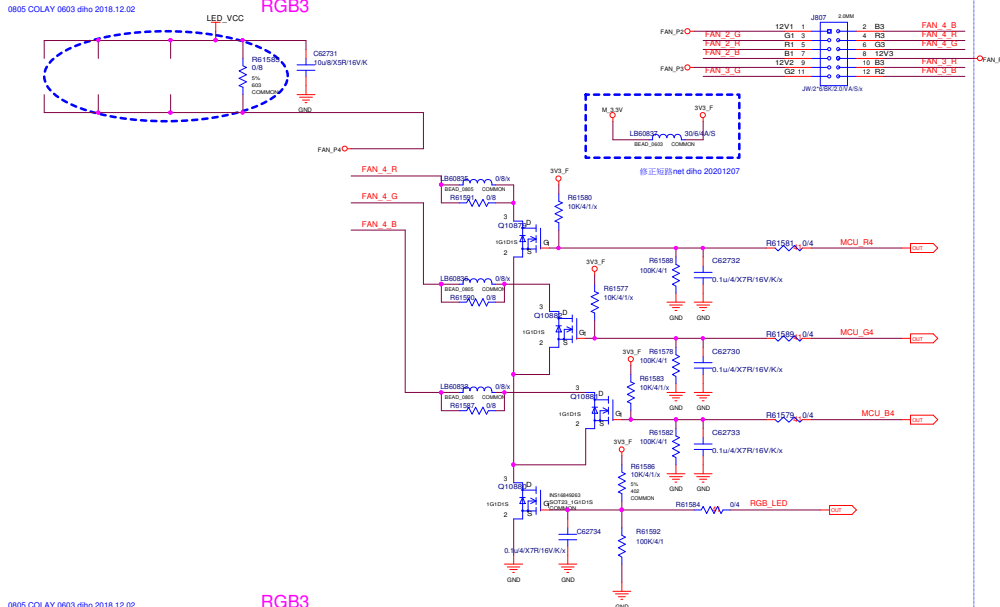
(5V - Ref 2.5V) / 5mA = 500 Ohm
(12V - Ref 2.5V) / 5mA = 1.9K Ohm

Vref = 2.5

INT: 27KHz
For EXT 12V plugin detect.



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GIGABYTE™

<Title>

Project Name: **GV-R67XTGAMING OC-12GD**

Rev: 1.0

Date: Wednesday, January 08, 2025

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