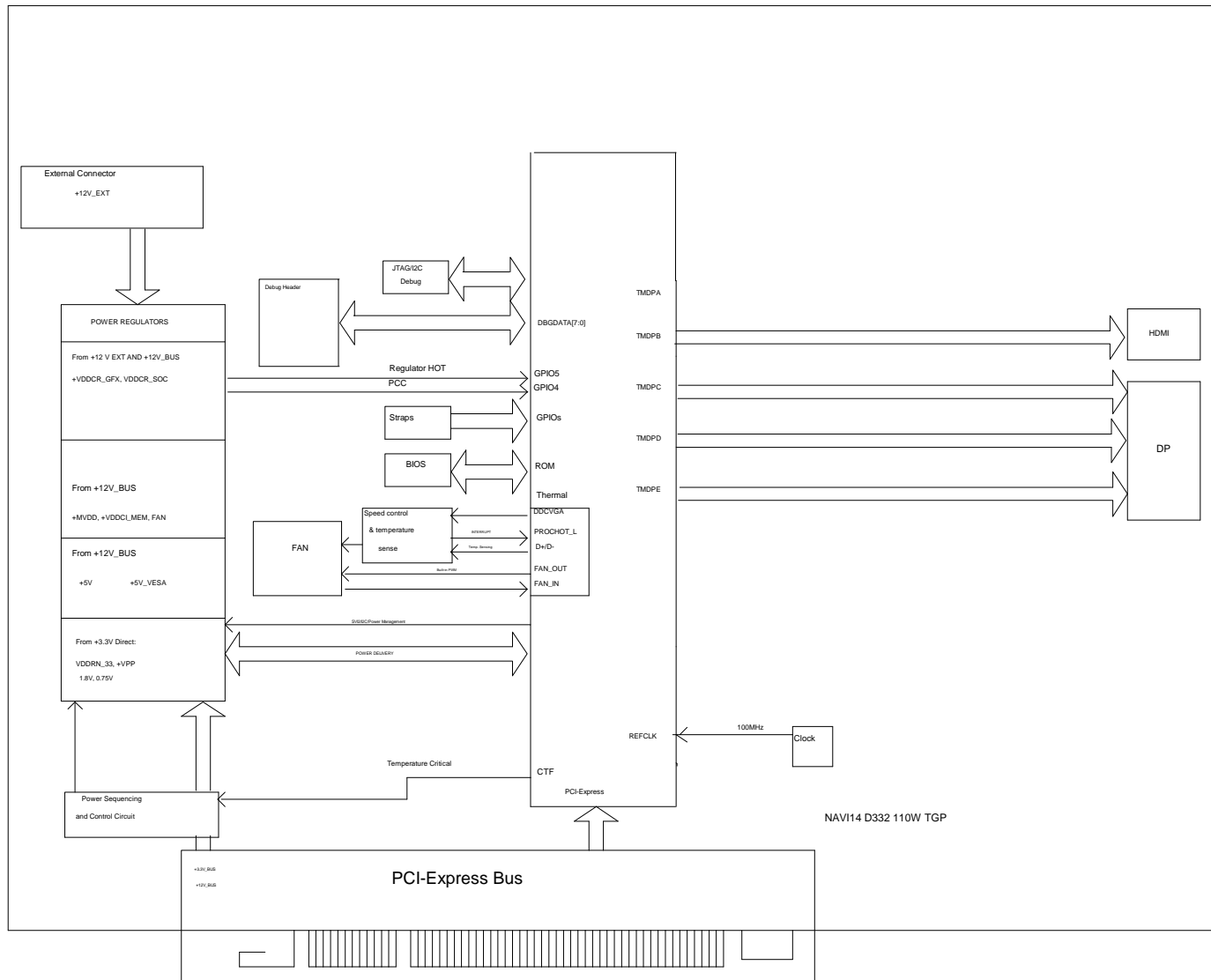


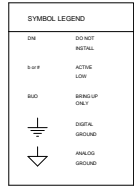
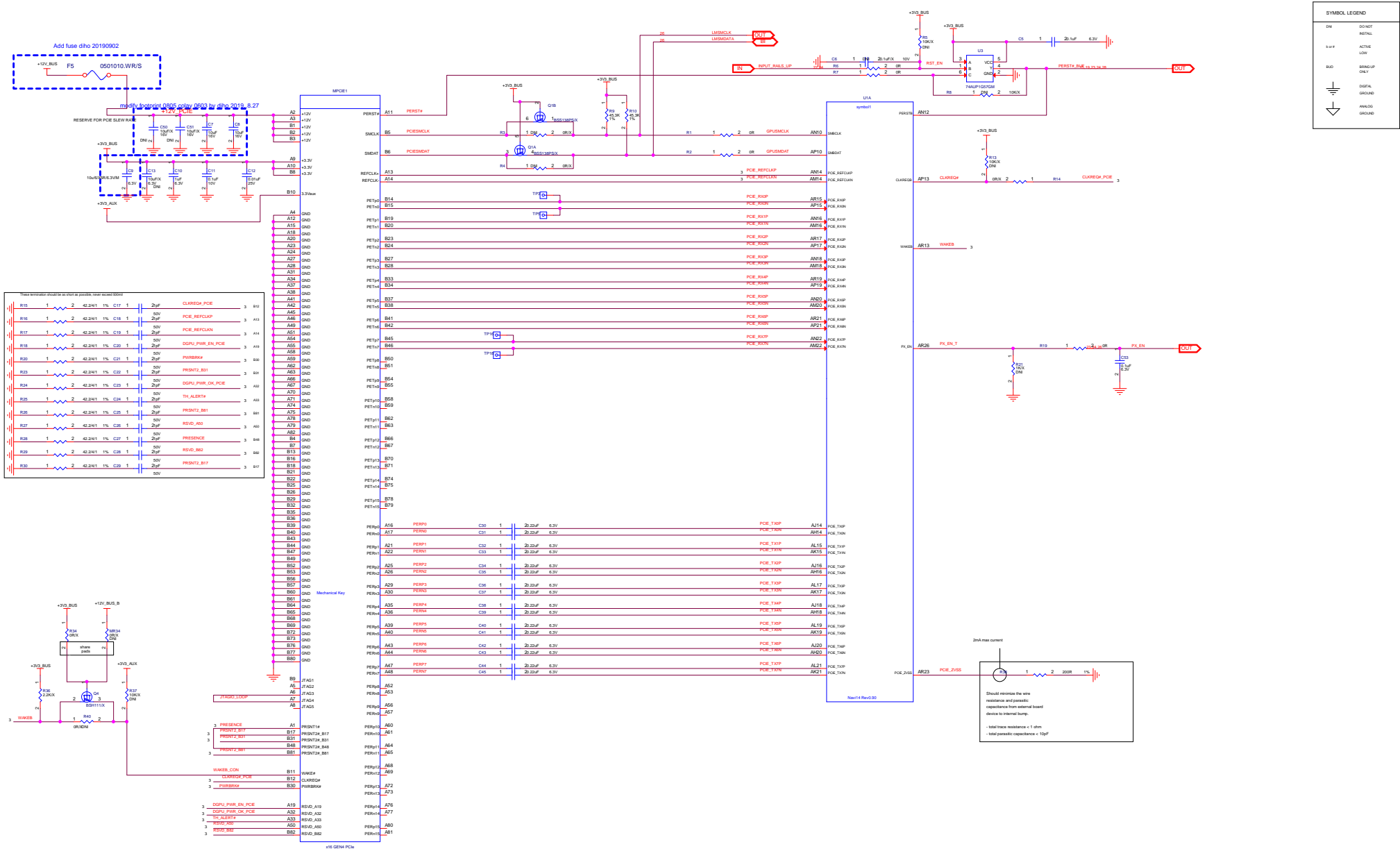
NAVI14 GDDR6 4PCS,10L 3xDPs +1xHDMI
 105-D332xx-00B RevB Desktop board(110W TGP)

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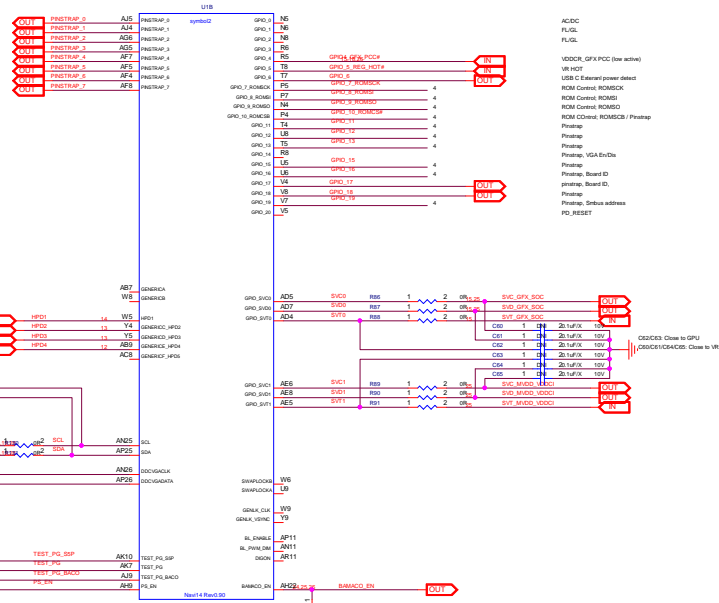
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	DEBUG CIRCUITS
2	BLOCK DIAGRAM	27	REVISION HISTORY
3	NAVI14 - PCIe Interface		
4	NAVI14 - GPIO, EXTRA		
5	NAVI14 - XTAL		
6	NAVI14 - POWER and GND		
7	NAVI14 - Decaps		
8	NAVI14 - MEM CH AB		
9	NAVI14 - MEM CH CD		
10	GDDR6 x16 - MEM CH AB		
11	GDDR6 x16 - MEM CH CD		
12	NAVI14 - TMDPAB - USB,HDMI		
13	NAVI14 - TMDPCD - DP,DP		
14	NAVI14 - TMDPE - DP		
15	REG VDDGFX/SOC CNTL		
16	REG VDDGFX		
17	REG VDDSOC		
18	REG PCC		
19	REG VDDCI/MVDD CNTL		
20	REG VDDCI/MVDD		
21	REG - 0V75		
22	LDO 1V8/PPPS/ISV_VESA		
23	MECHANICAL AND THERMAL		
24	POWER MANAGEMENT		
25	SVI2		



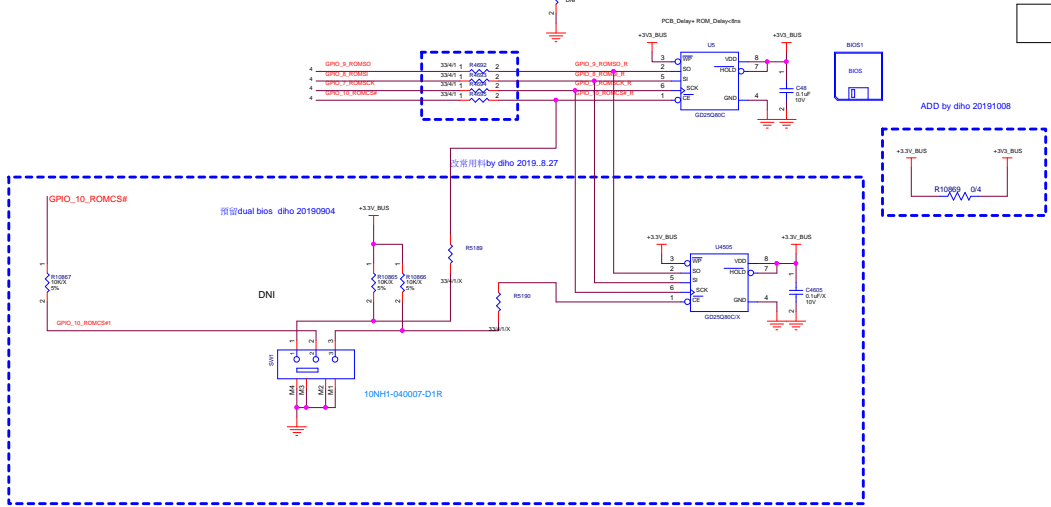
NAVI14 D332 110W TGP

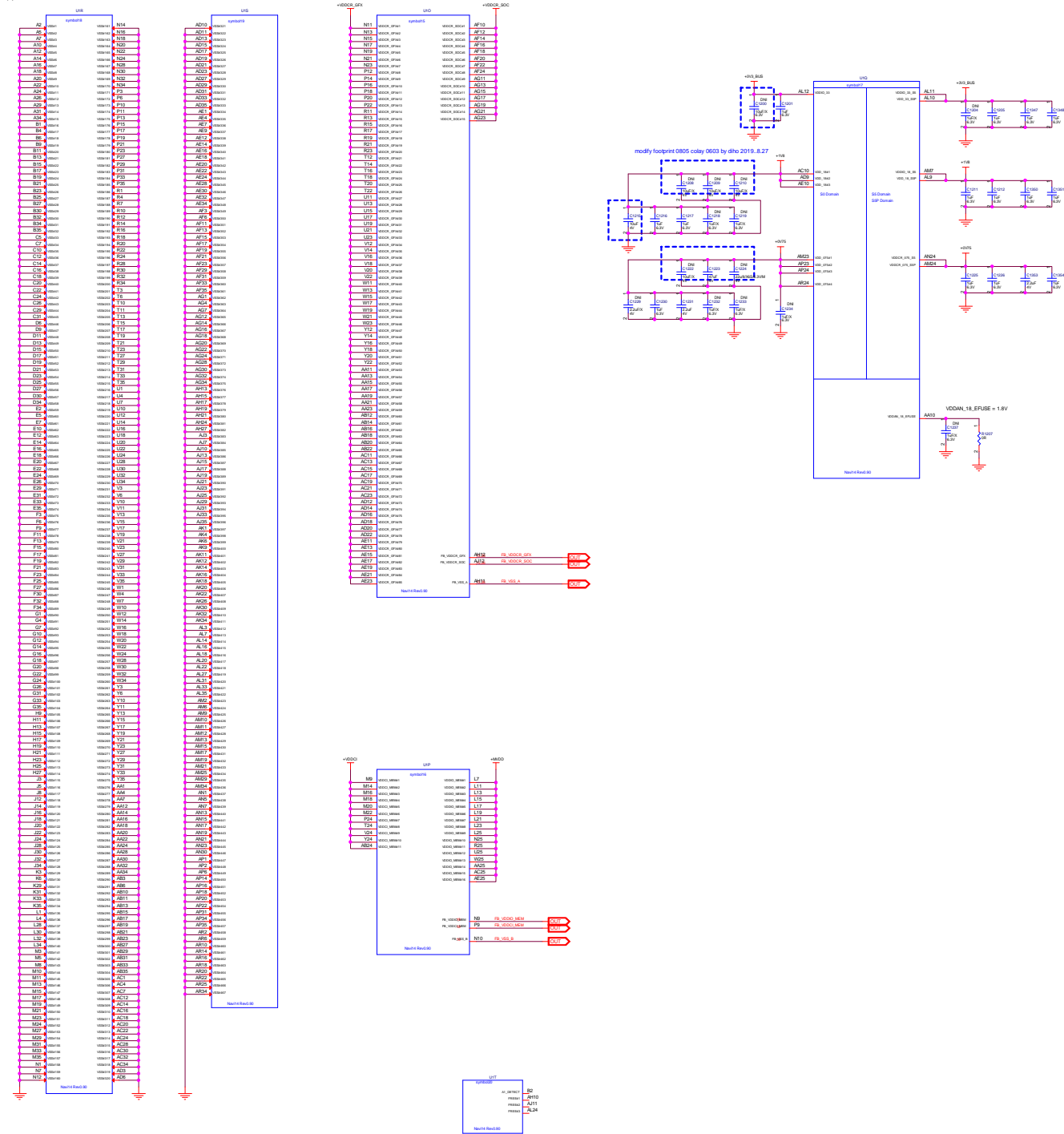


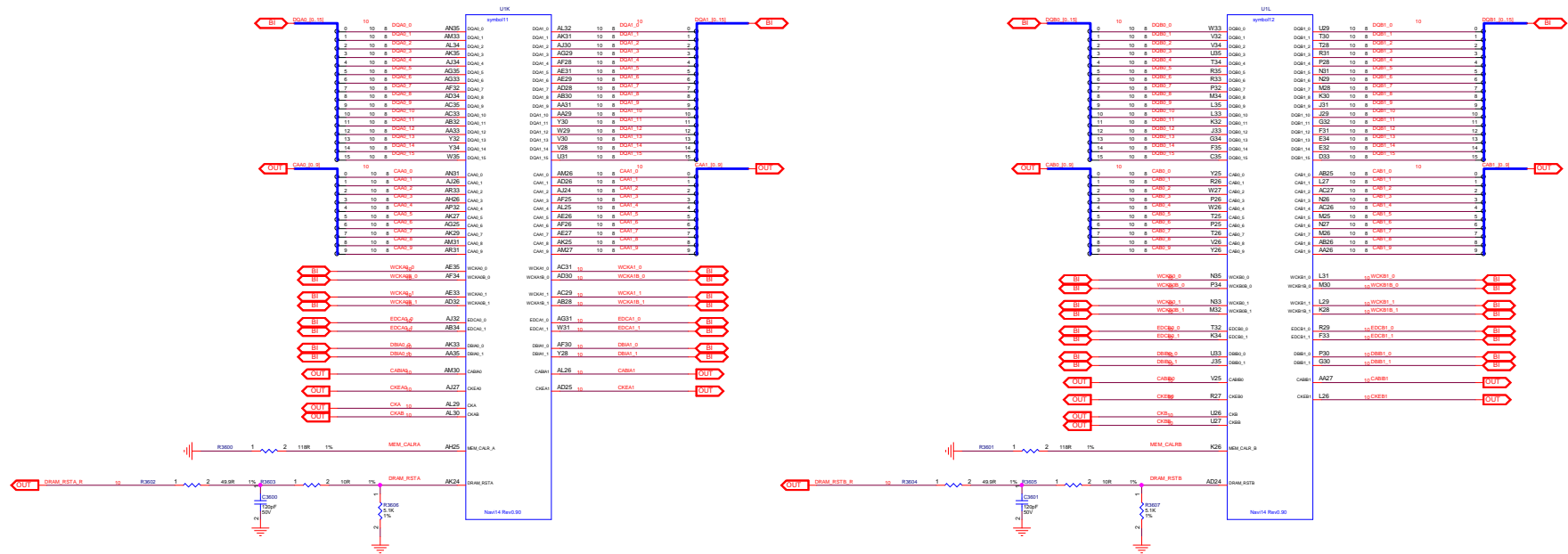
14nm bit address	14nm bit address	FUNCTION	IO BUS	DEVICE
0x00	0x00	VDDCR_GFX/SOC	SCL/SDA	U6011R33217
0x02	0x04	MVDD/VDDCI	SCL/SDA	U7011NC981022
0x03	0x0B	PCDgressived	SCL/SDA	U40011CS8601
0x0B	0x00	GE Temperature	DOCVGACK/DATA	U40001MP102A
0x0C	0x0B	EXT SENSOR	DOCVGACK/DATA	U40011LM66163

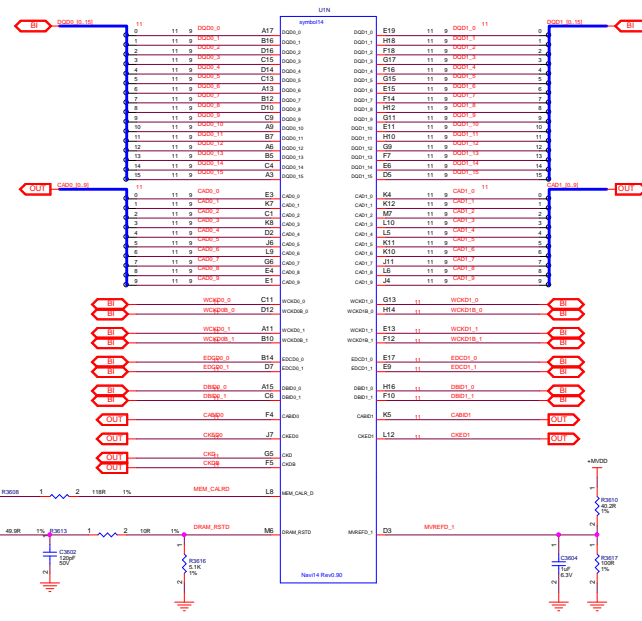
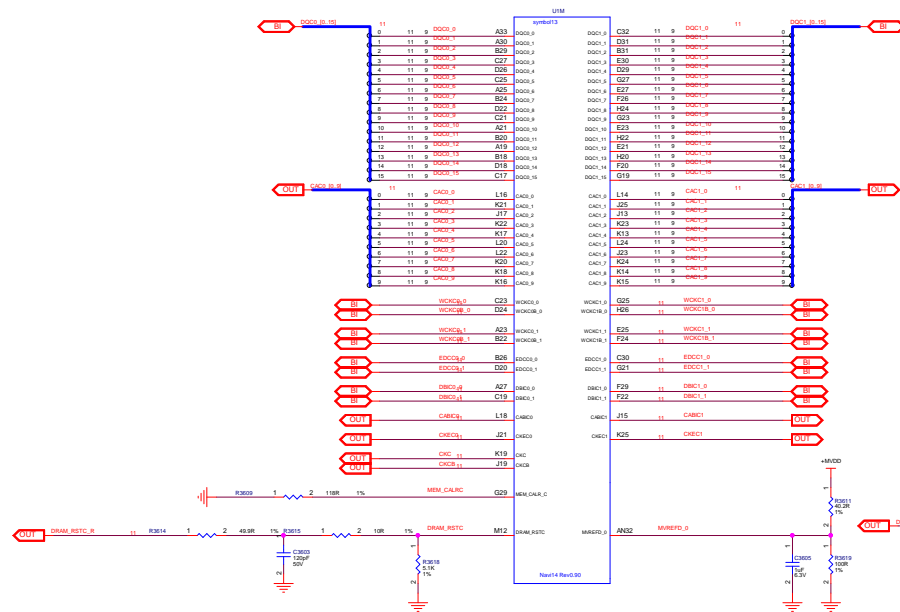


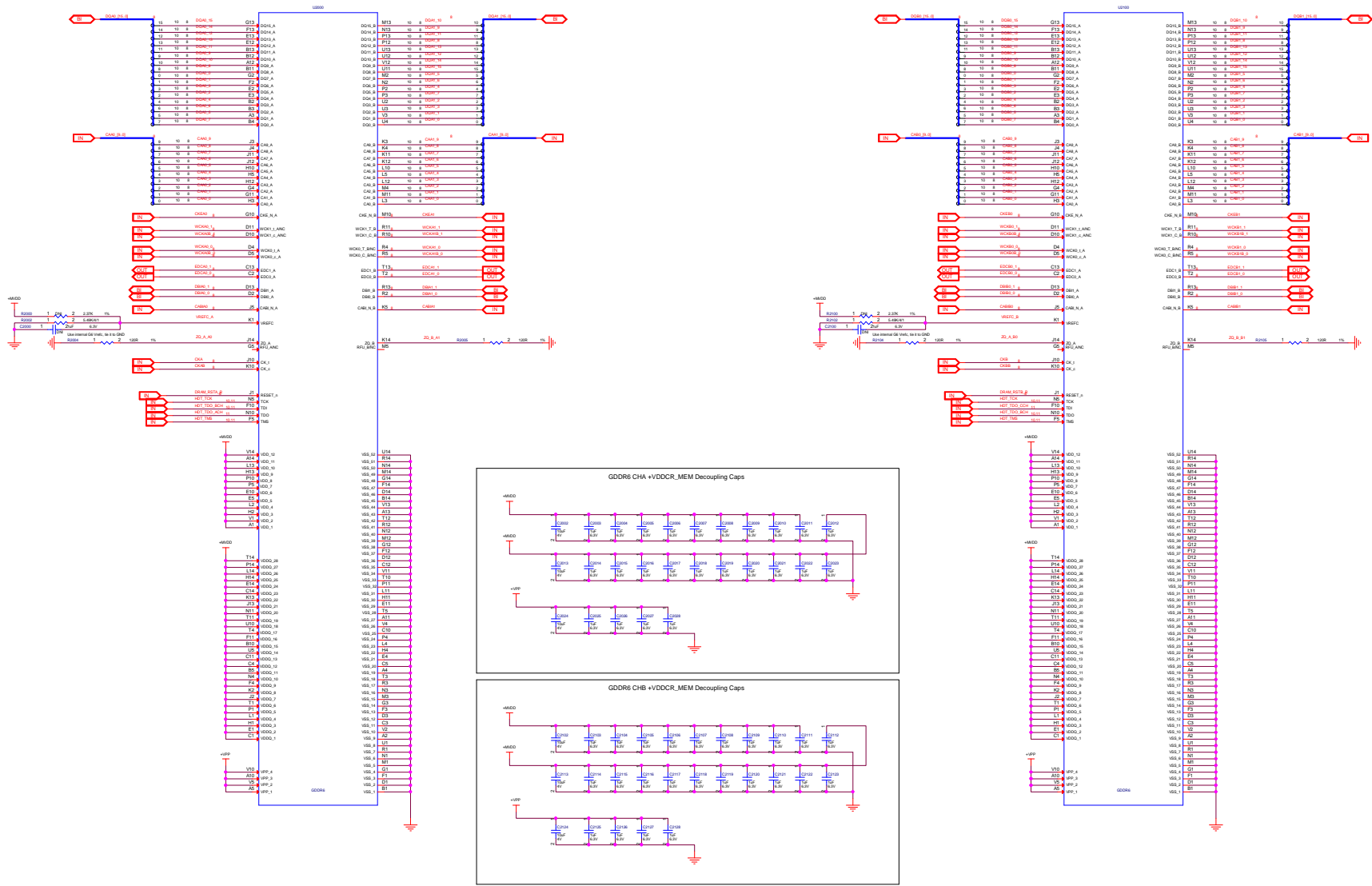
User	Internal Default Value	Definition
BIF	R151 1 2 10KΩ R152 1 2 10KΩ	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
	R153 1 2 10KΩ R154 1 2 10KΩ	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ power management capability is disabled 1: CLKREQ power management capability is enabled
	R156 1 2 10KΩ R157 1 2 10KΩ	PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing mode(half swing)
	R158 1 2 10KΩ R159 1 2 10KΩ	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognized as the systems VGA controller
DCE	R160 1 2 10KΩ R161 1 2 10KΩ	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs
	R162 1 2 10KΩ R163 1 2 10KΩ	PINSTRAP_AUD[1:0] 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected Default(PINSTRAP_AUD[1:0]) = 000
	R164 1 2 10KΩ R165 1 2 10KΩ	
	R166 1 2 10KΩ R167 1 2 10KΩ R168 1 2 10KΩ R169 1 2 10KΩ	
Platform	R170 1 2 10KΩ R171 1 2 10KΩ	PINSTRAP_FIG[1:0] - No definition on NV
	R172 1 2 10KΩ R173 1 2 10KΩ	PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
	R174 1 2 10KΩ R175 1 2 10KΩ	
	R176 1 2 10KΩ R177 1 2 10KΩ R178 1 2 10KΩ R179 1 2 10KΩ	PINSTRAP_BFL_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100 - 0MBIT (ST) M2SPR0A 101 - 1MBIT (ST) M2SPR10A 101 - 2MBIT (ST) M2SPR20 101 - 4MBIT (ST) M2SPR40 101 - 8MBIT (ST) M2SPR80 101 - 16MBIT (CHINGIS) PMSL0102 101 - 1MBIT (CHINGIS) PMSL0100 Default(PINSTRAP_BFL_MEM_AP_SIZE) = 101
SMU	R182 1 2 10KΩ R183 1 2 10KΩ	PINSTRAP_SMBUS_ADDR 0: 0x4th 1: 0x2th
	R184 1 2 10KΩ R185 1 2 10KΩ	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device
	R124 1 2 10KΩ R125 1 2 10KΩ	GPIO_5

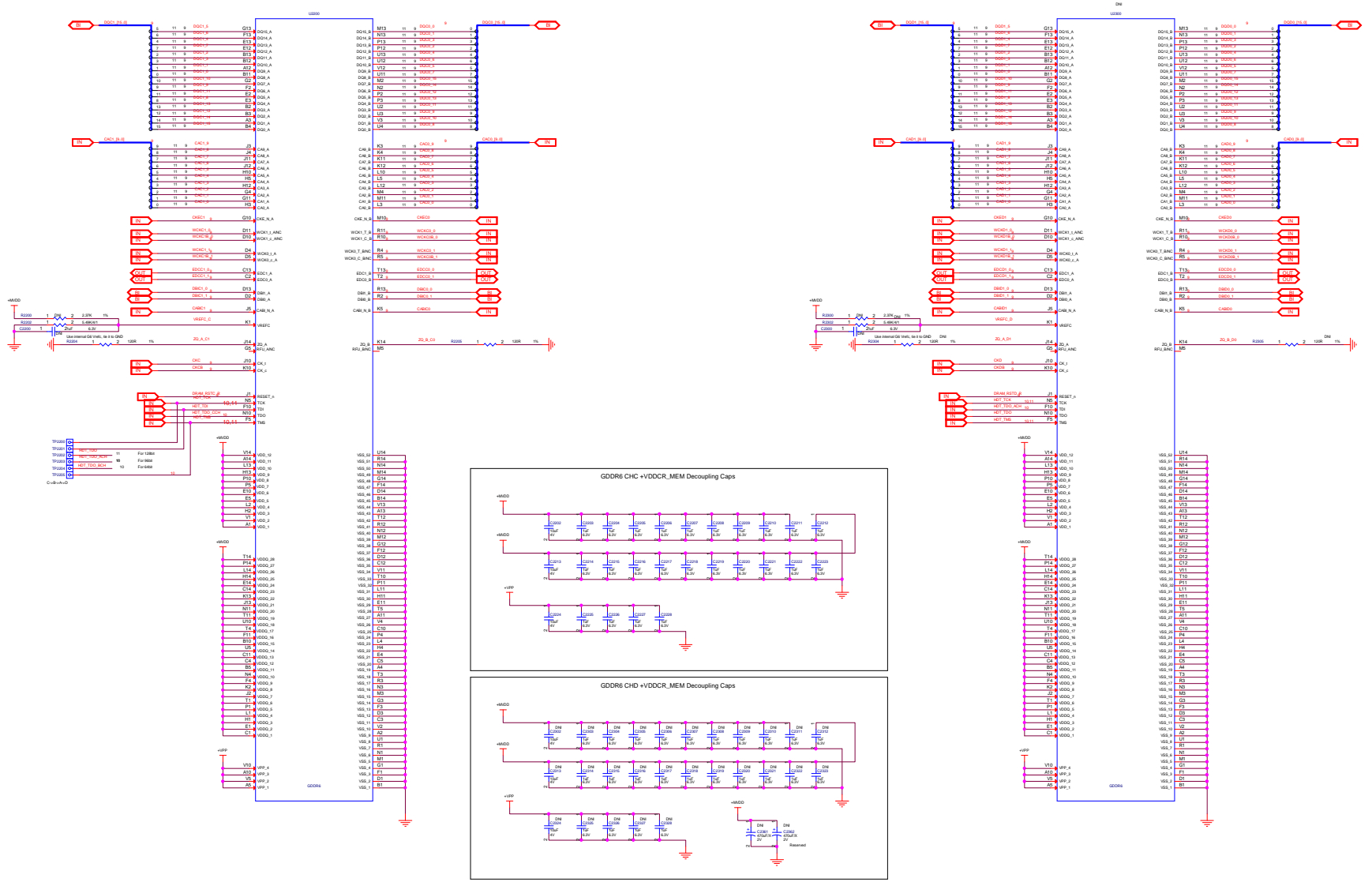


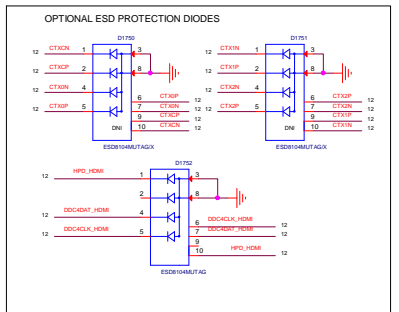
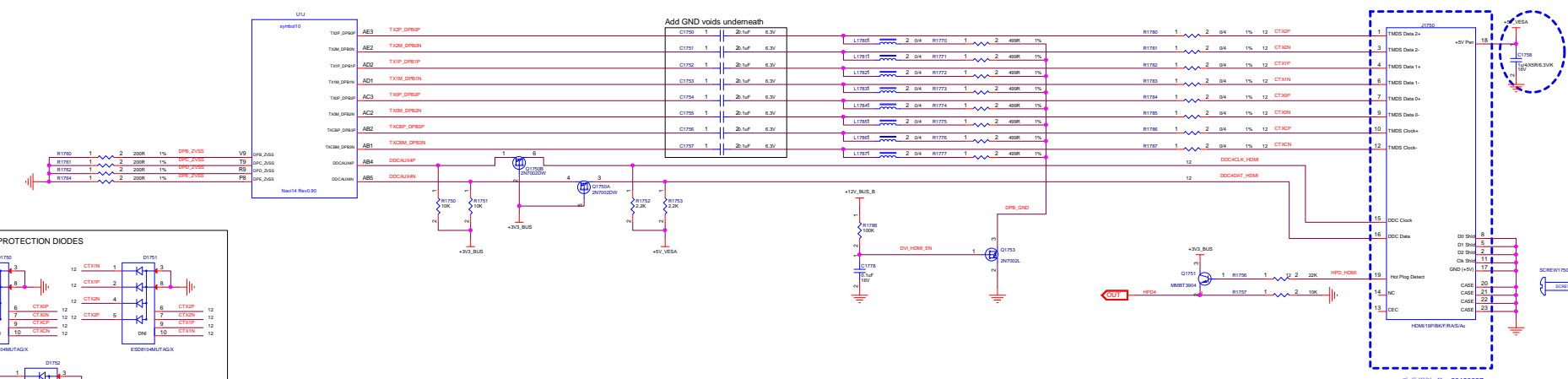
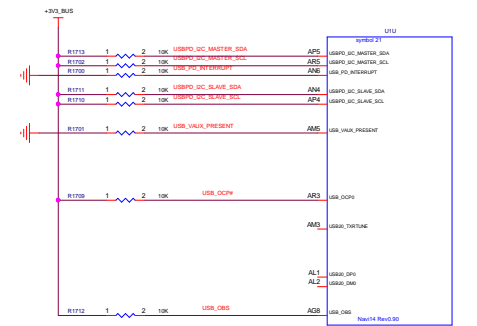
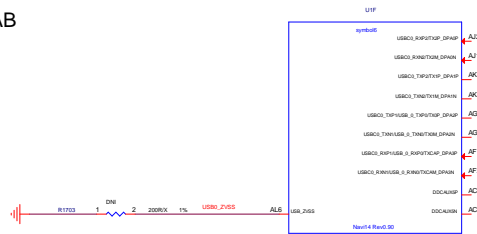


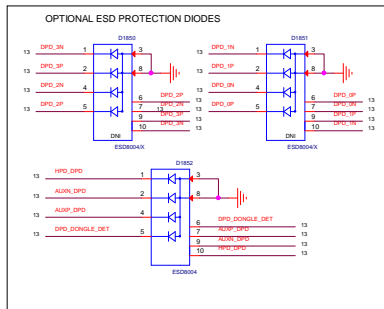
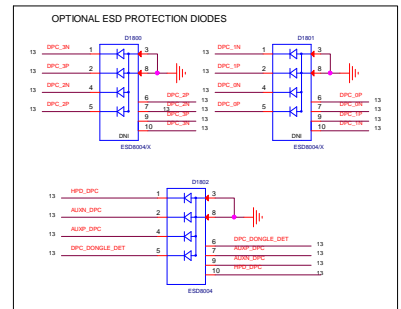
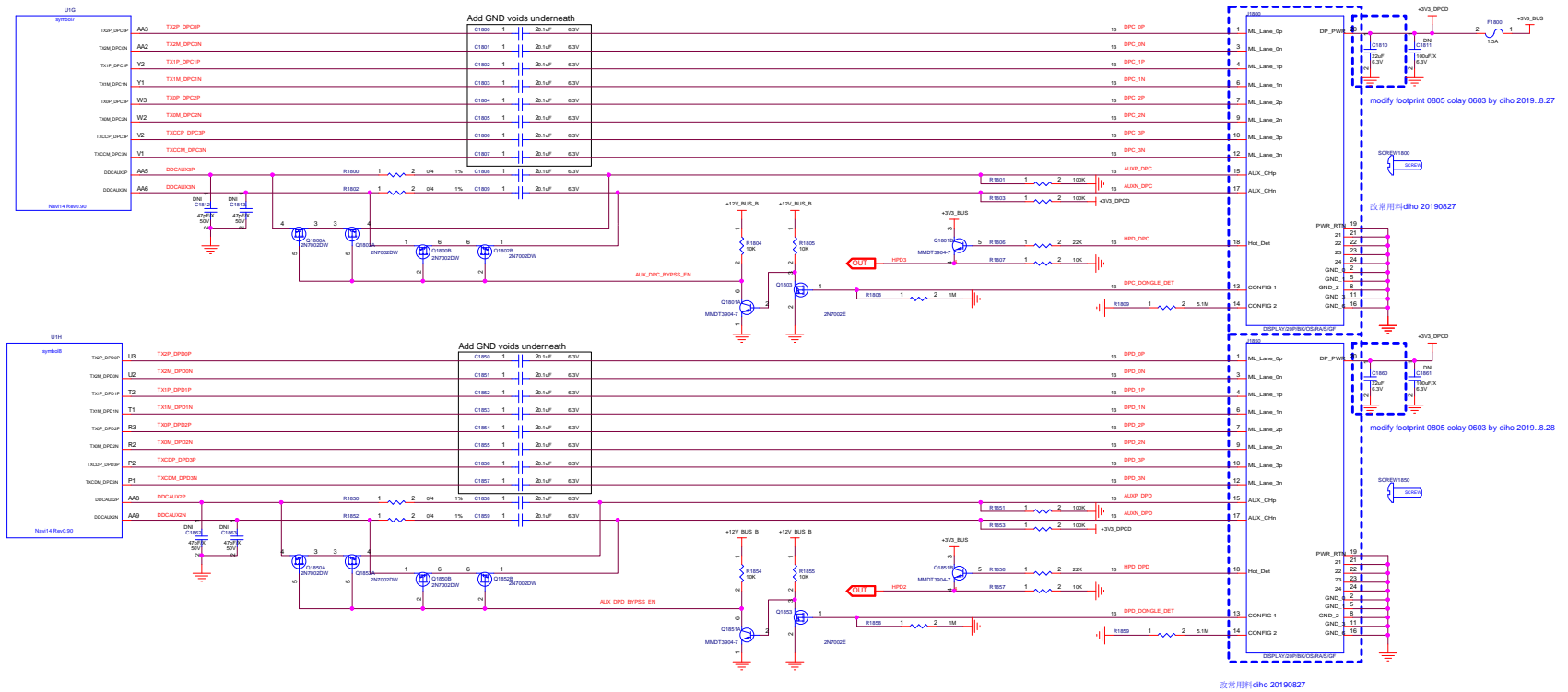


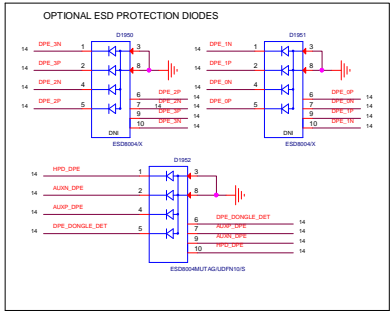
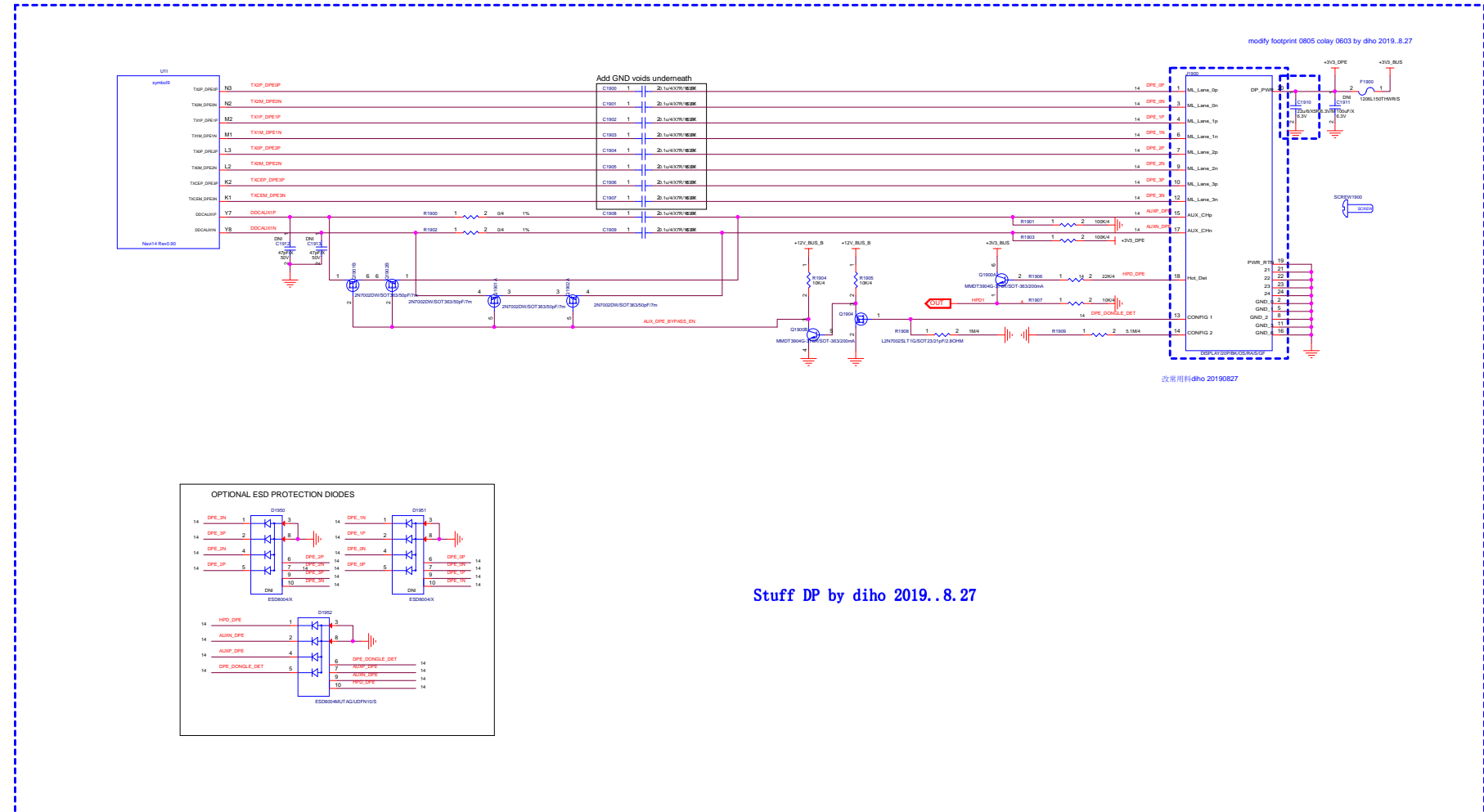






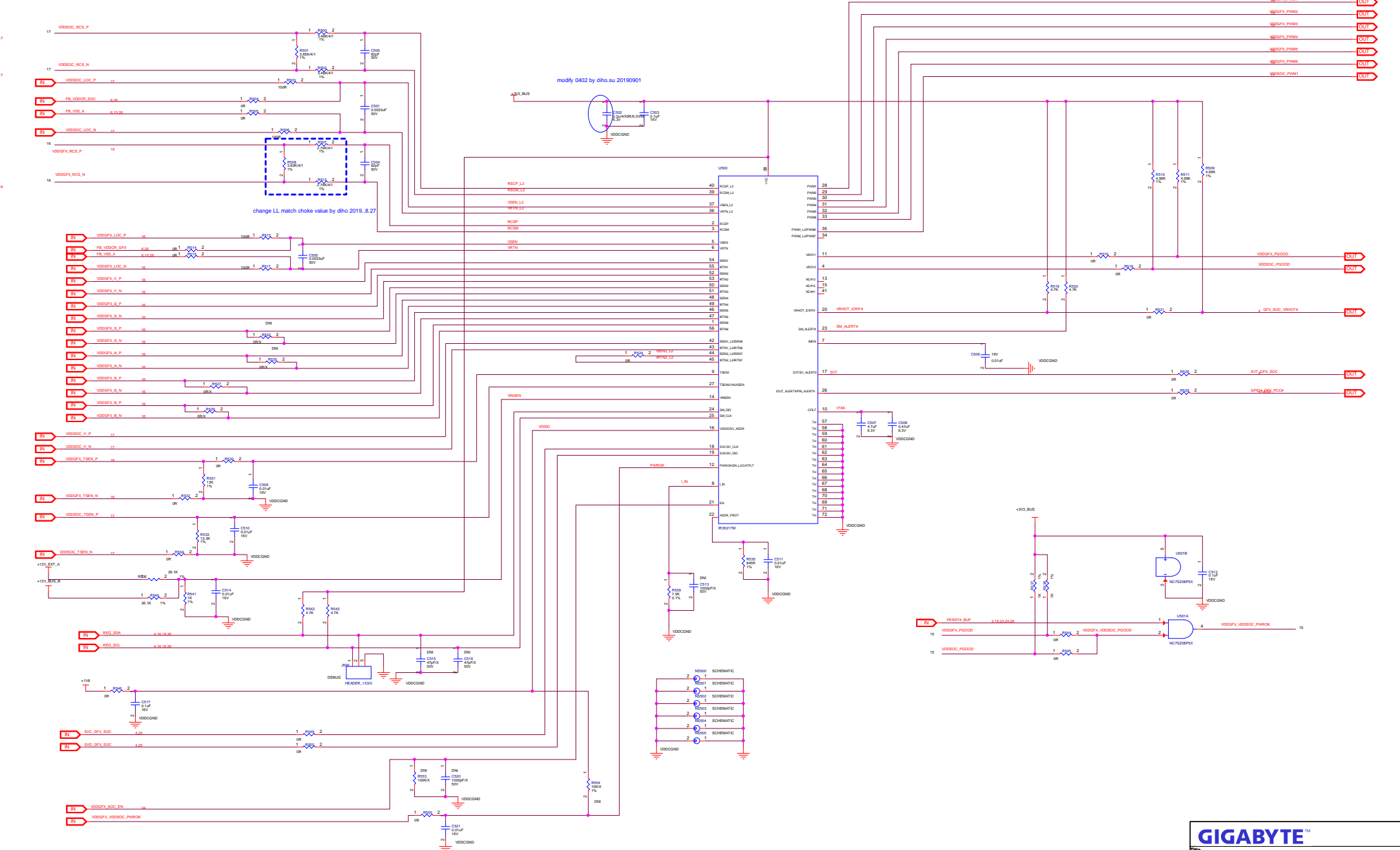




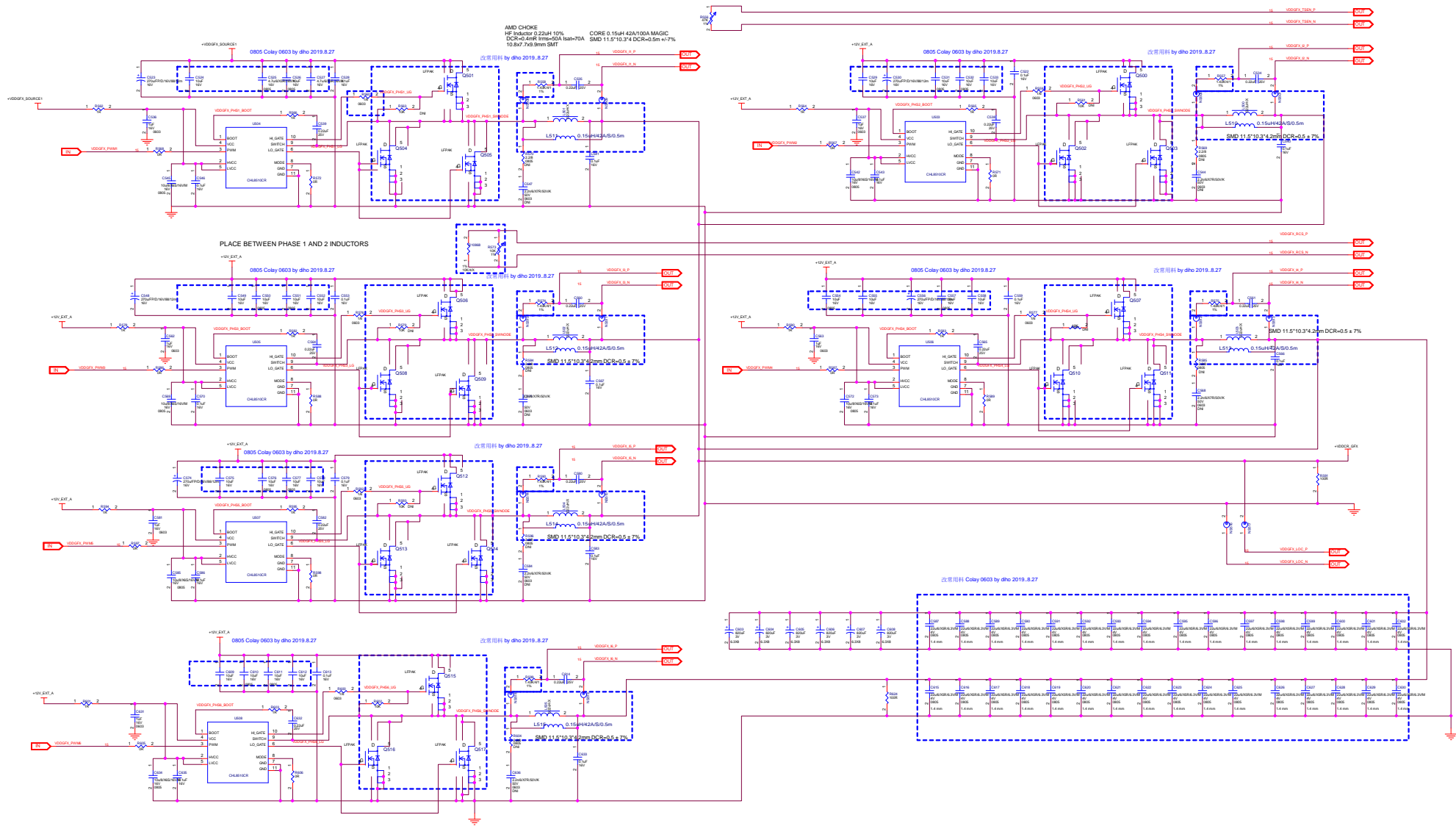


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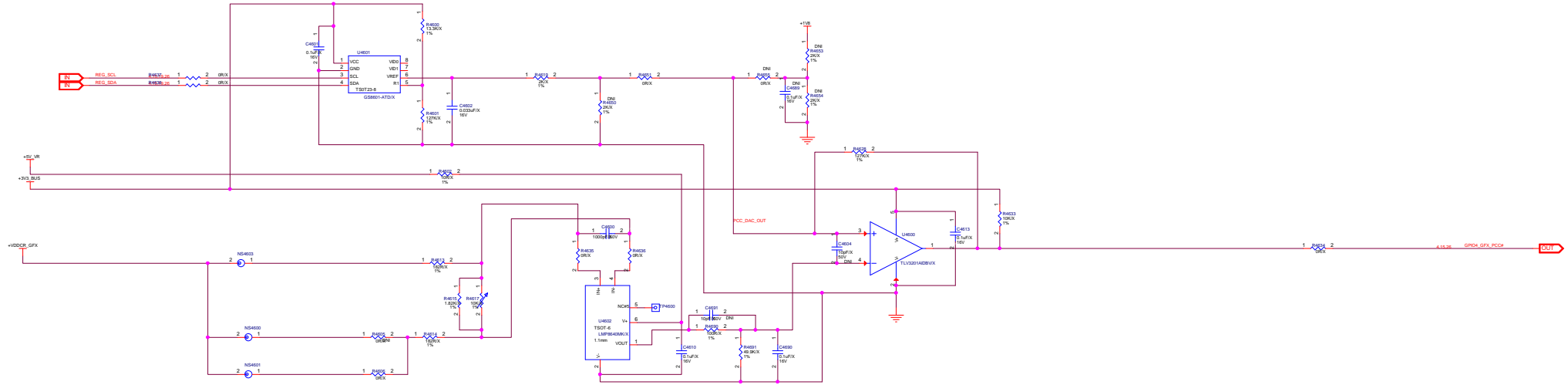
REG - VDDGX/VDDSOC CTRL

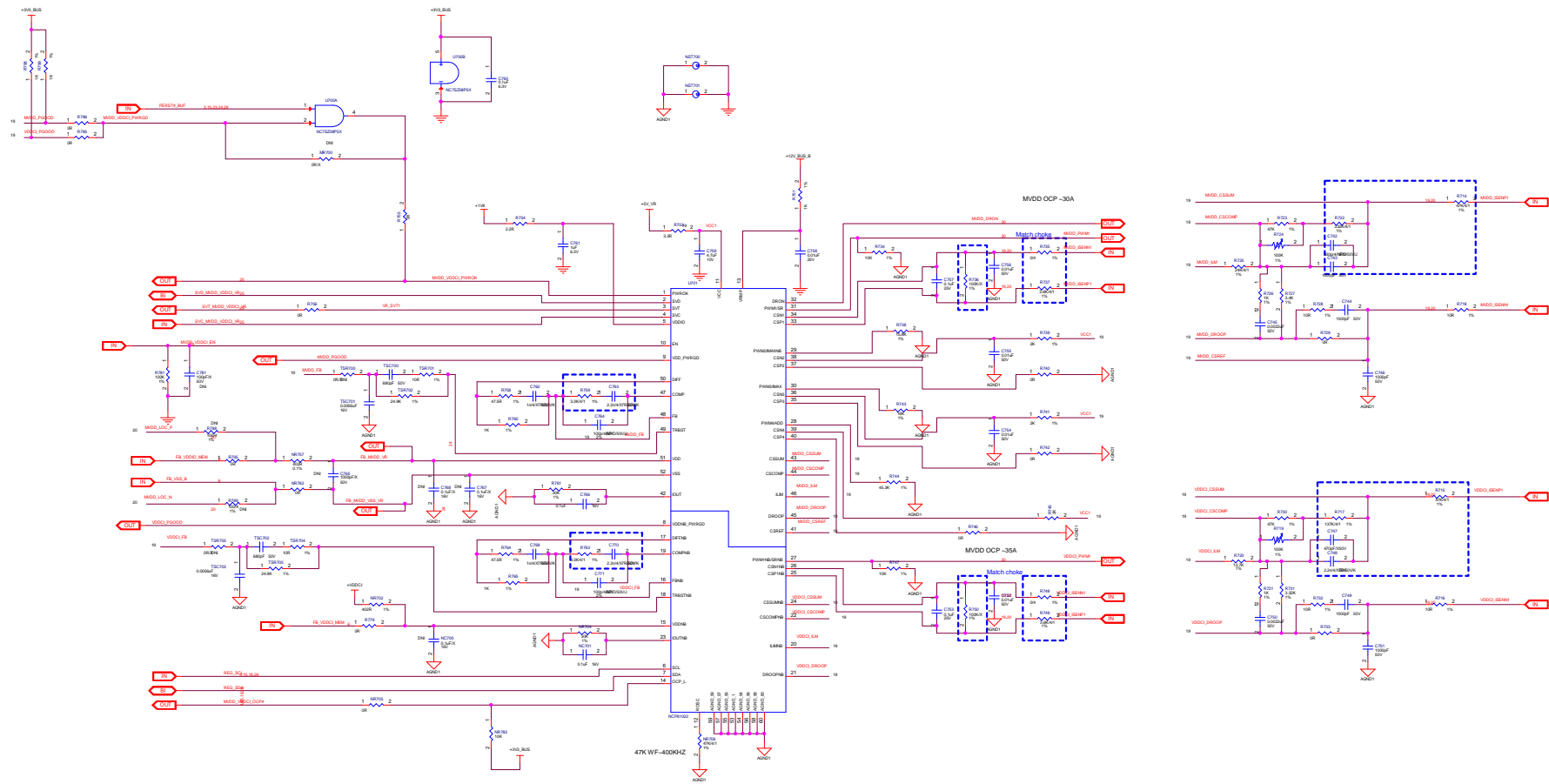


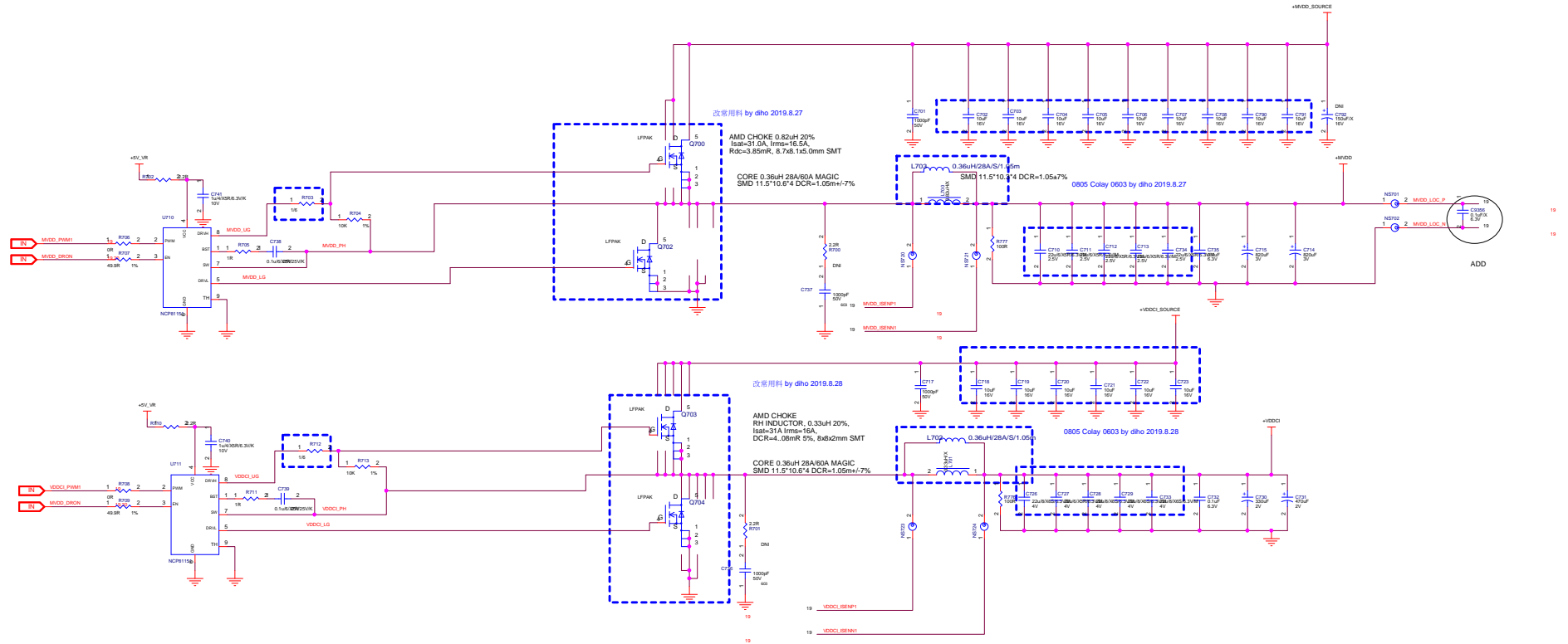
PLACE NEXT TO PHASE 3 HALF BRIDGE



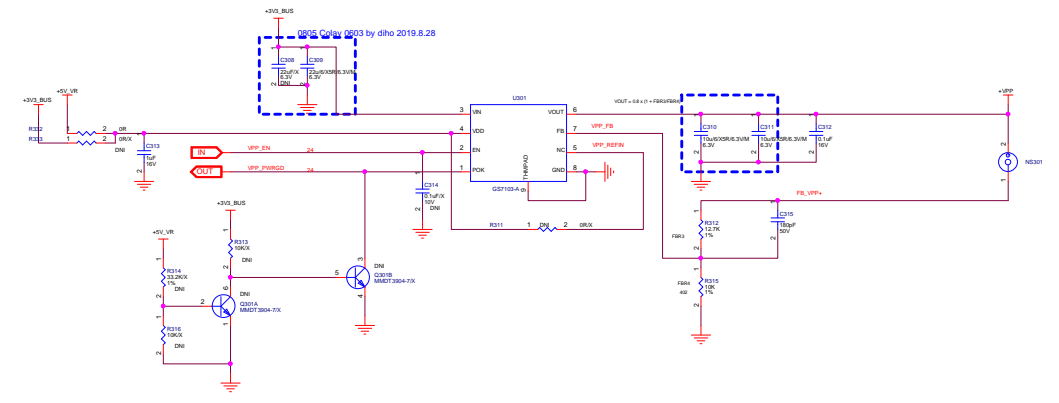
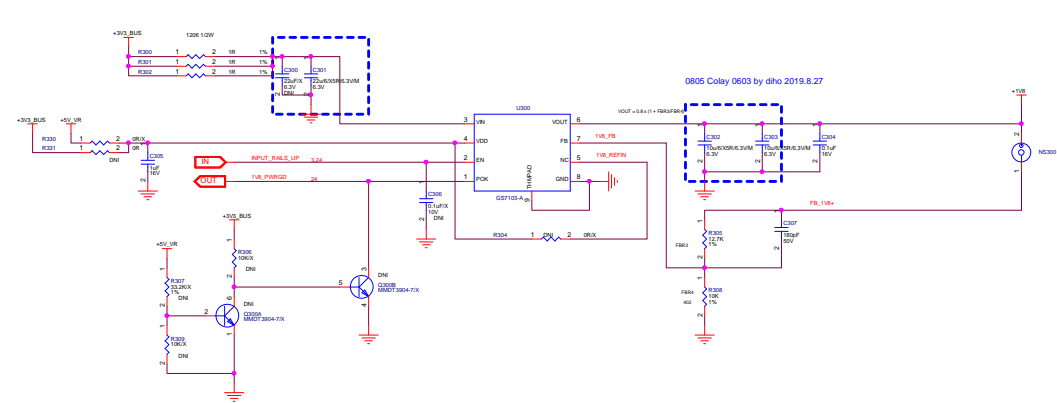
1.8V REFERENCE DAC
 INITIAL VOLTAGE = 1.8V
 I2C ADDRESS(7bit8bit) 0x53/0xA6



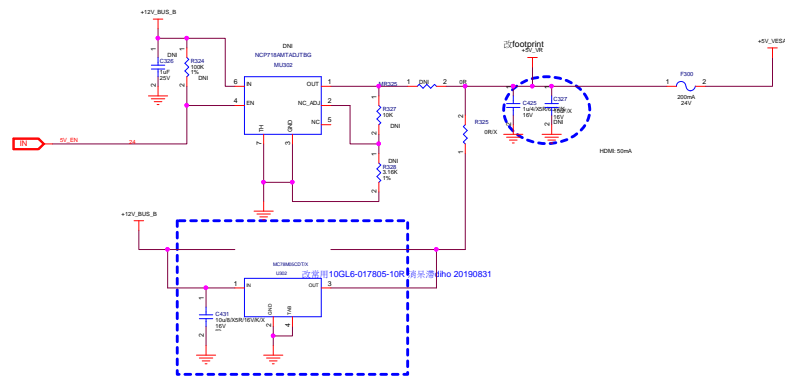


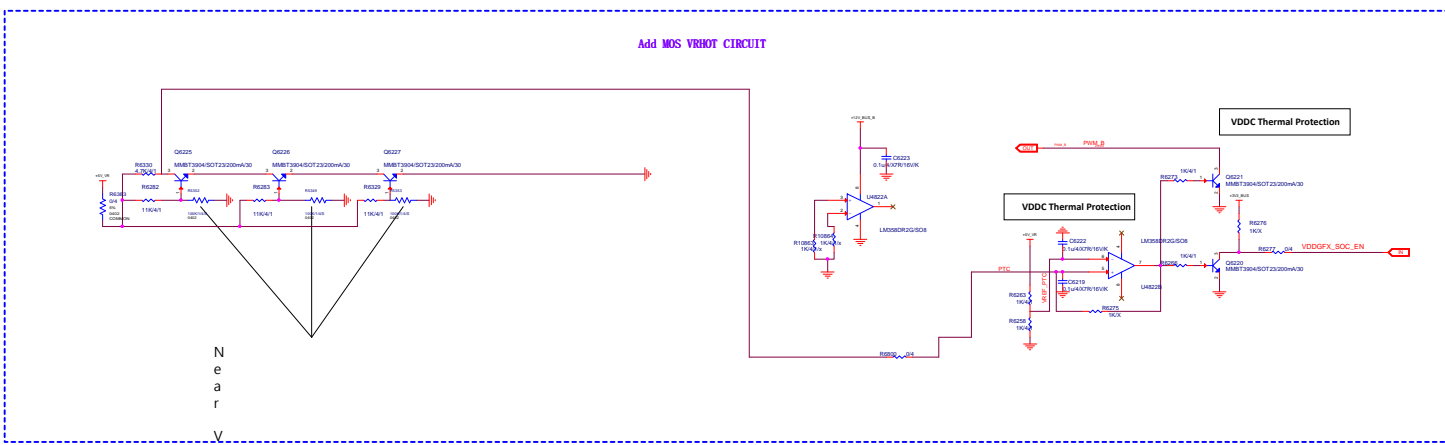
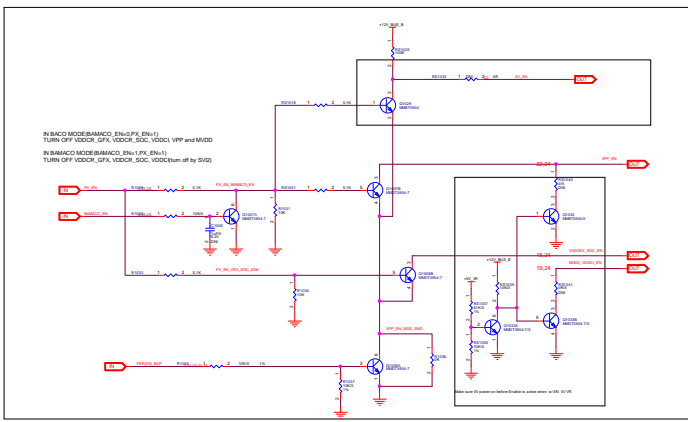
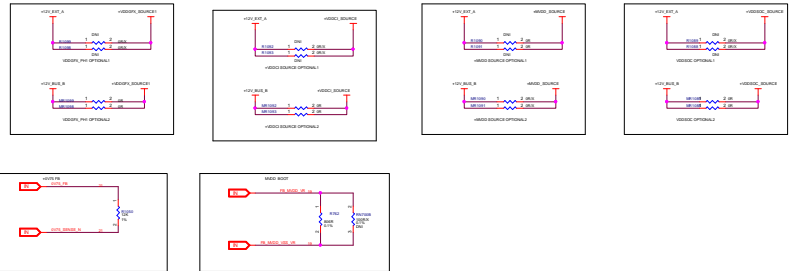
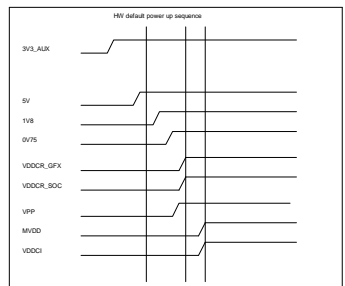
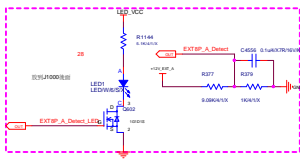
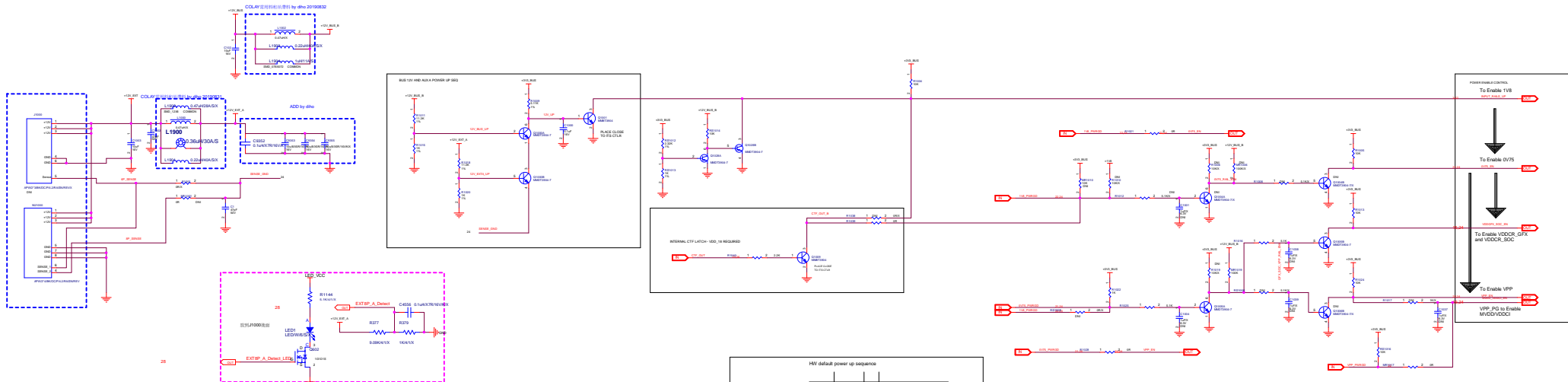


LDO - 1V8/VPP/5V



5V REGULATOR



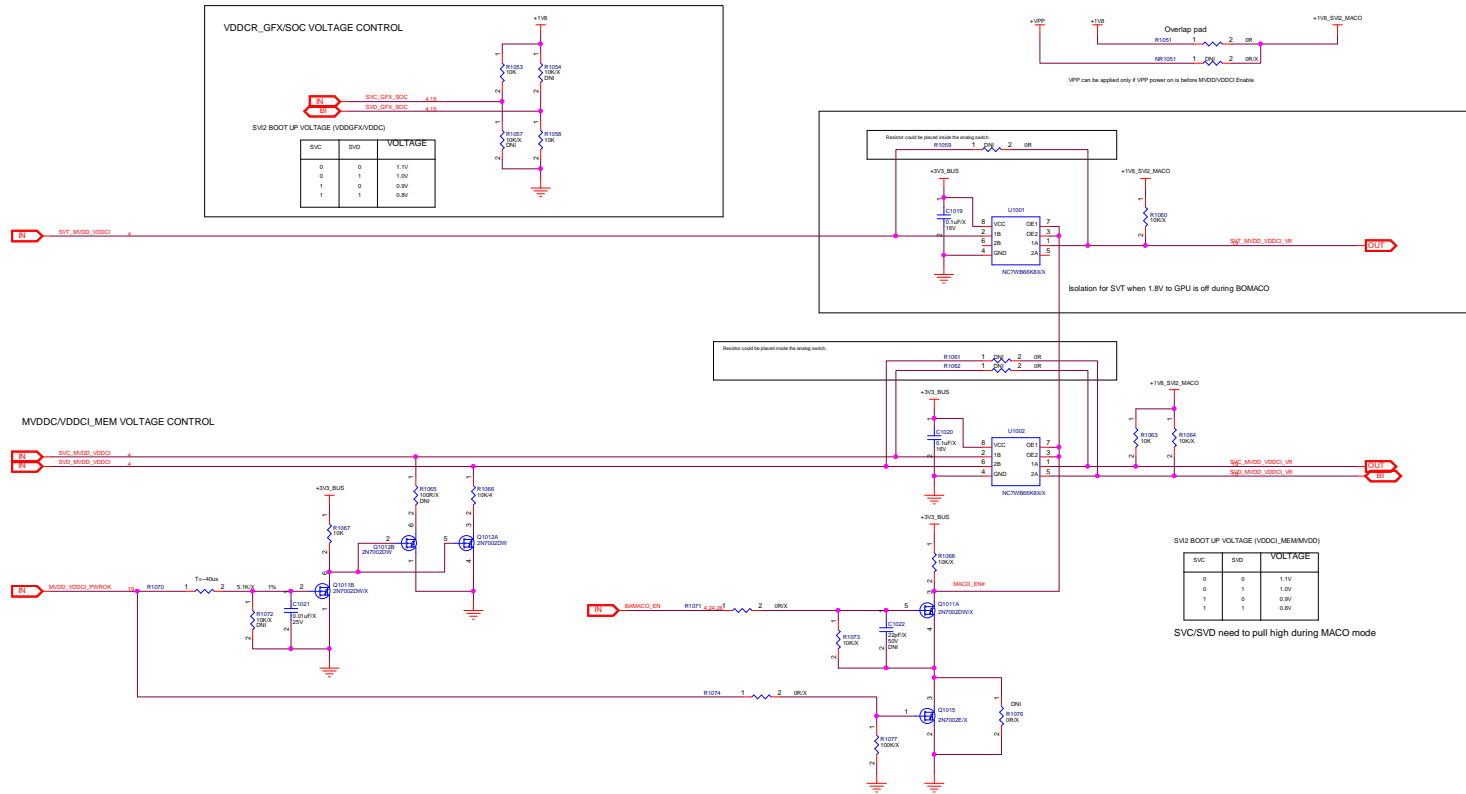


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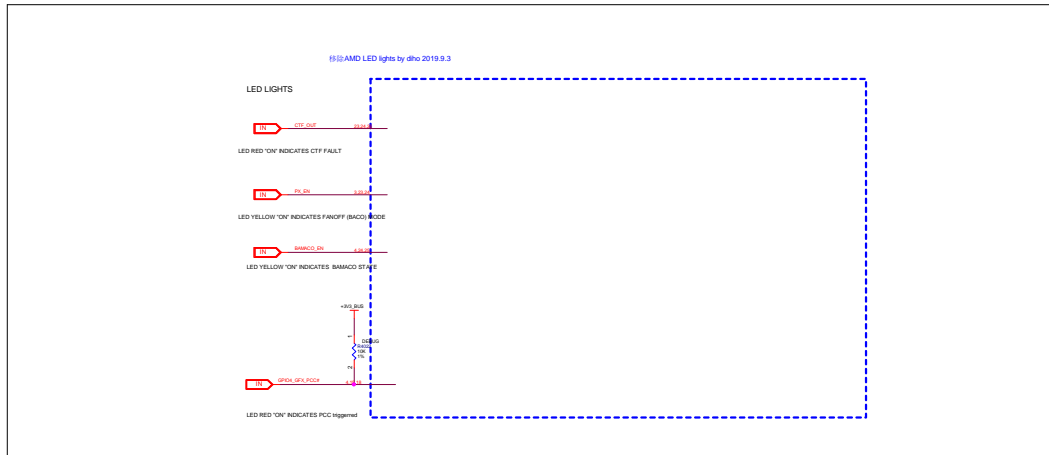
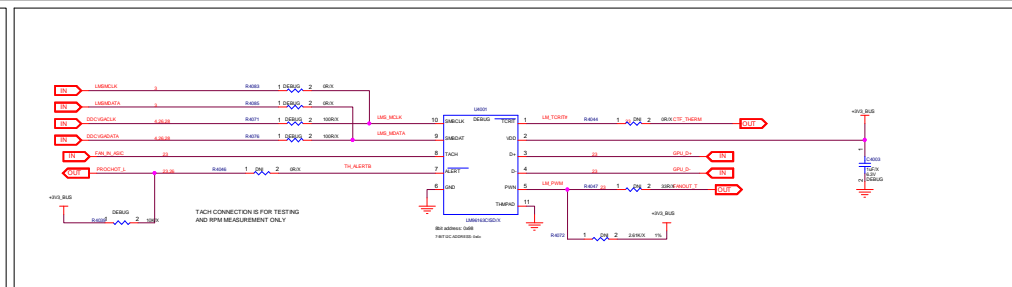
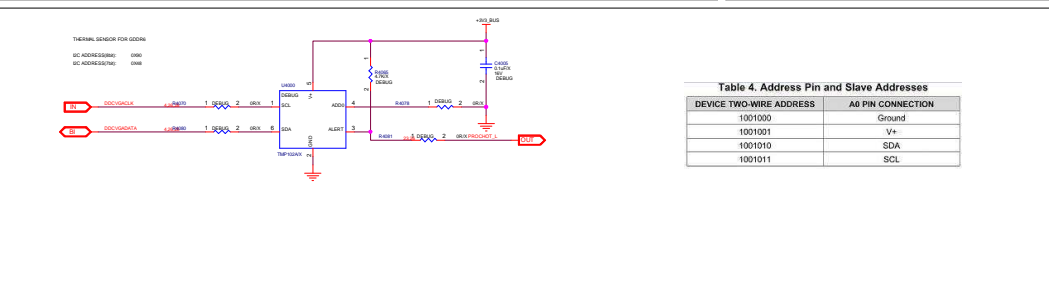
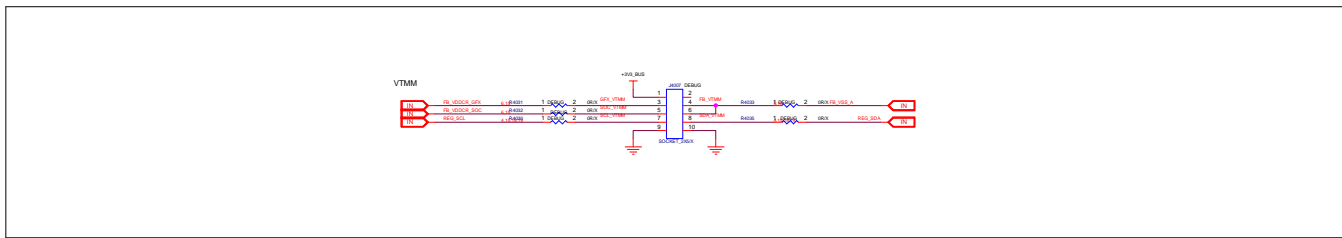
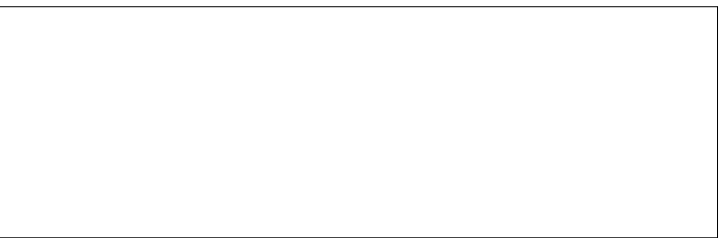
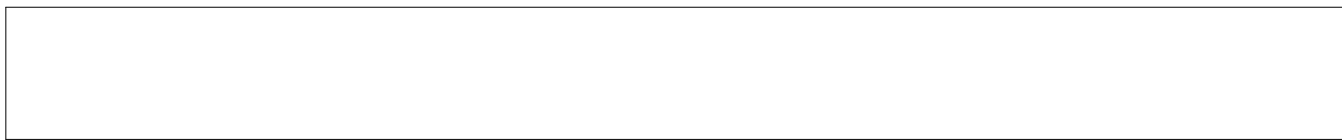
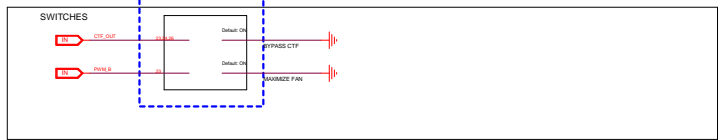
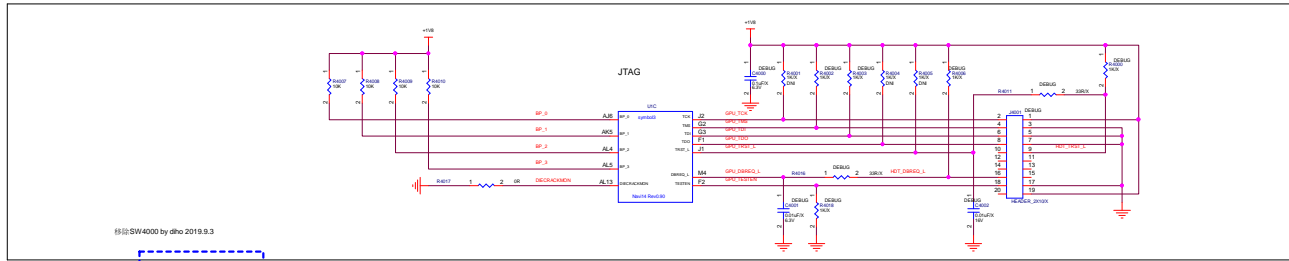
V
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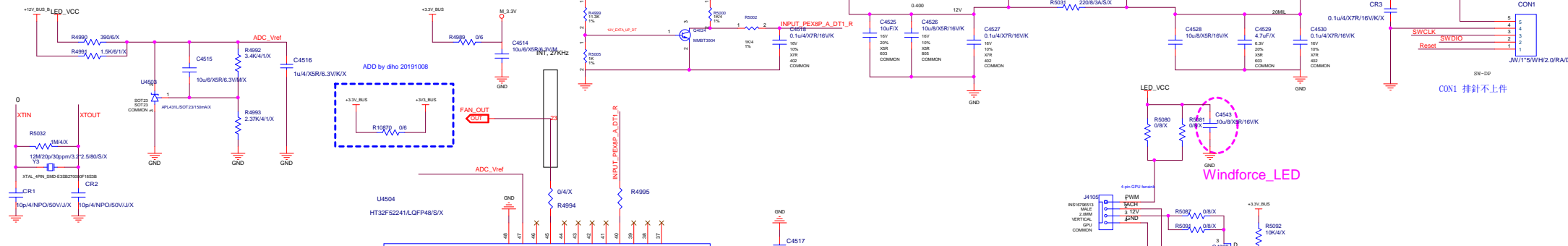


(29) DEBUG CIRCUIT

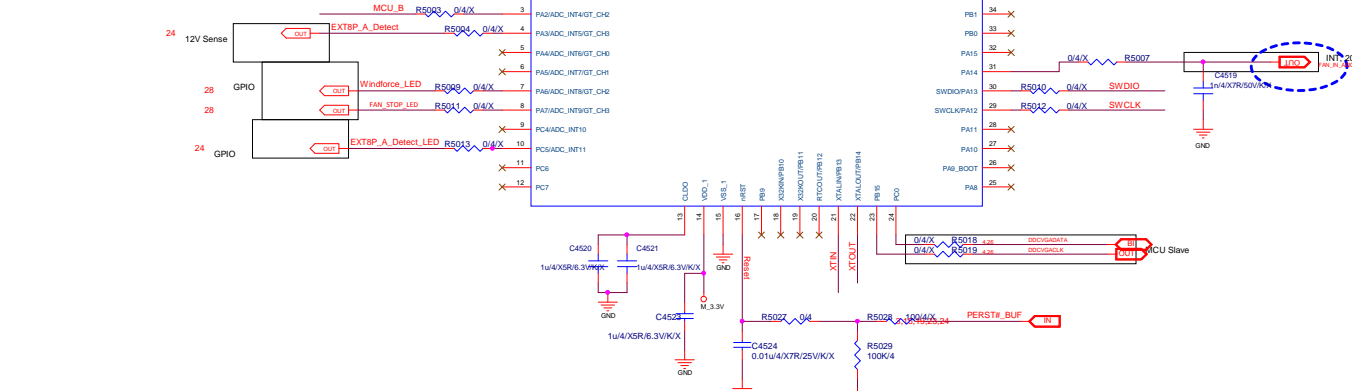


1.00	004	05/30/2018	Initial schematics
		12/28/2018	change all 41720105010 parts to 41720105000
1.00	008	04/16/2019	ADD 01150 01460 01600 01150 ADD R170 AND CHANGE M100 LOCAL SENSE POINT ADD R1000 R1003 M1100 M1100 and message gba phase1-3 input source ADD R4623 R4654 R4655 C4659 Change T01: 0.32uH/52001 160000 R148 308R3 162800000G NR704 30K/3 1603000000 R143 18C/1601602000 C147 470F/1H17004F1000 C148 220pF/4 170021000

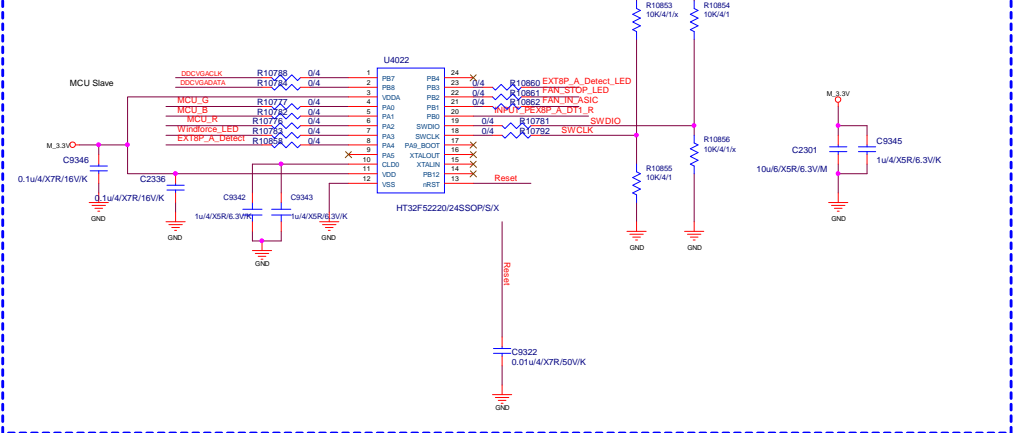
GIGABYTE™			
REVISION HISTORY			
Rev	Document Number	Rev	
1.0	GV-R55XTOC-8GD	1.0	
Date:	Wednesday, October 23, 2019	Sheet	27 of 28



FAN Stop LED



COLAY HT23F52220 for costdown by diho.su 20190902



Windforce_LED

