

PG161-A00

TU106 6GB GDDR6, 192b, X16 DVI-D/DP + DP + HDMI


TABLE OF CONTENTS

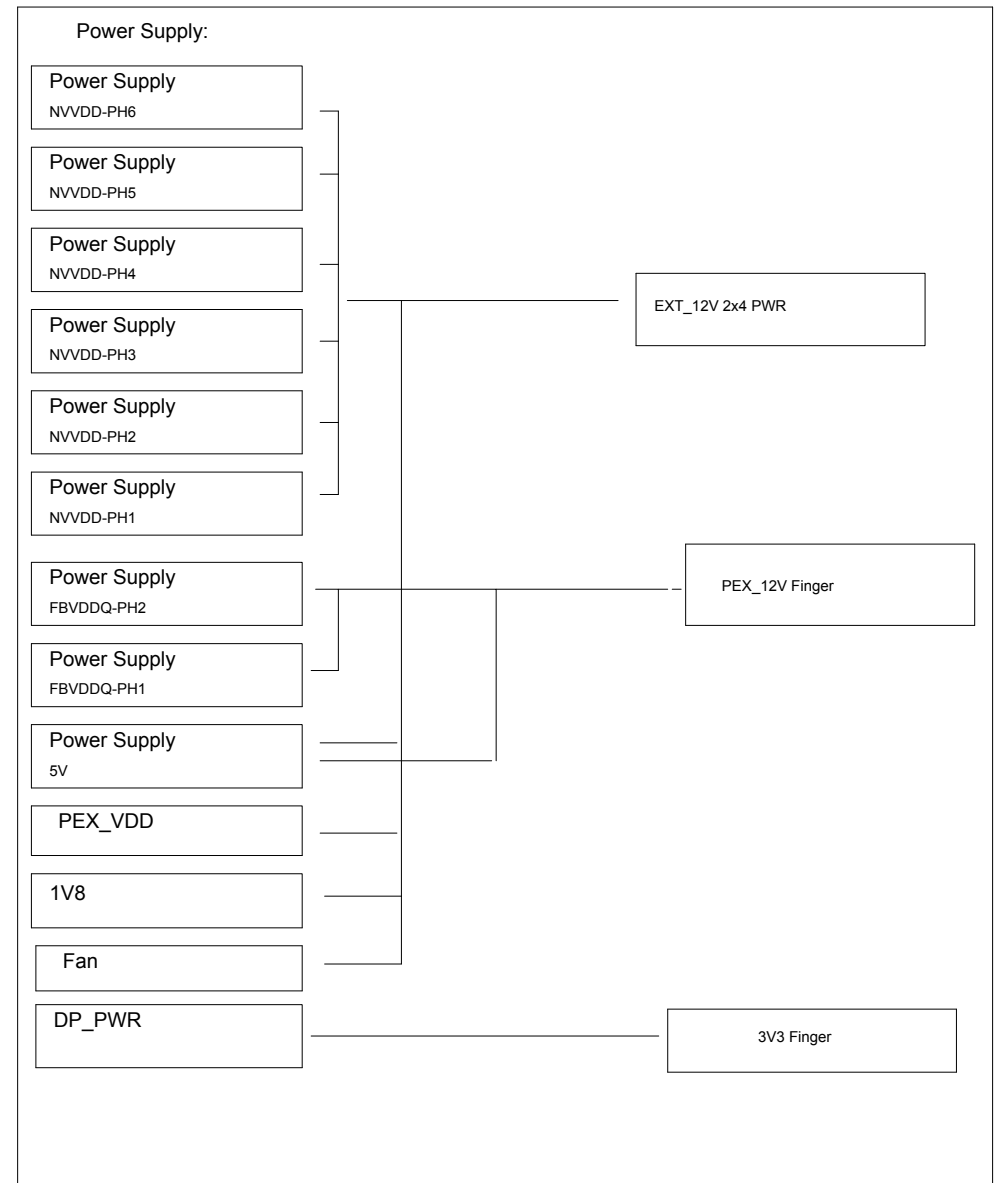
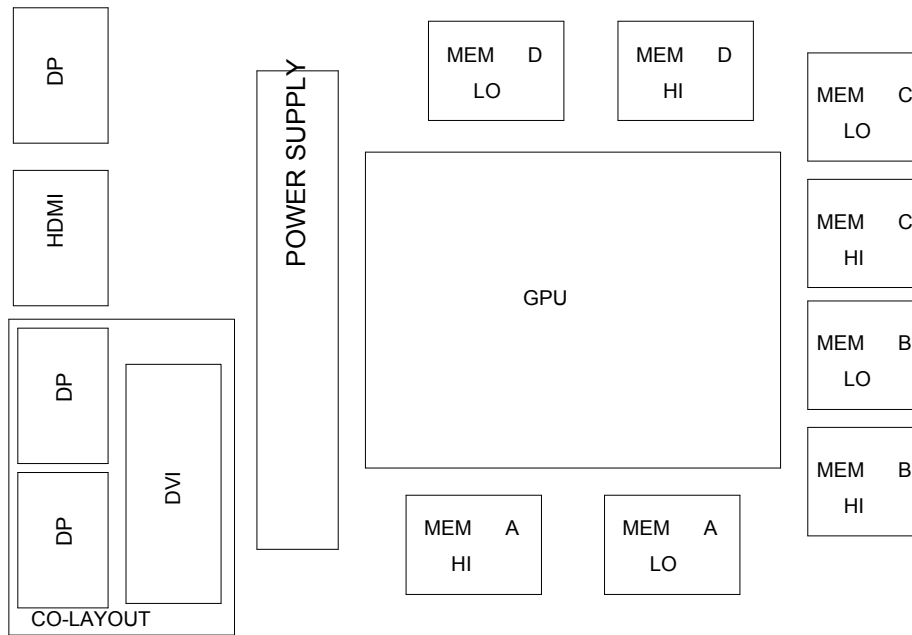
Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCIE RC TERM
5	MEMORY: GPU_FB_AB
6	MEMORY: FBA[31:0]
7	MEMORY: FBA[63:32]
8	MEMORY: FBB[31:0]
9	MEMORY: FBB[63:32]
10	MEMORY: GPU_FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	GPU PWR & GND
16	GPU Decoupling
17	GPU Decoupling2
18	IO: IFPAB DVI-D-DL
19	IO: IFPA DP
20	IO: IFPB DP
21	IO: IFPE & IFPF USBC NC
22	IO: IFPC HDMI
23	IO: IFPD DP
24	IO: NVHS Interface and Frame Lock
25	MISC1: Thermal, JTAG, GPIO, STEREO

Page	Description
26	MISC2: ROM, XTAL, STRAPS
27	PS: 1V8_AON
28	PS: 5V
29	PS: PEXVDD
30	PS: FBVDDQ
31	PS: FBVDDQ PH2
32	PS: NVVDD Controller
33	PS: NVVDD Controller OVR3i
34	PS: NVVDD Phase 6,4
35	PS: NVVDD Phase 3,5
36	PS: NVVDD Phase 2,1
37	PS: Input Power Balancing Switcher
38	PS: Input, Filtering, and Monitoring
39	PS: STEERING, UPB & HOT-UNPLUG
40	PS: Type-C BuckBoost
41	PD PPC
42	PS: 12V & 3V3_A SWITCHER
43	SEQ: 5V, 1V8, NV3V3 ENABLE
44	SEQ: NV, PEX, FB ENABLE
45	SEQ: VOLTAGE MONITOR
46	SEQ: DISCHARGE
47	SEQ: MISC
48	LOGO LED
49	LED DRIVER & BOOST
50	FAN

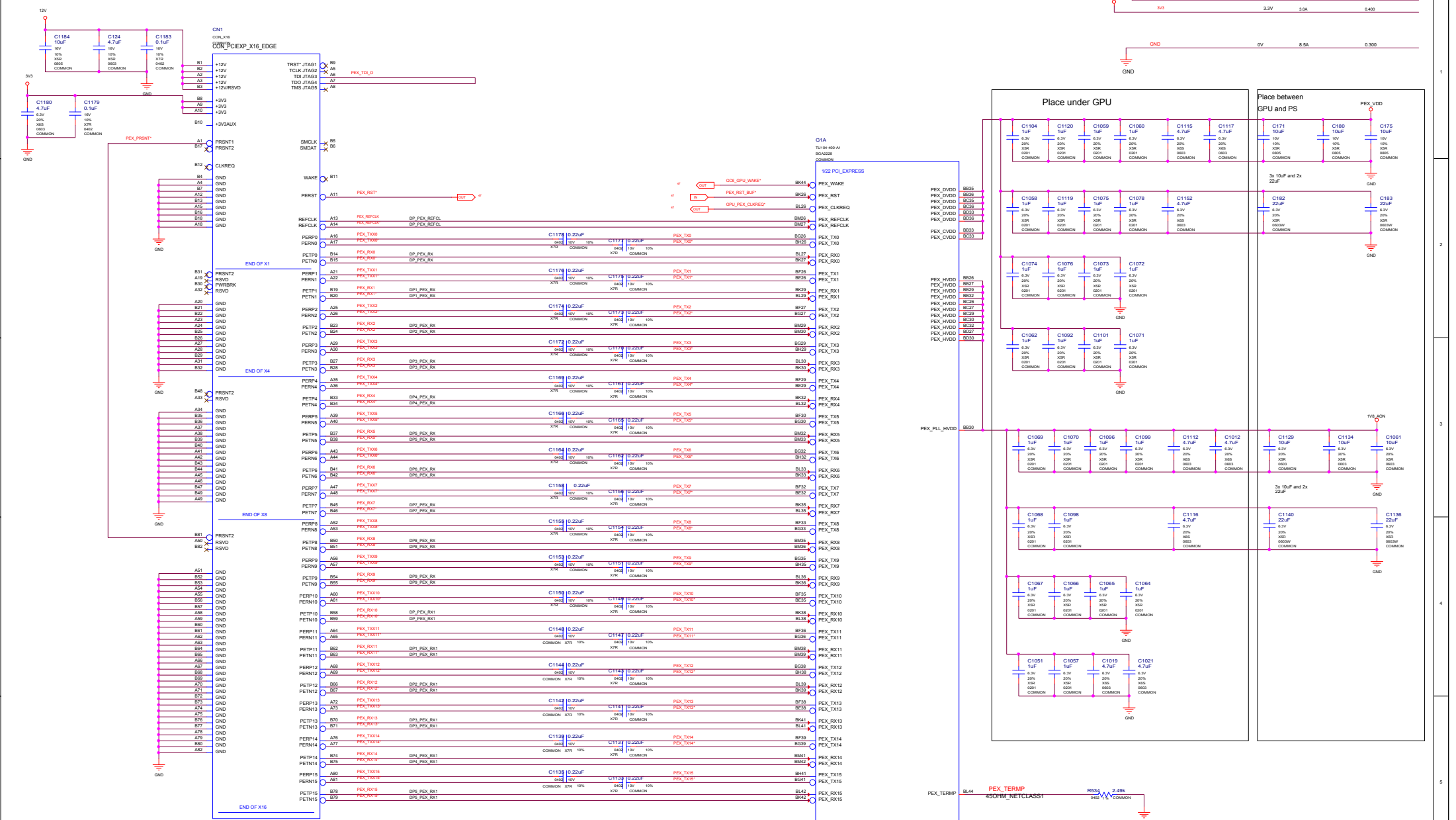
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51	PS: Pre-filter
52	MECH
53	PTC
V375-20	
1. 移除 CO-LAY	
2. Core Power: uP9512SQKI (QFN 4x4) + (NCP302045 x 4)	
Memory Power: I32-S725602-N03 + (UBIQ 3103+3107*2)	
3. P.34 add R779	
4. P.30 & 44 移除PS_FBVDQ_BUFF換頁符號	
換 FBVDQ controller · 換成1PHASE 上1下2	
5. P.52 add HDMI & DVI 螺絲	
6. IO 換常用料 · footprint 不變	
V379-10	
線路:	
1. 基於V375-1.2刪除GDDR6貼PG165 SKU0 GDDR5線路 ·	
拉GPIO10做VREF ·	
2. DRAM Power MOSFET改成Dual-N MOSFET ·	
物料:	
1. 基於V375-58S DRAM PWM換成NIKO / GS7222	
並調成GDDR5電壓準位 · 相數2改1 ·	
2. Core Power相數4改3 ·	
3. OVR-M換UPI / USS650 ·	

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MICRO-STAR INT'L CO.,LTD			
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Size	Document Description	Rev	
Custom	Page1: Table of Contents	1.0	
Date:	Monday, January 14, 2019	Sheet	1 of 53



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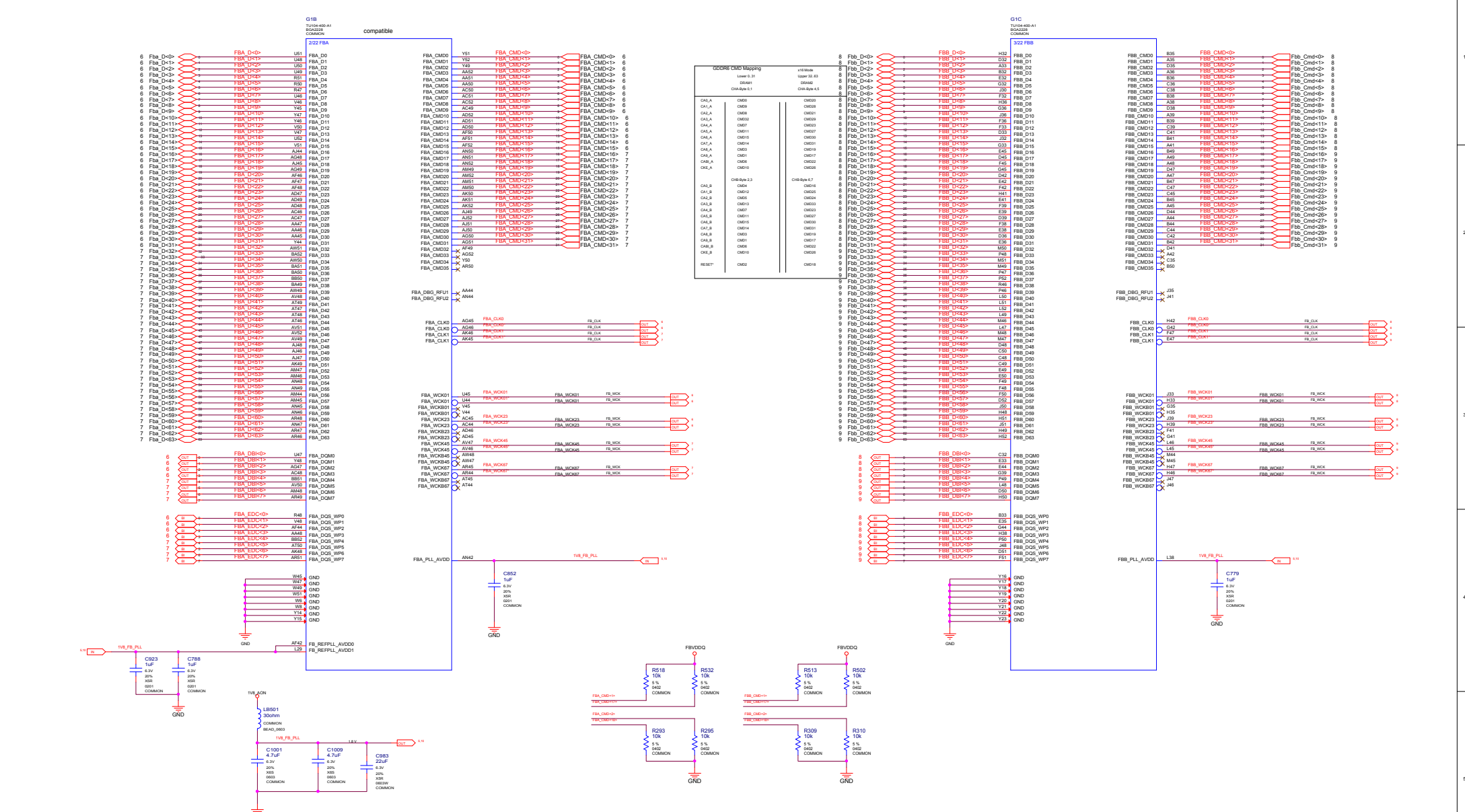
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		Size: Custom	Document Description: Page3: PCI Express
Date: Tuesday, January 15, 2019		Sheet: 3 of 53	

NO PEX GEN4 SUPPORT DELETE RC TERMINATIONS


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Custom	Page4: PCIE RC TERM	1.0
Date:	Monday, January 14, 2019	Sheet 4 of 53



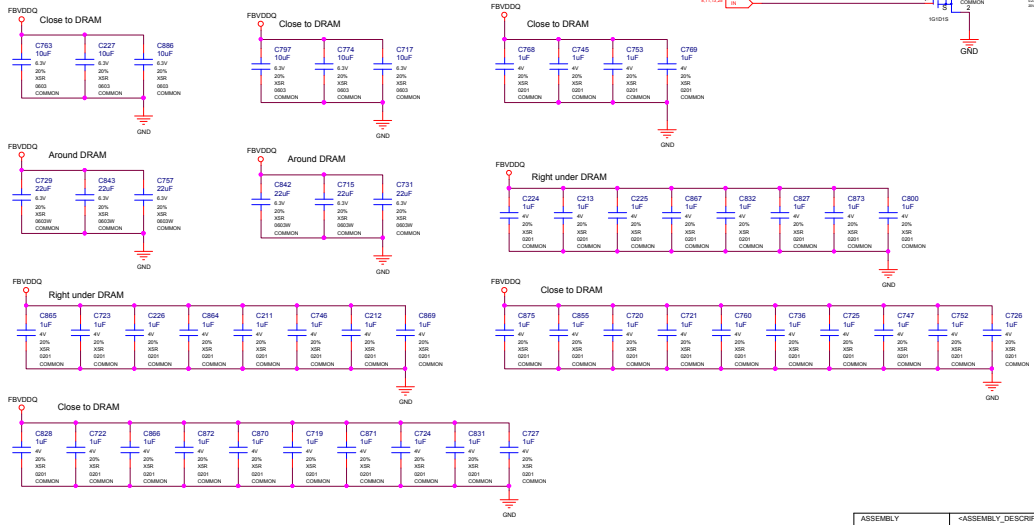
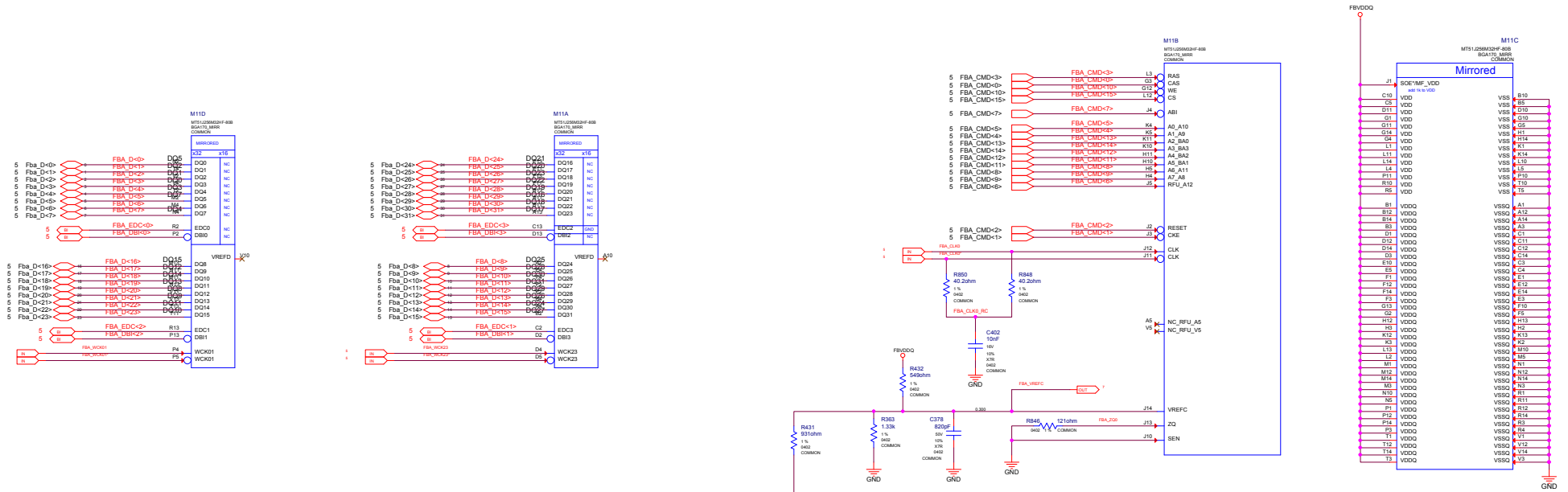
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MS-V379

Size	Document Description	Rev
Custom	Page5: MEMORY: GPU Partition A/B	1.0

Date: Tuesday, January 16, 2019 (Sheet 5 of 63)



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MS-V379

Doc: Custom Page: MEMORY: FBA Partition 31.0 Rev: 1.0

Date: Tuesday, January 15, 2018 Sheet: 8 of 13

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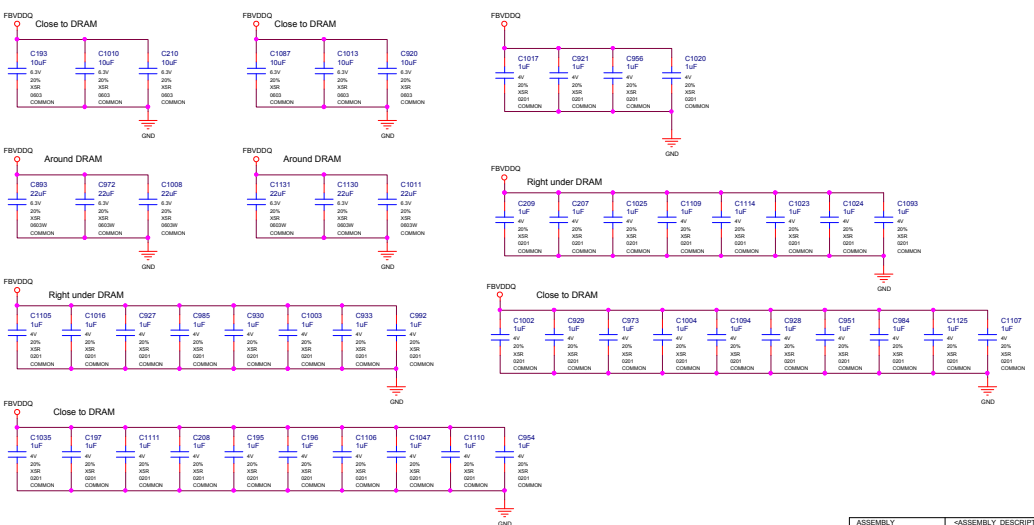
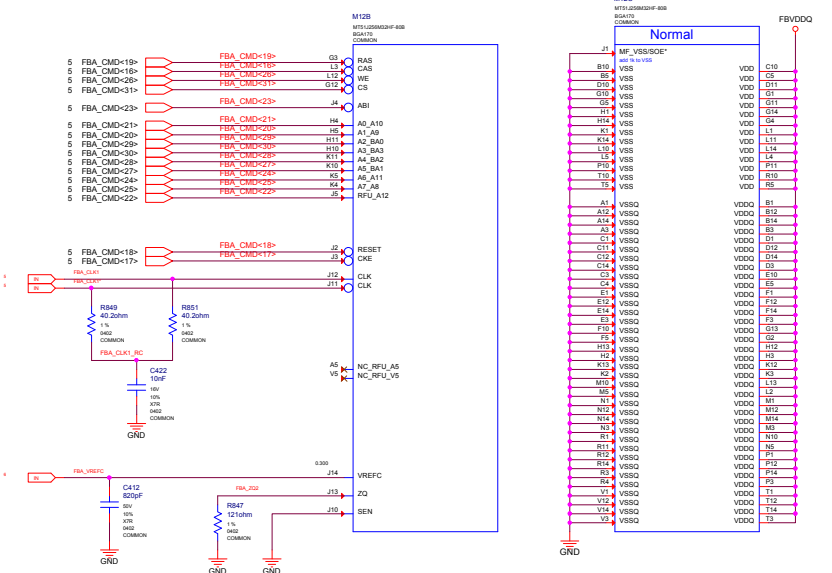
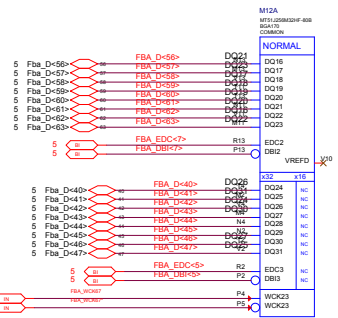
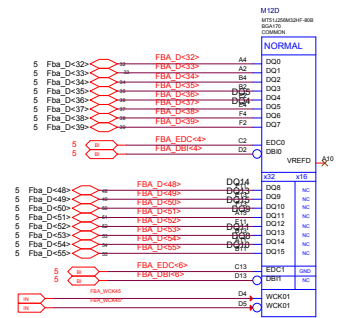
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BOM REV B

PAGE 5 OF 42

DATE 14-DEC-2018

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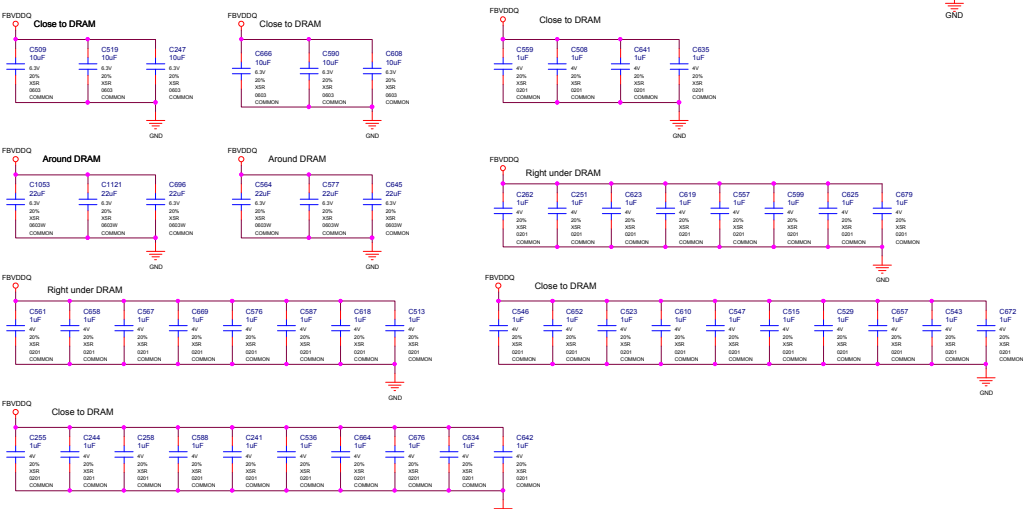
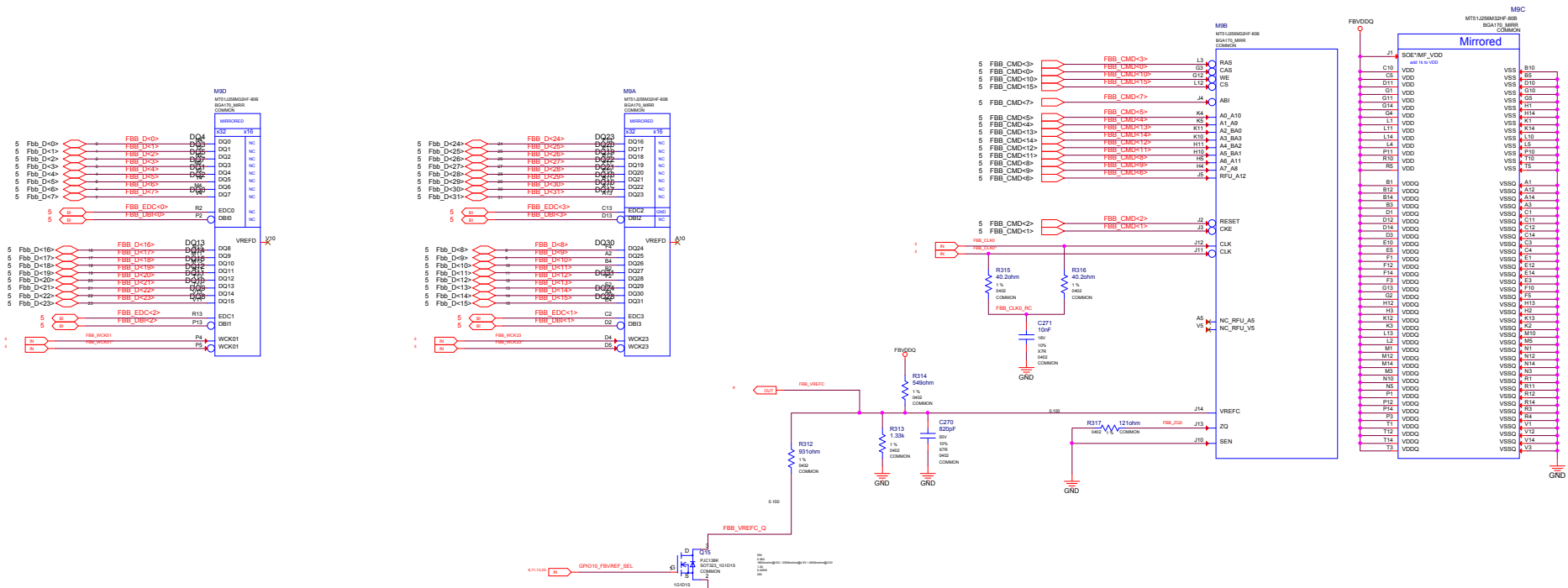
Date: Tuesday, January 15, 2018 Sheet: 7 of 53

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NV_PN	600-1G165-BASE-000
PCB REV	PG165-ADD
BOM REV	B
PAGE	6 OF 42
DATE	14-DEC-2018

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Date: January 15, 2019 | Sheet 8 of 83
 Rev 1.0

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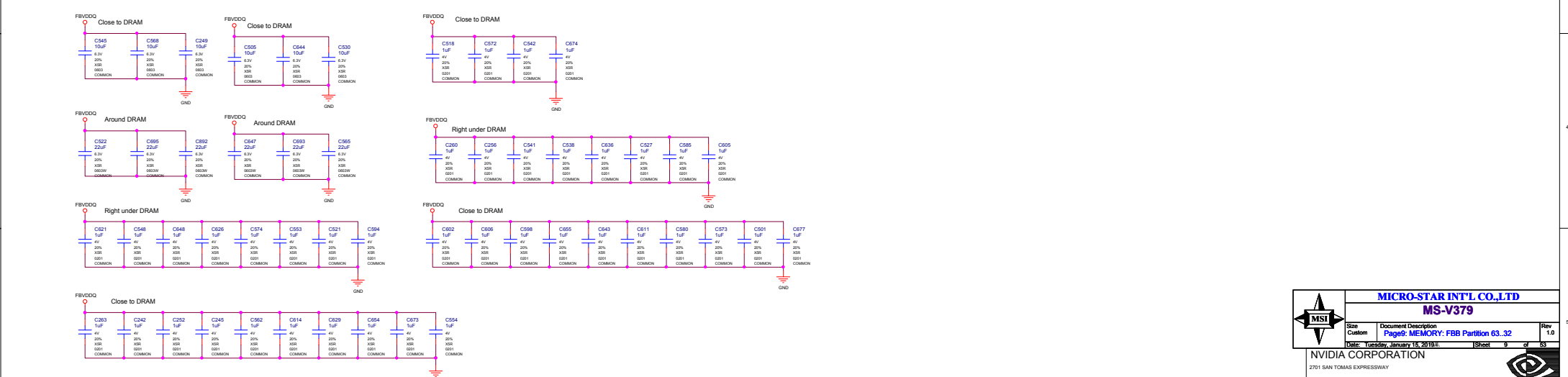
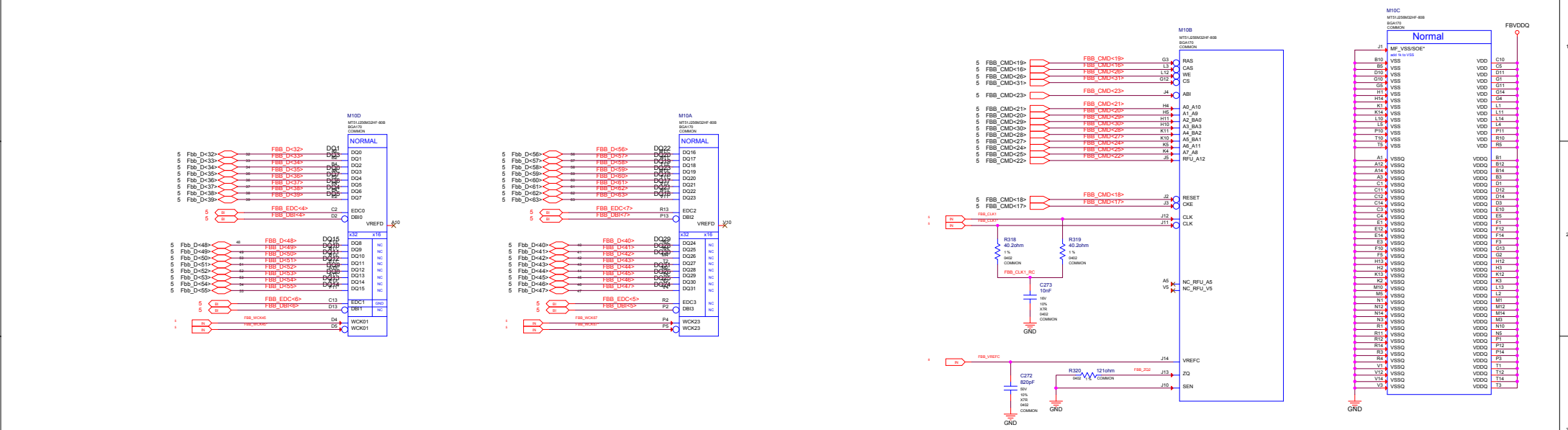
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PAGE
 DATE

7 OF 42
 14/DEC/2018

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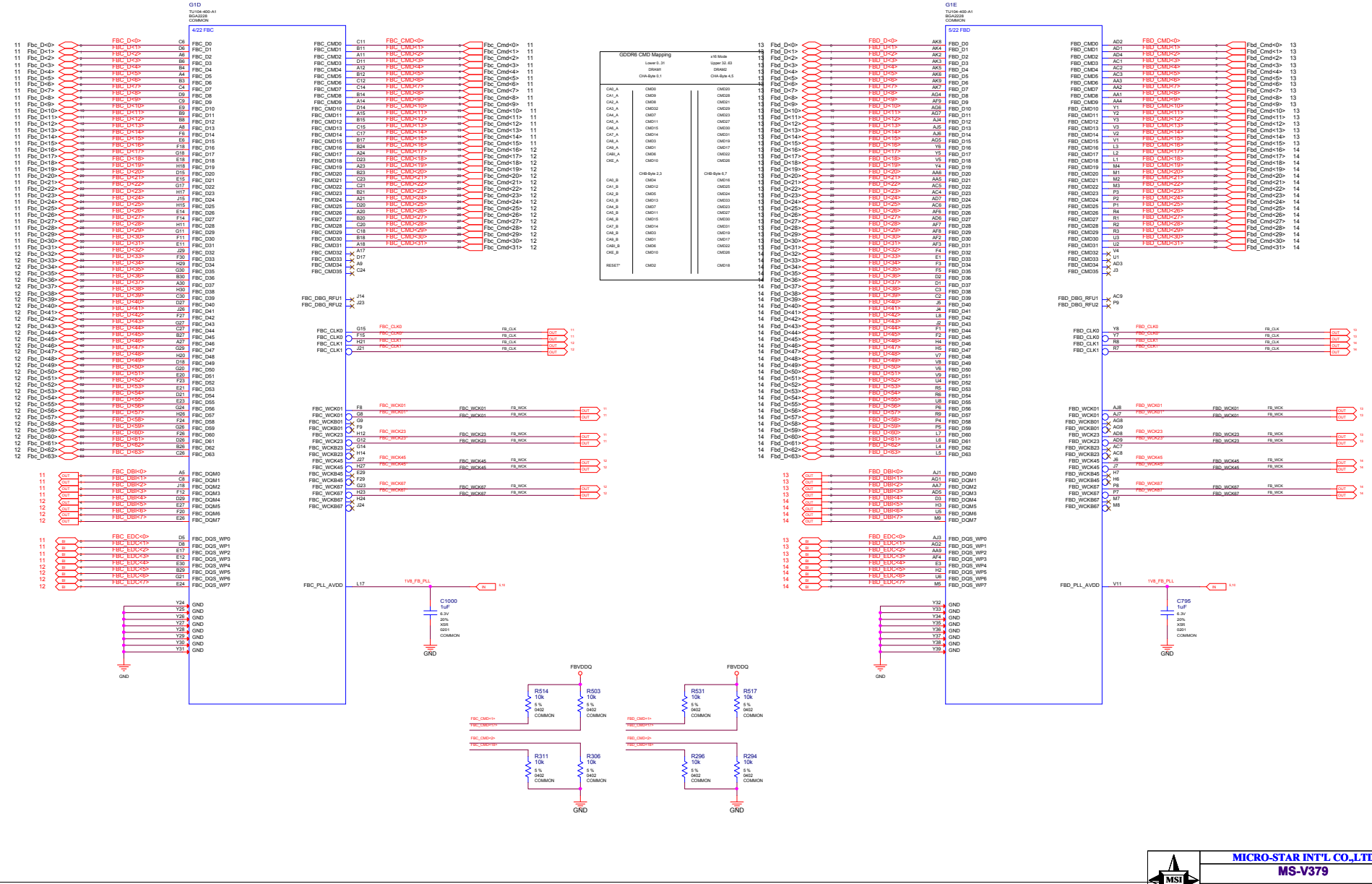
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MICRO-STAR INT'L CO.,LTD
MS-V379

Size: Custom | Document Description: Page9: MEMORY: FBB Partition 63..32 | Rev: 1.0
Date: Tuesday, January 15, 2019 | Sheet: 9 of 63

NVIDIA CORPORATION
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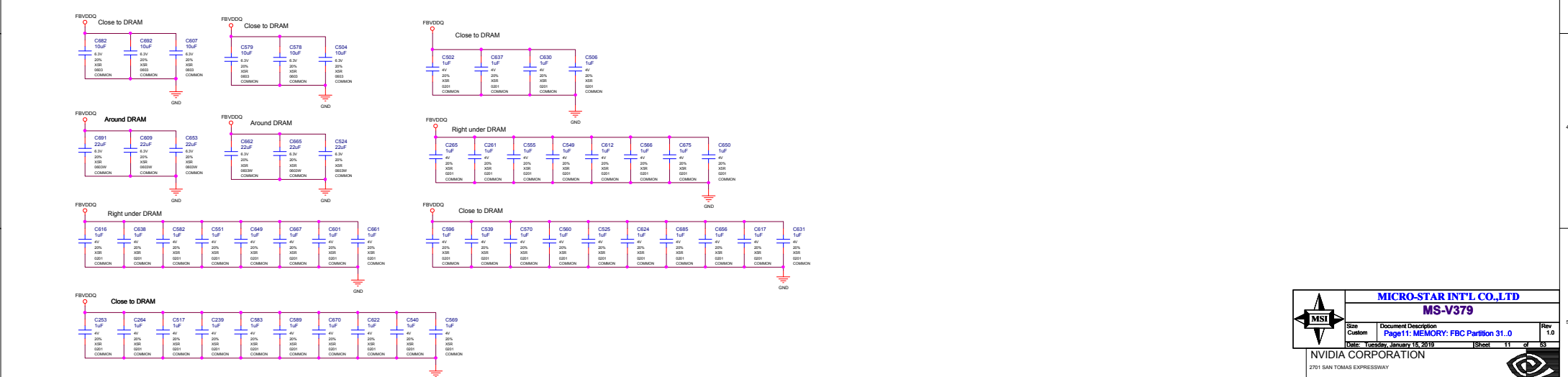
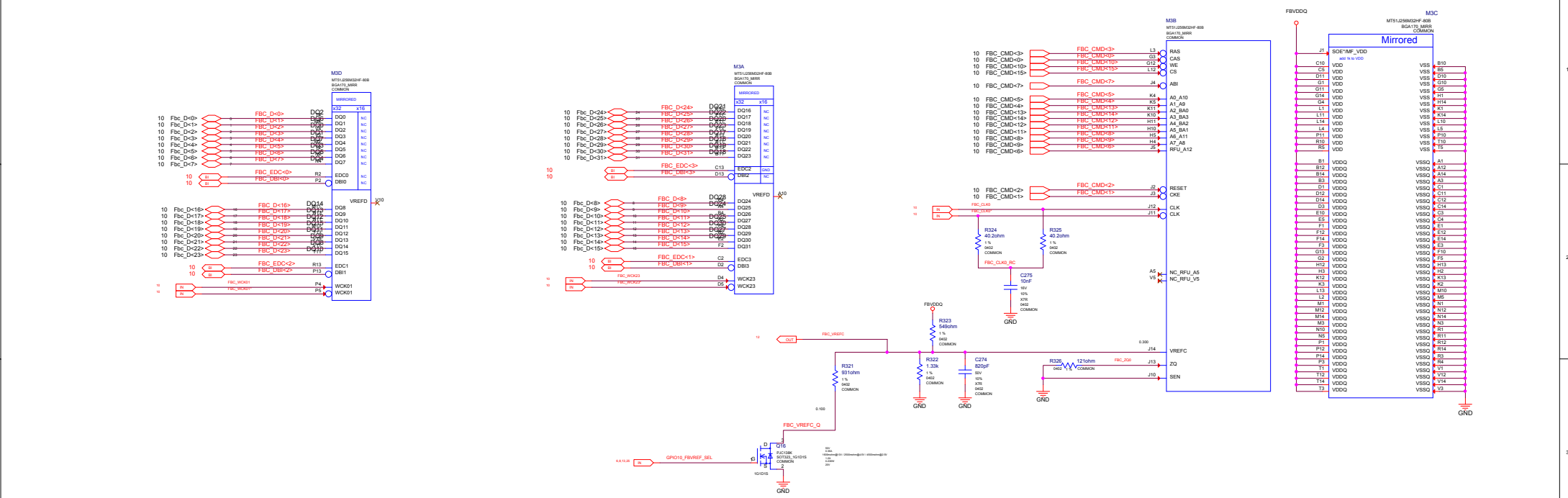
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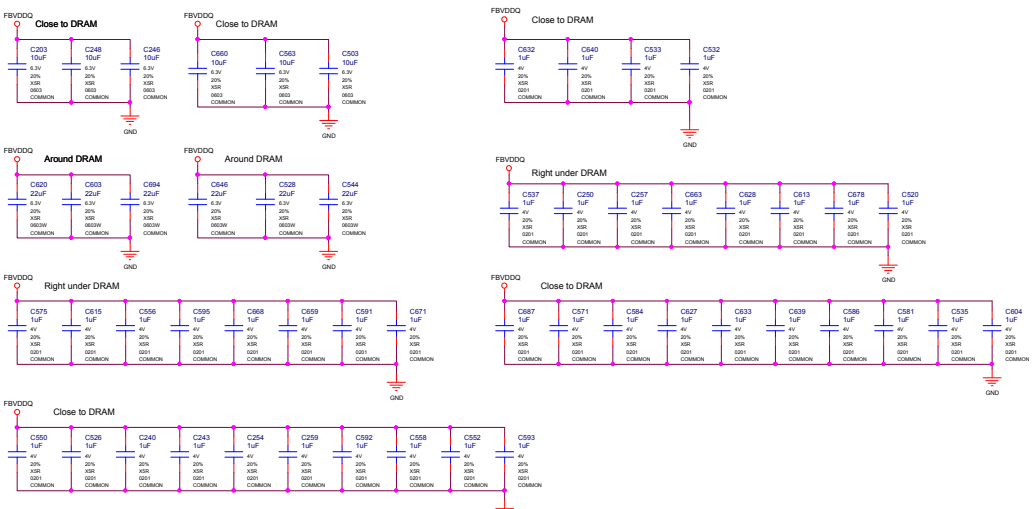
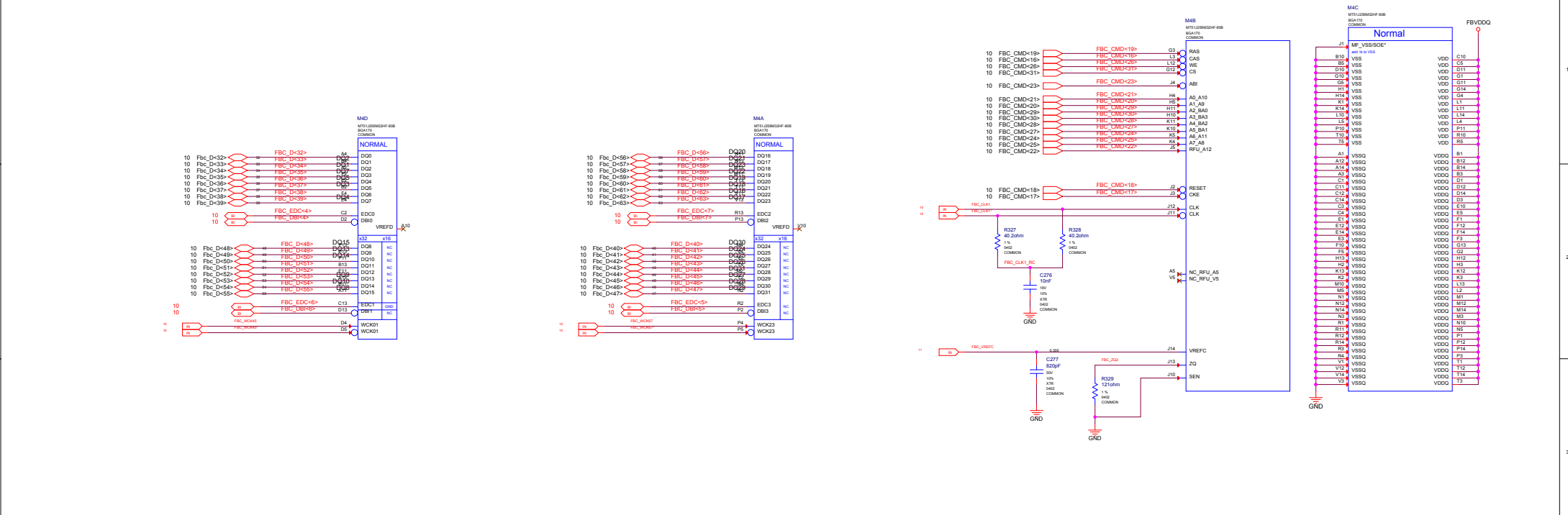
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MS-V379

Size	Document Description	Rev
Custom	Page10: MEMORY: GPU Partition C/D	1.0
Date:	Tuesday, January 15, 2019	Sheet 10 of 53



		MICRO-STAR INT'L CO.,LTD		
		MS-V379		
Size	Document Description			Rev
Custom	Page11: MEMORY: FBC Partition 31..0			1.0
Date:	Tuesday, January 15, 2019			Sheet 11 of 83
NVIDIA CORPORATION				
2701 SAN TOMAS EXPRESSWAY				
SANTA CLARA, CA 95050, USA				
NV_PN	600-1G165-BASE-000			
PCB REV	PG165-ADD	PAGE	10 OF 42	
BOM REV	B	DATE	14-DEC-2018	

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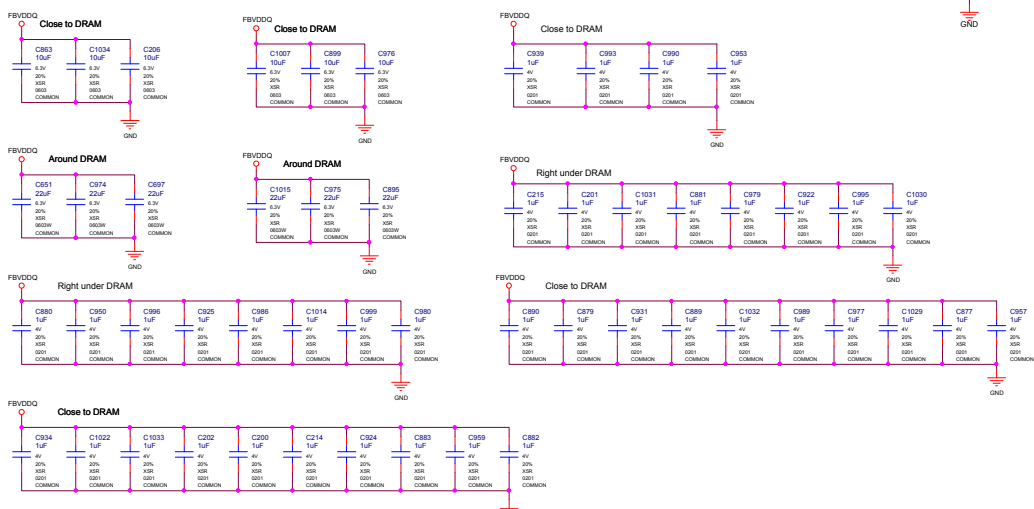
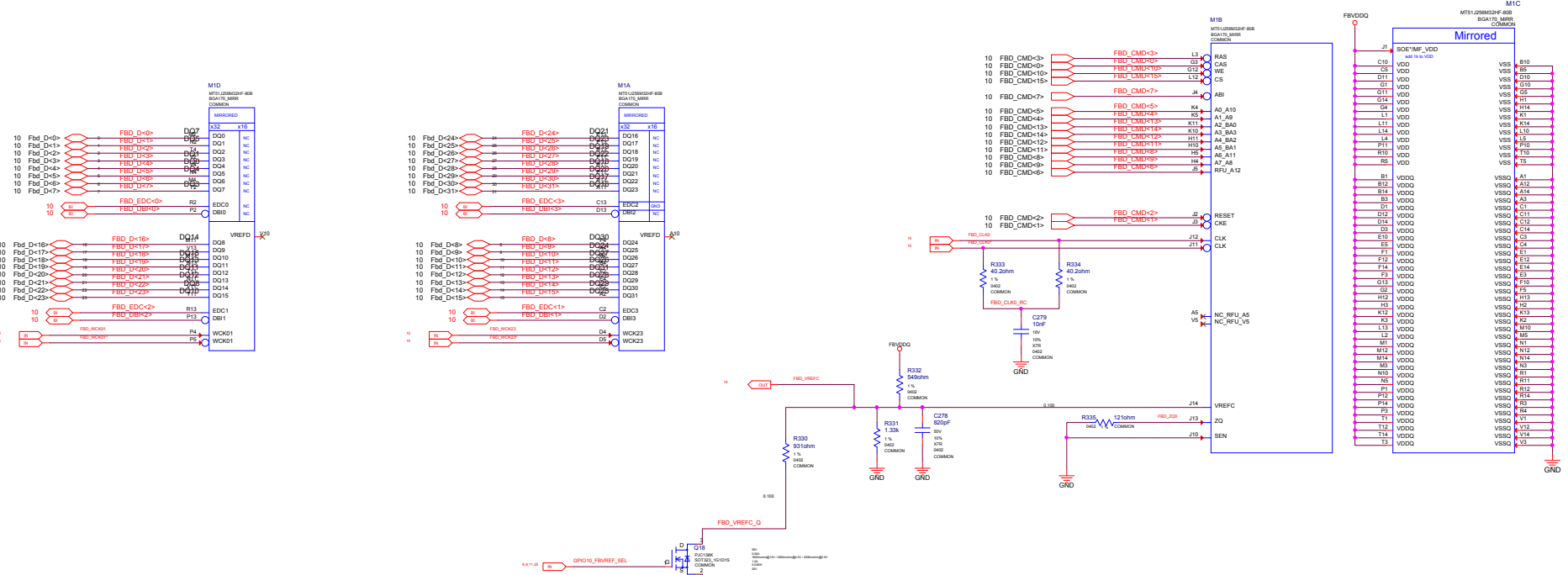
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MS-V379

Size	Document Description	Rev
Custom	Page12: MEMORY: FBC Partition 63.32	1.0
Date:	Tuesday, January 15, 2019	Sheet 12 of 63

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NV_PN	600-1G165-BASE-000	PAGE	11 OF 42
PCB REV	PG165-ADD	DATE	14-DEC-2018

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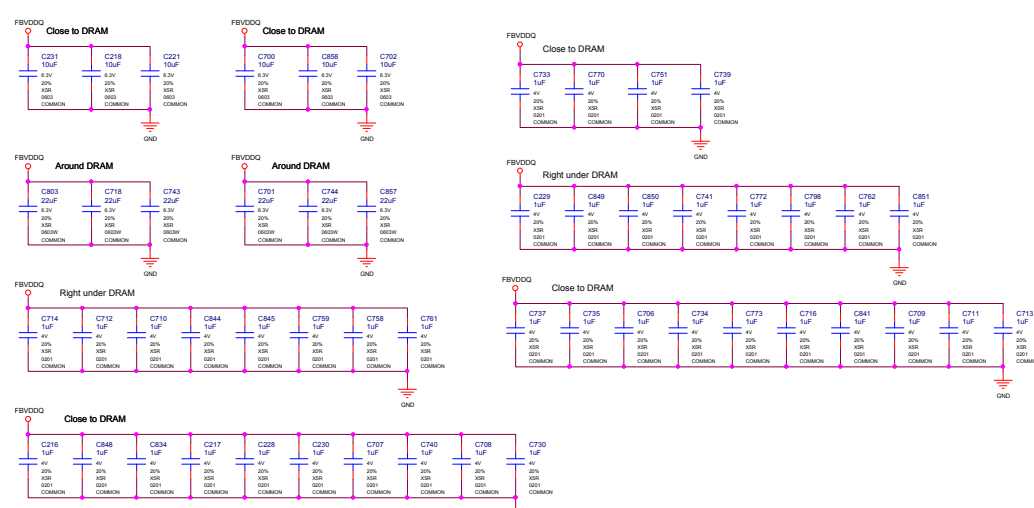
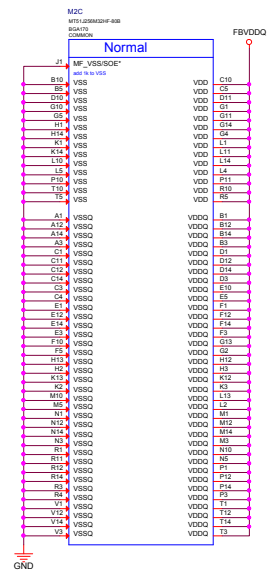
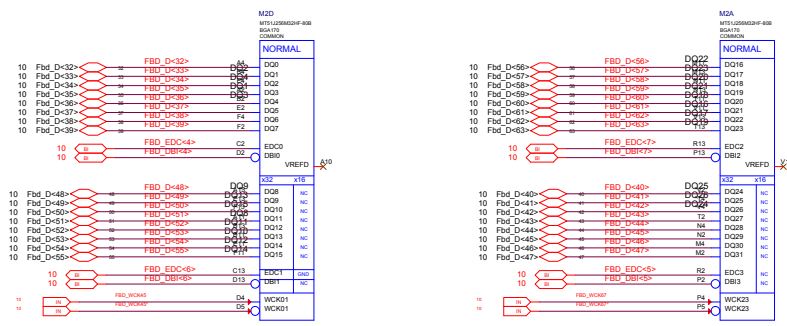
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	Date: Tuesday, January 15, 2019	Sheet 13	of 53

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PAGE DETAIL	MEMORY: FBD[31..0]
NV_PN	600-1G165-BASE-000
PCB REV	PG165-A00
BOM REV	B
PAGE	12 OF 42
DATE	14/DEC/2018

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MS-V379

Rev 1.0

Customer: **Page14: MEMORY: FBD Partition 63..32**

Date: **Tuesday, January 15, 2019**

Document Description: **Page14: MEMORY: FBD Partition 63..32**

Sheet **14** of **63**

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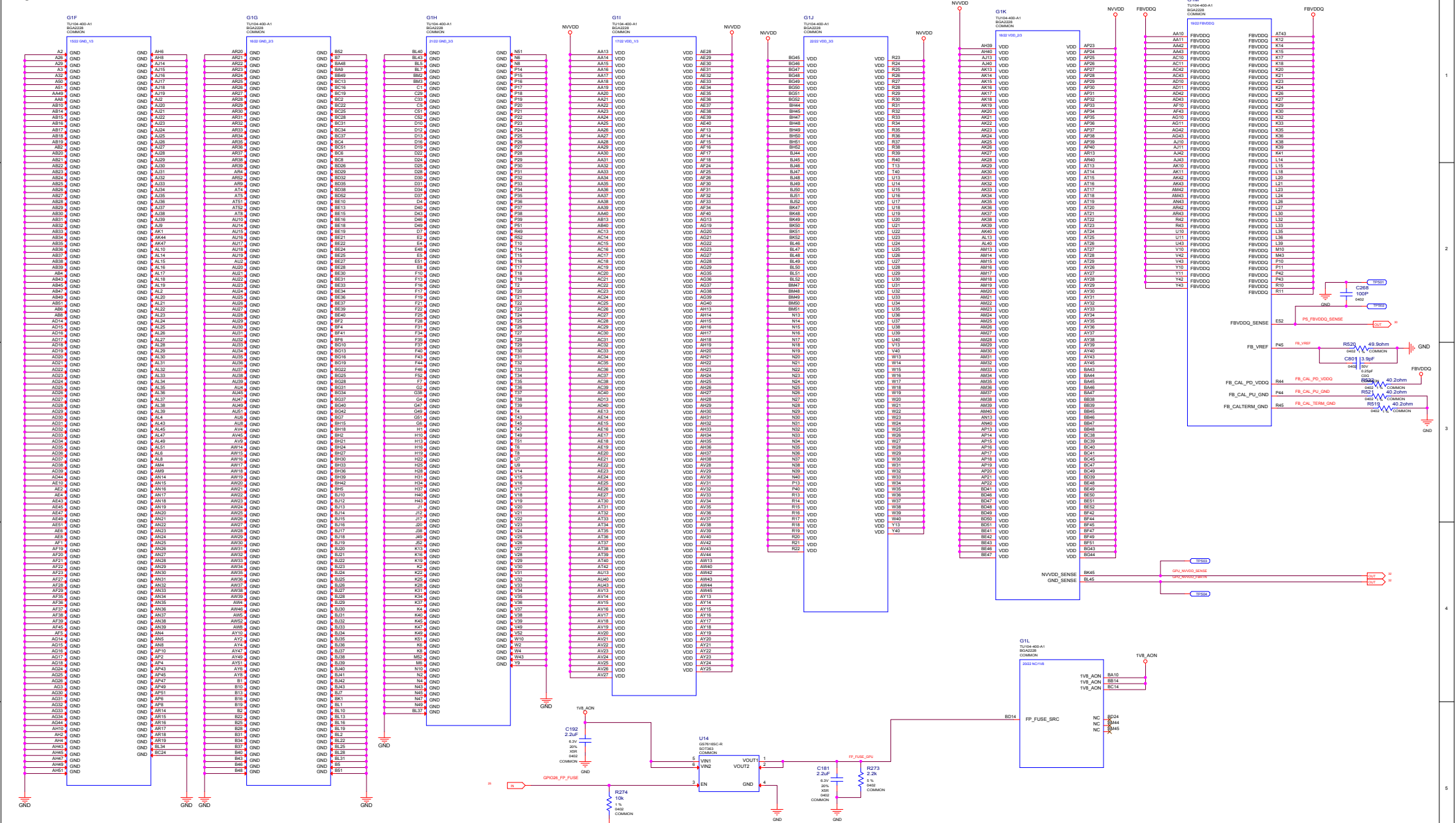
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PAGE: **13 OF 42**

DATE: **14-DEC-2018**

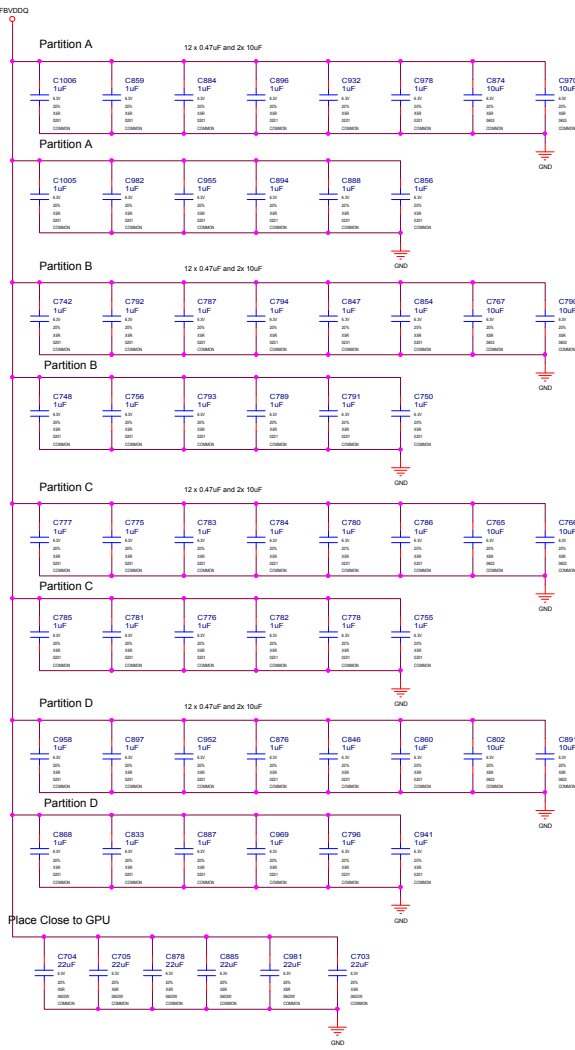
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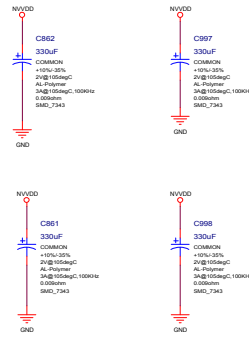
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		Date: Tuesday, January 15, 2019	Sheet 15 of 63

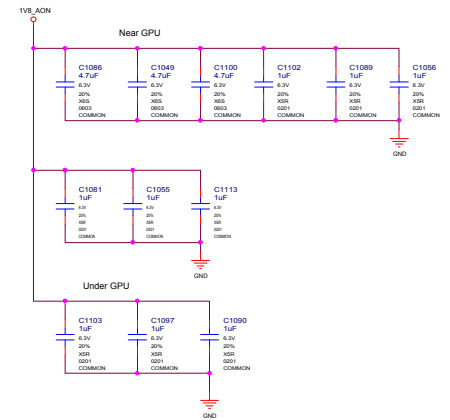
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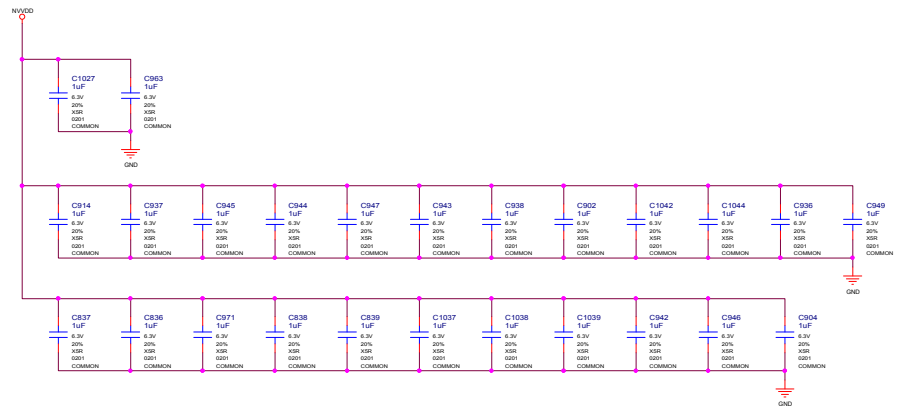
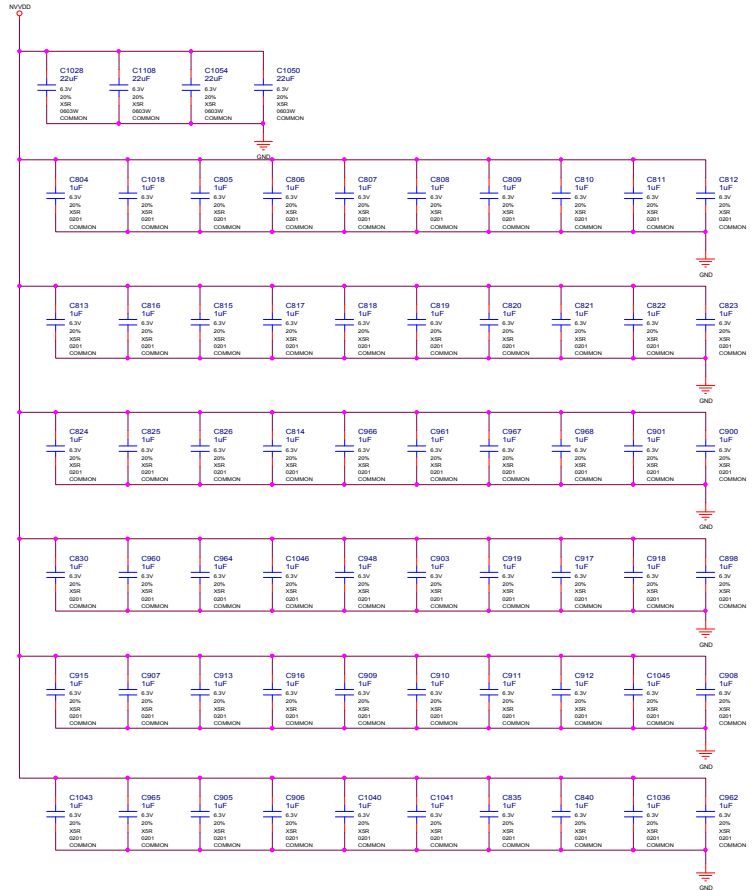
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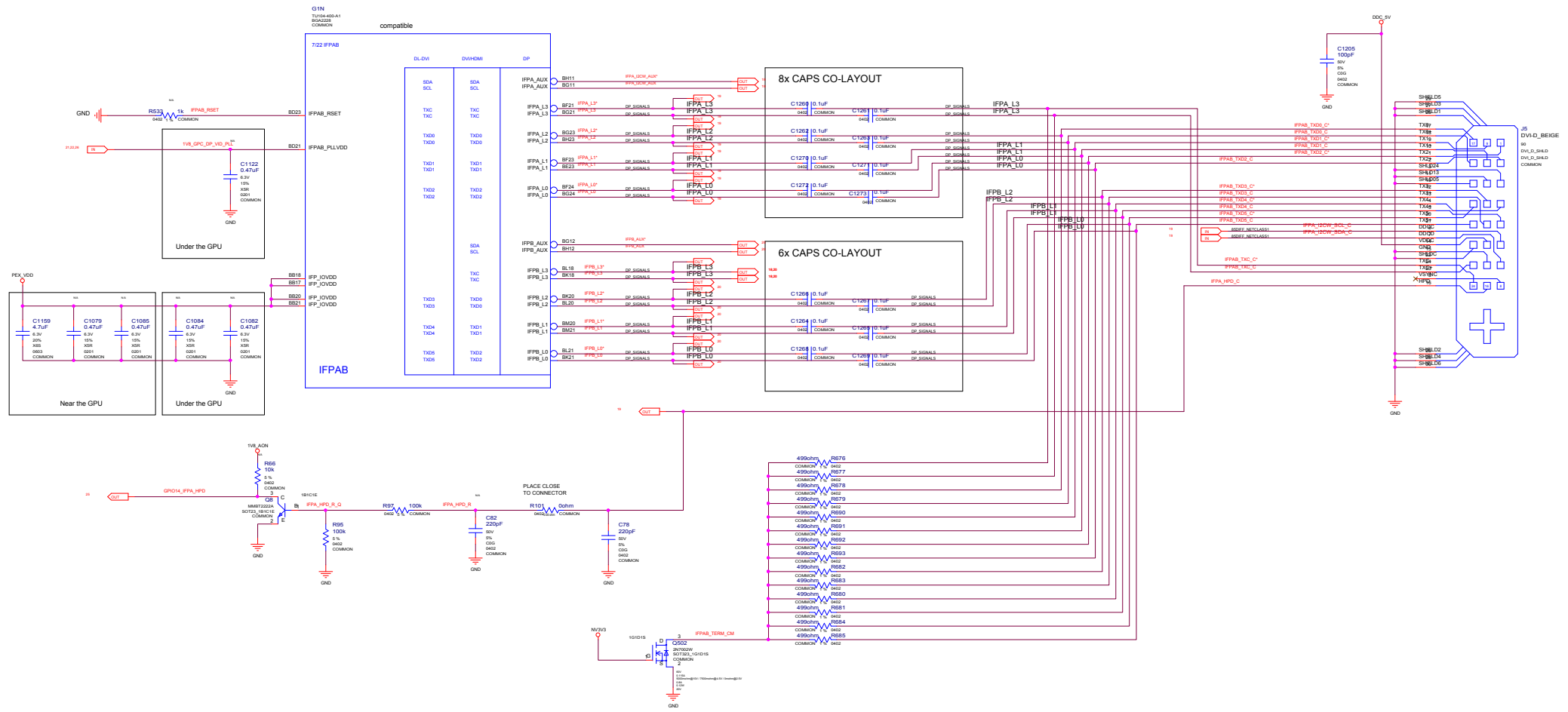
		MICRO-STAR INT'L CO.,LTD	
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Size	Document Description	Rev	
Custom	Page16: GPU Decoupling 1	1.0	
Date: Tuesday, January 15, 2019		Sheet 16 of 53	

NVDD



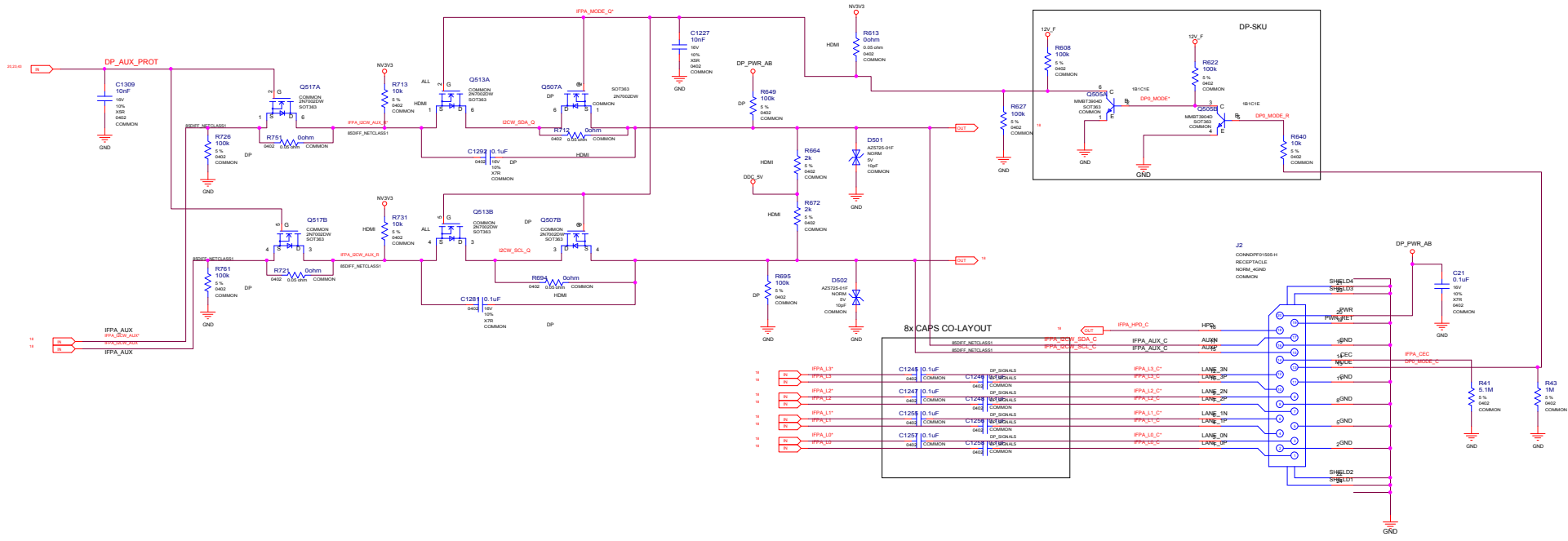
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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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MICRO-STAR INT'L CO., LTD MS-V379		
Size: Custom	Document Description: Page18: IFPAB DVI-D-DL	Rev: 1.0
Date: Tuesday, January 15, 2019	Sheet: 18 of 63	



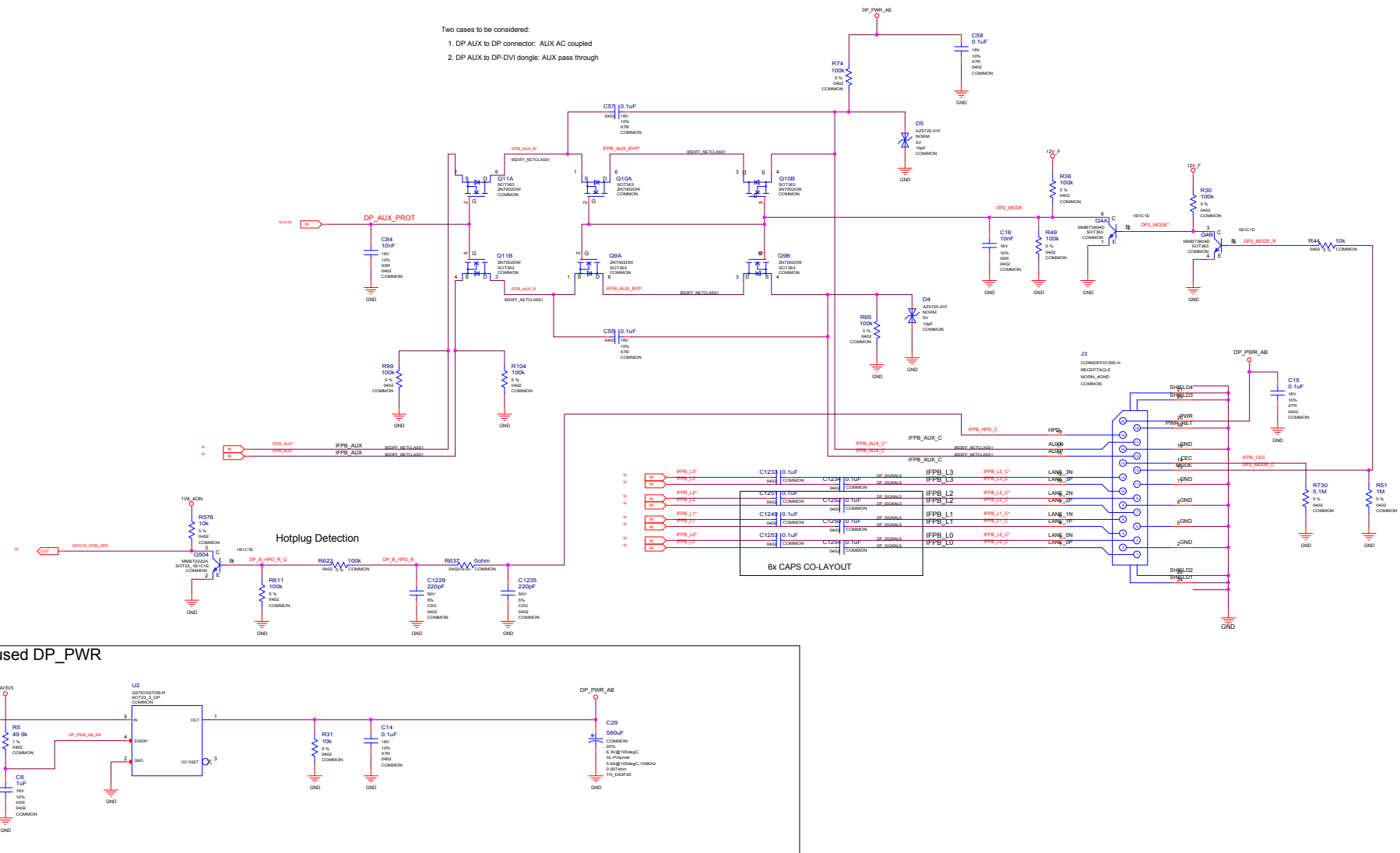
IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

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MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size	Document Description	Rev
Custom	Page19: IFPA DP	1.0
Date:	Tuesday, January 16, 2019	Sheet 19 of 53

IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



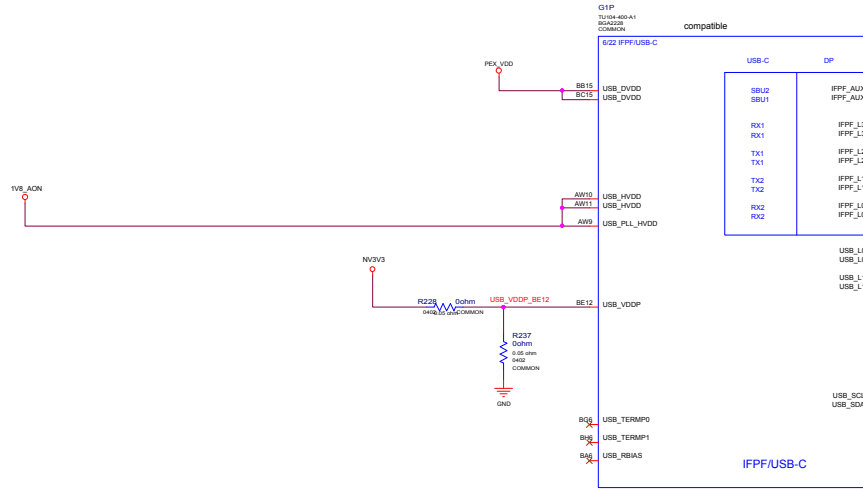
Hotplug Detection

Fused DP_PWR

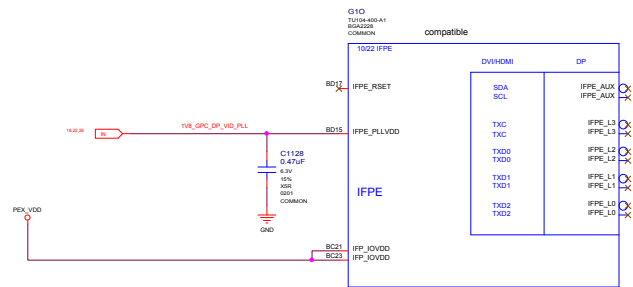
6x CAPS CO-LAYOUT

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MS-V379		
Size Custom	Document Description Page20: IFPB DP	Rev 1.0
Date: Tuesday, January 16, 2019		Sheet 20 of 53



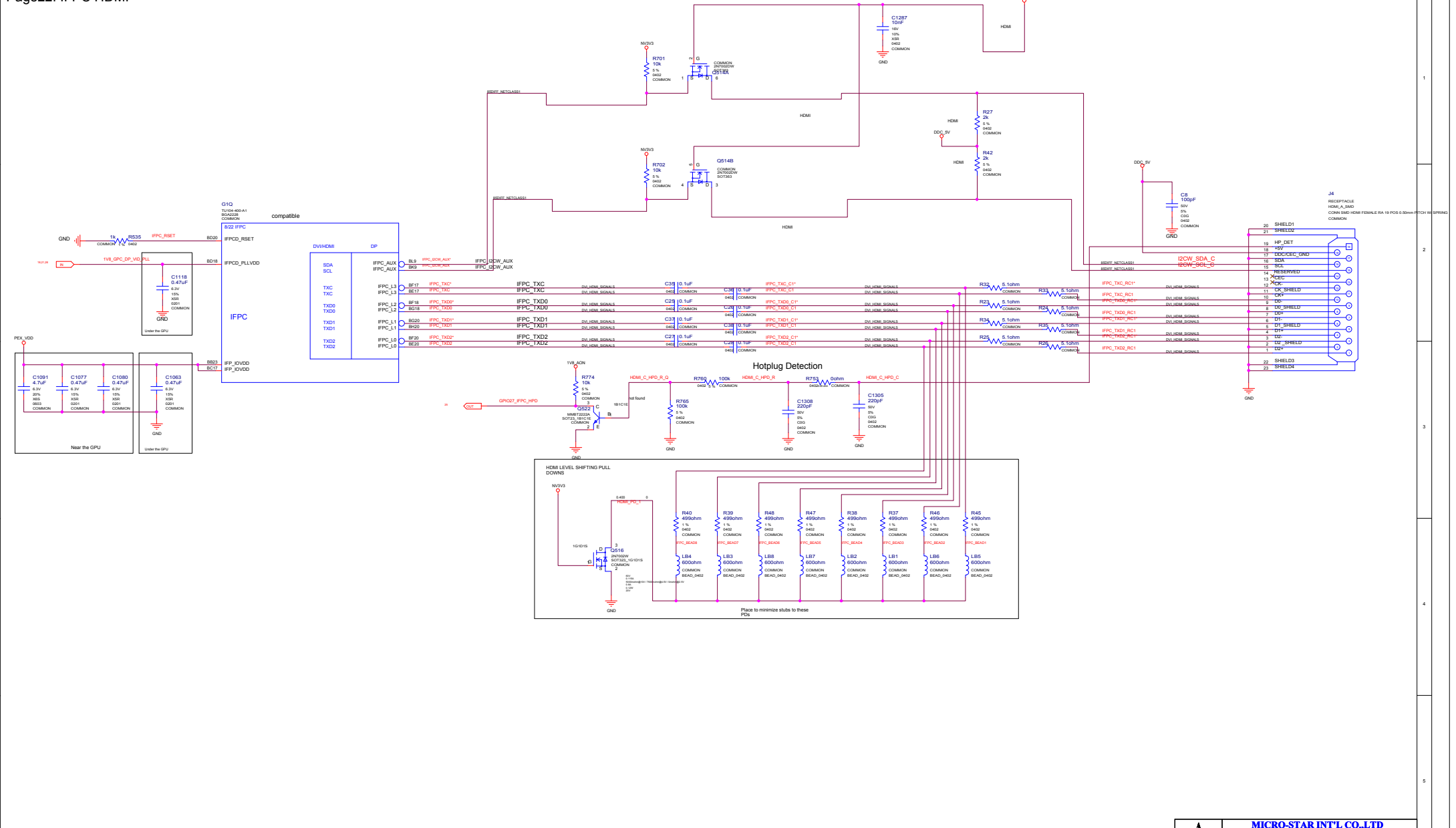
IFPF NC



IFPE NC

		MICRO-STAR INT'L CO.,LTD	
MS-V379			
Size	Document Description	Rev	
Custom	Page21: IFPE & IFPF USB-C NC	1.0	
Date: Tuesday, January 15, 2019		Sheet	21 of 53

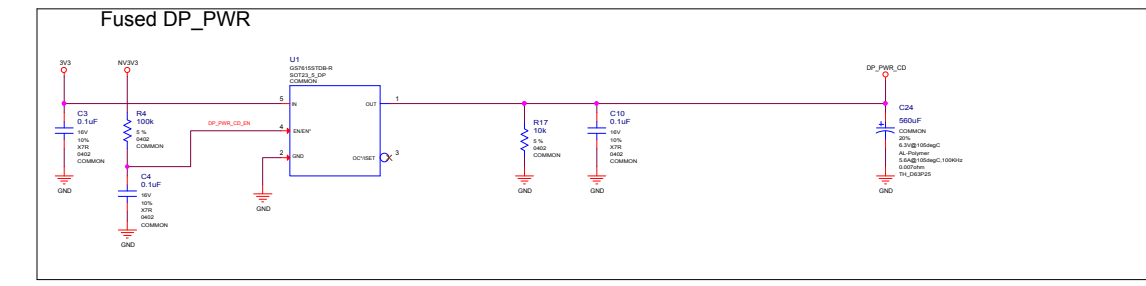
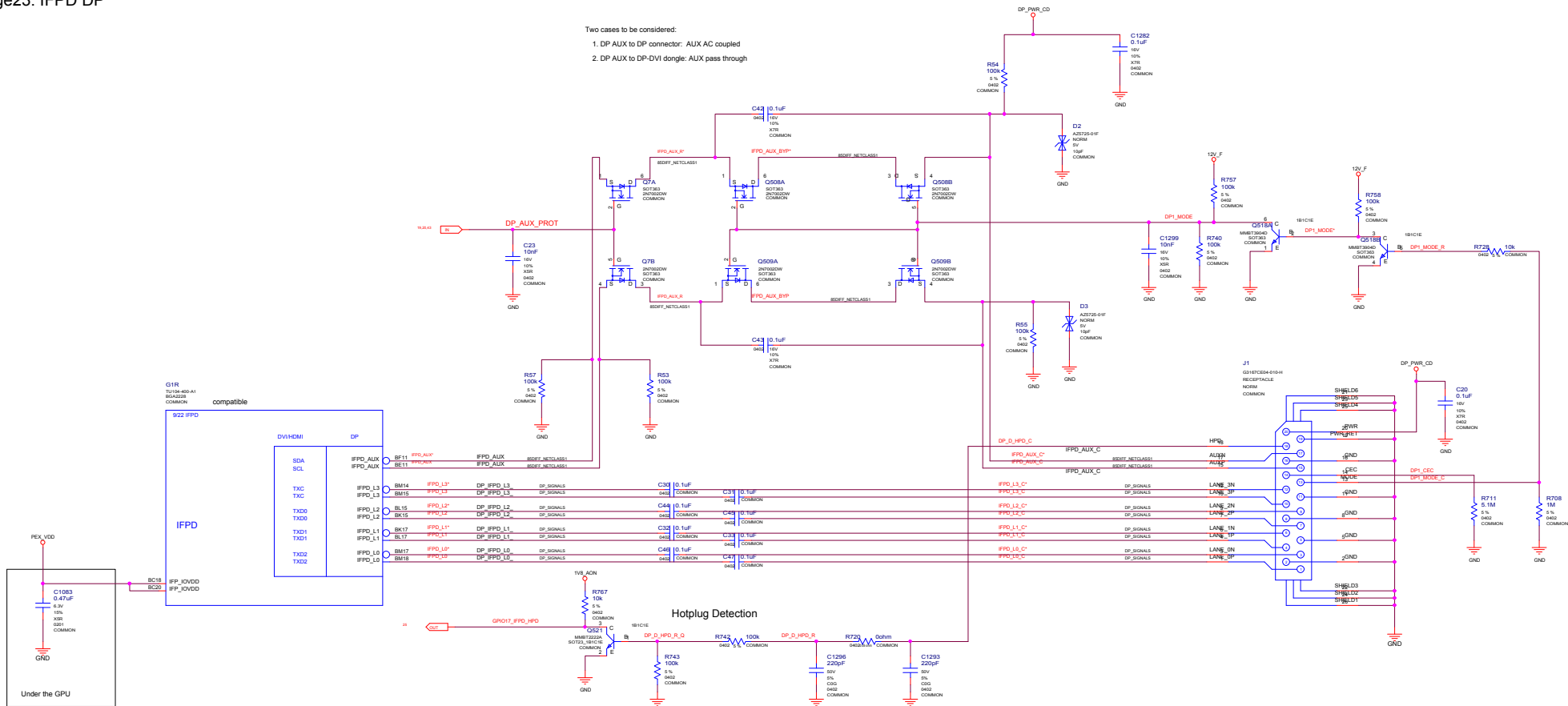
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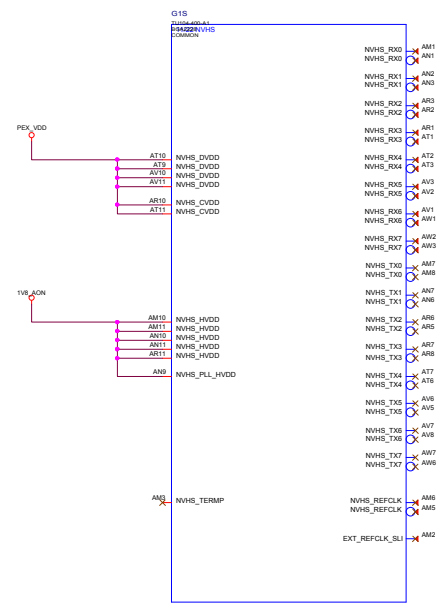
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	MS-V379	
	See Custom Date: Tuesday, January 16, 2018	Document Description Page22: IFPC HDMI Sheet 22 of 53


Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

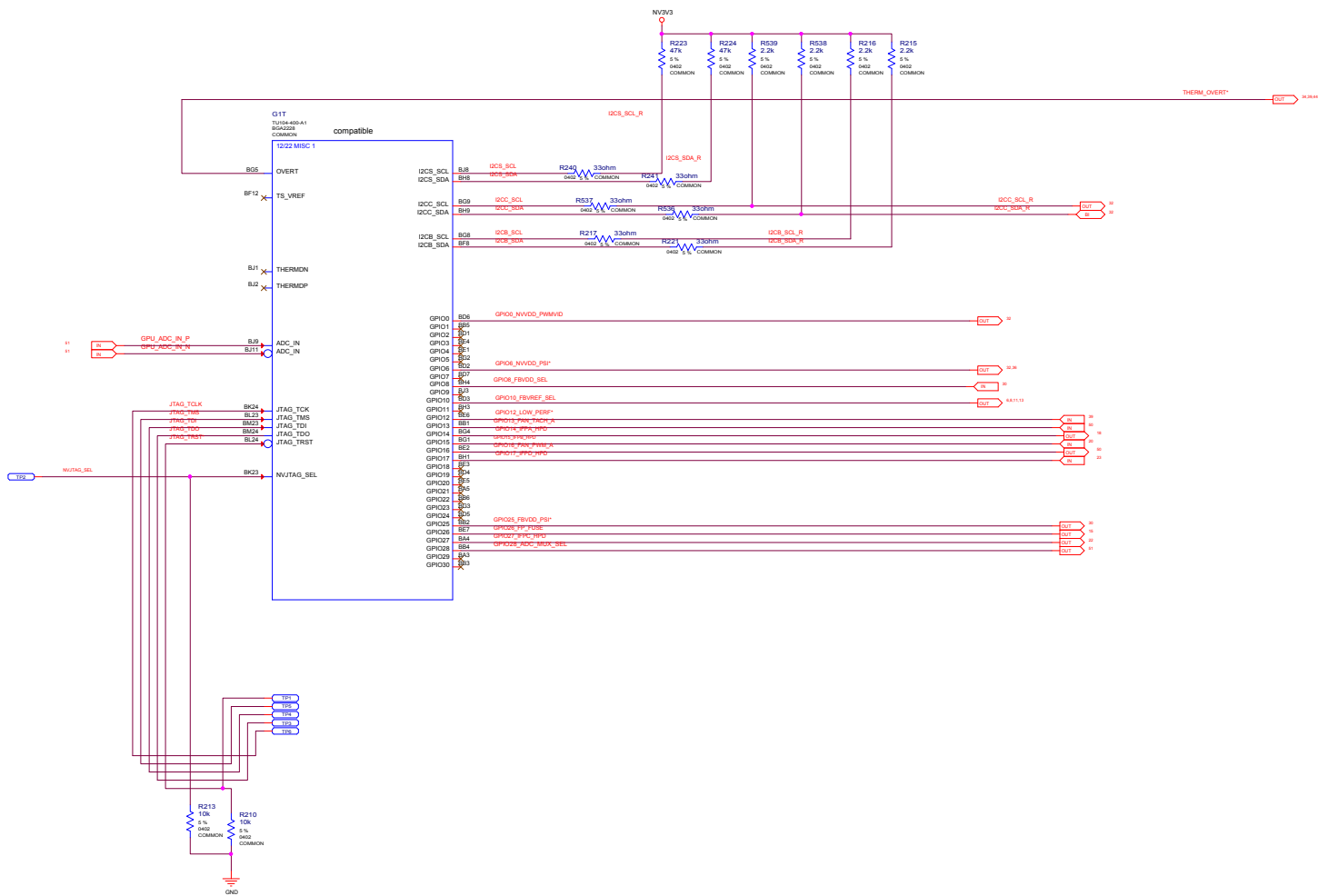


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			MICRO-STAR INT'L CO.,LTD	
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Size Custom	Document Description Page24: NVHS Interface and Frame Lock			Rev 1.0
Date: Tuesday, January 15, 2019			Sheet	24 of 63



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			MS-V379	
Size	Document Description	Rev		
Custom	Page25: MISC1: Fan, Thermal, JTAG, GPIO	1.0		
Date:	Tuesday, January 15, 2019	Sheet	25	of 53

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

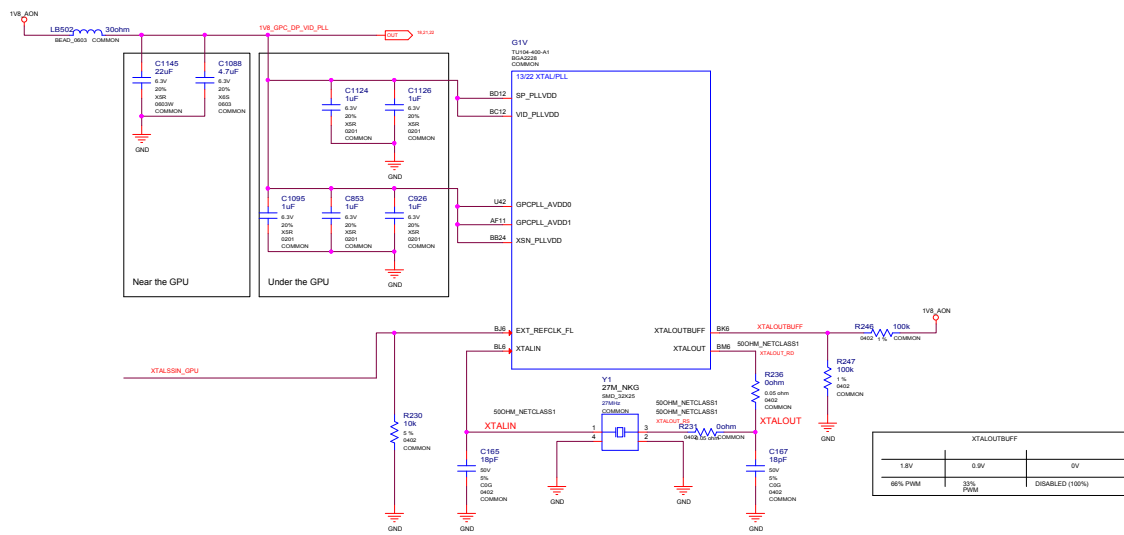
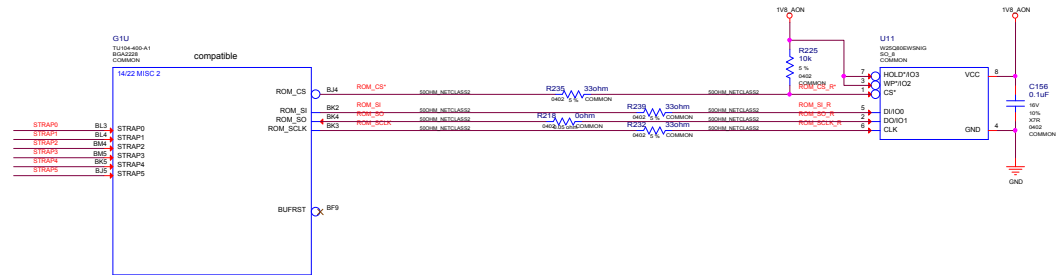
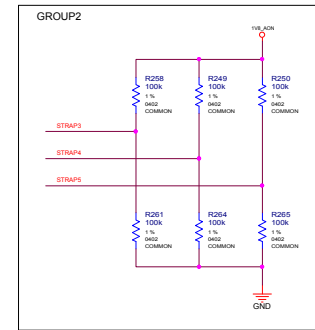
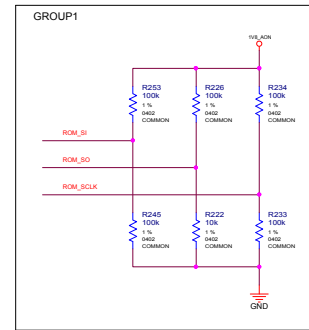
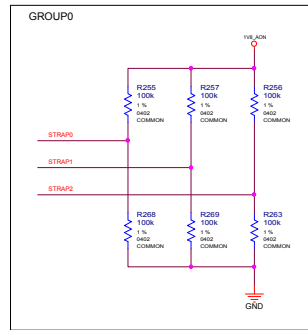
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

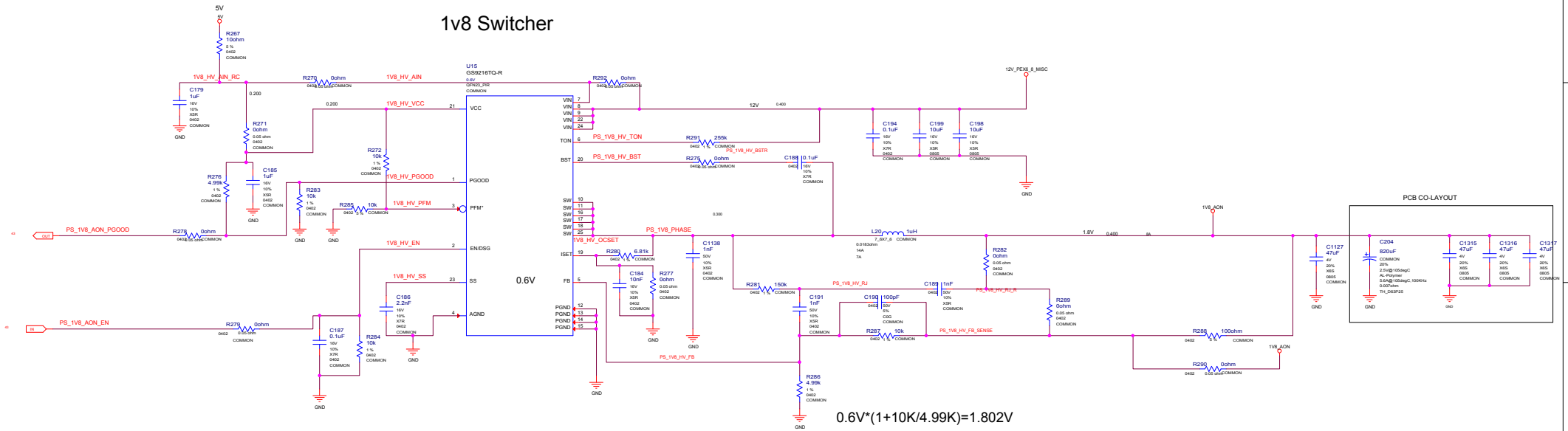
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



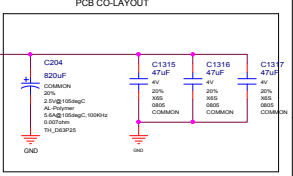
XTALOUTBUFF	
1.8V	0V
66% PWM	DISABLED (100%)

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1v8 Switcher

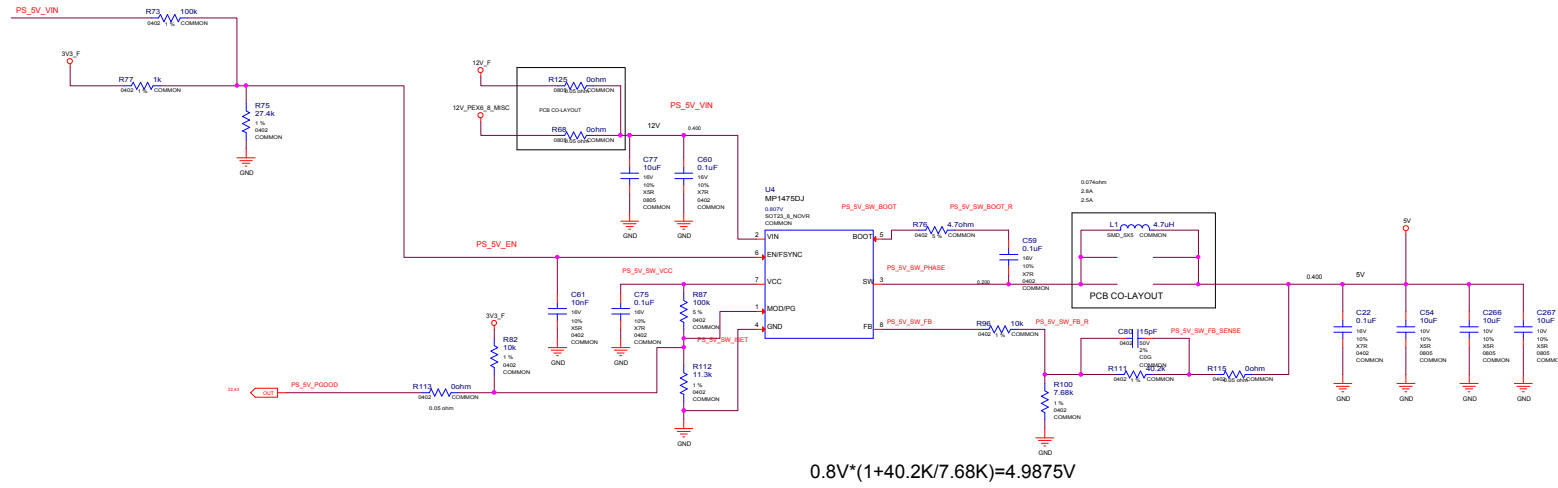


$$0.6V * (1 + 10K / 4.99K) = 1.802V$$



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Size	Document Description	Rev		
Custom	Page27: PS: 1V8_AON	1.0		
Date:	Tuesday, January 15, 2019	Sheet	27	of 53

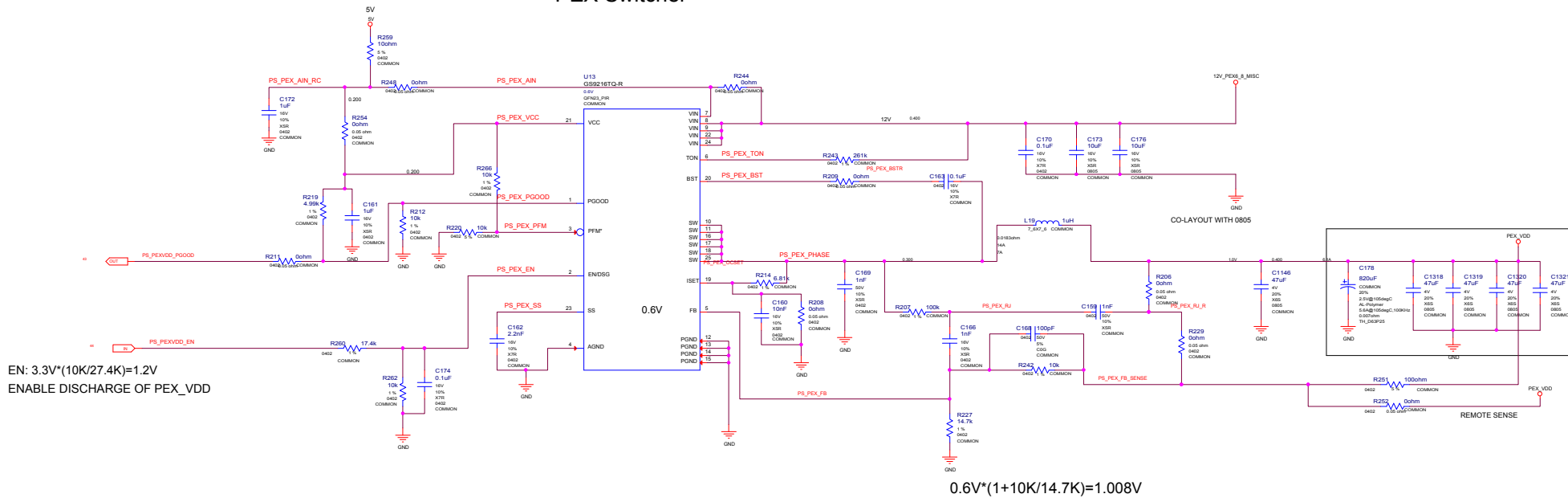


$$0.8V * (1 + 40.2K / 7.68K) = 4.9875V$$

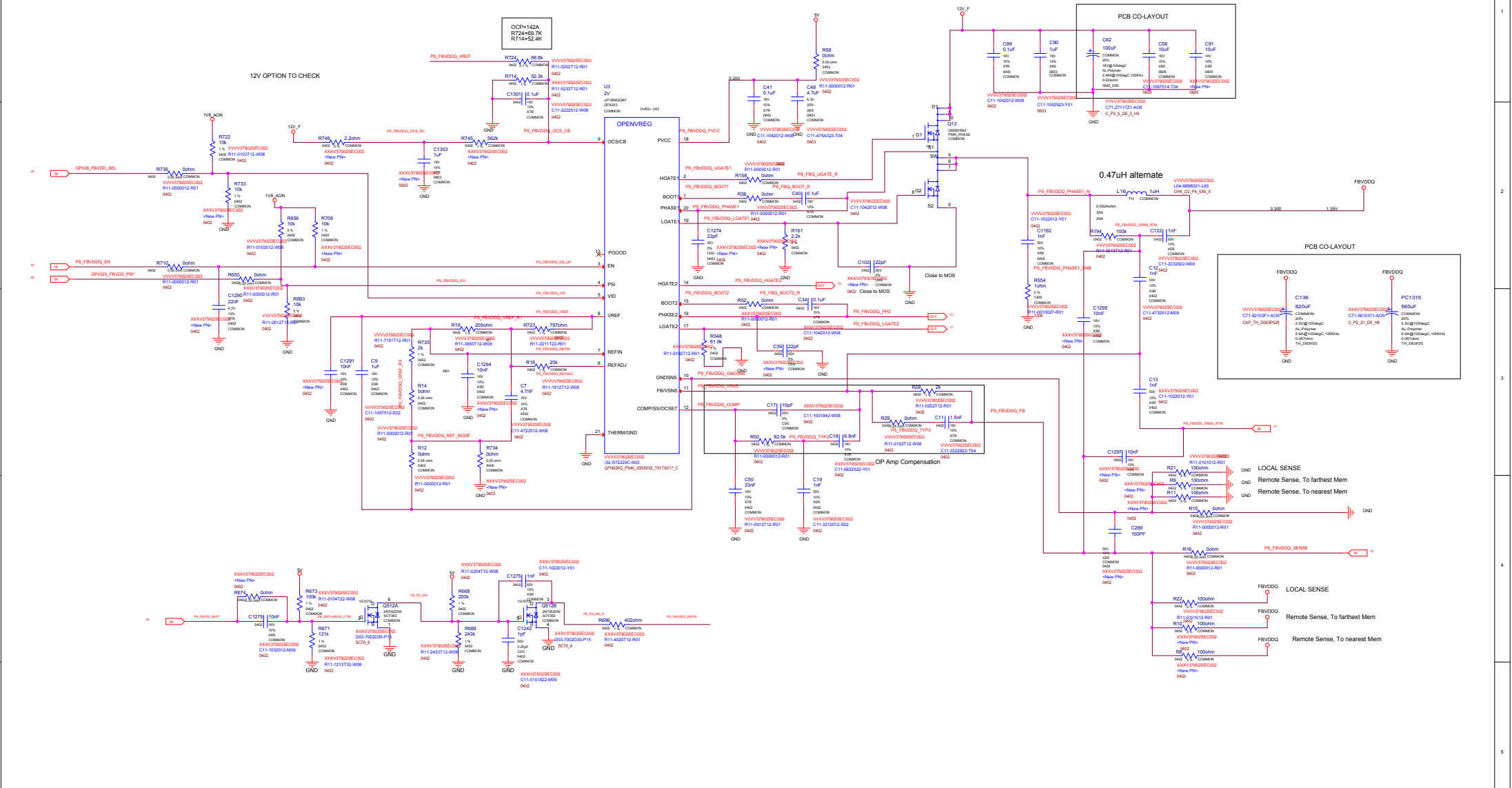
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Size Custom	Document Description Page28: PS: 5V	Rev 1.0
Date: Tuesday, January 15, 2019	Sheet 28 of 53	


PEX Switcher



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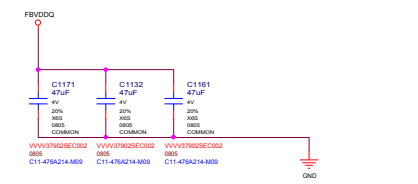
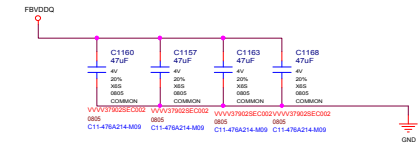
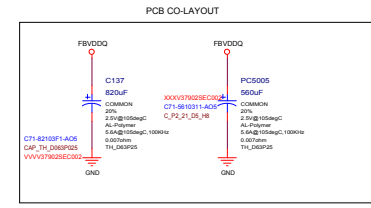
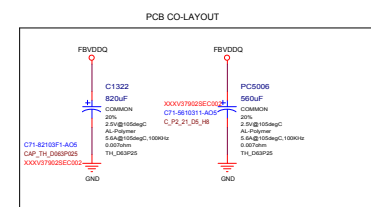
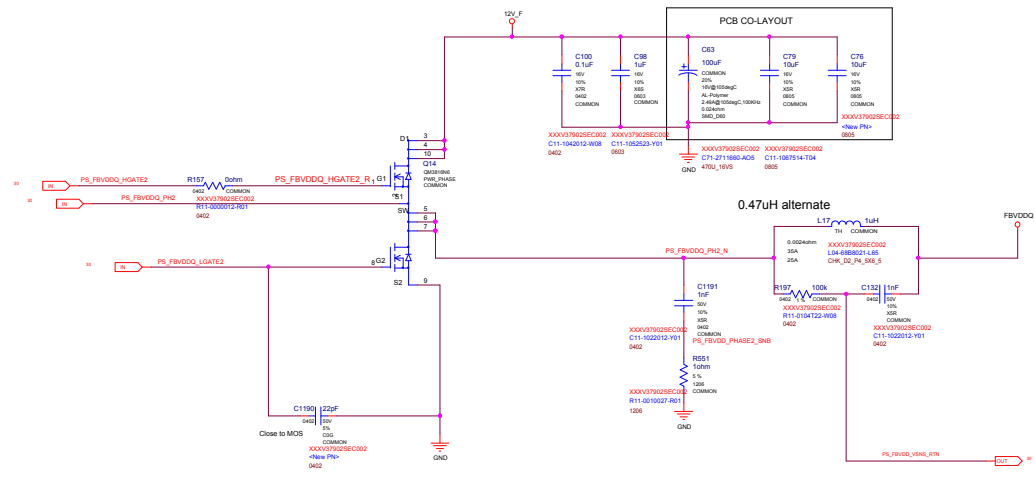


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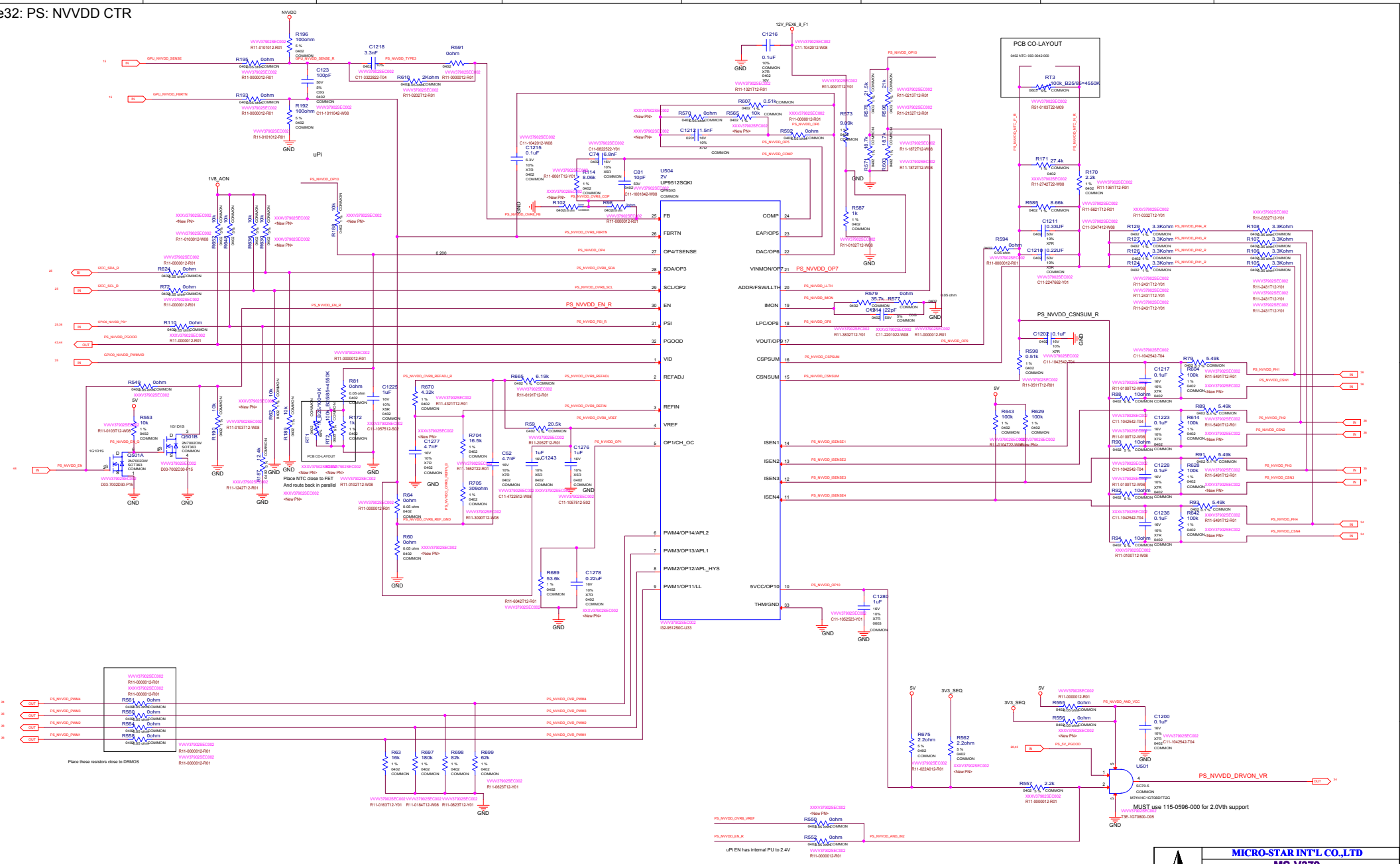
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Date	Document Description	Rev
Tuesday, January 15, 2019	Page30: PS: FBVDDQ	1.0
Sheet	30	of 63



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MS-V379		
Size	Document Description	Rev
Custom	Page31: PS: FBVDDQ PH2	1.0
Date: Tuesday, January 16, 2018 10:18:00 AM		Sheet 31 of 63



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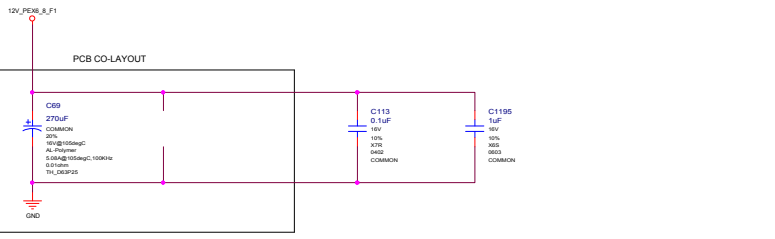
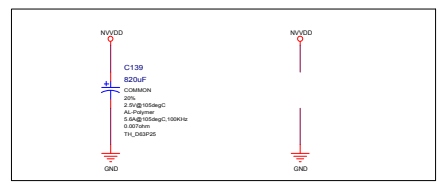
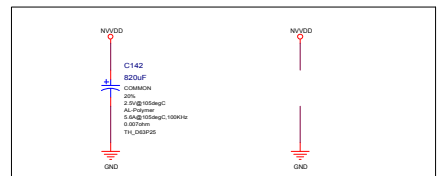
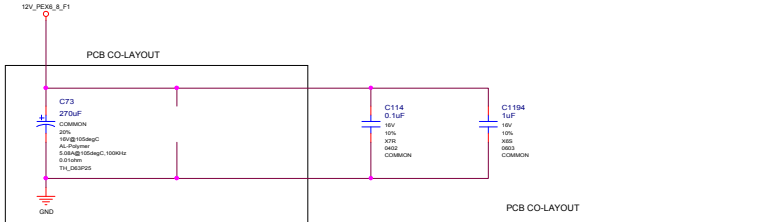
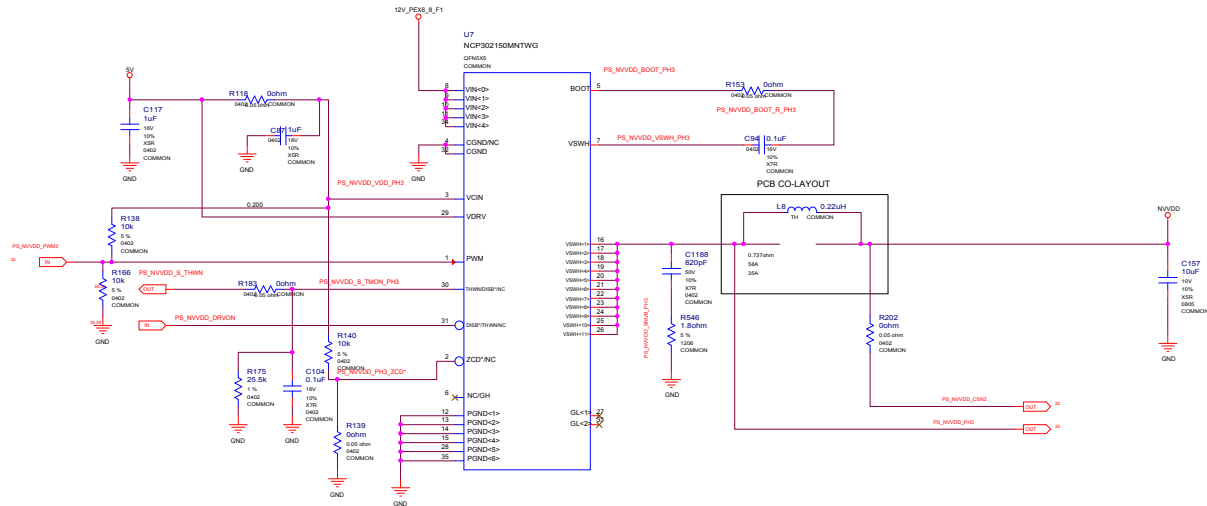
		MICRO-STAR INT'L CO.,LTD	
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Size	Custom	Document Description	Page32: PS: NVVDD CTR
Date:	Tuesday, January 15, 2019	Sheet	32 of 53

DROP OVR3i SOLUTION

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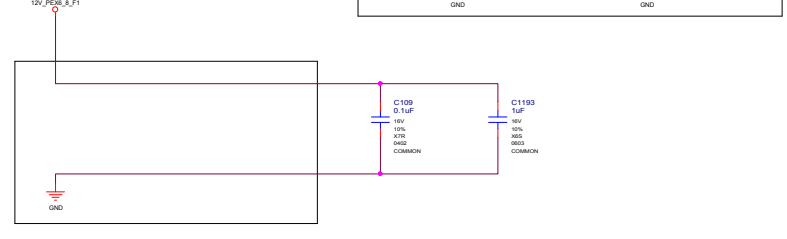
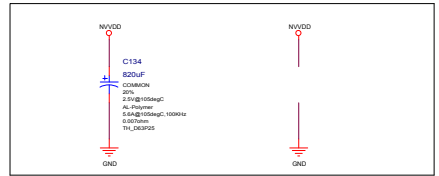
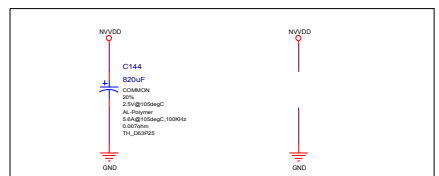
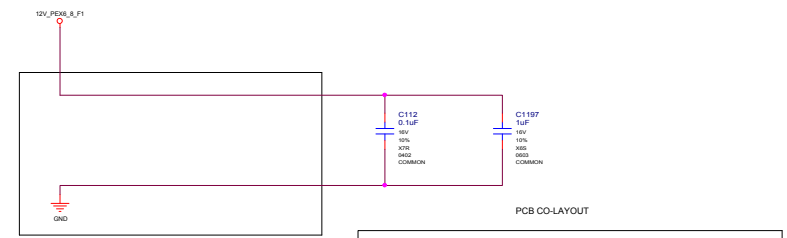
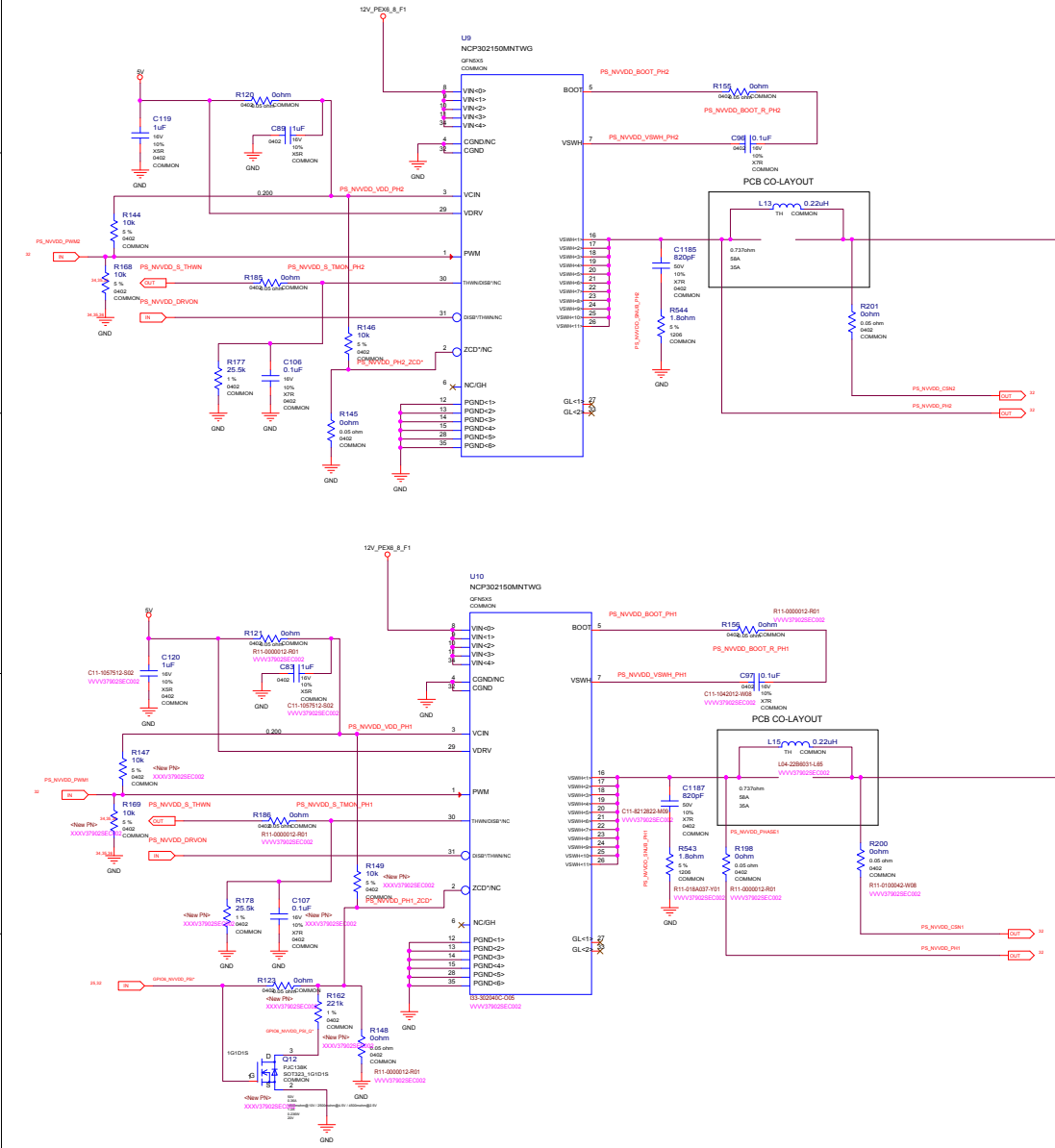


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MS-V379		
Size	Document Description	Rev
Custom	Page33: PS: NVVDD CTR OVR3i	1.0
Date:	Monday, January 14, 2019	Sheet 33 of 63



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MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size Custom	Document Description Page35: PS: NVVDD PH3&5	Rev 1.0
Date: Tuesday, January 15, 2019	Sheet 35	of 63



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MICRO-STAR INT'L CO.,LTD		
MS-V379		
Rev	Document Description	Rev
1.0	Page36: PS: NVVDD PH2&1	1.0
Date:	Tuesday, January 15, 2019	Sheet 36 of 63

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DELETE RAIL BALANCE CIRCUIT

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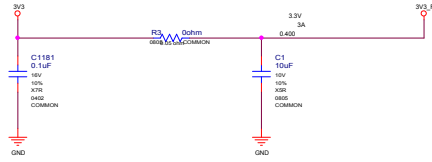
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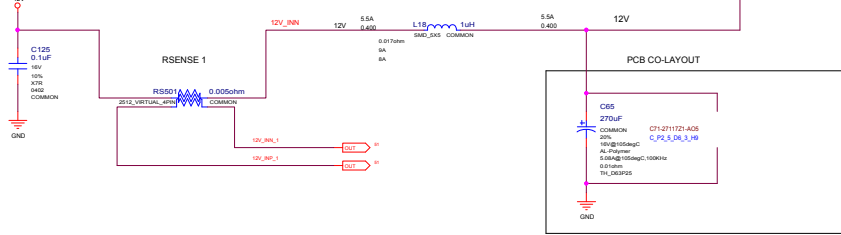
MICRO-STAR INT'L CO.,LTD
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Size	Document Description	Rev
Custom	Page37: Input Power Balancing Switcher	1.0
Date: Monday, January 14, 2019	Sheet	37 of 63

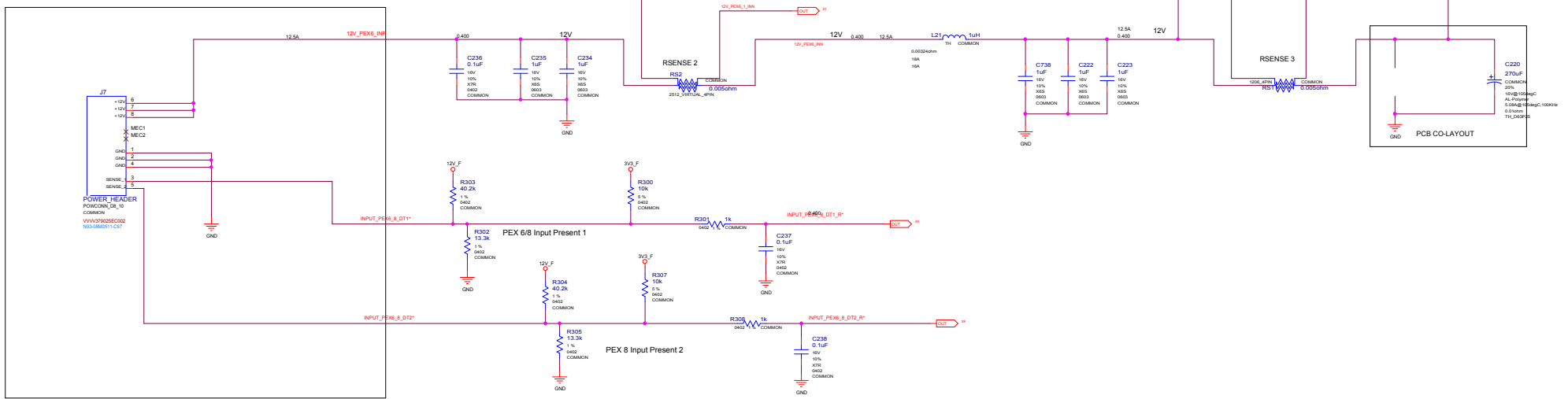
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



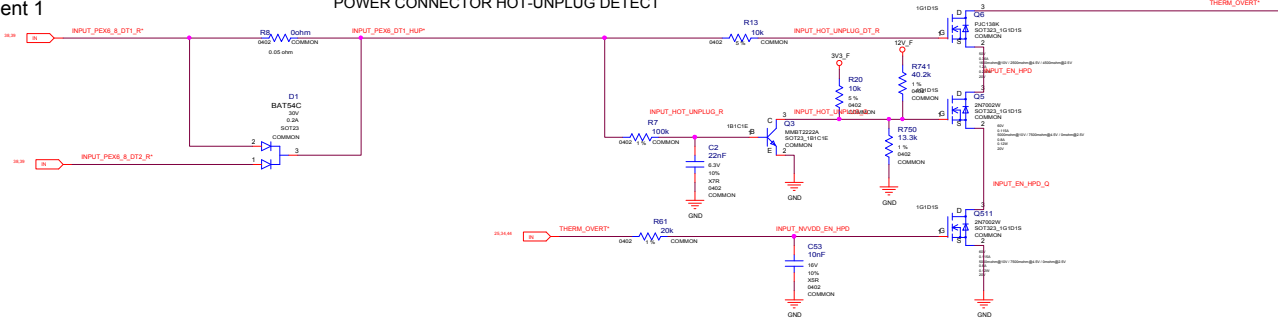
PEX8 INPUT 1 - 2x4 PCIe CON 150W



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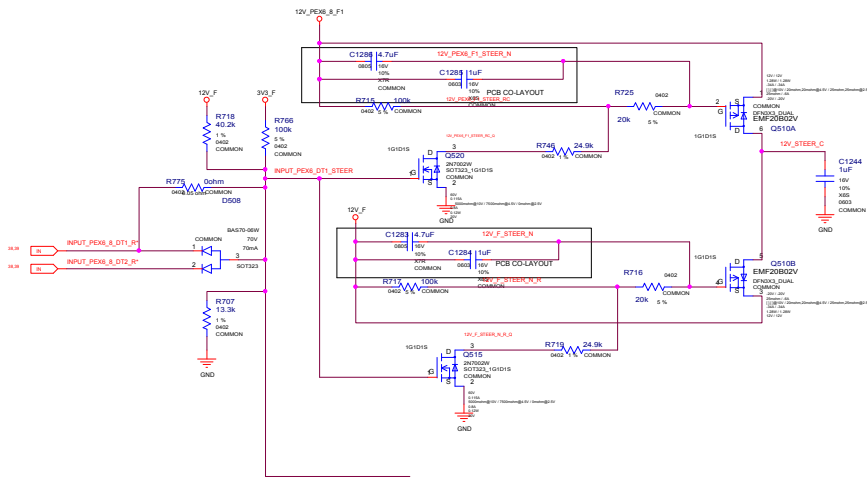
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

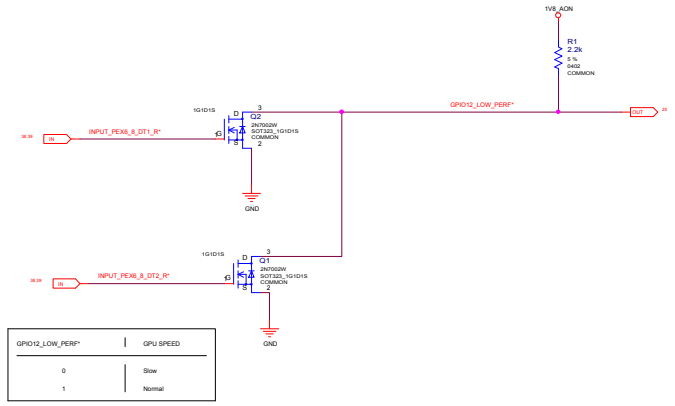


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPU012_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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Size	Document Description	Rev
Custom	Page40: BUCKBOOST	1.0
Date: Monday, January 14, 2019	Sheet 40 of 53	

A B C D E F G H

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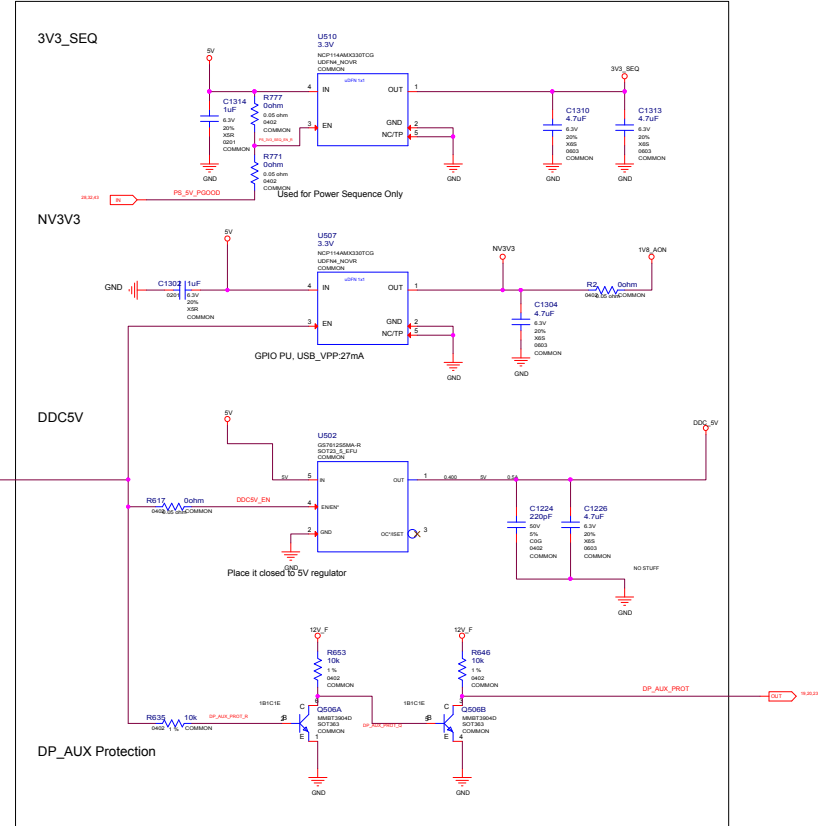
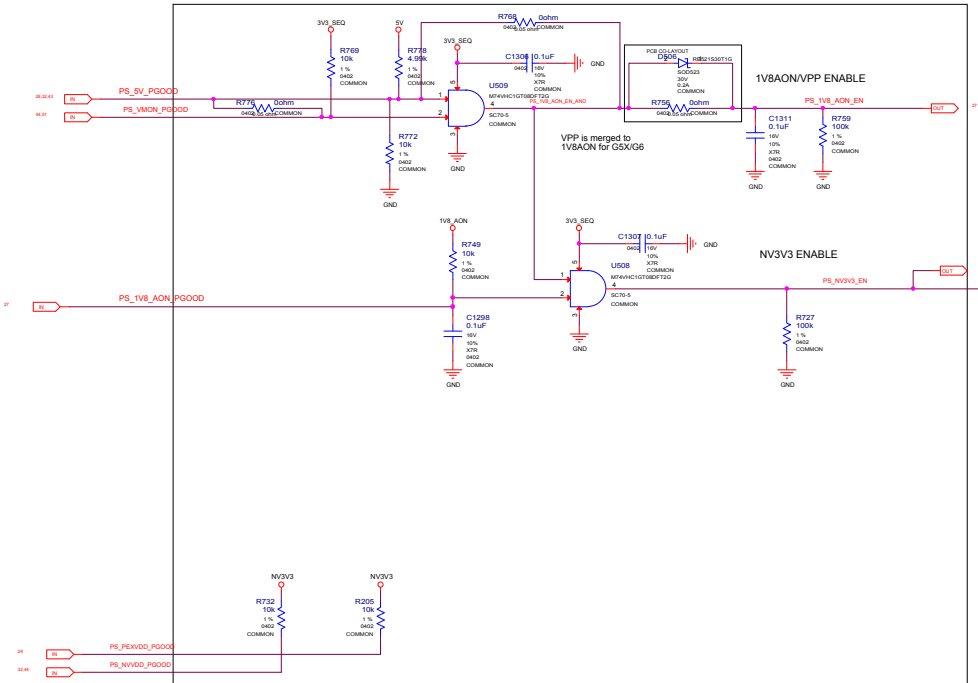
Size	Document Description	Rev
Custom	Page41: PPC	1.0
Date: Monday, January 14, 2019		Sheet 41 of 53

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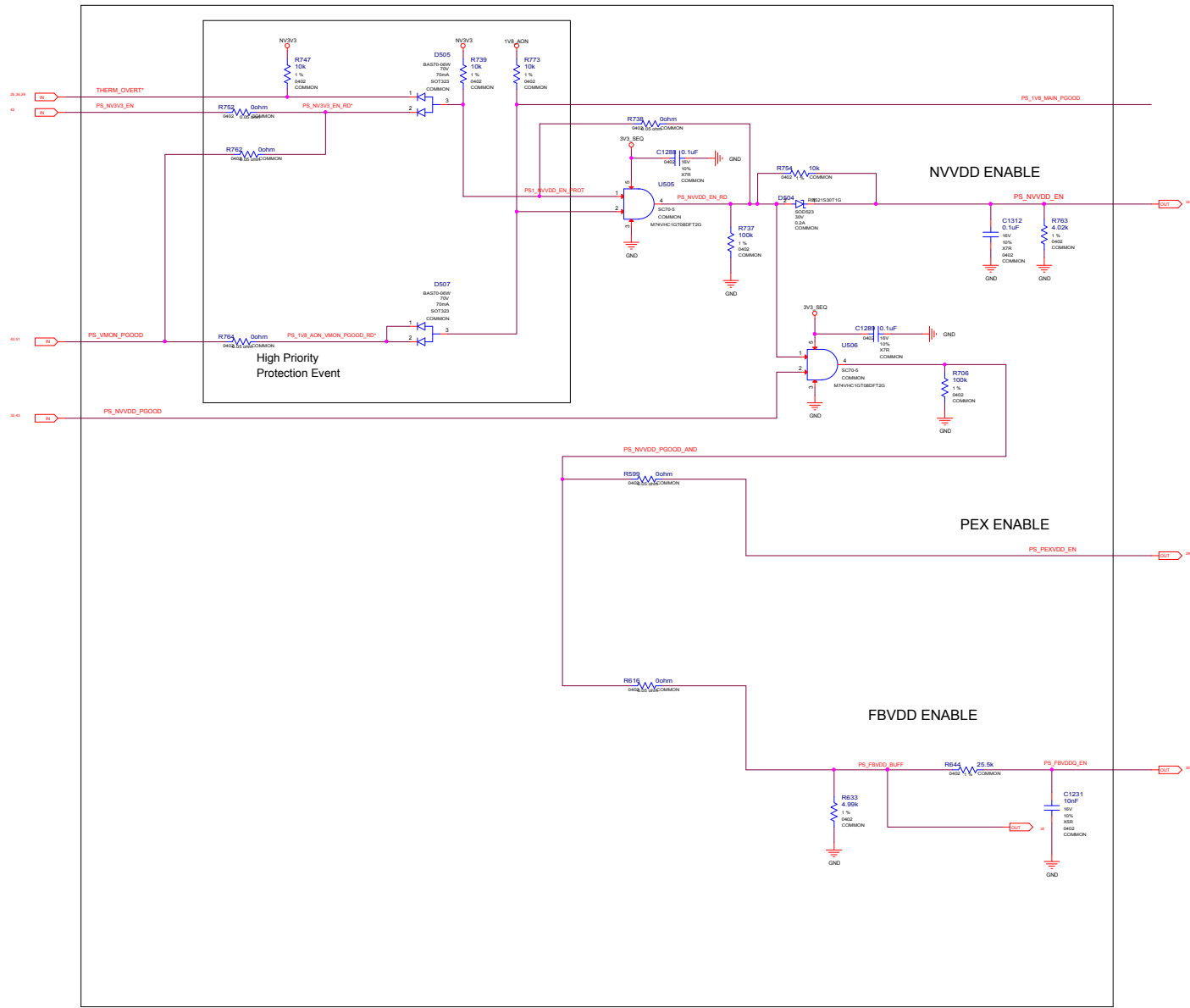
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MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size	Document Description	Rev
Custom	Page42: 12V & 3V3_A SWITCHER	1.0
Date: Monday, January 14, 2019	Sheet	42 of 53



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		Size: Custom Document Description: Page44: SEQ:NV,PEX,FB ENABLE Date: Tuesday, January 15, 2019	Rev: 1.0 Sheet: 44 of 63

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Size	Document Description	Rev
Custom	Page45: SEQUENCE:Voltage Monitor	1.0
Date: Monday, January 14, 2019	Sheet	45 of 53

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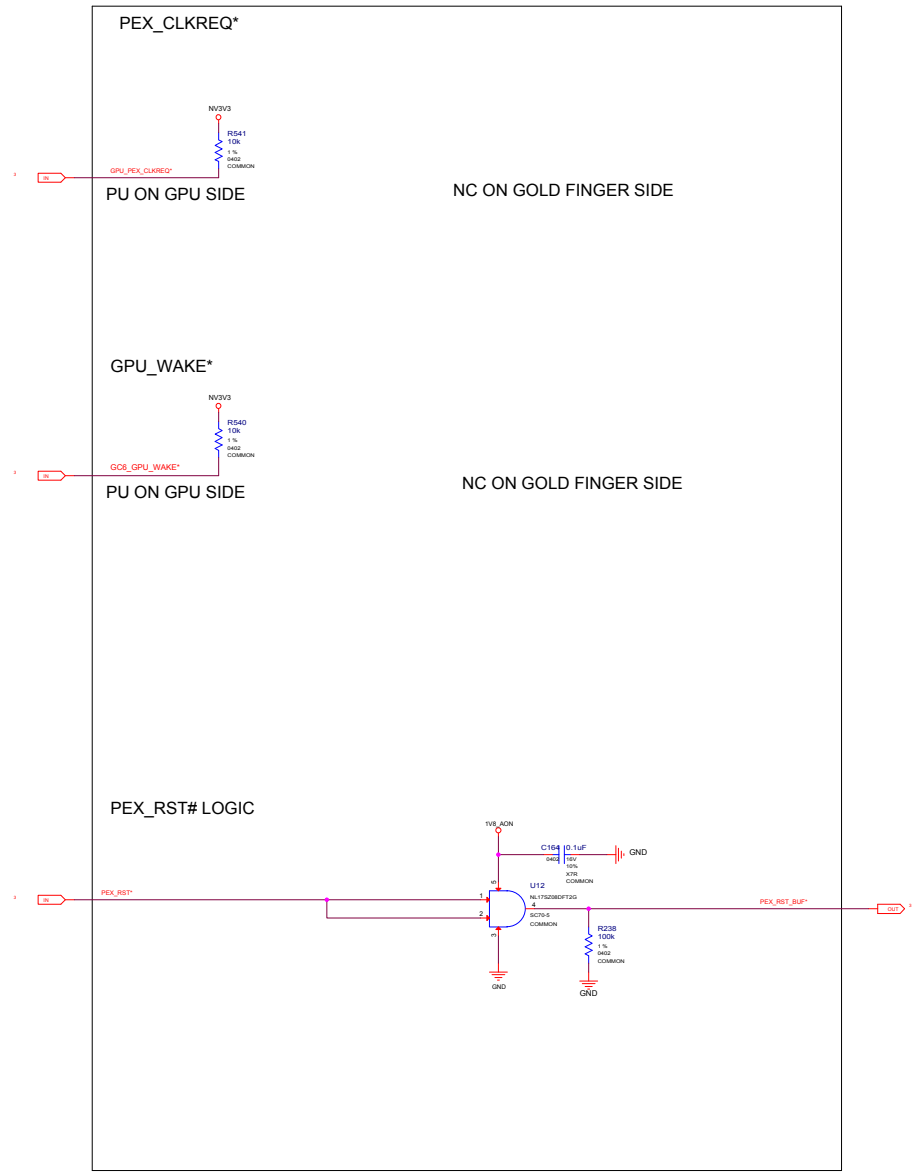
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			MS-V379	
Size	Document Description			Rev
Custom	Page46: SEQUENCE:Discharge			1.0
Date: Monday, January 14, 2019		Sheet 46 of 53		

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		MS-V379	
Size Custom	Document Description Page47: SEQUENCE:MISC	Rev 1.0	
Date: Tuesday, January 15, 2019		Sheet 47	of 53

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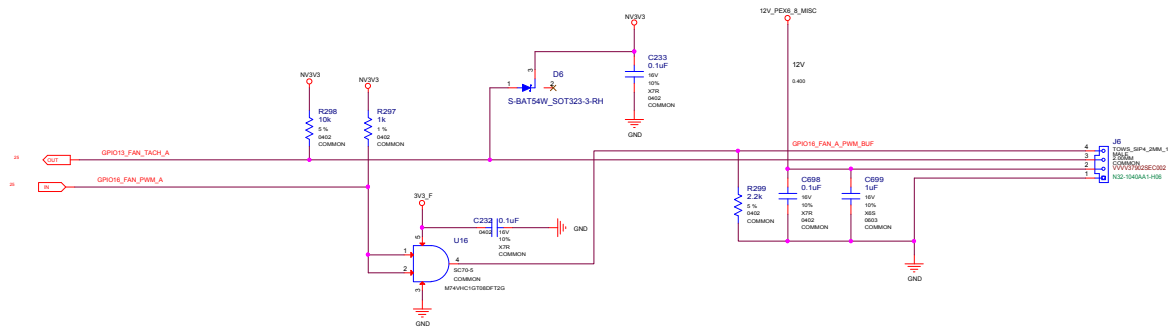


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MS-V379		
Size	Document Description	Rev
Custom	Page48: LOGO LED	1.0
Date: Monday, January 14, 2019	Sheet 48 of 53	


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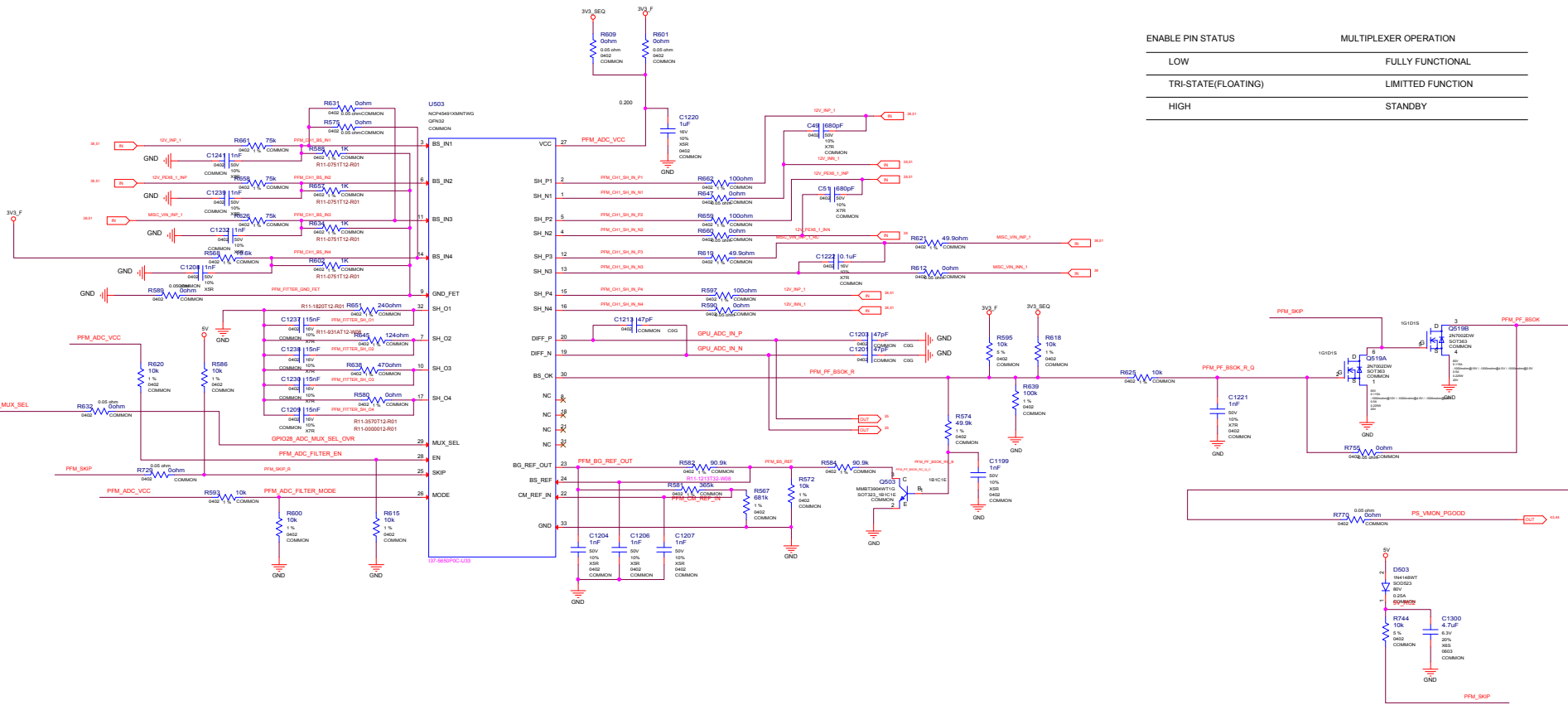
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	MS-V379		
	Size	Document Description	Rev
	Custom	Page49: LED DRIVER & Boost	1.0
Date: Monday, January 14, 2019		Sheet 49 of 53	



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	MS-V379	
Size Custom	Document Description Page50: FAN	Rev 1.0
Date: Tuesday, January 15, 2019		Sheet 50 of 53



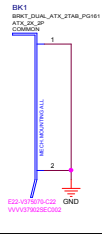
MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

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MS-V379		
Size Custom	Document Description Page51: PWR SENSE	Rev 1.0
Date: Tuesday, January 16, 2019	Sheet 61 of 63	

Bracket:



FAN:



BACK STIFFENER:



MOSFET Heatsink:



DUST COVER:



for PTA ERP:



Bracket Screw:

BKTSCREW1



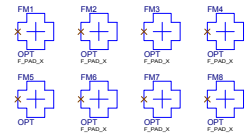
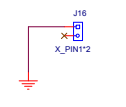
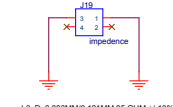
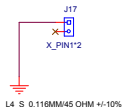
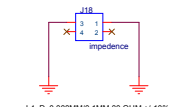
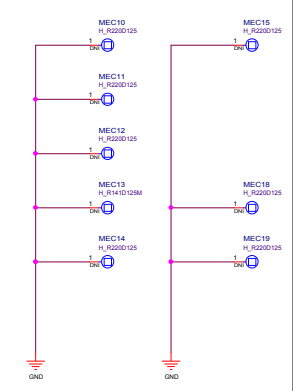
DPSCREW1



BOARD STIFFENER



Mechanical Holes Symbol:



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Size Custom	Document Description Page52: MECH	Rev 1.0
Date: Tuesday, January 15, 2019		Sheet 82 of 83

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Size	Document Description	Rev
Custom	Page53: PTC	1.0
Date: Monday, January 14, 2019	Sheet	53 of 53