

PG161-A01

TU116 6GB 12Gbps GDDR6 DVI-D/DP/DP + HDMI + DP

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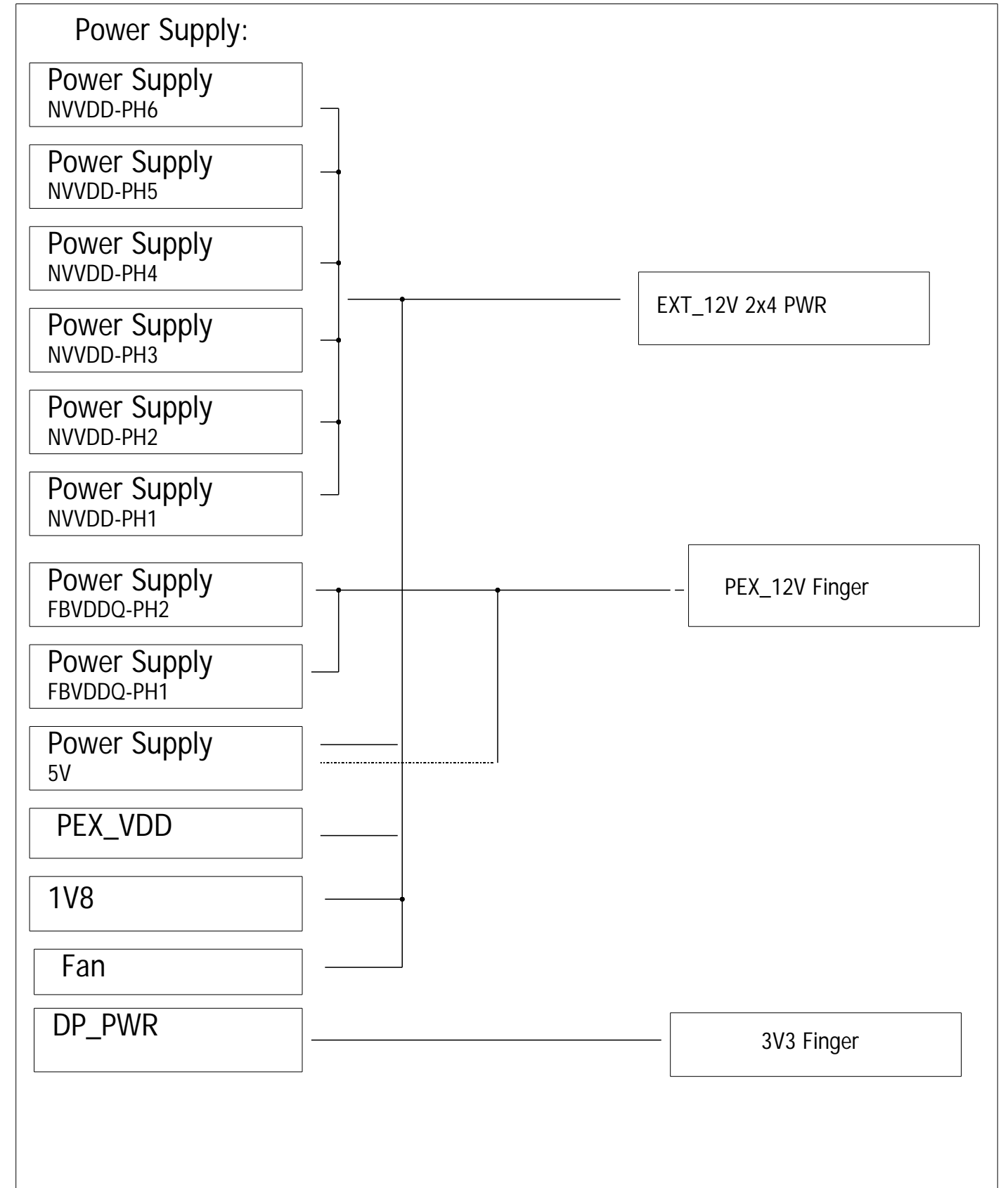
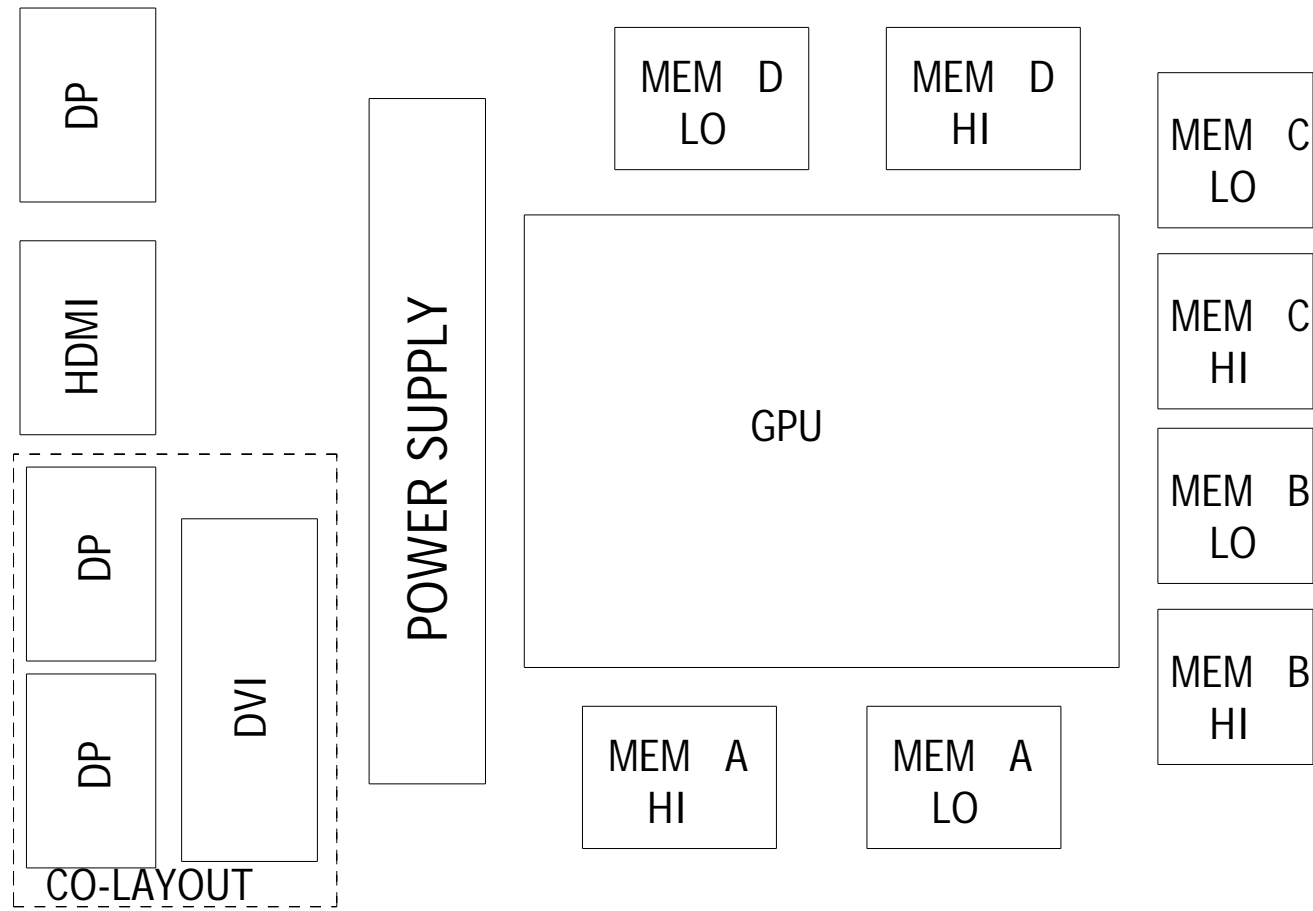
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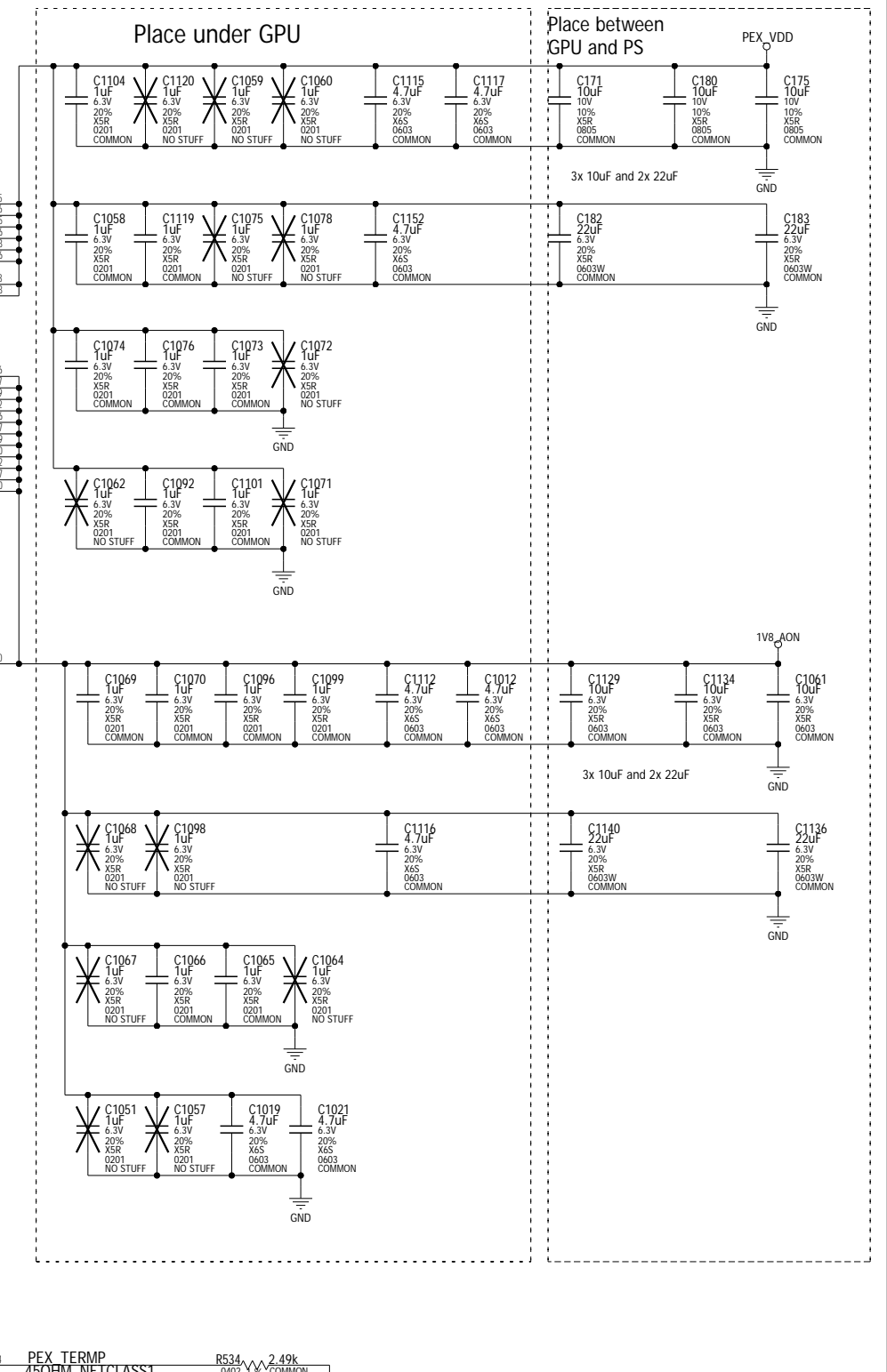
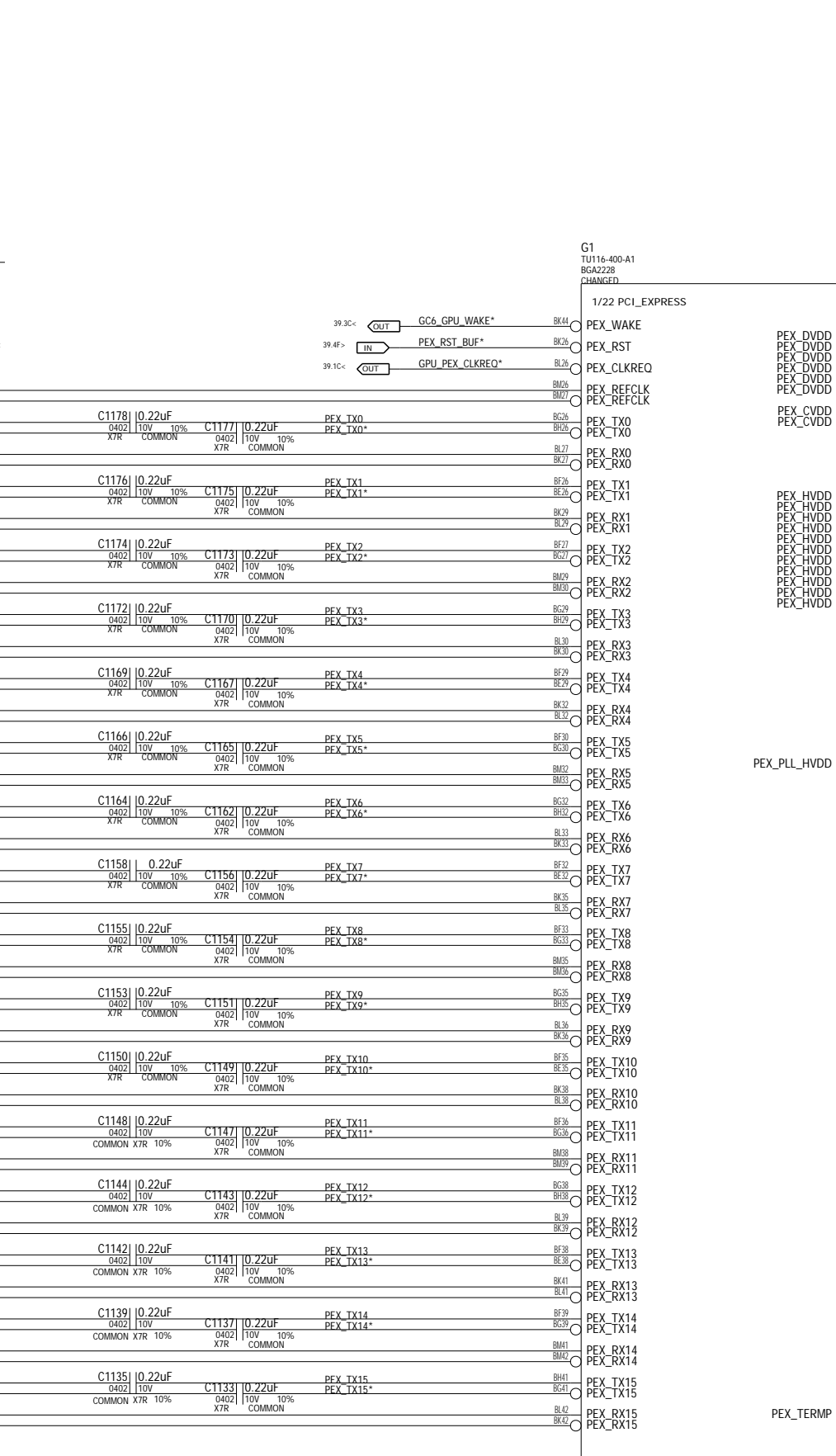
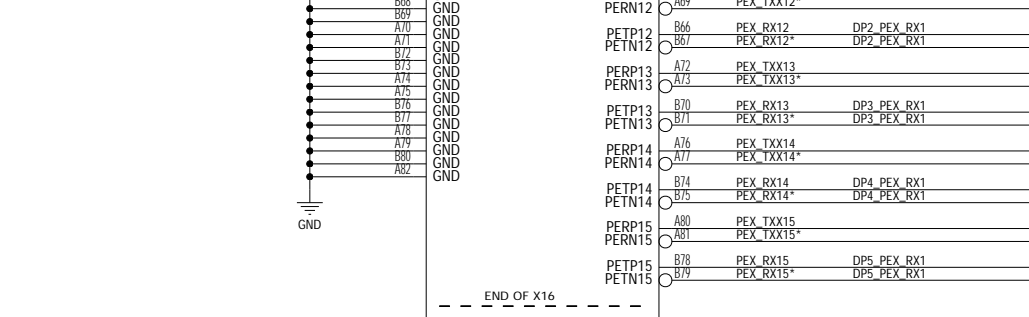
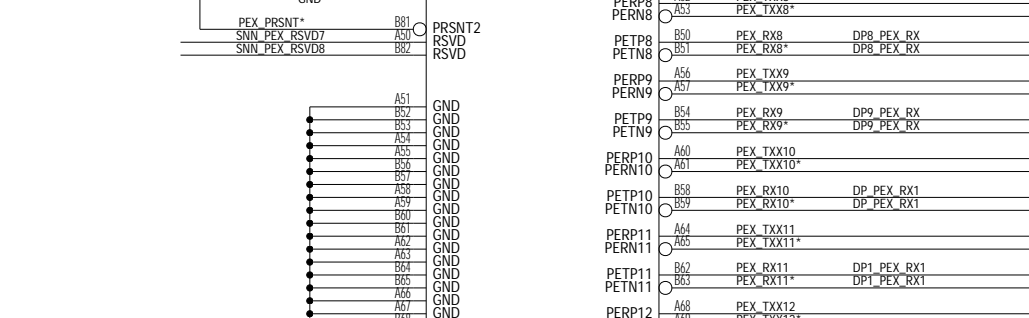
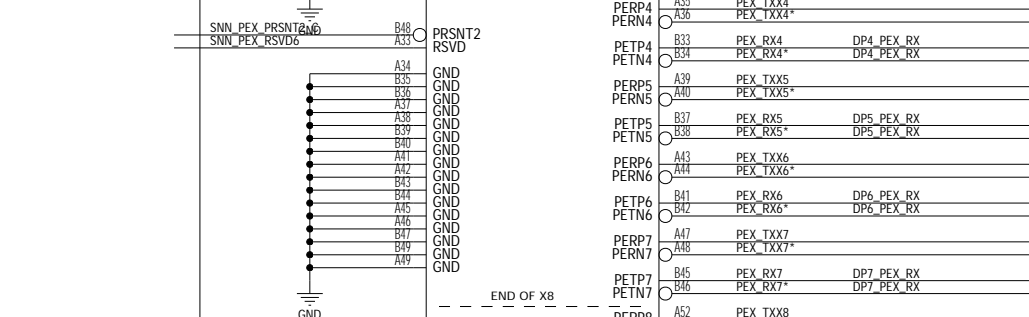
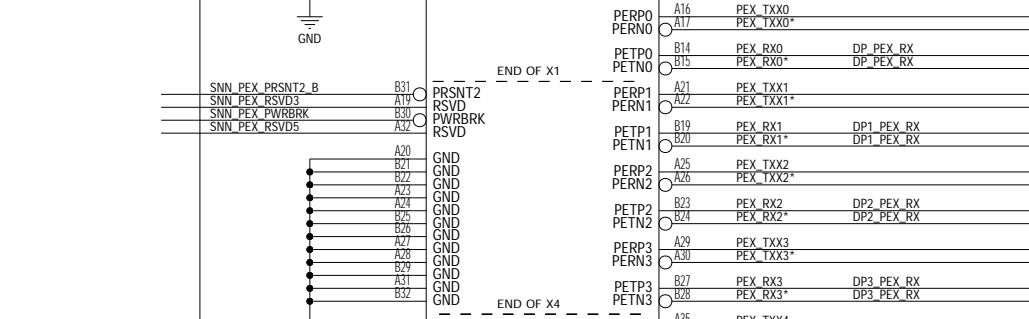
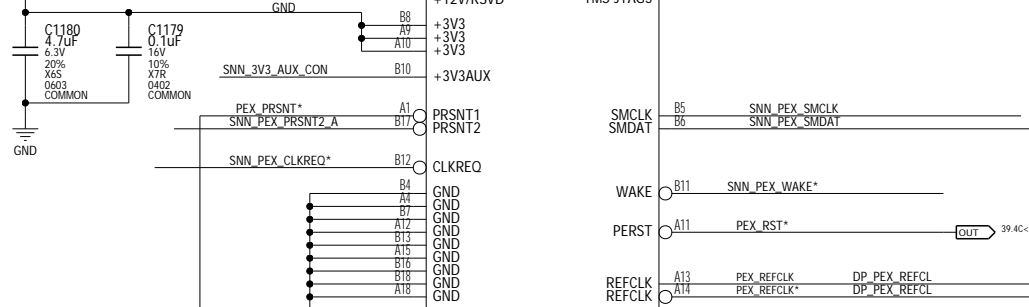
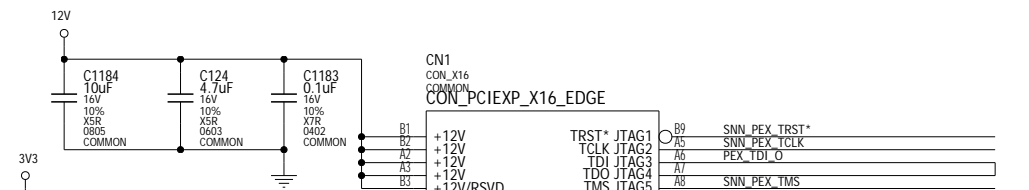
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VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	5.5A	0.406
3V3	3.0A	0.400



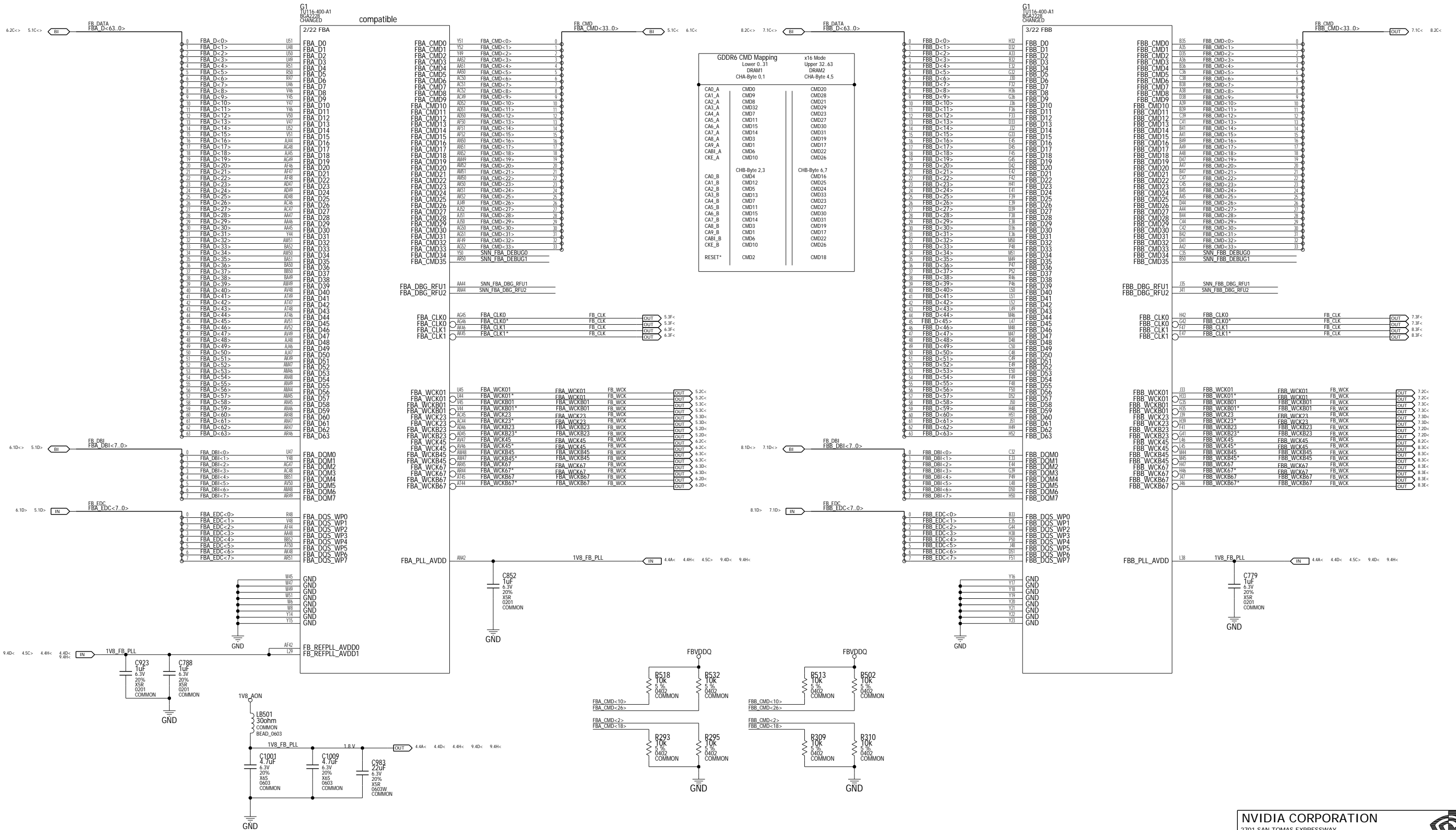
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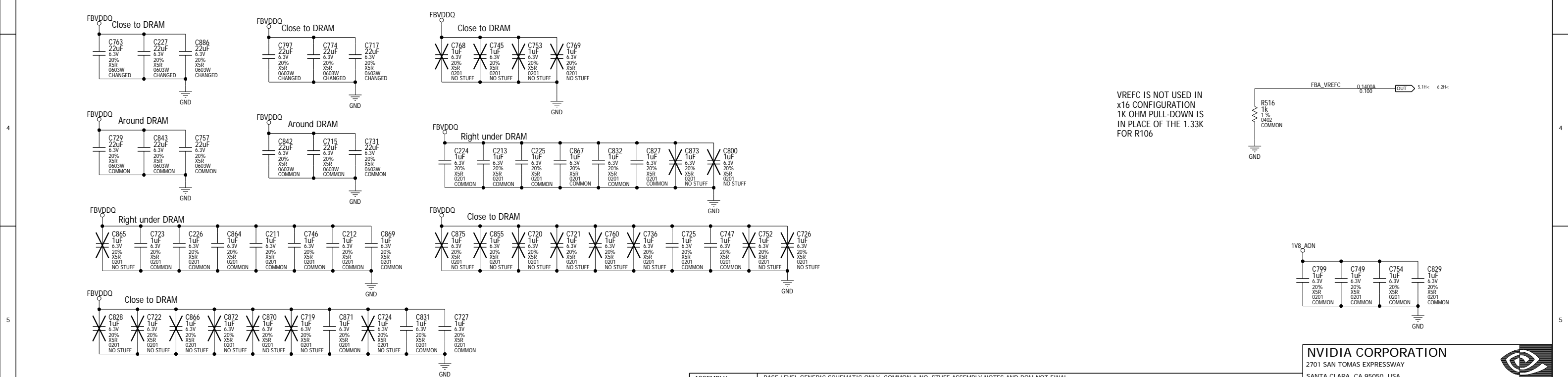
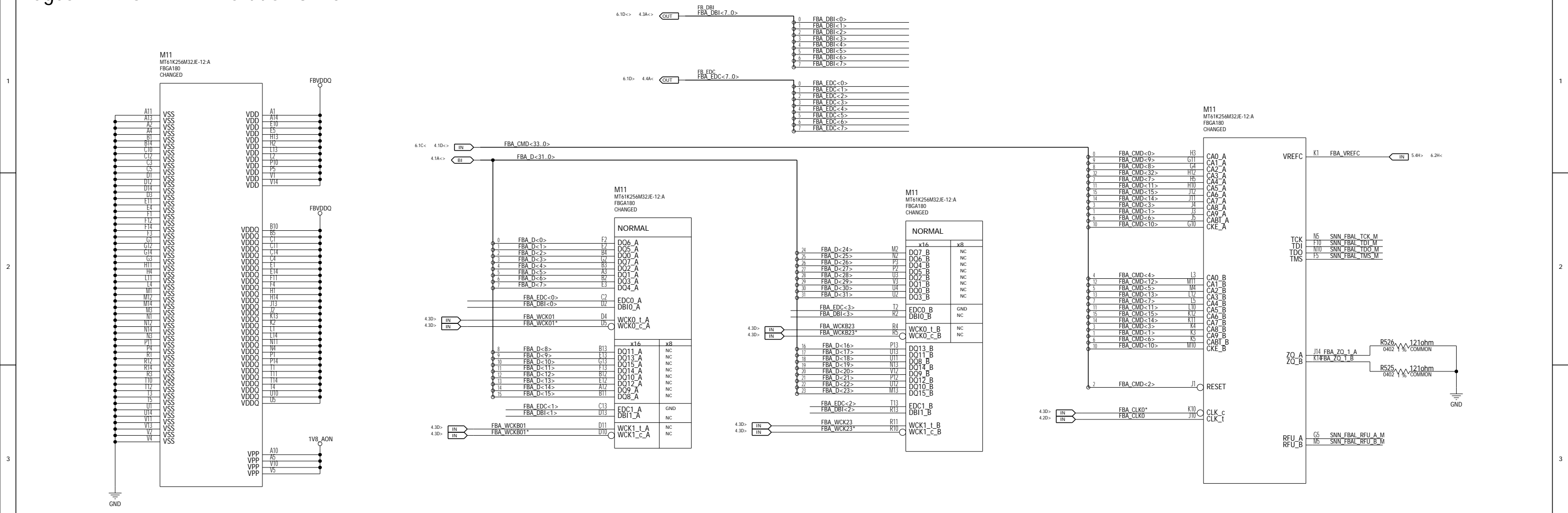
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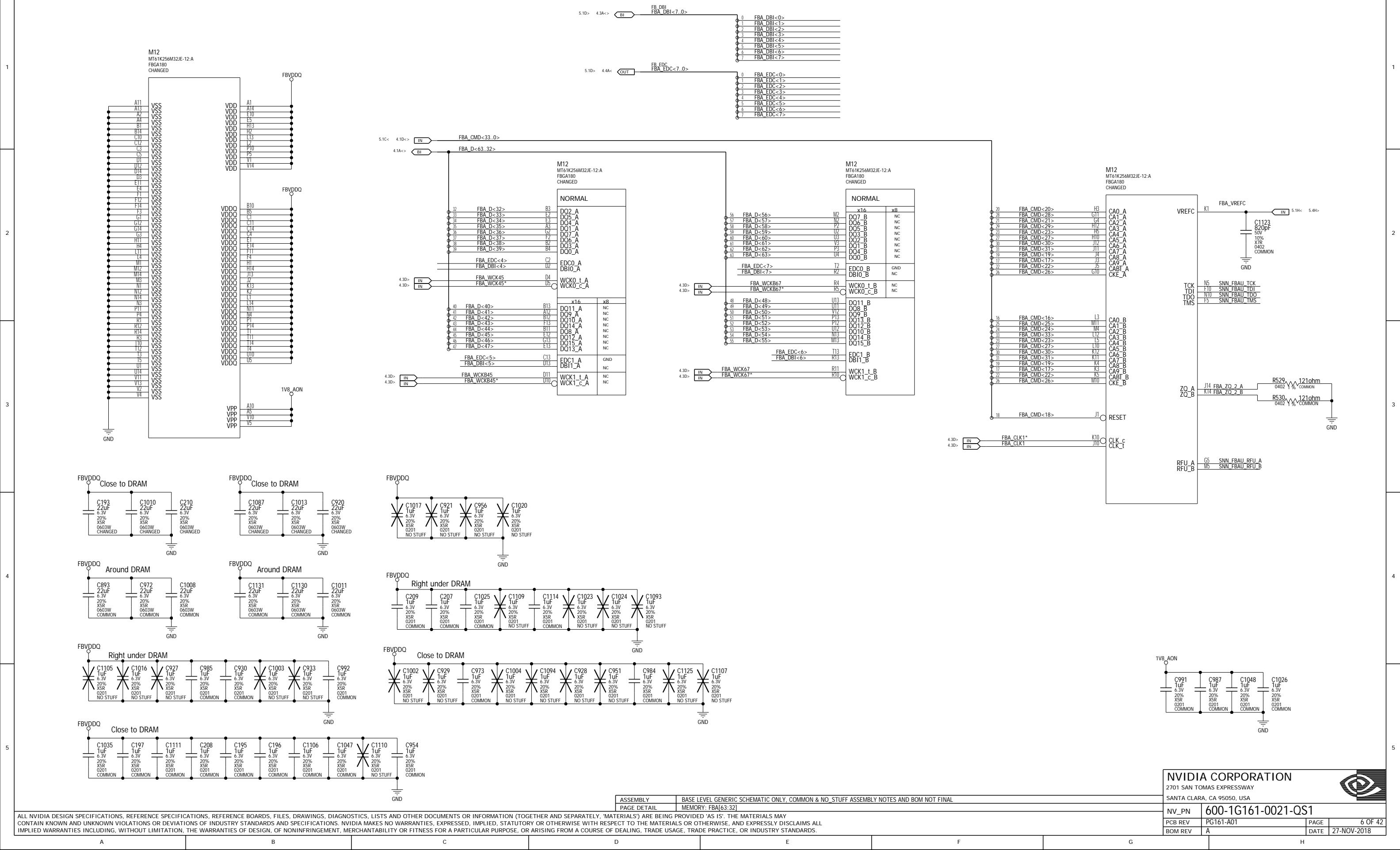
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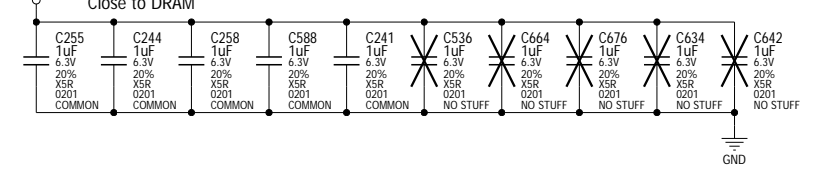
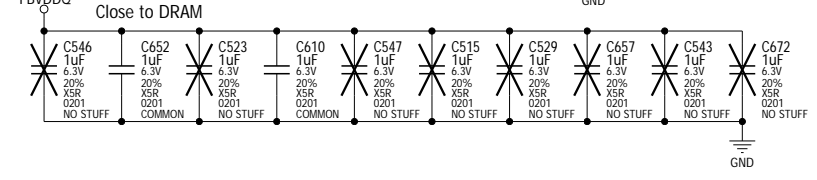
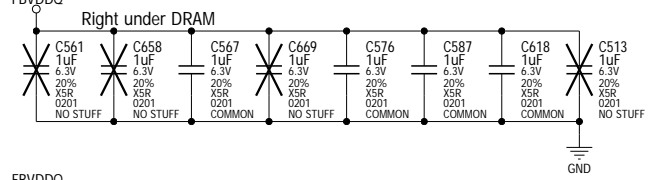
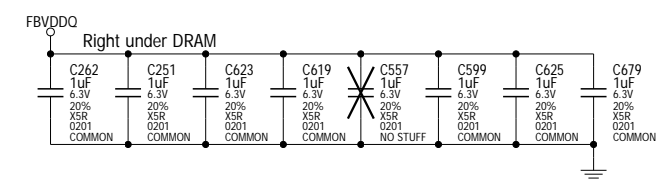
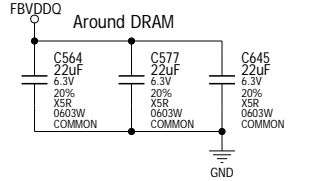
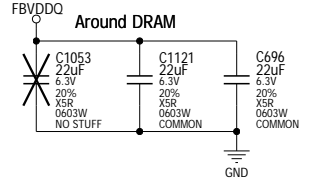
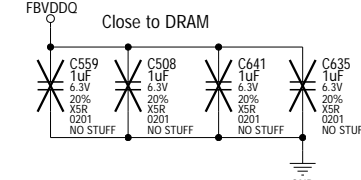
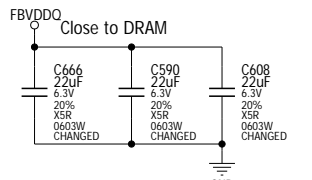
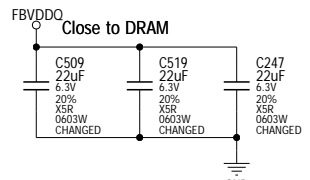
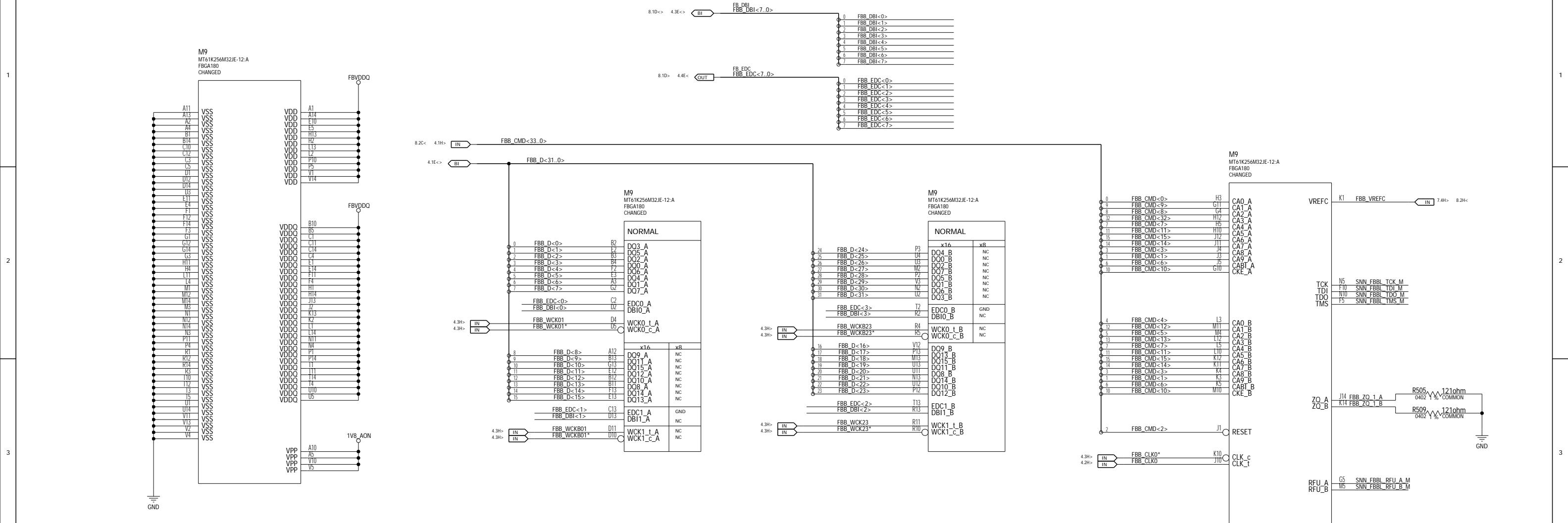
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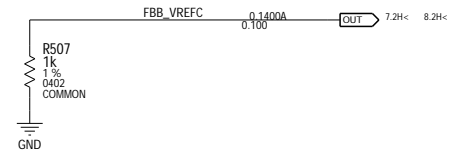


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1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R104



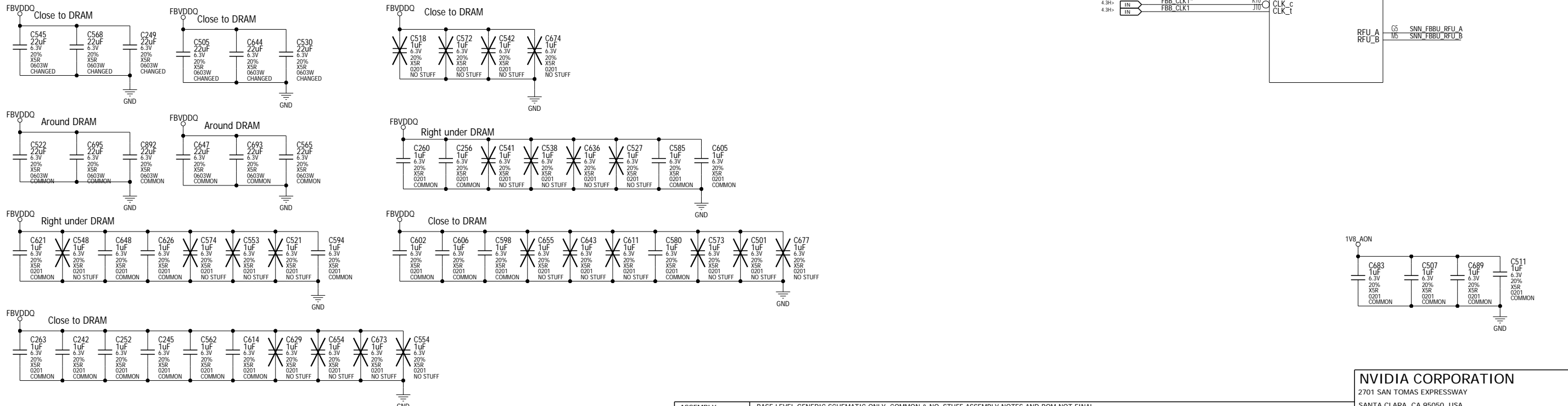
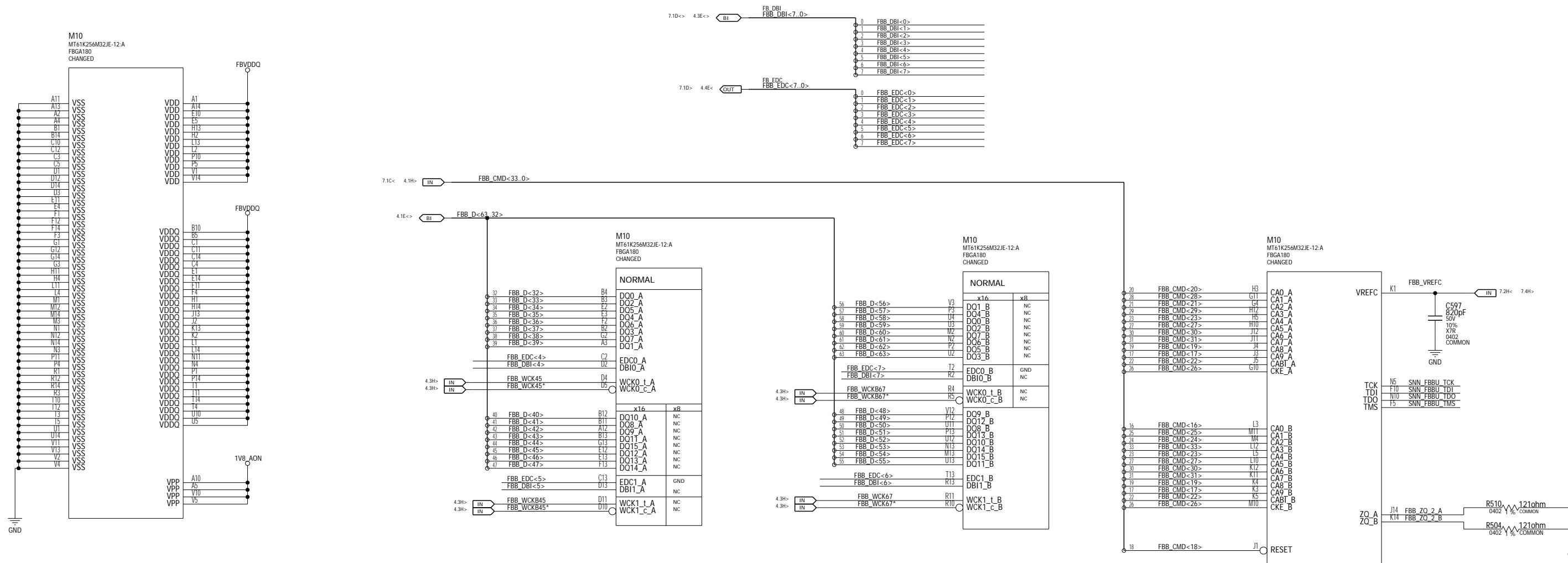
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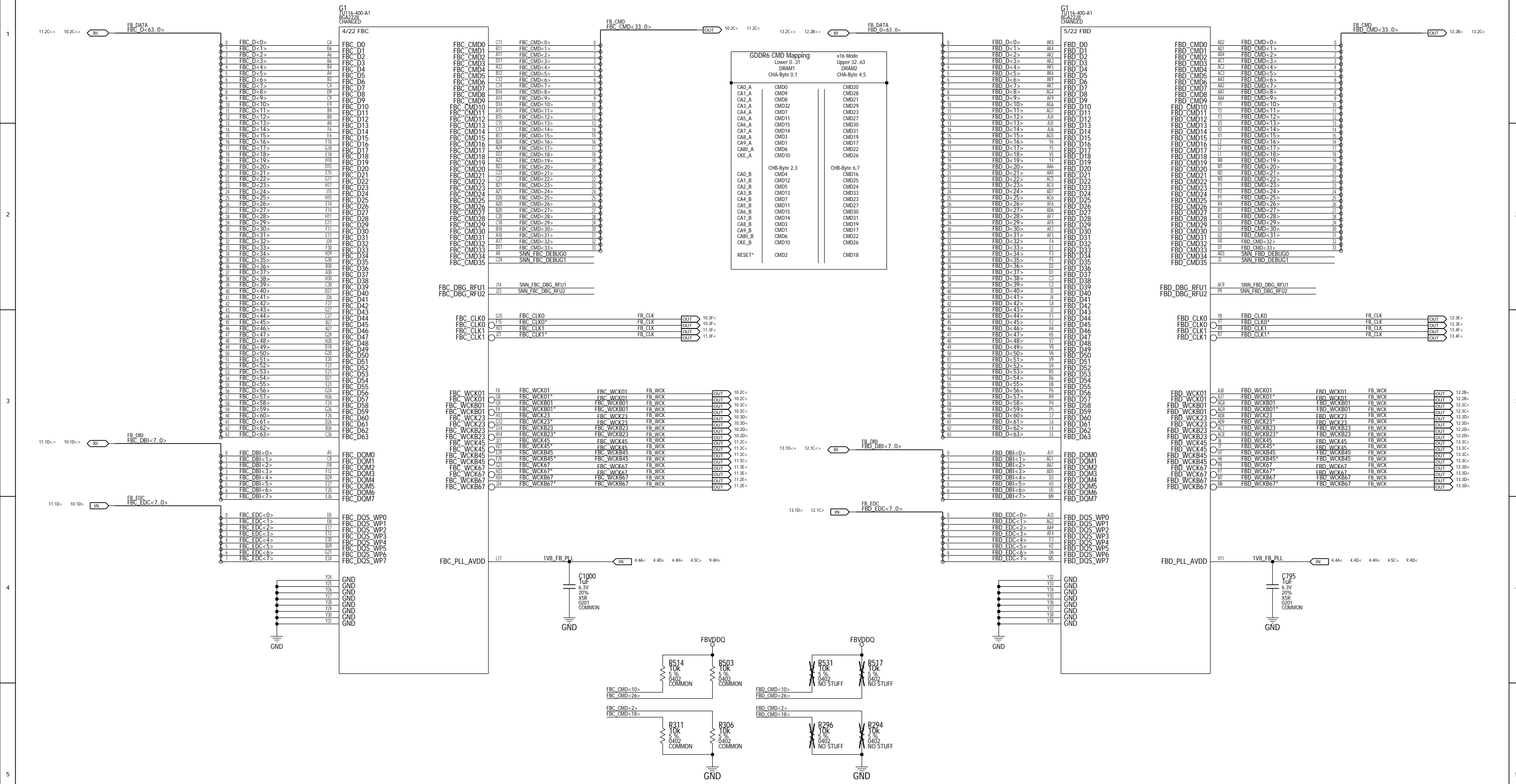
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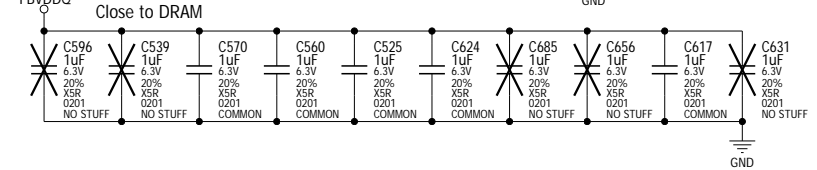
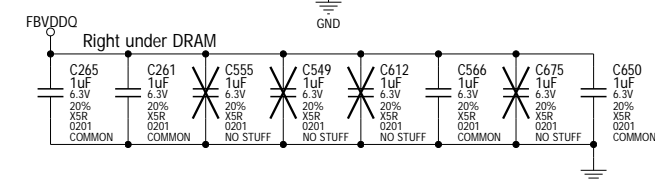
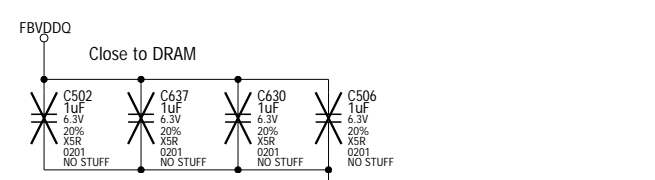
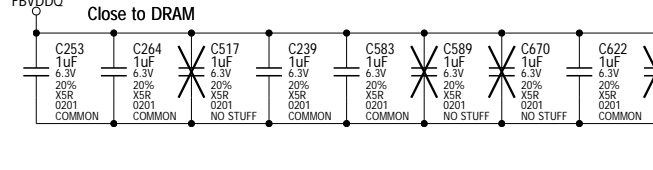
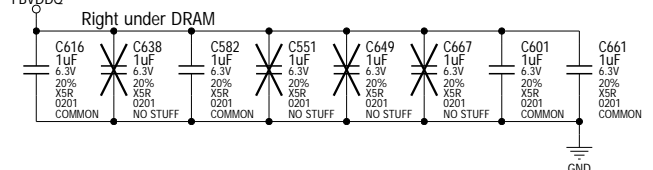
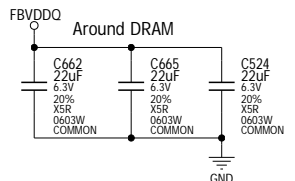
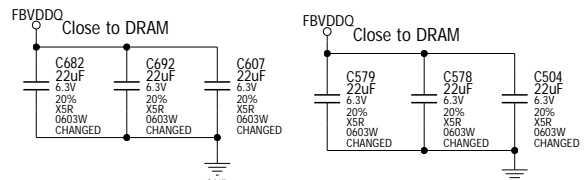
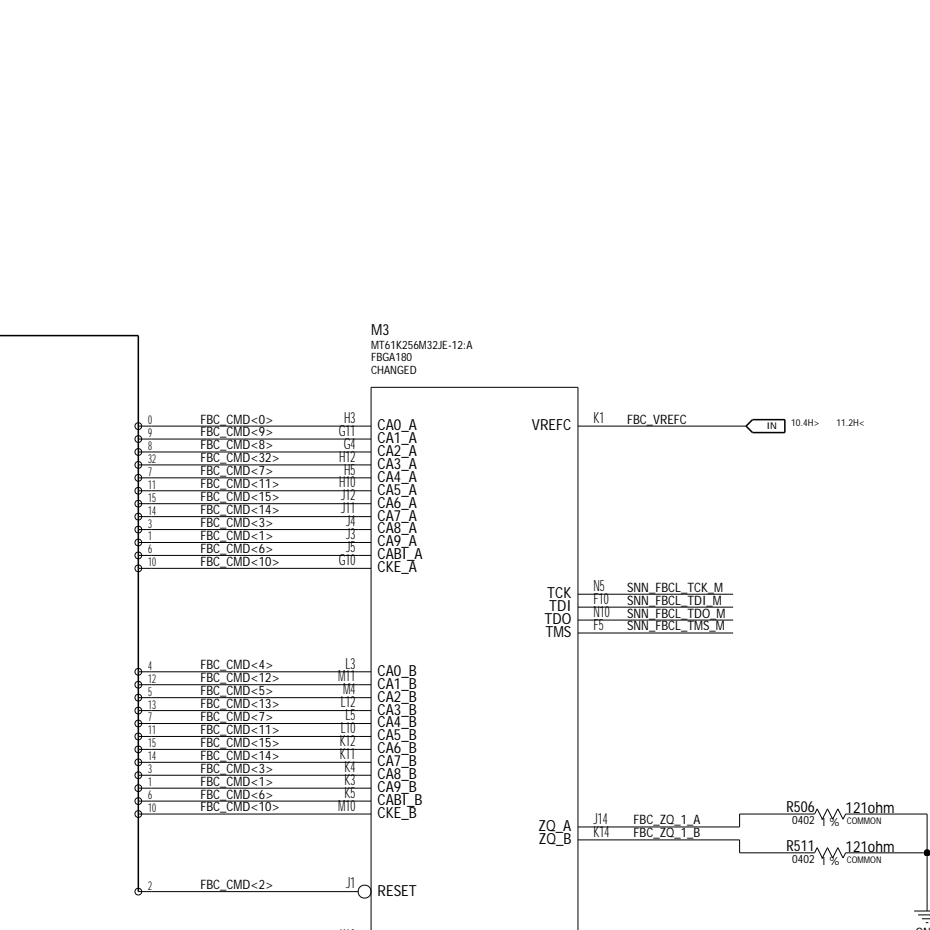
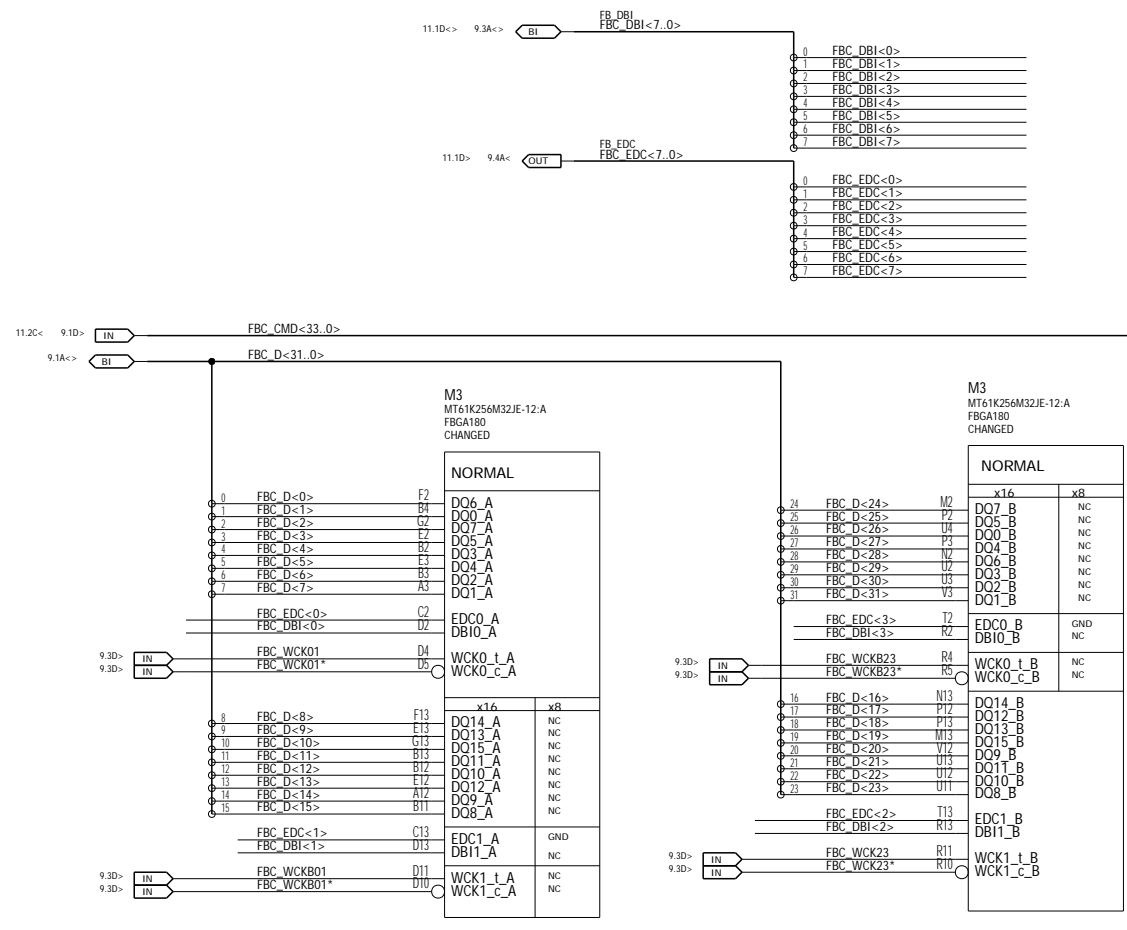
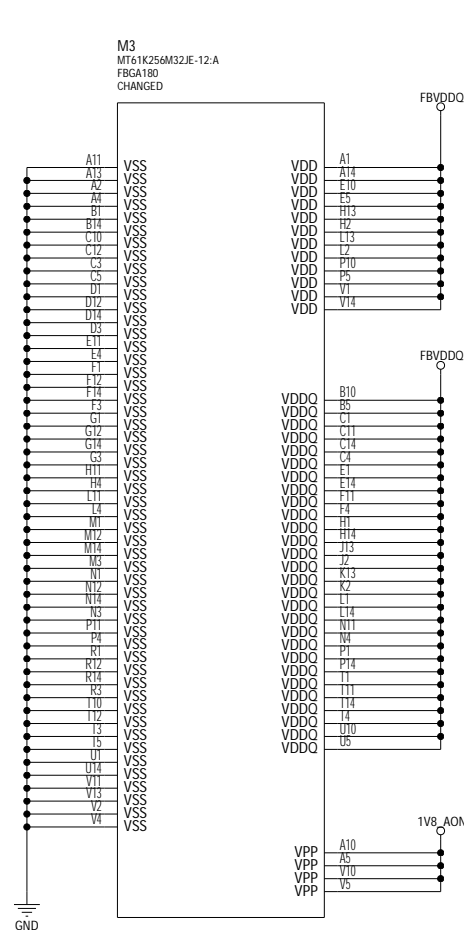
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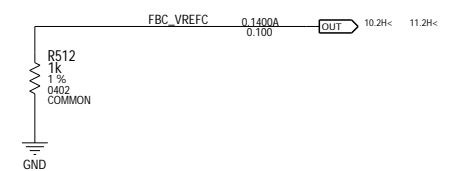
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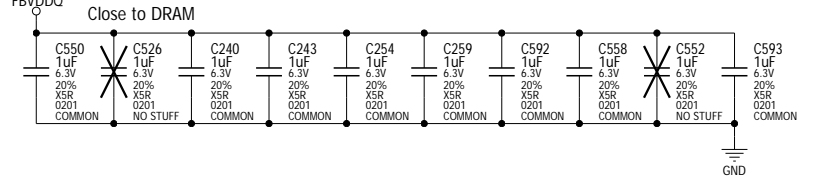
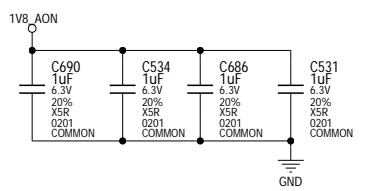
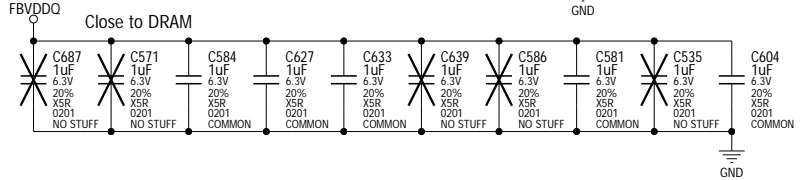
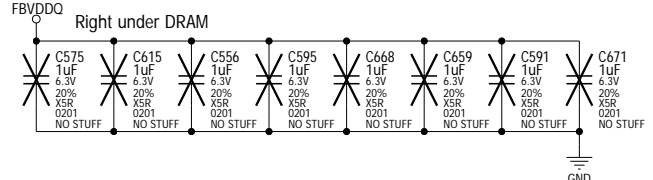
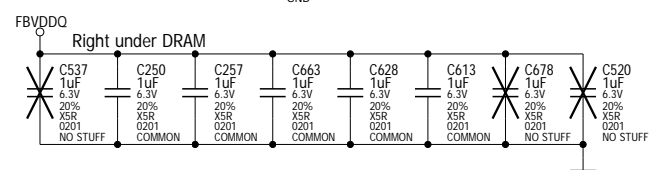
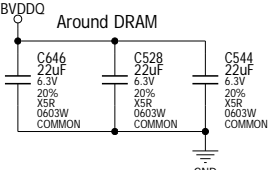
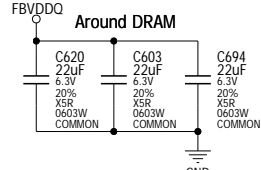
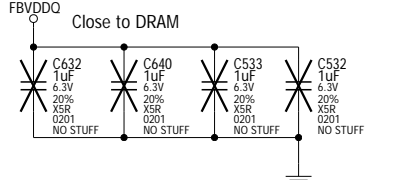
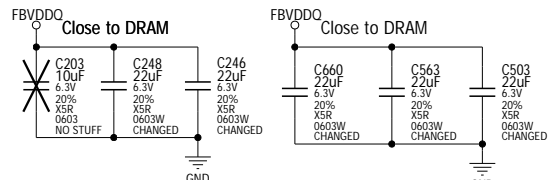
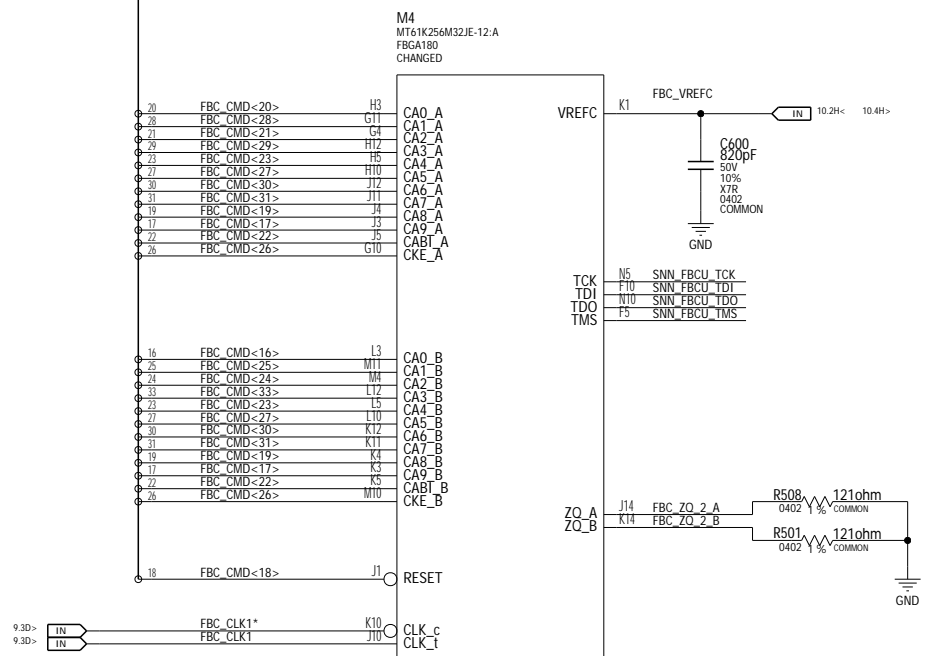
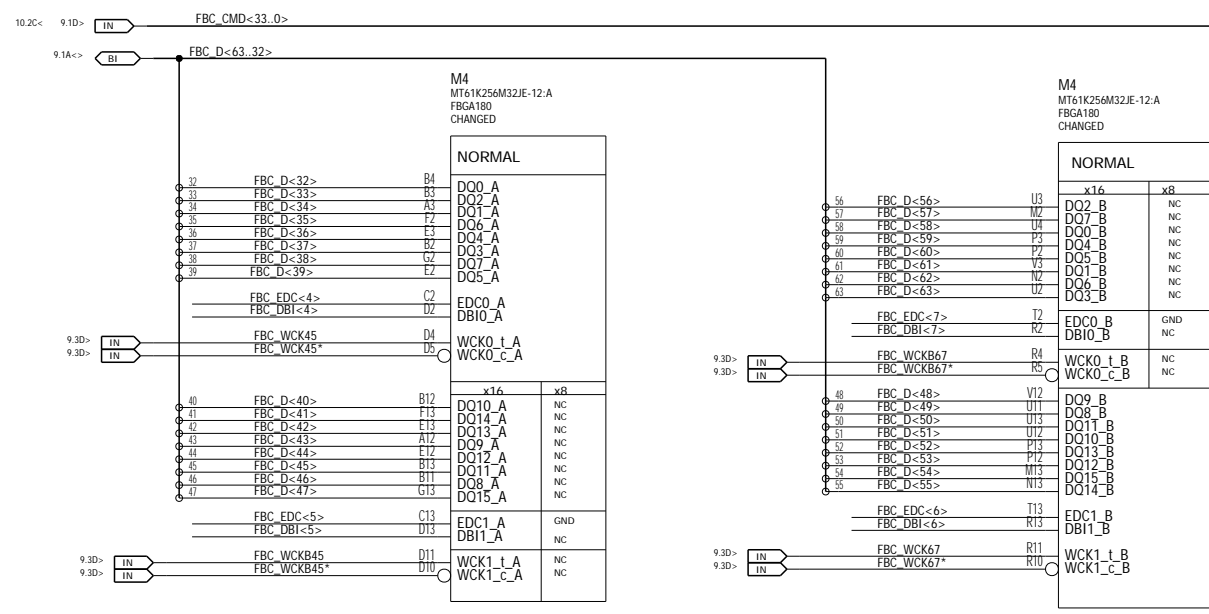
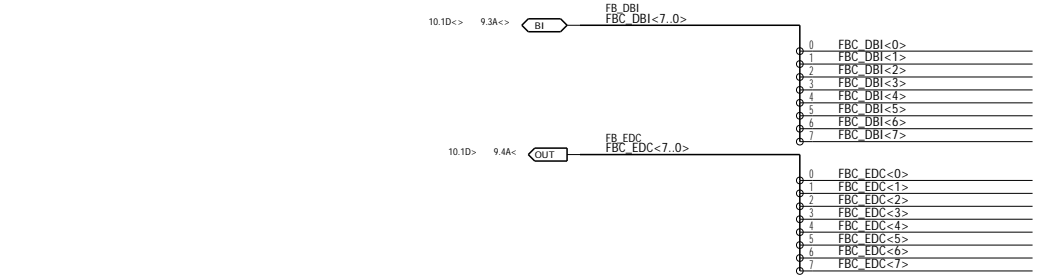
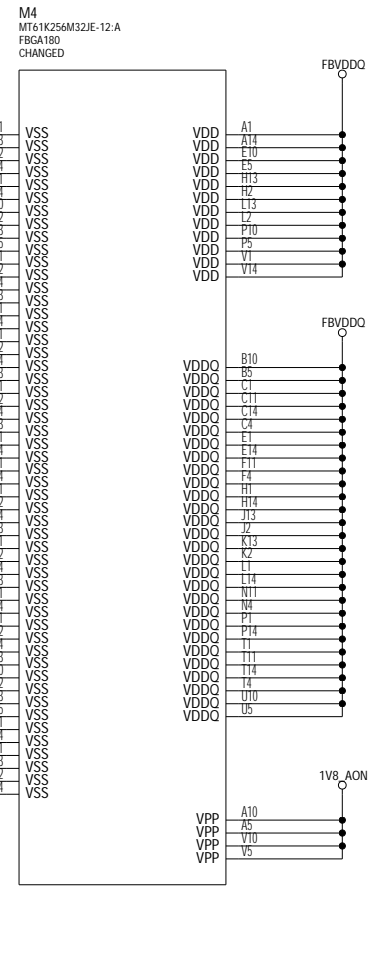


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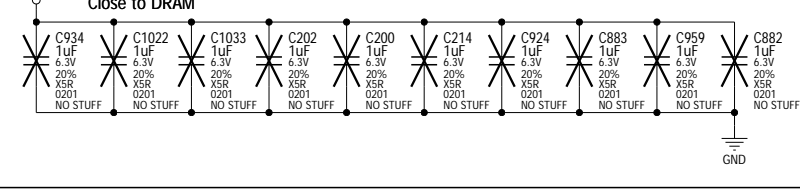
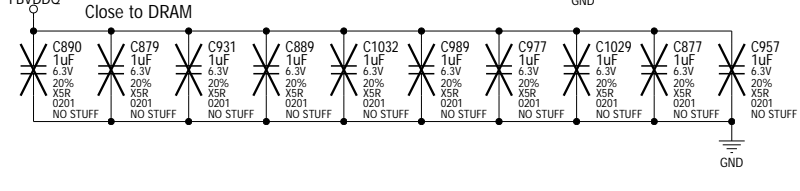
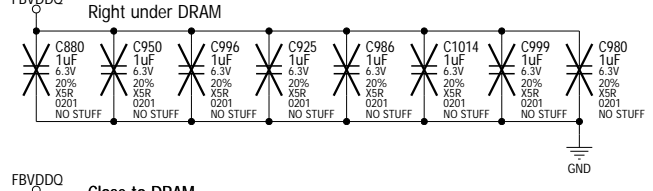
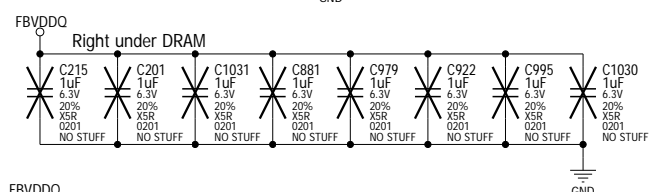
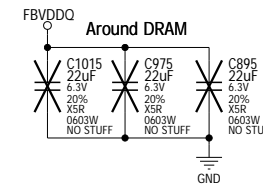
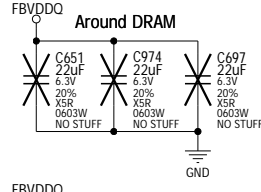
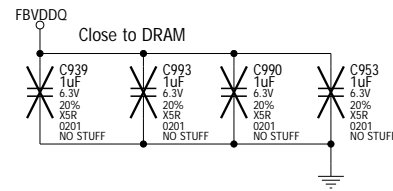
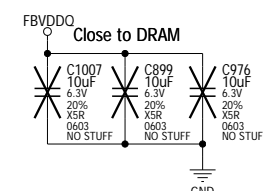
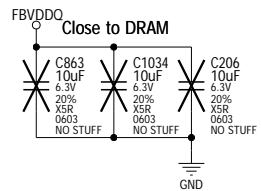
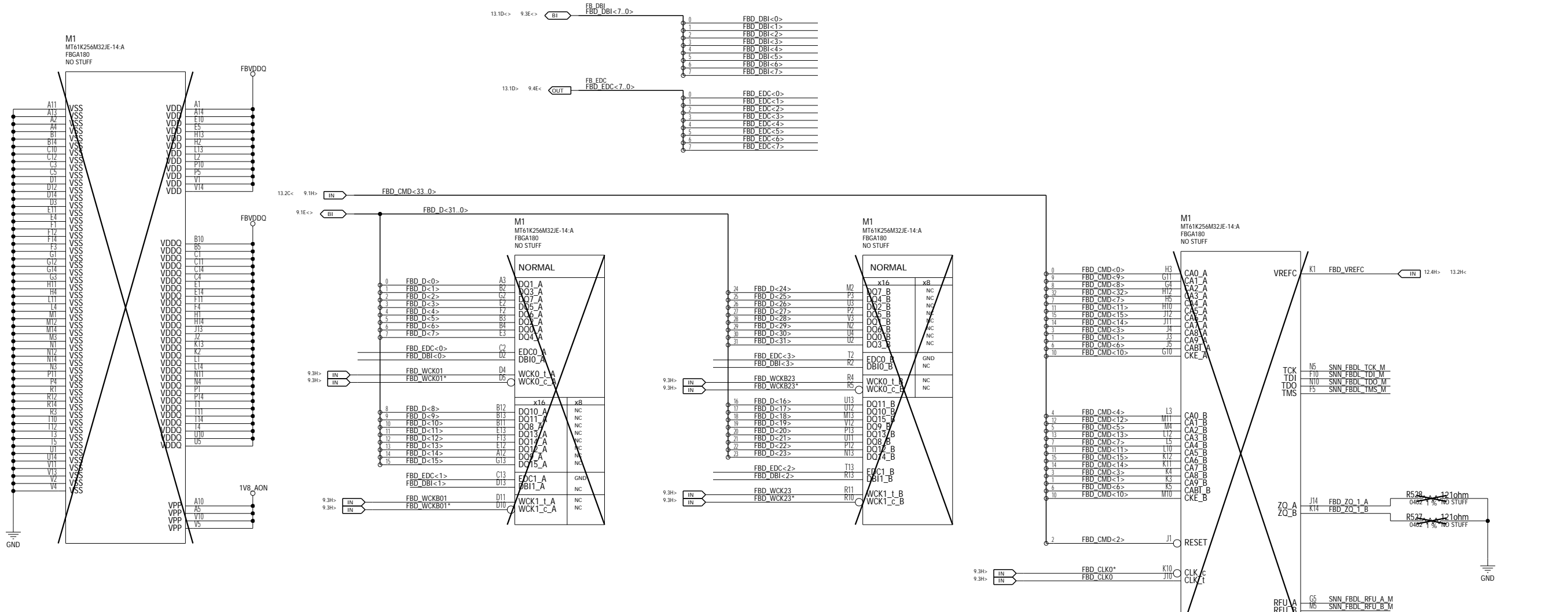
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 PCB REV: PG161-A01
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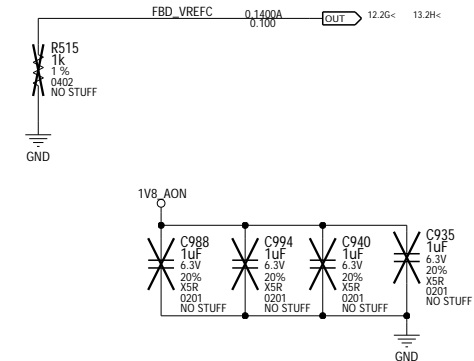
DATE: 27-NOV-2018

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
 PAGE DETAIL: MEMORY: FBC[63:32]

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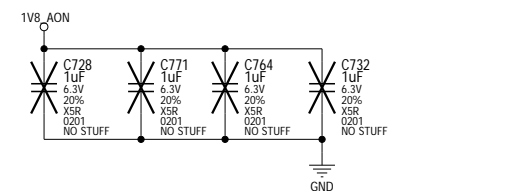
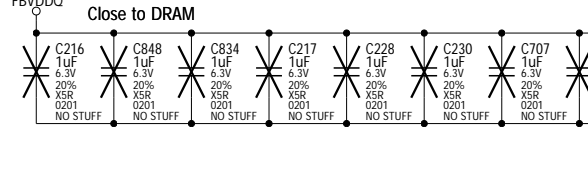
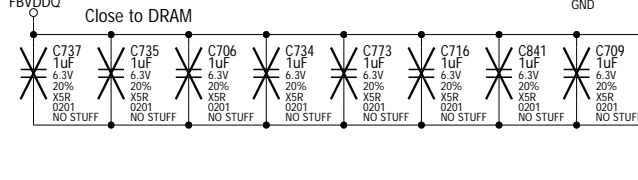
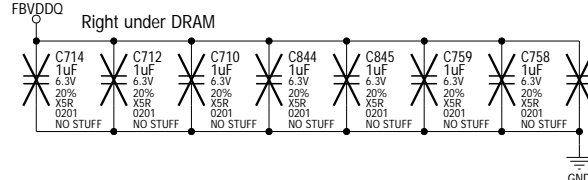
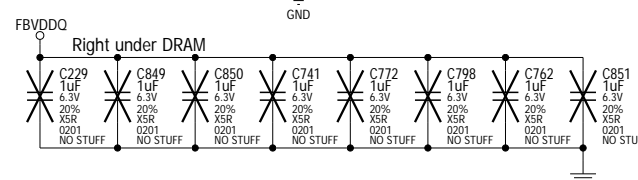
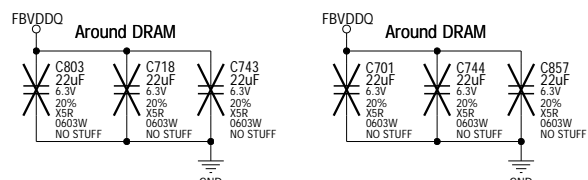
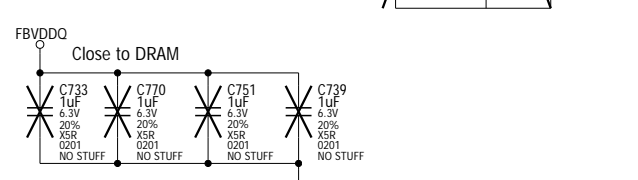
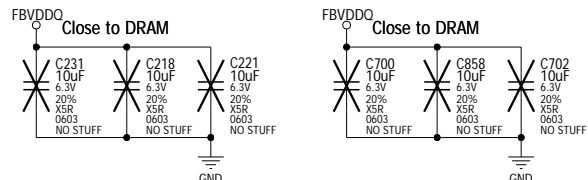
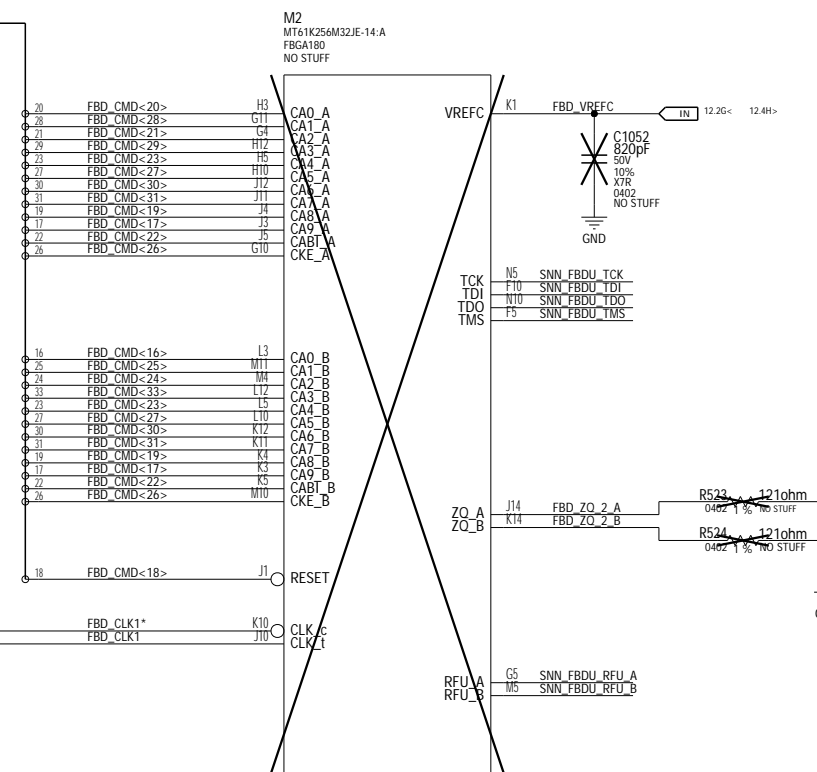
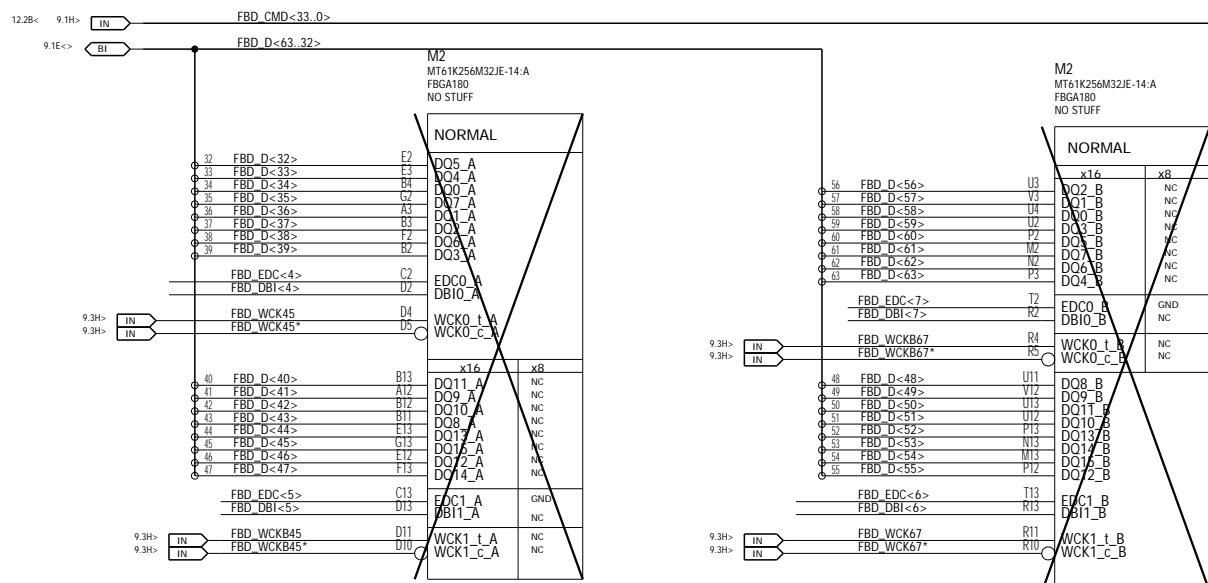
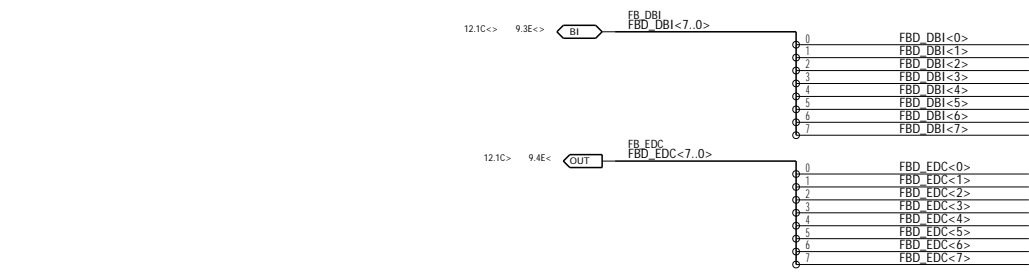
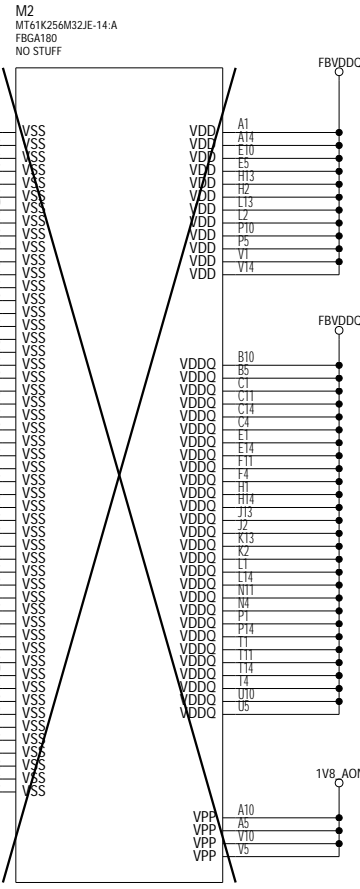


VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R62



ASSEMBLY		BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL	
PAGE DETAIL		MEMORY: FBD[31:0]	
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
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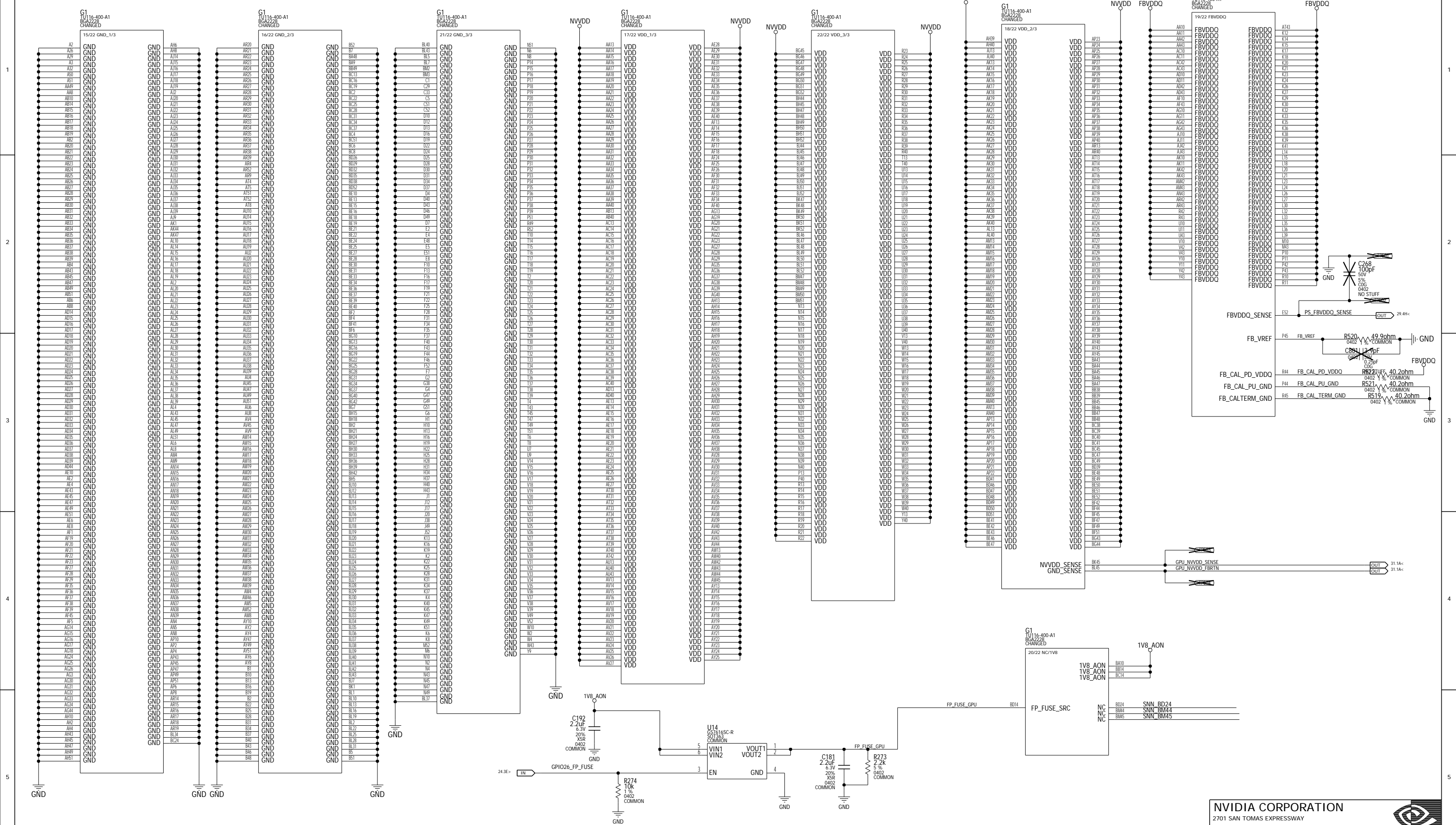
NV_PN: 600-1G161-0021-QS1
 PCB REV: PG161-A01
 BOM REV: A

DATE: 27-NOV-2018

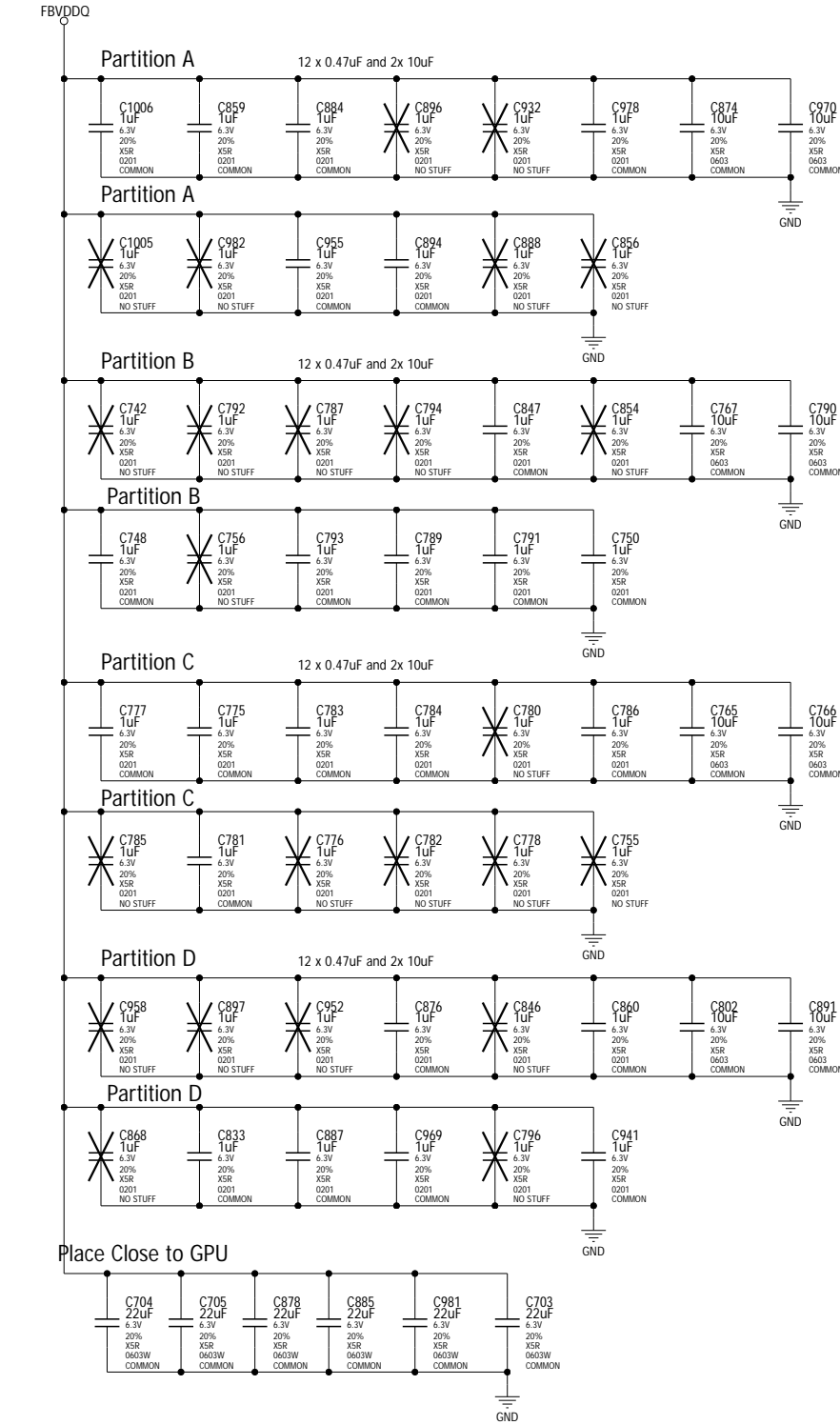
PAGE: 13 OF 42

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
 PAGE DETAIL: MEMORY: FBD[63:32]

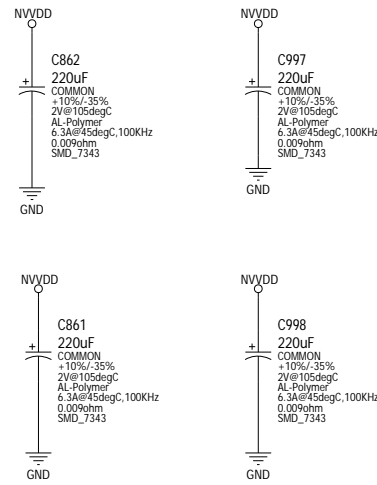
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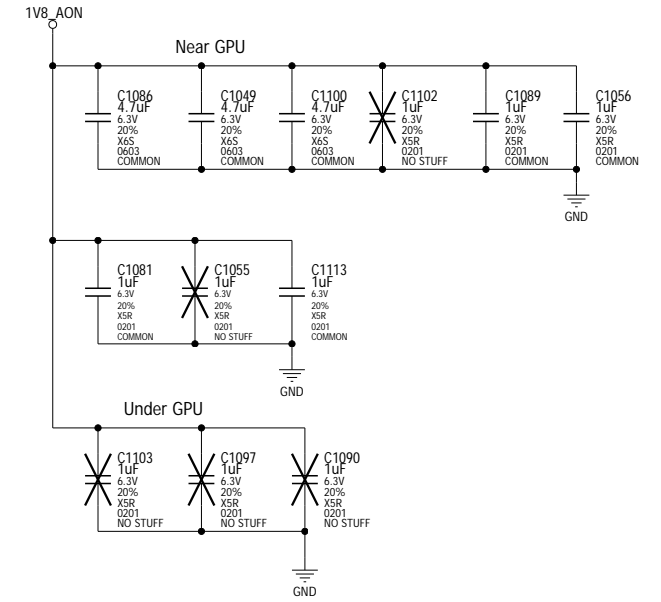
FBVDDQ



NVVDD



1V8_AON



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU Decoupling

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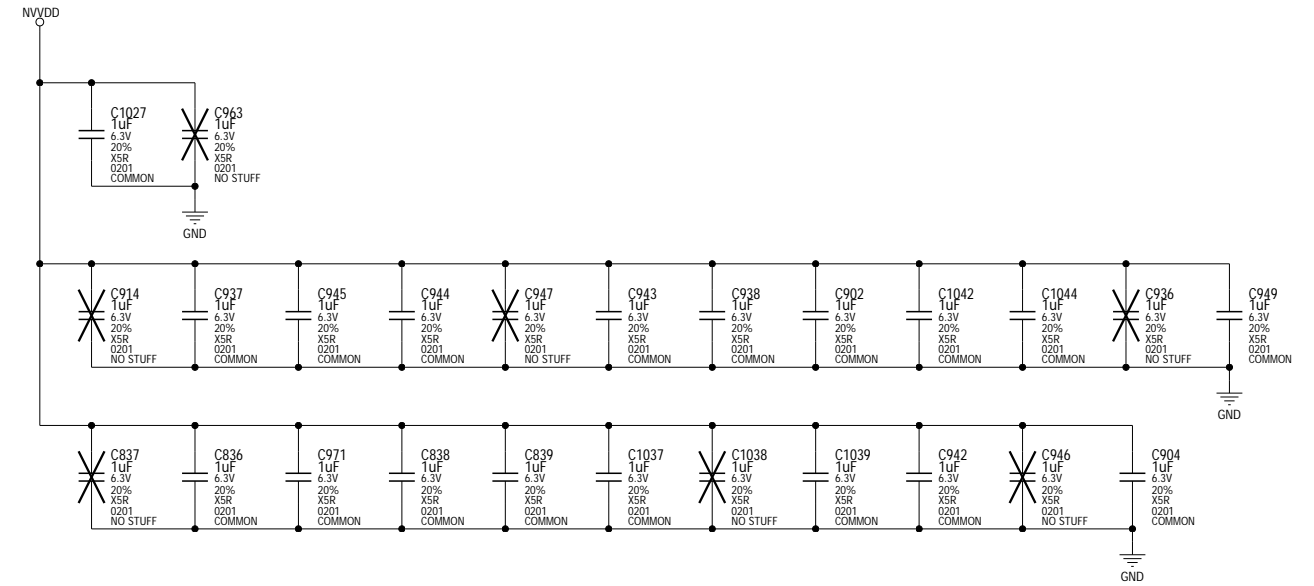
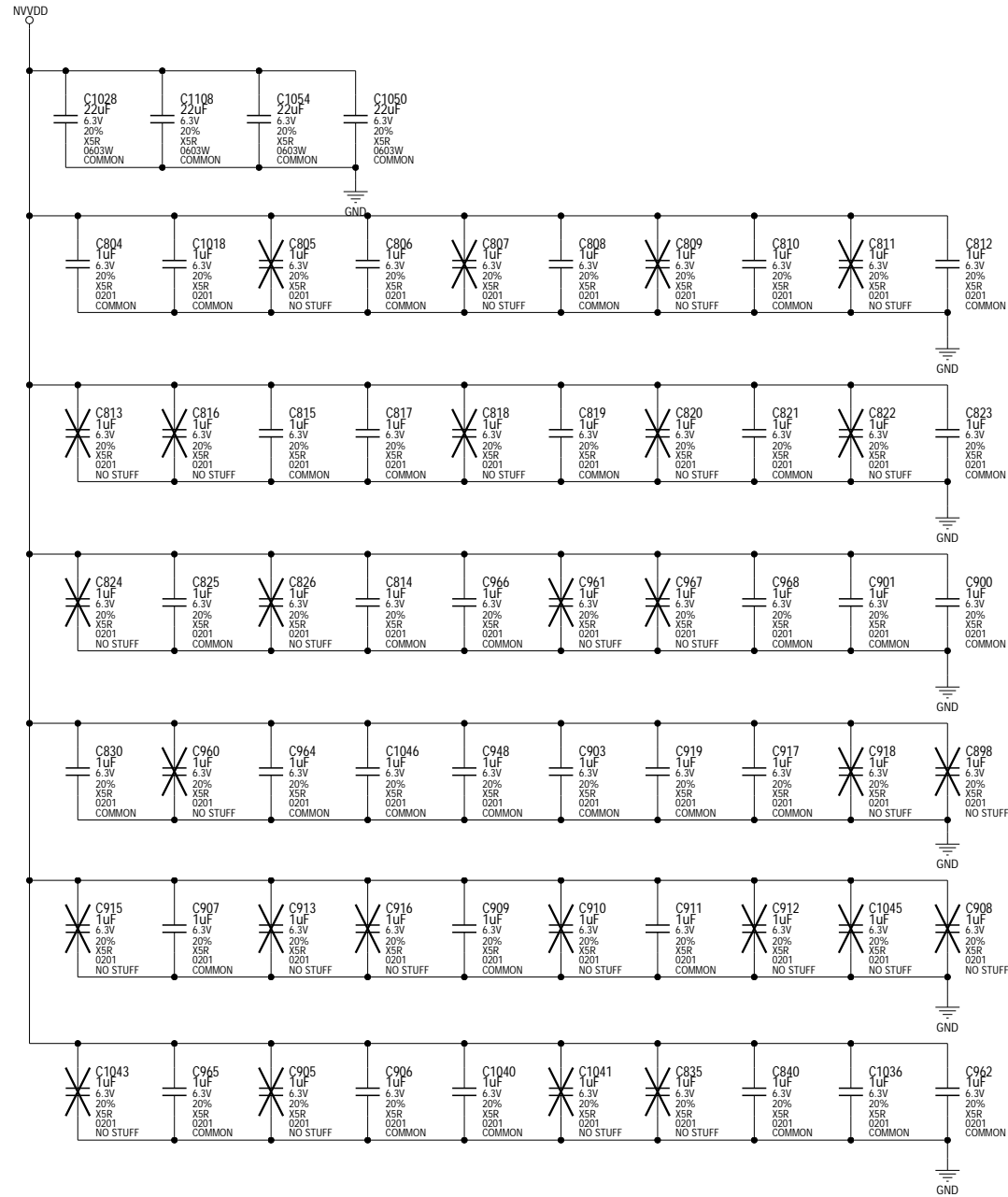


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Page16: GPU Decoupling 2

NVVD



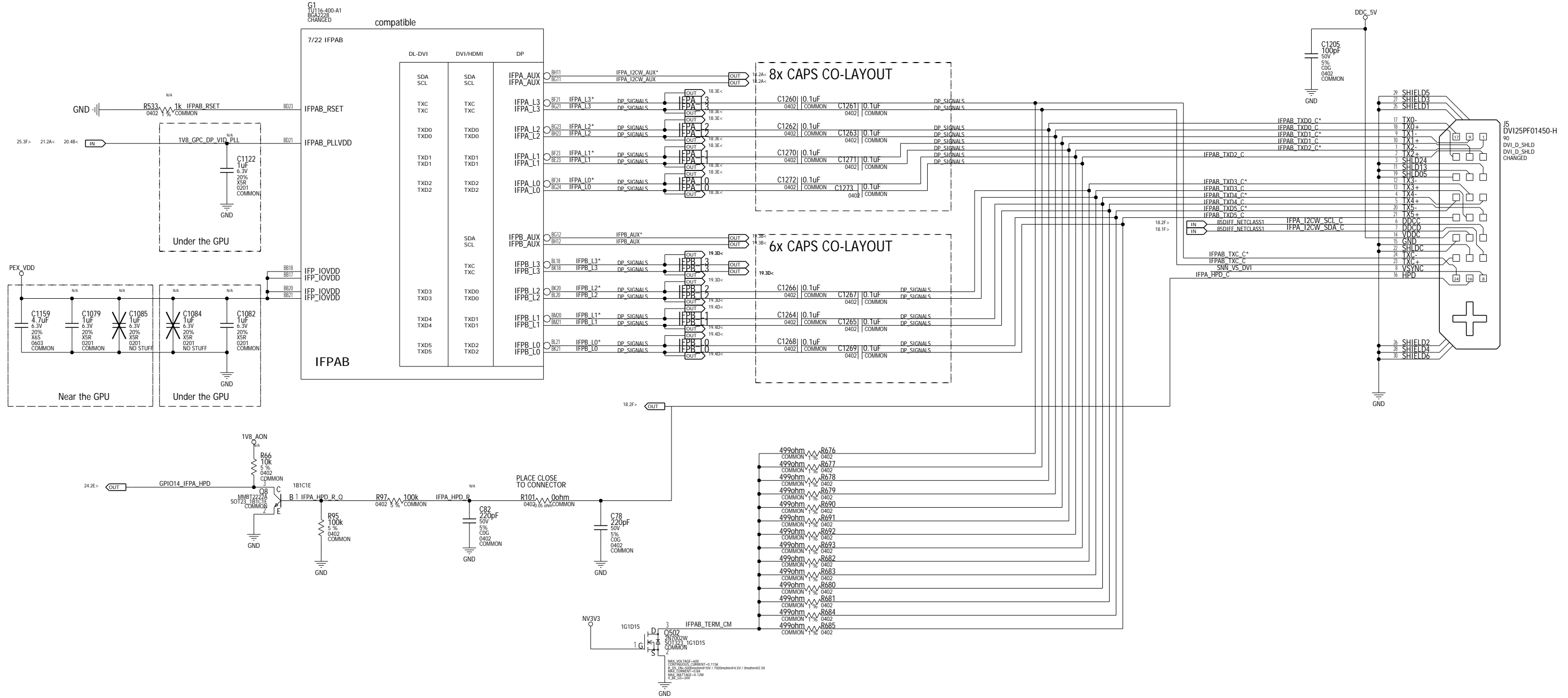
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PAGE DETAIL	GPU Decoupling2

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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP

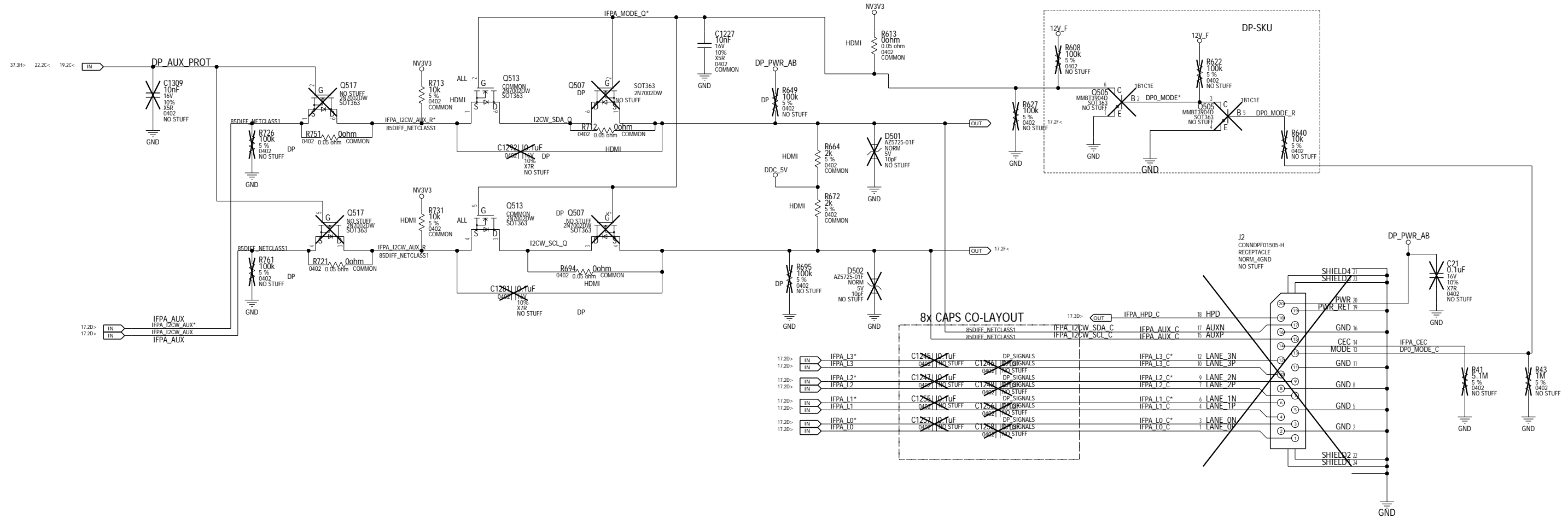


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IO: IFPAB DVI-D-DL



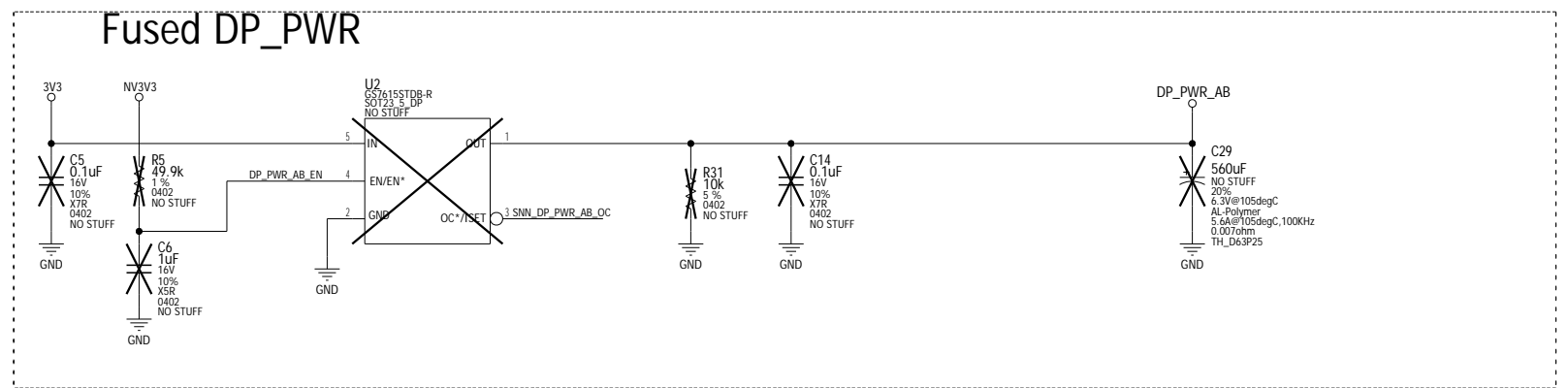
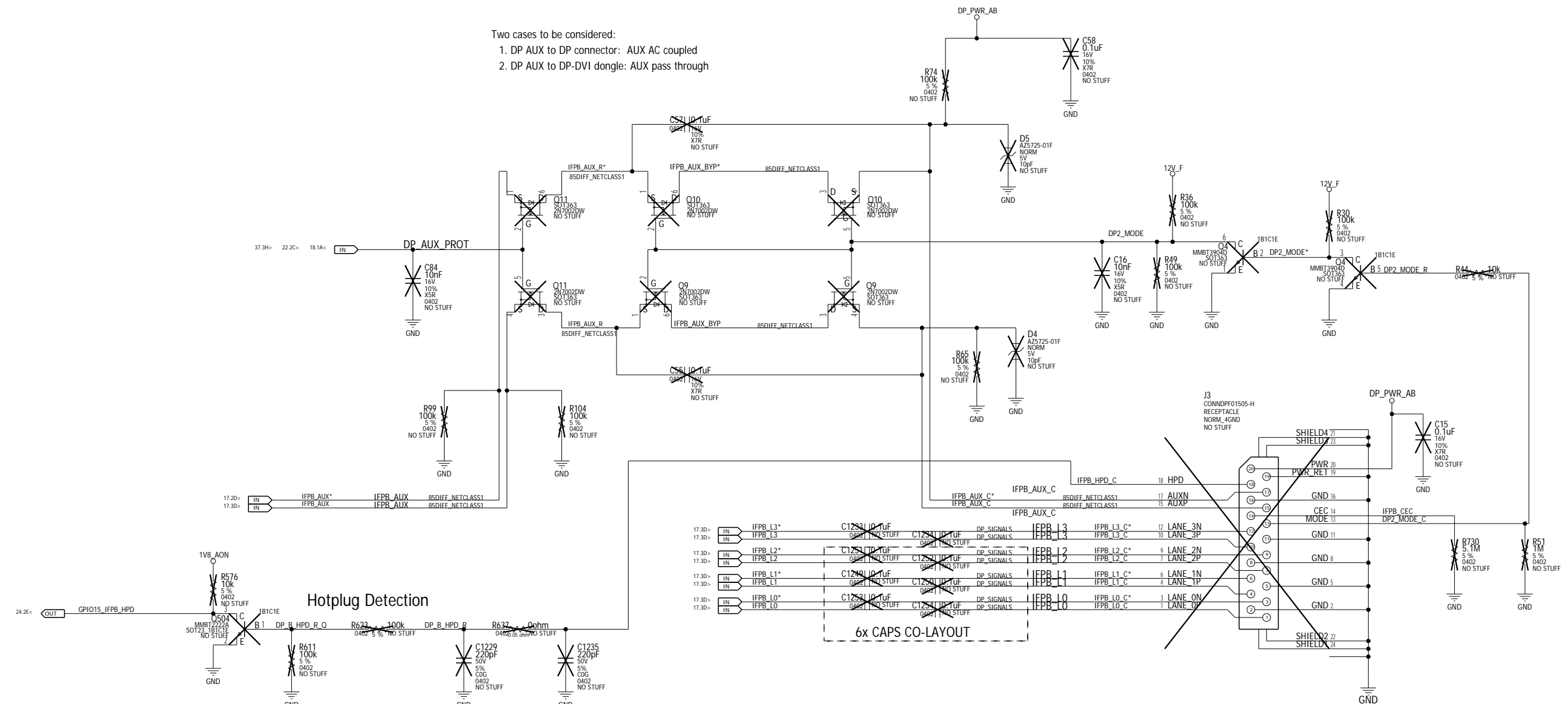
IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IO: IFPA DP

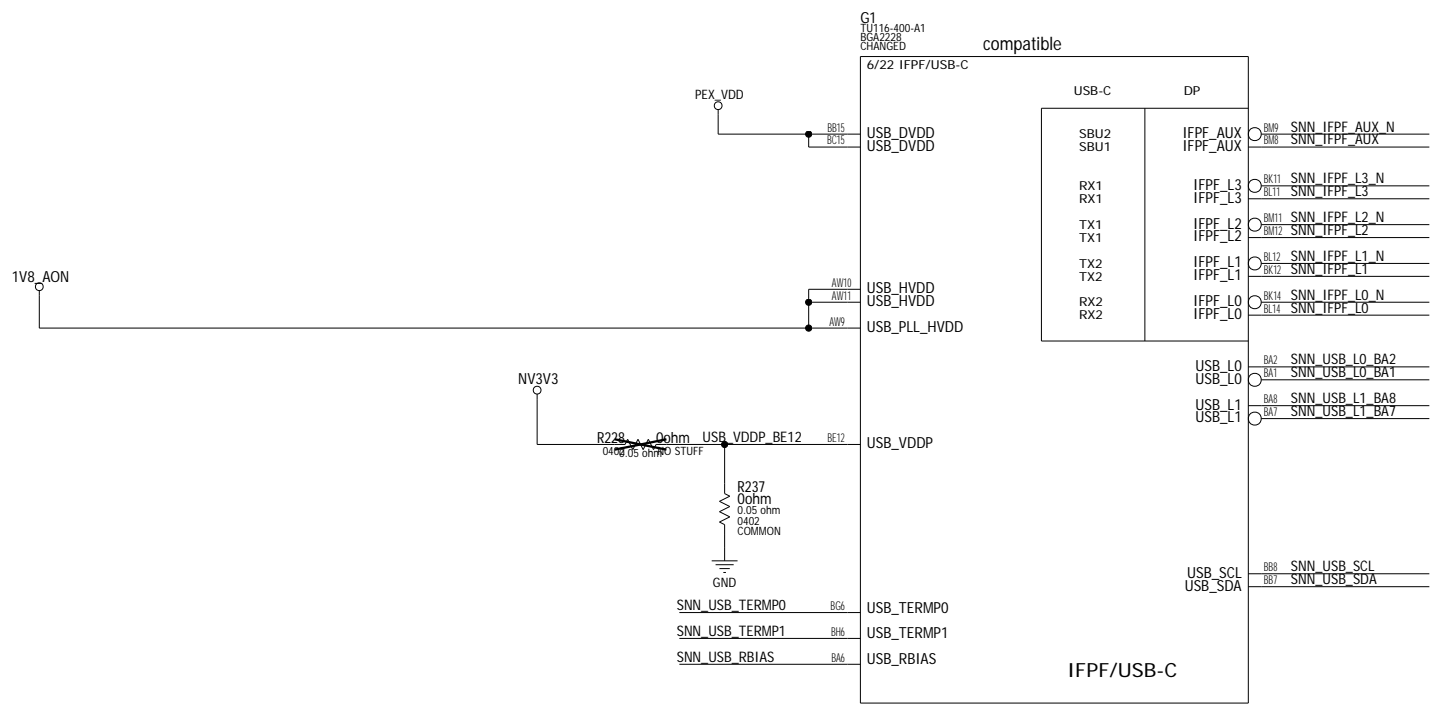
IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

- Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

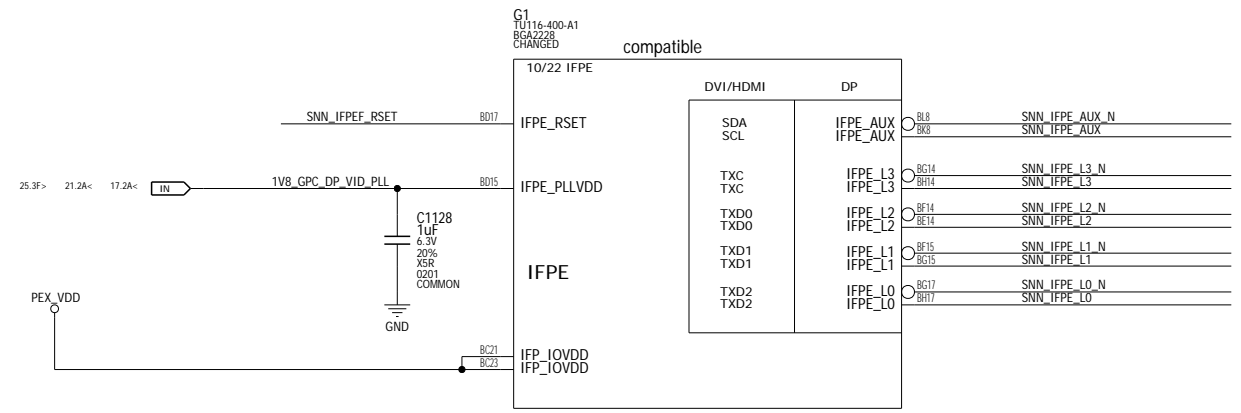


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ASSEMBLY PAGE DETAIL	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL IO: IFPB DP
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IFPF NC

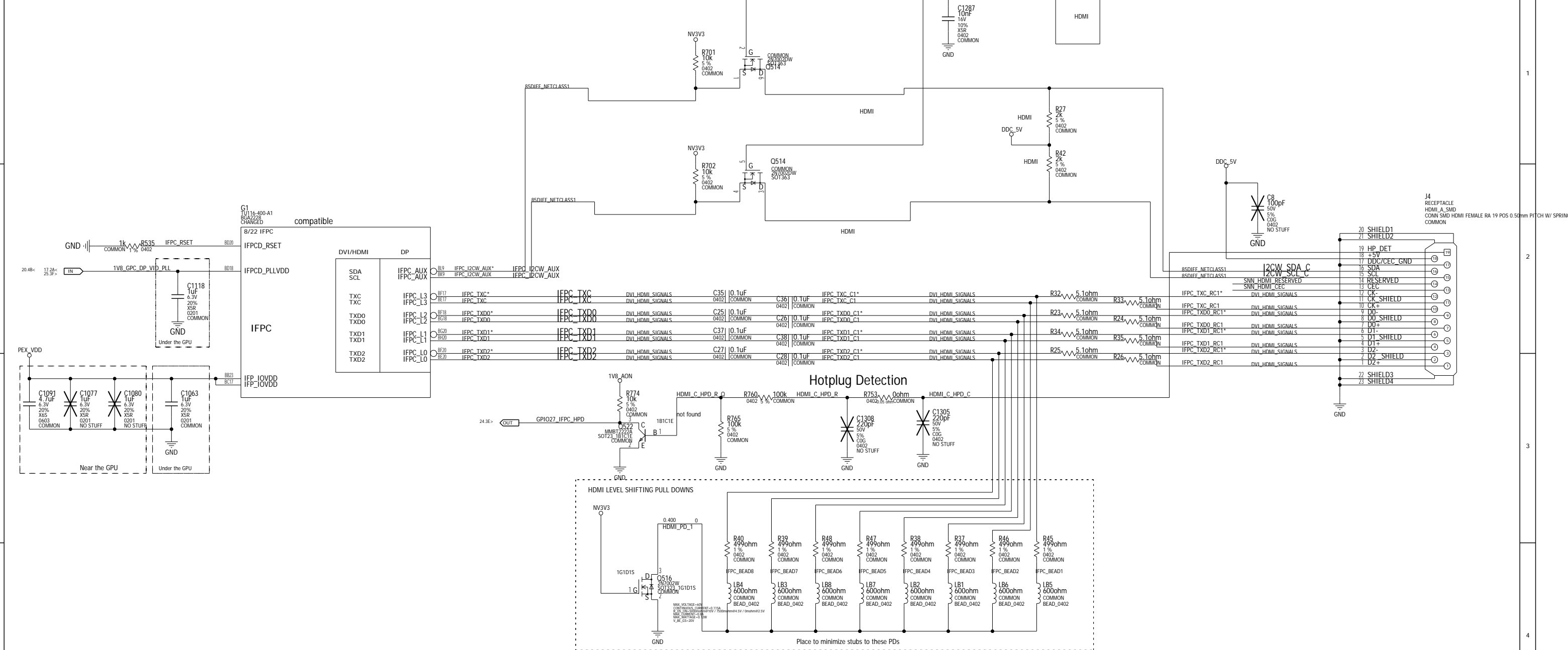


IFPE NC

ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

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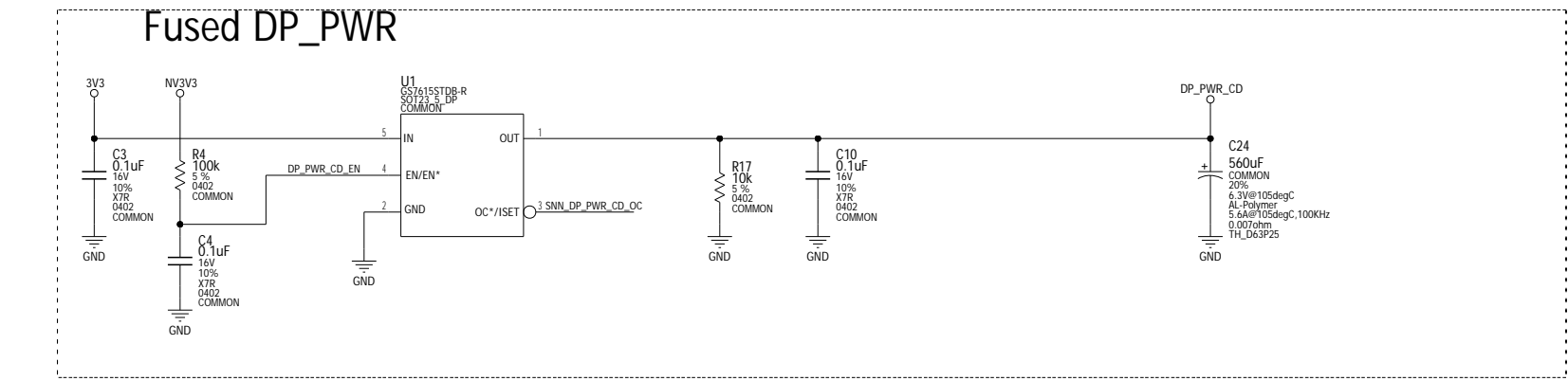
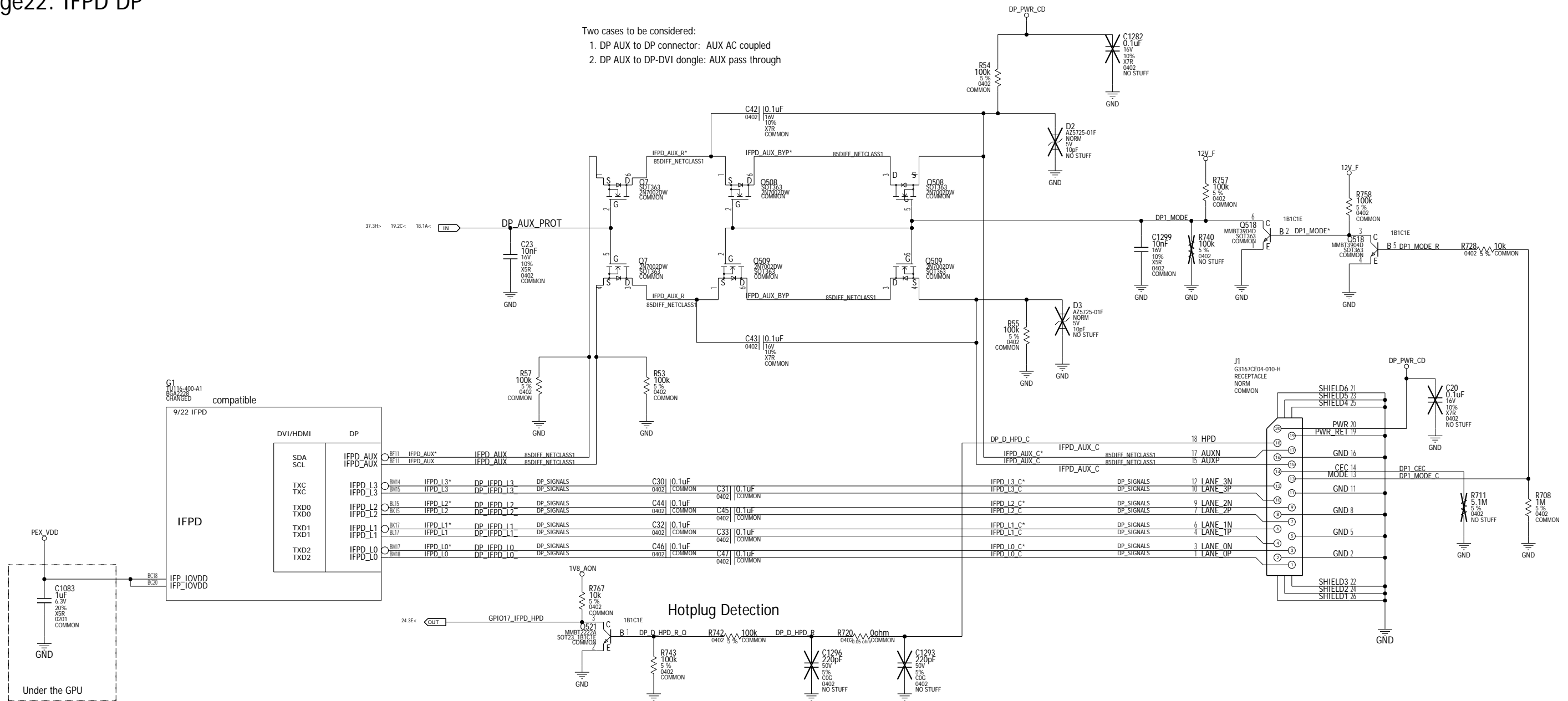
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IO: IFPC HDMI

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PAGE	21 OF 42
DATE	27-NOV-2018

- Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

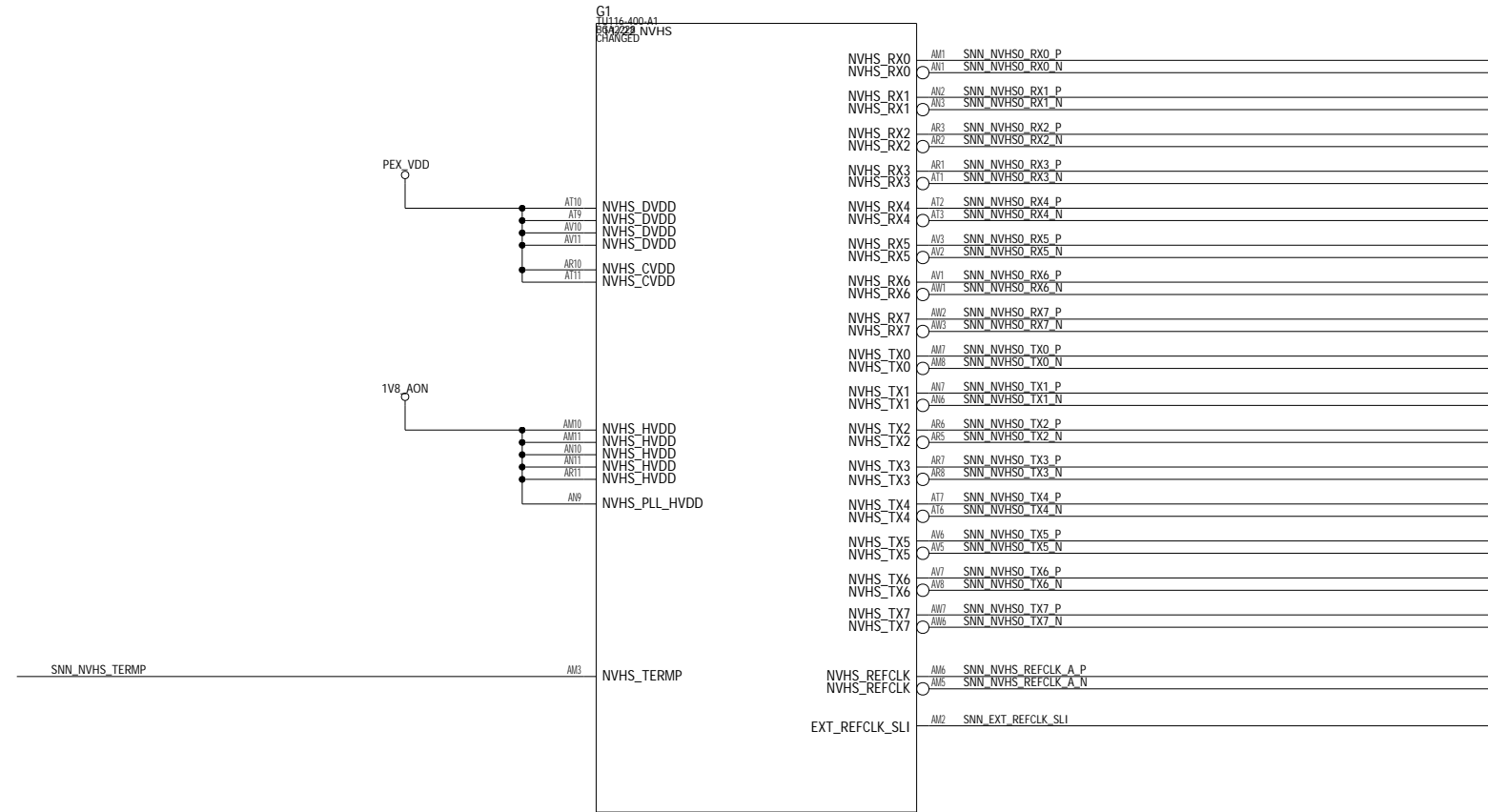


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NV_PN	600-1G161-0021-QS1		
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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL IO: IFPD DP

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Page23: NVHS Interface and Frame Lock



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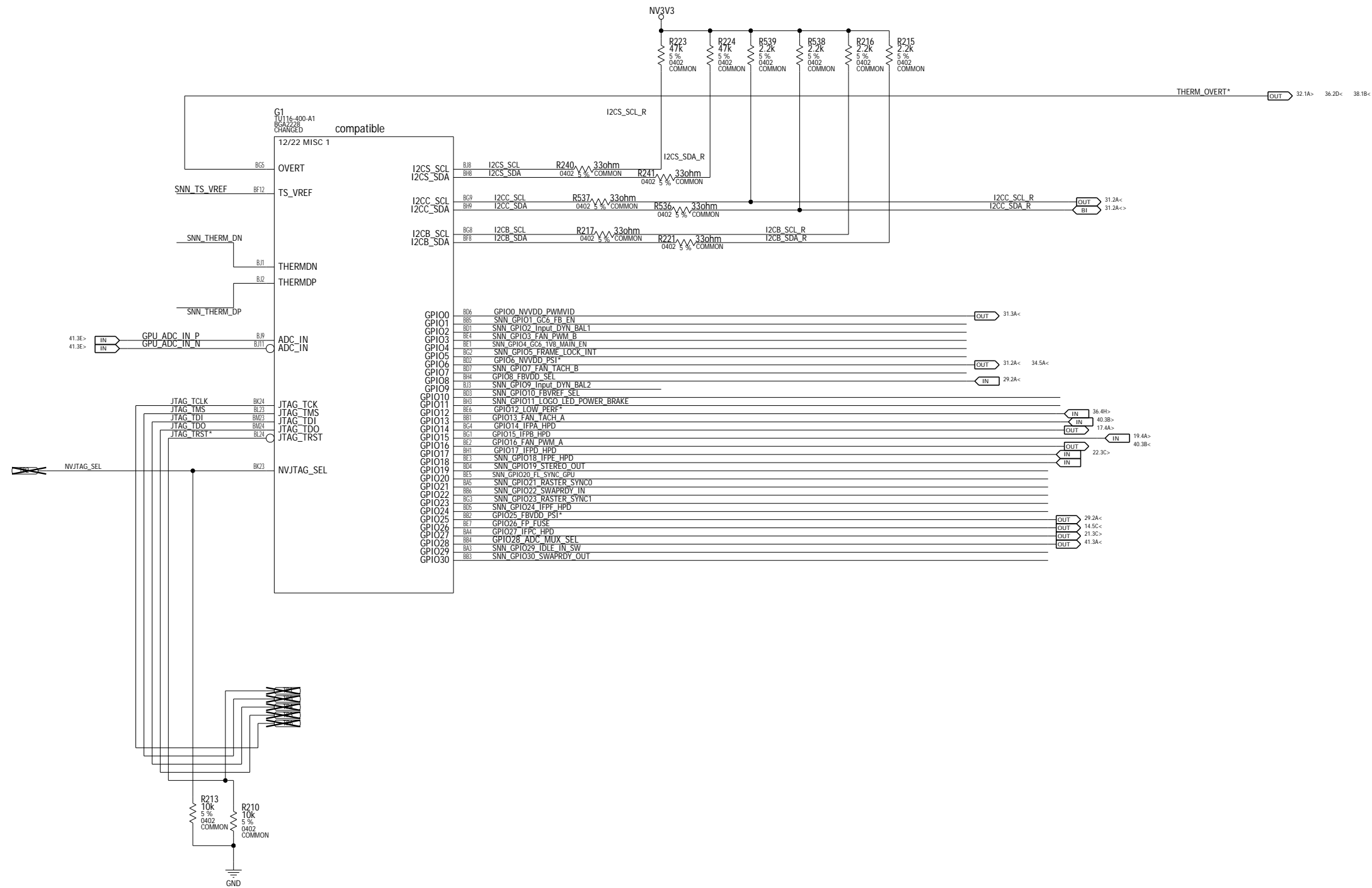


ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL IO: NVHS Interface and Frame Lock

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC1: Thermal, JTAG, GPIO, STEREO

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

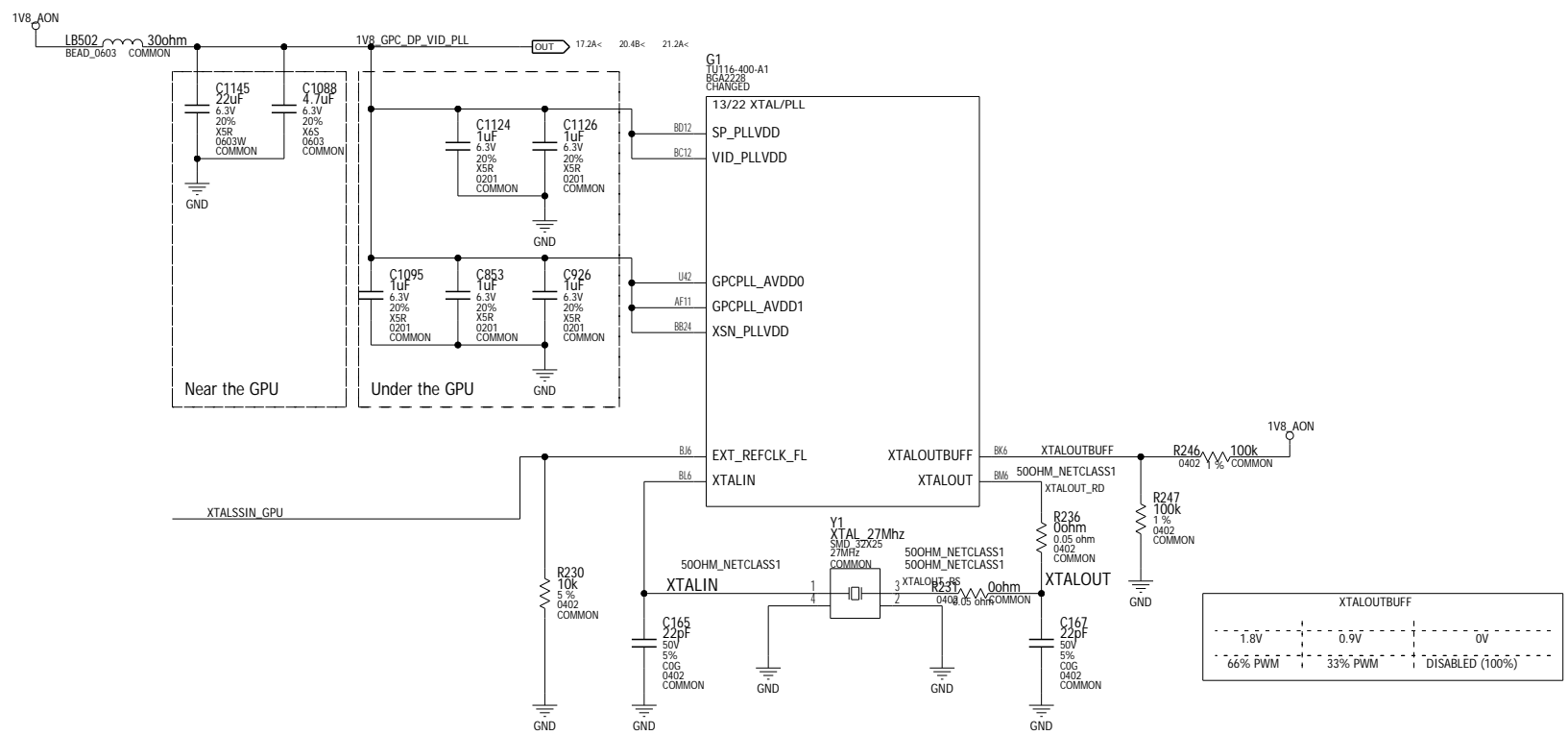
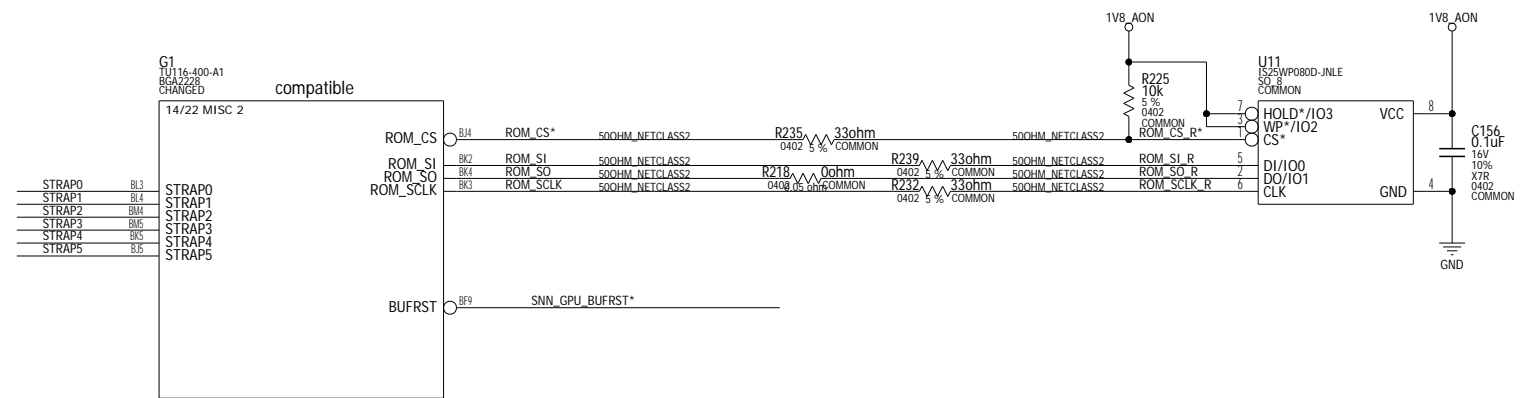
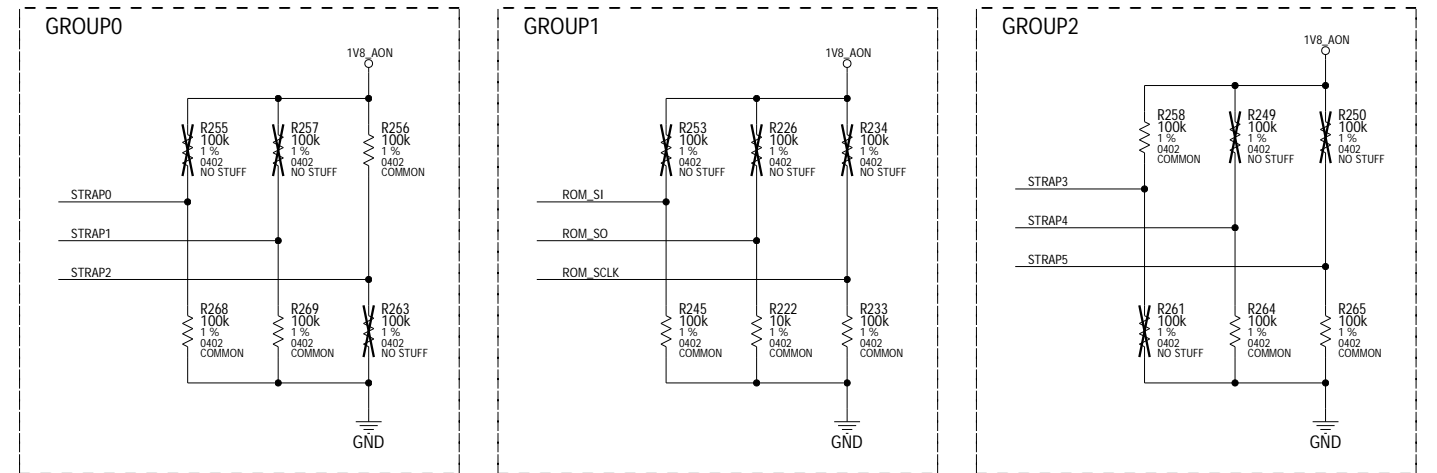
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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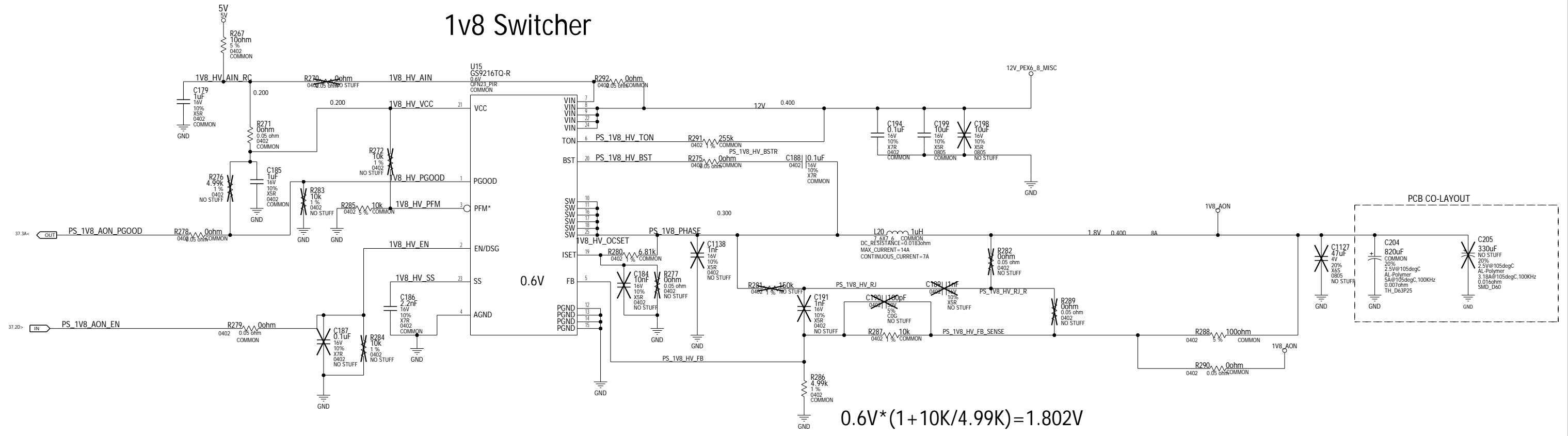
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PCB REV: PG161-A01
BOM REV: A

PAGE: 25 OF 42
DATE: 27-NOV-2018

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PAGE DETAIL: MISC2: ROM, XTAL, STRAPS

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1v8 Switcher

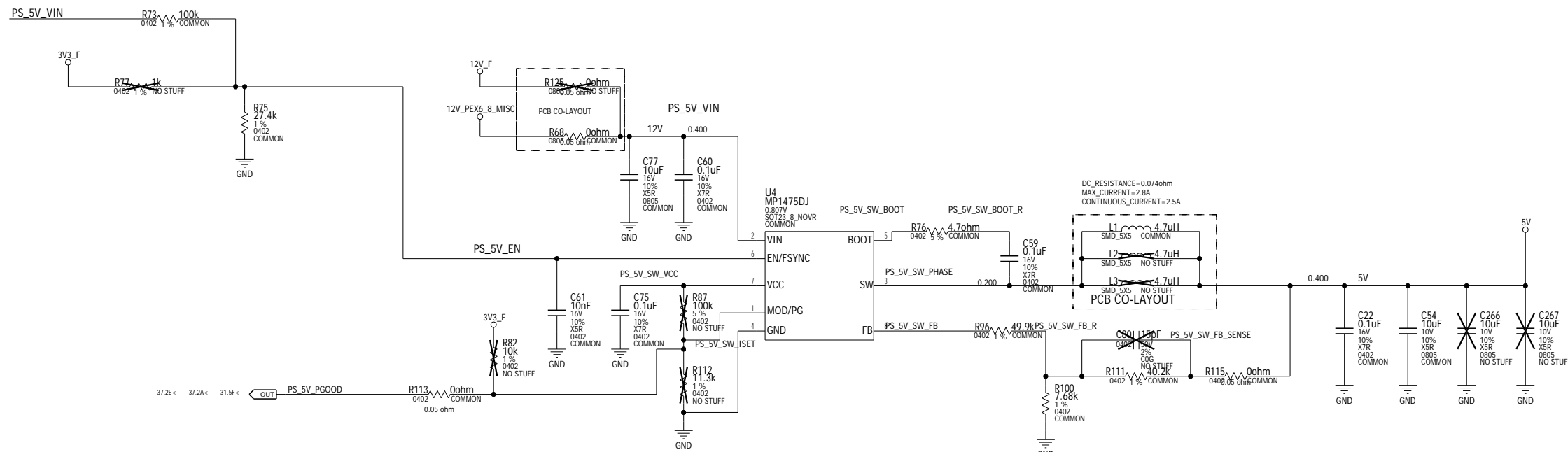


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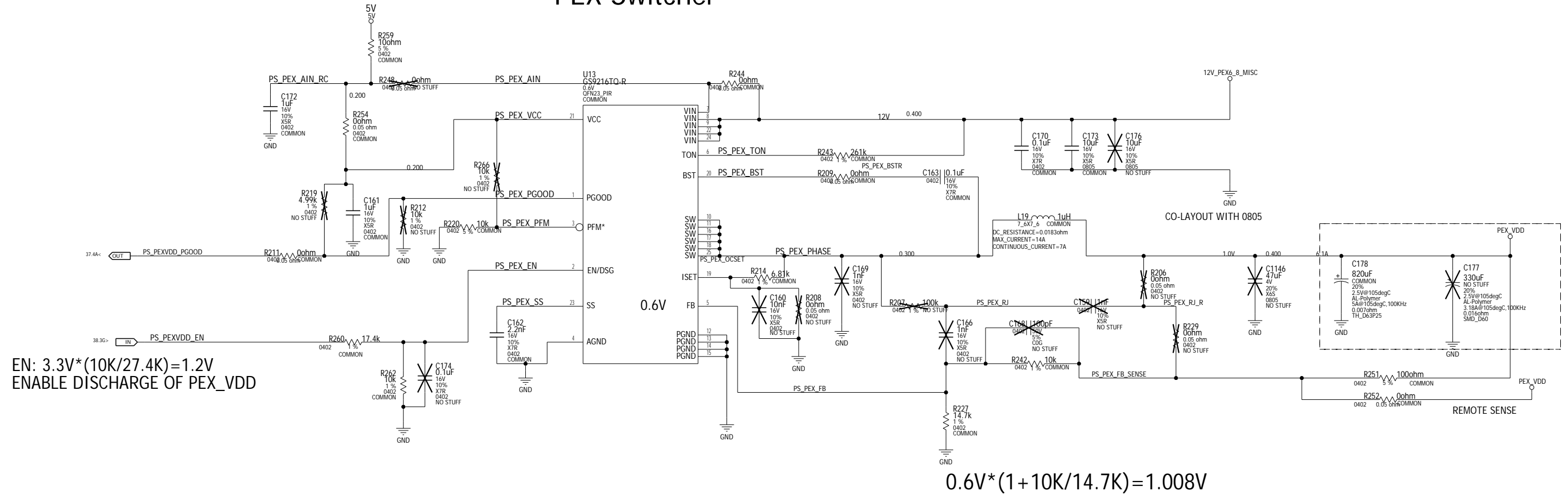
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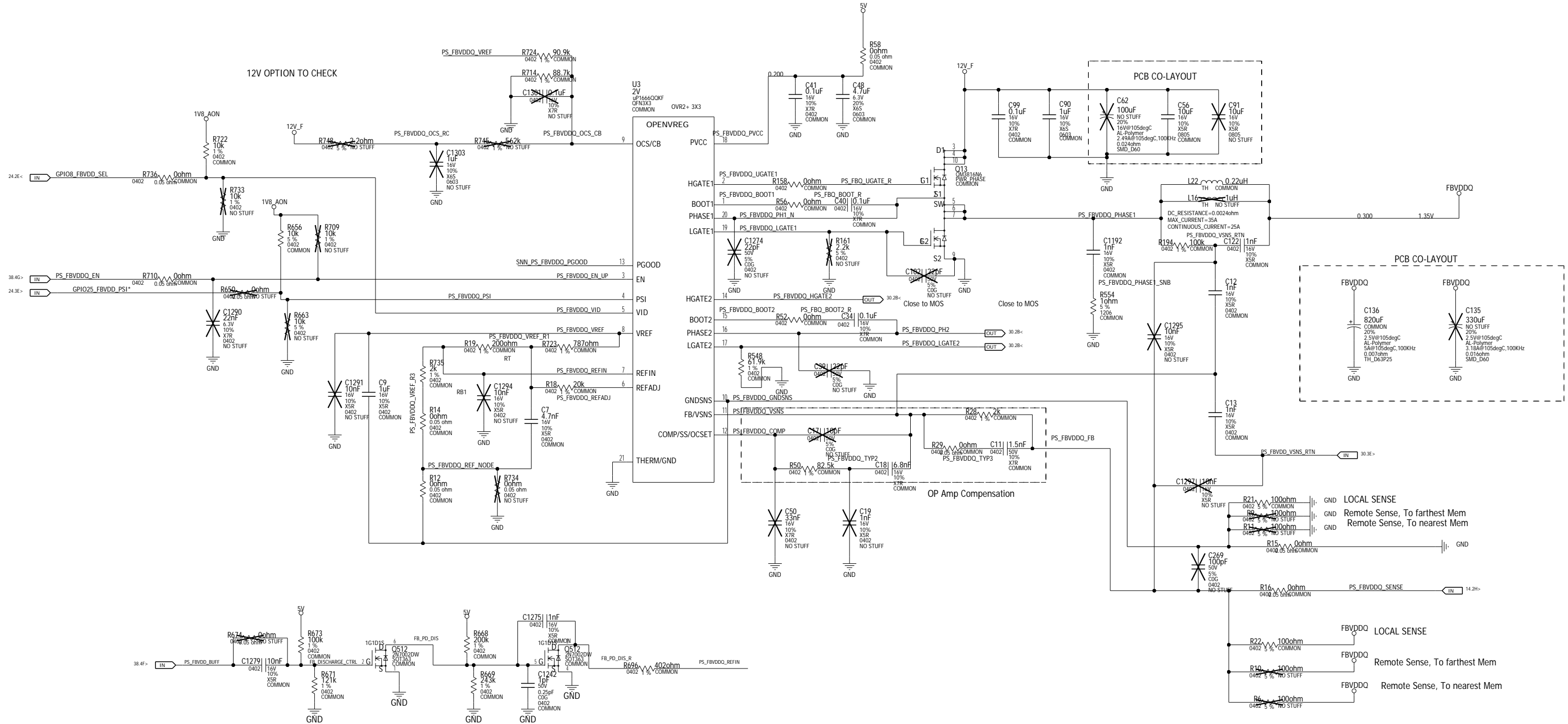
PEX Switcher



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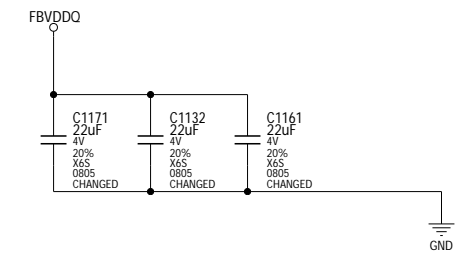
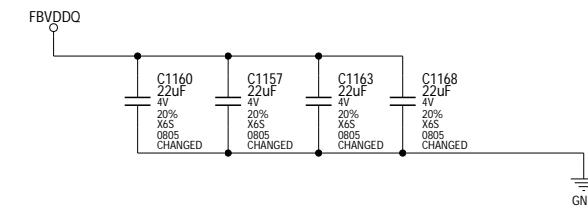
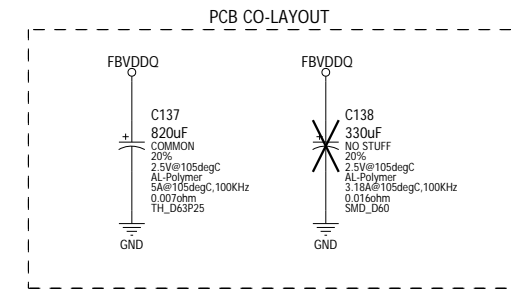
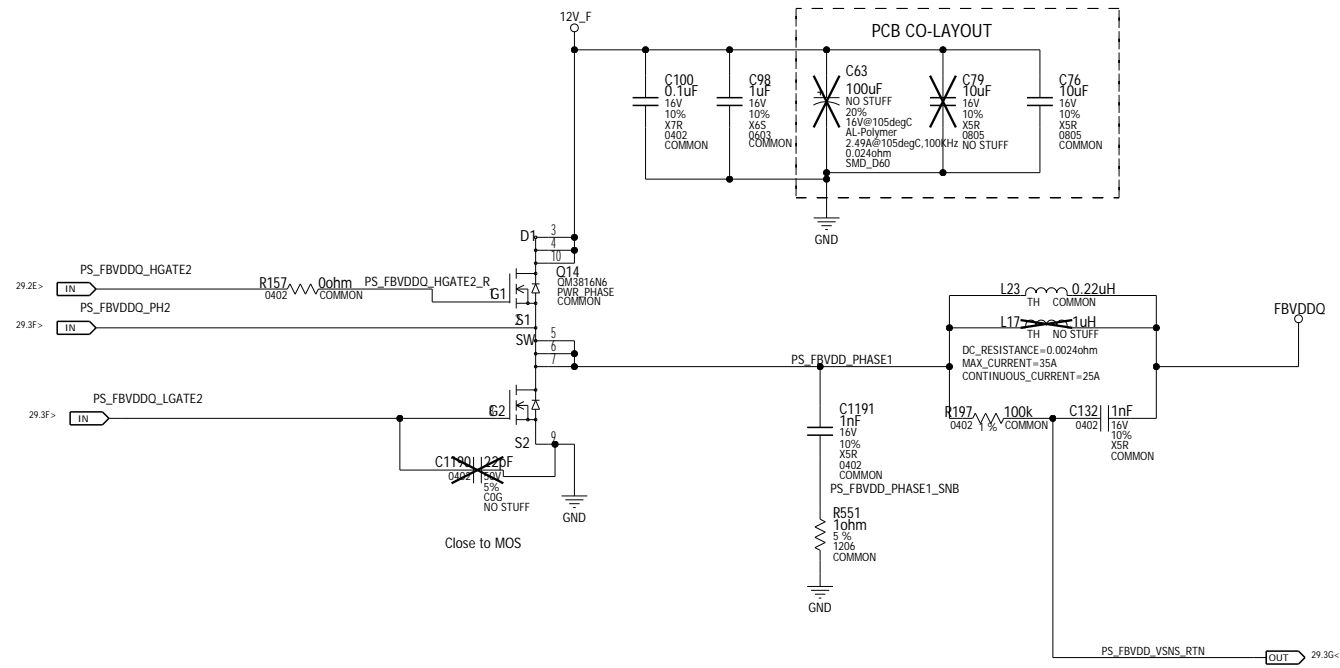
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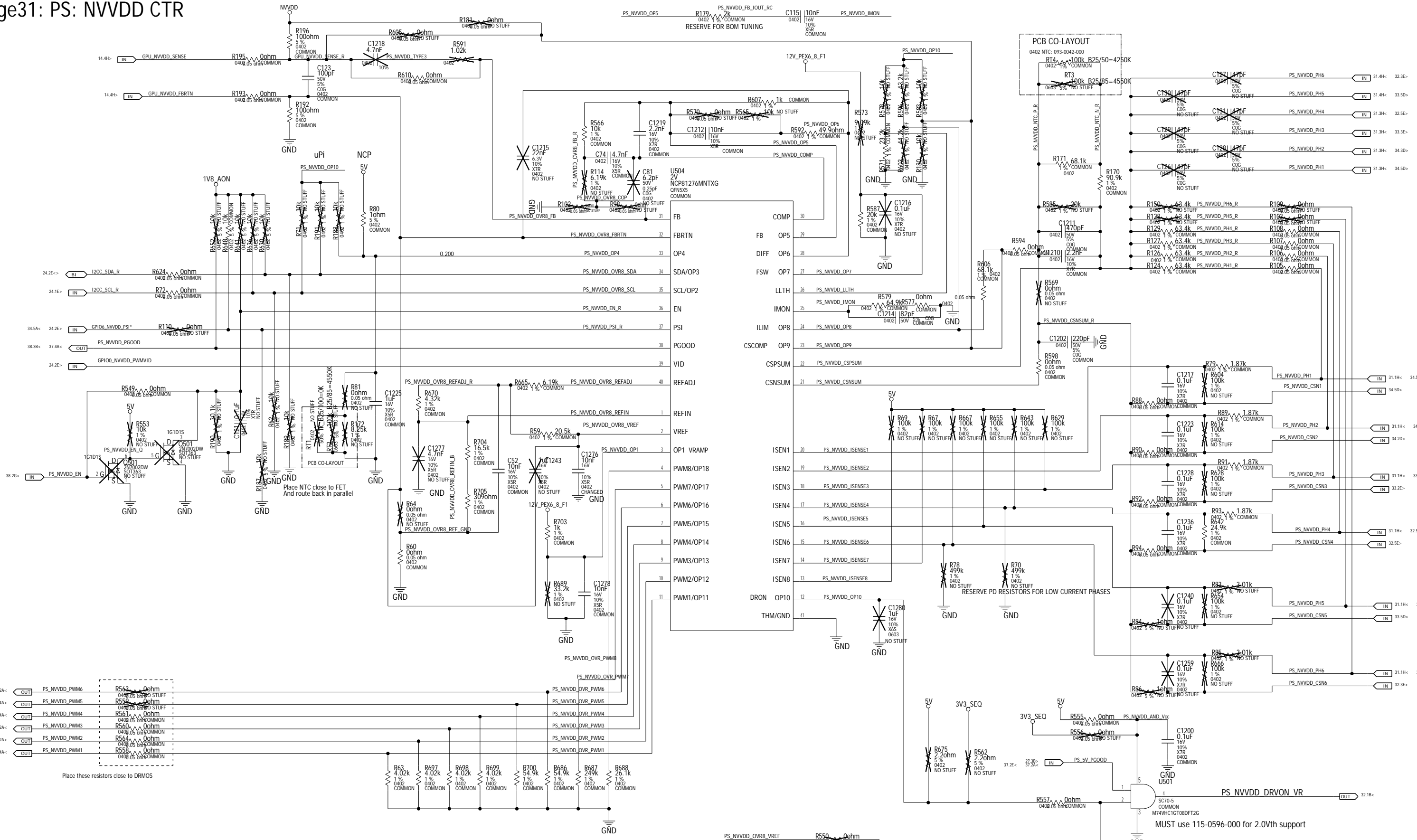


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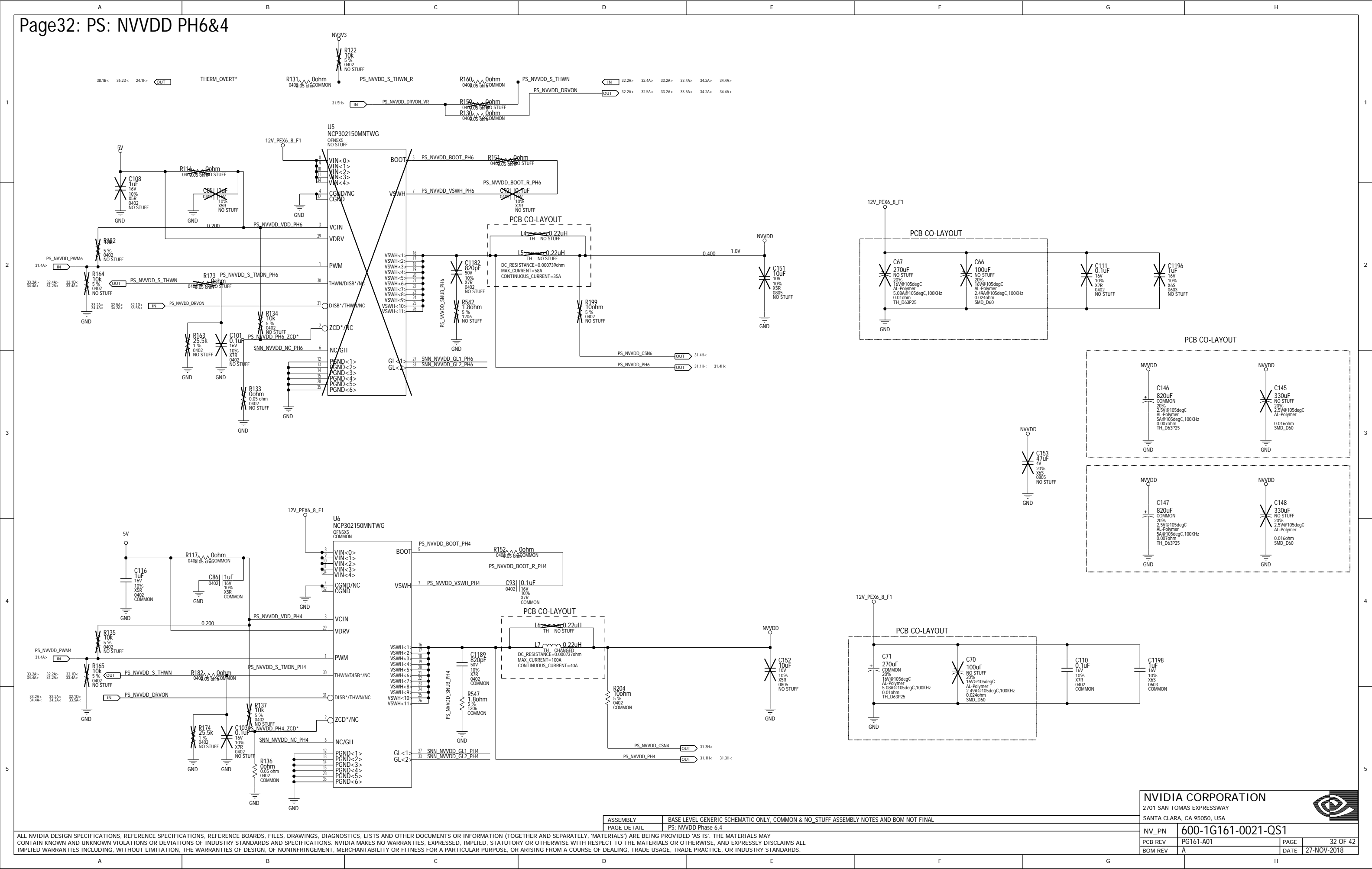


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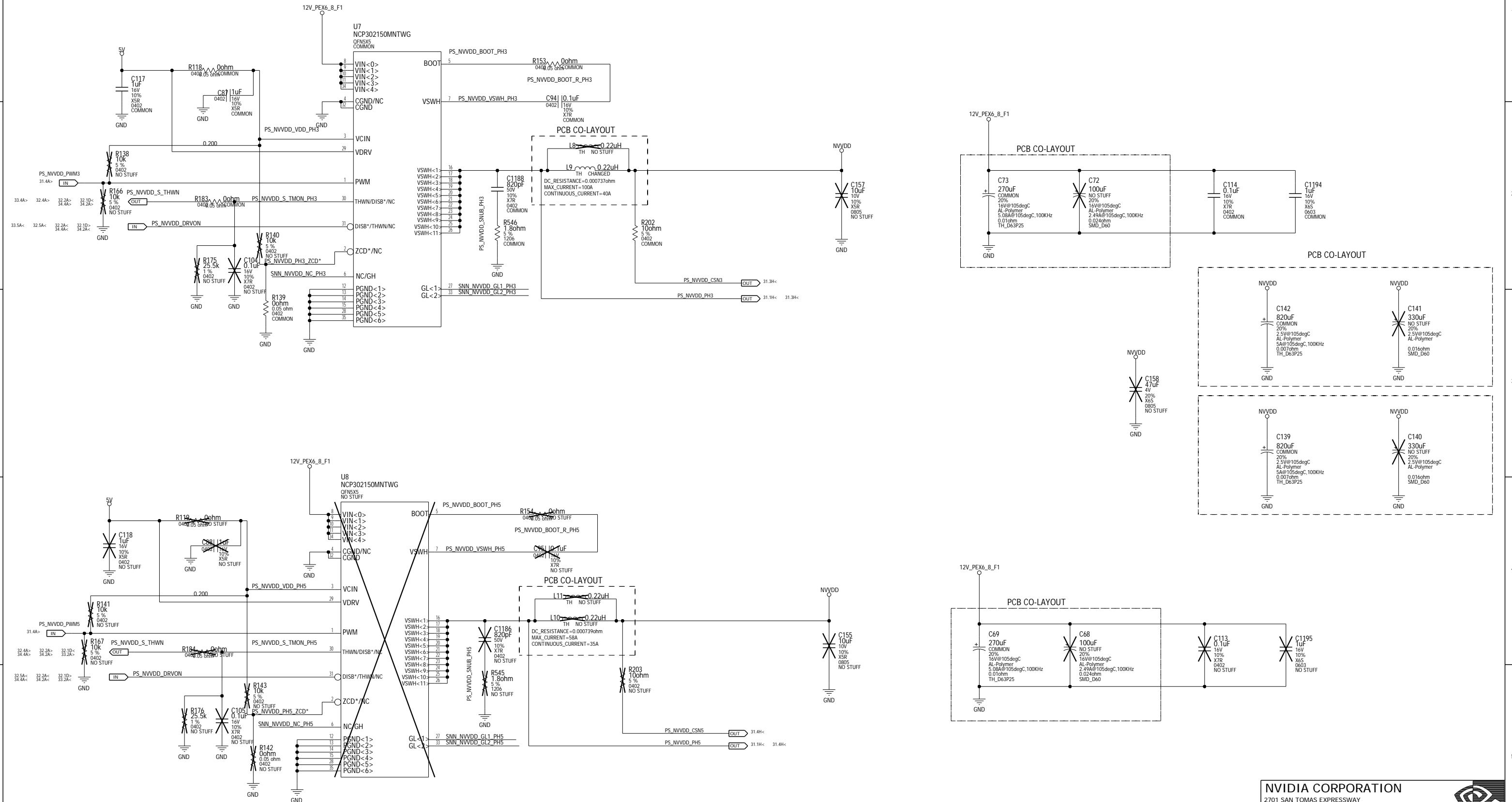
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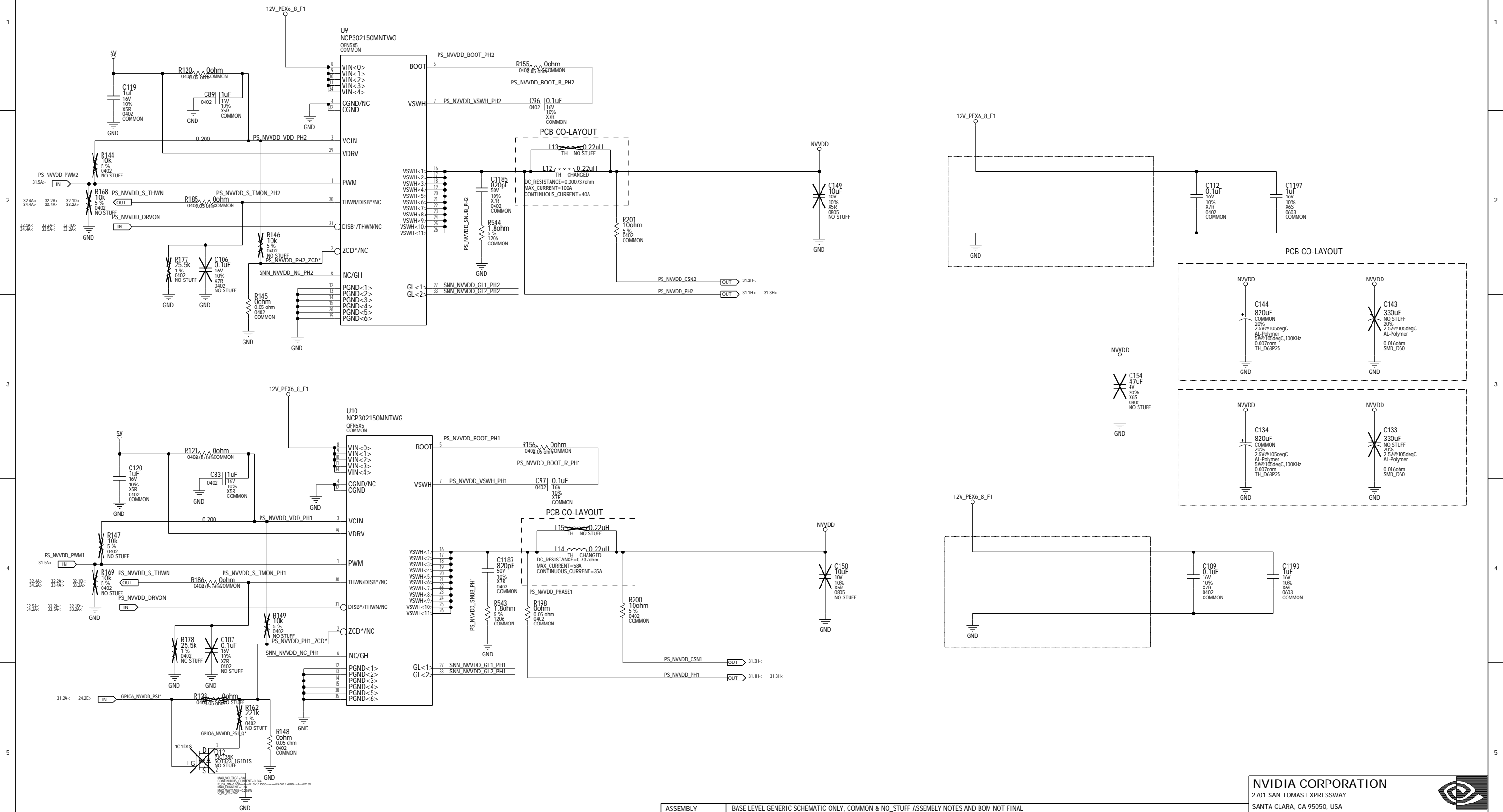
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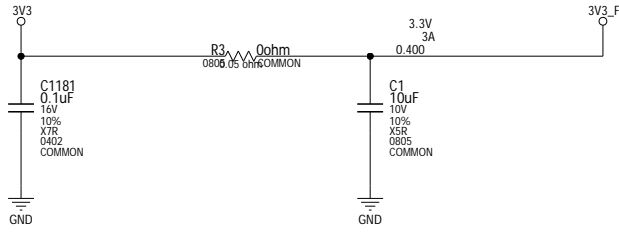
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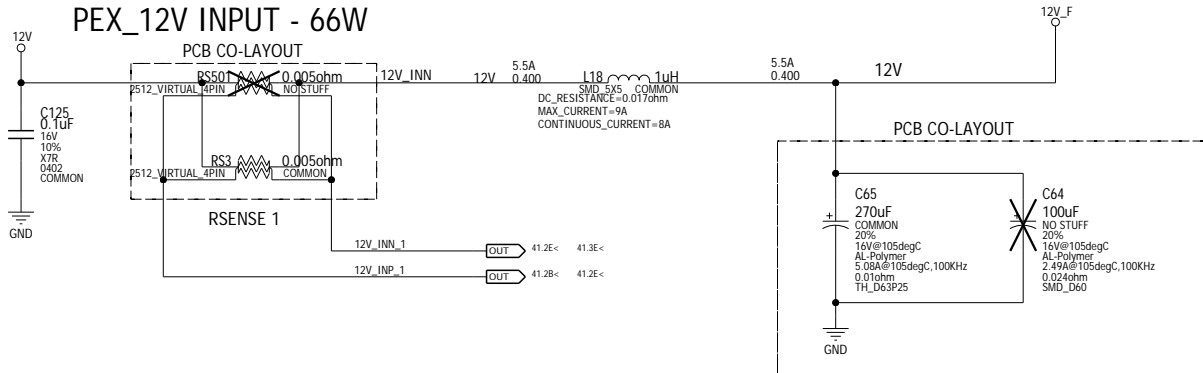
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PCB REV	PG161-A01	PAGE	34 OF 42
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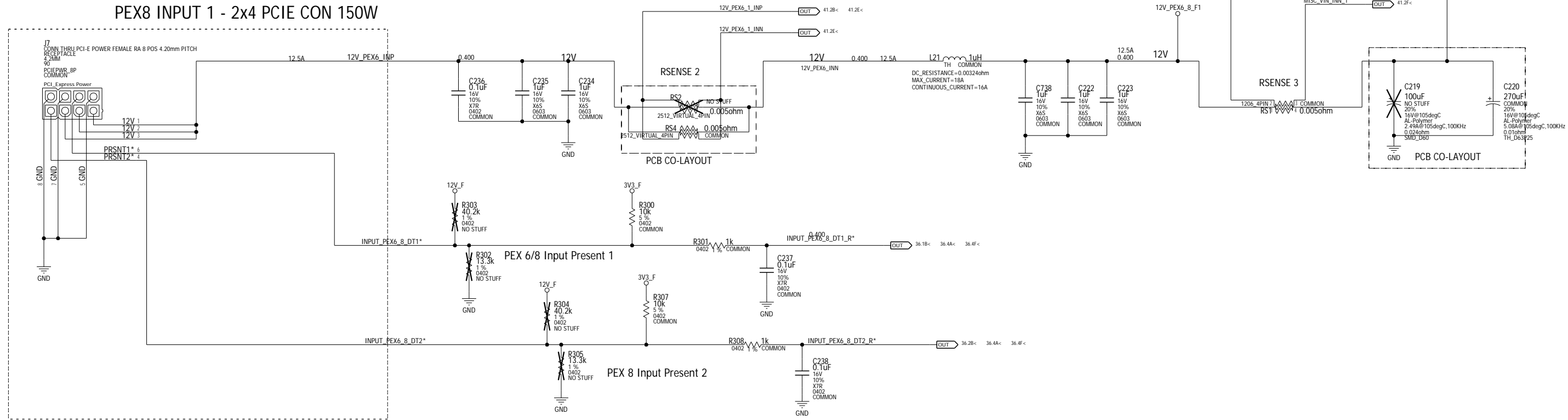
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



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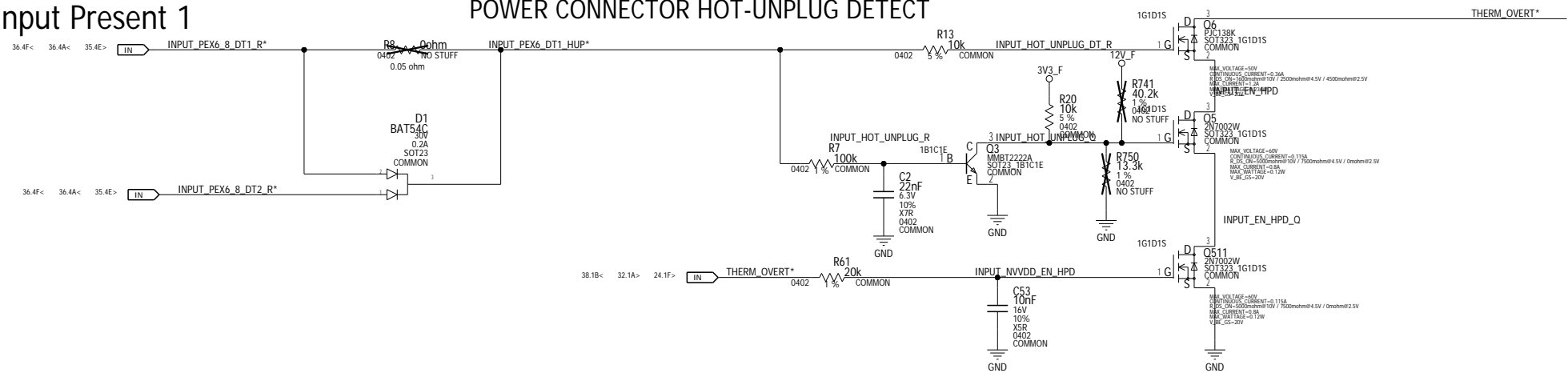
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PCB REV	PG161-A01	PAGE	35 OF 42
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Input, Filtering, and Monitoring

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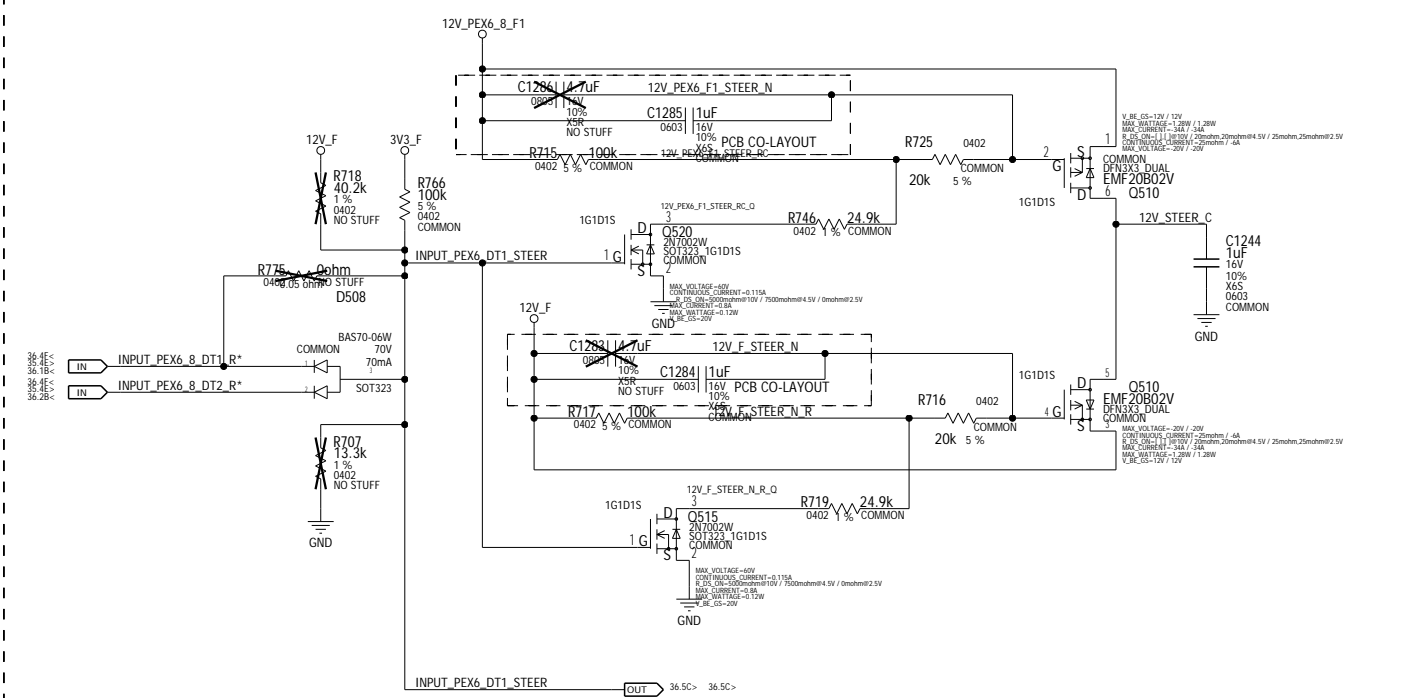
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

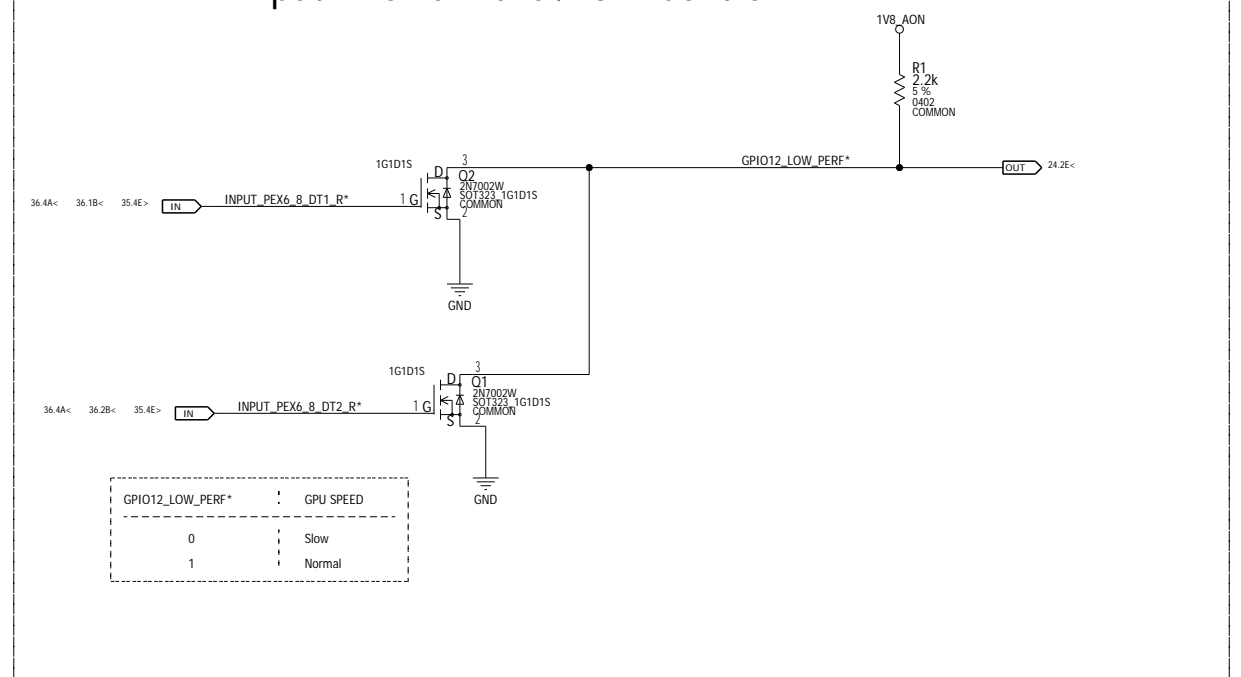


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

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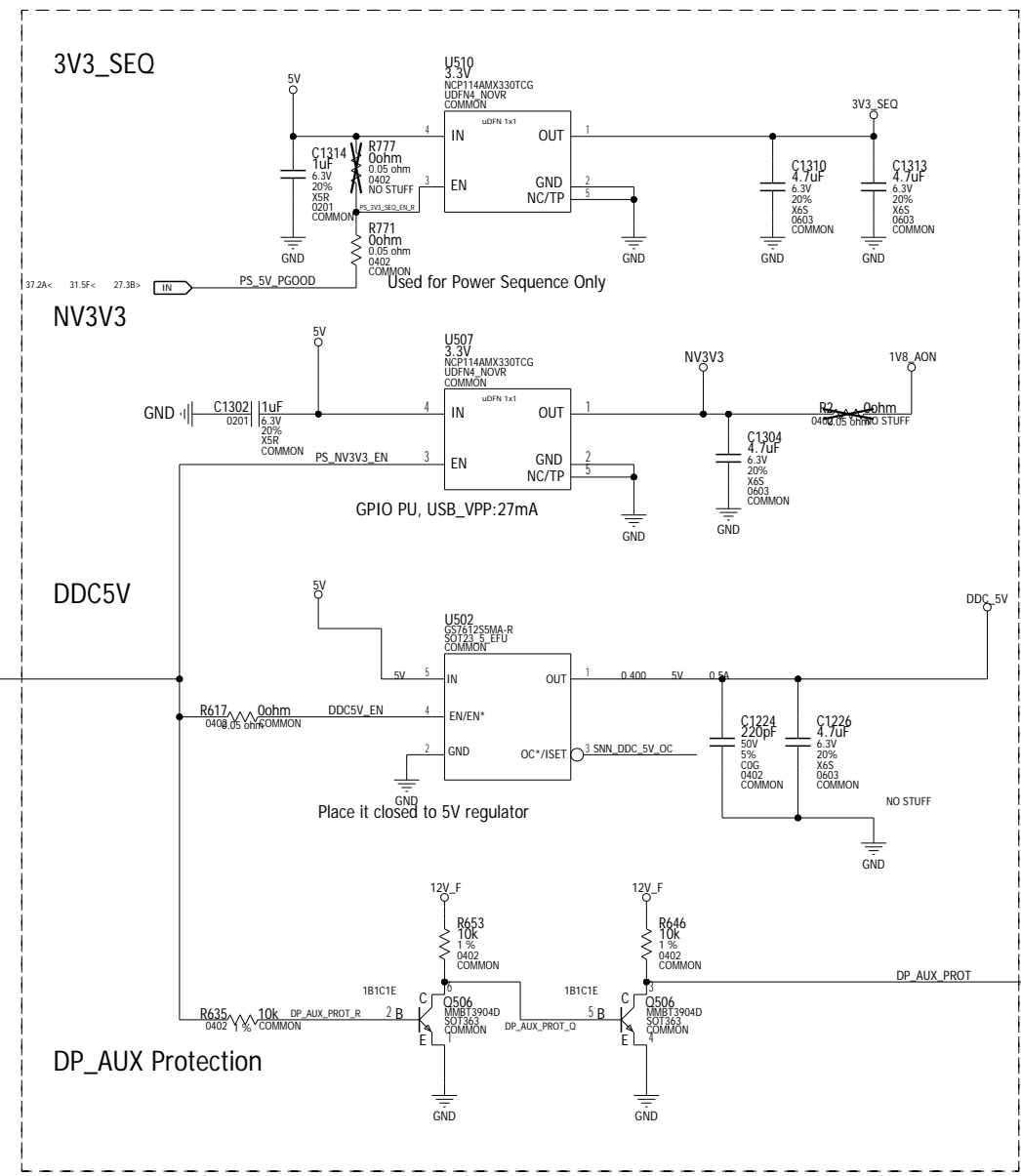
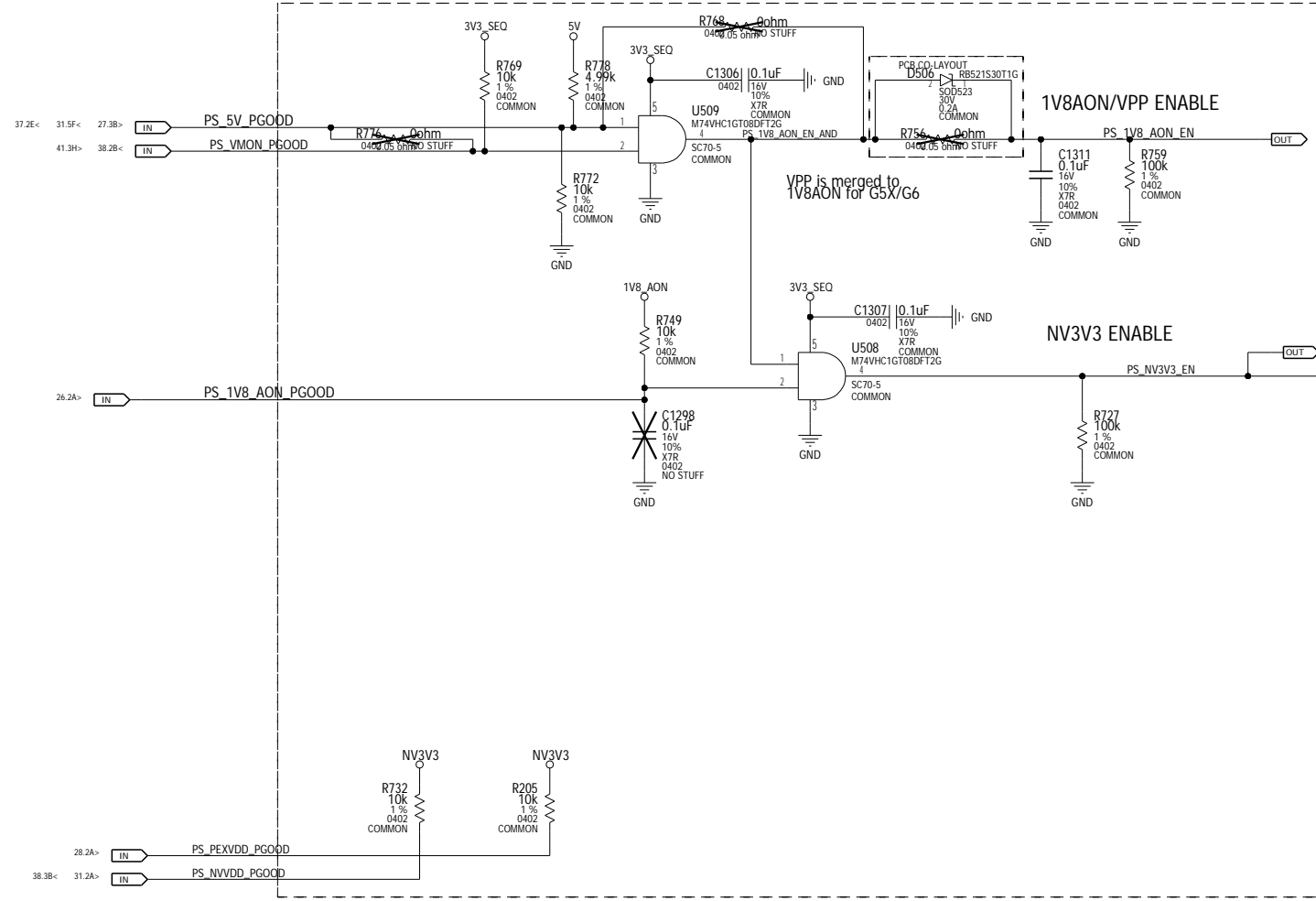
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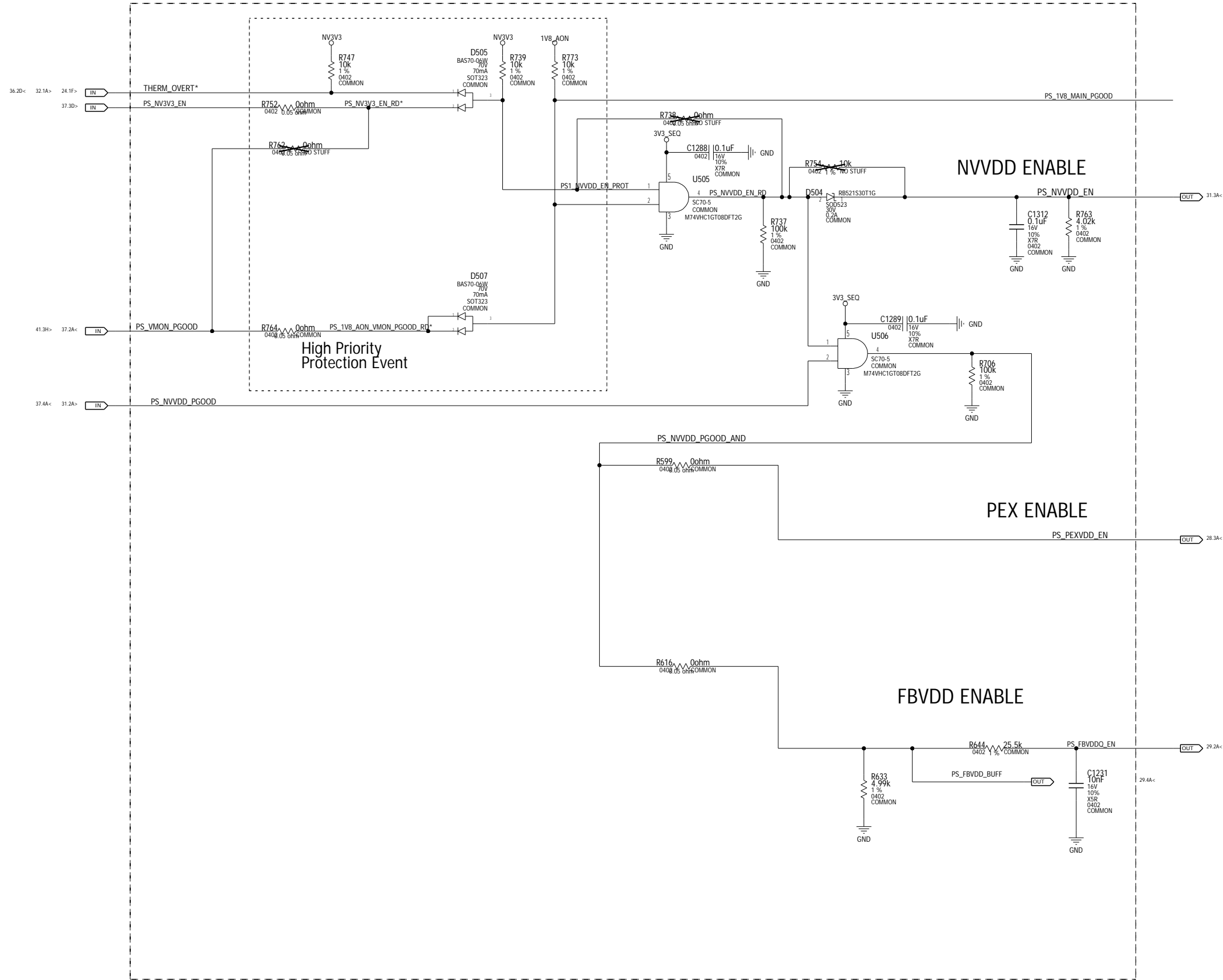
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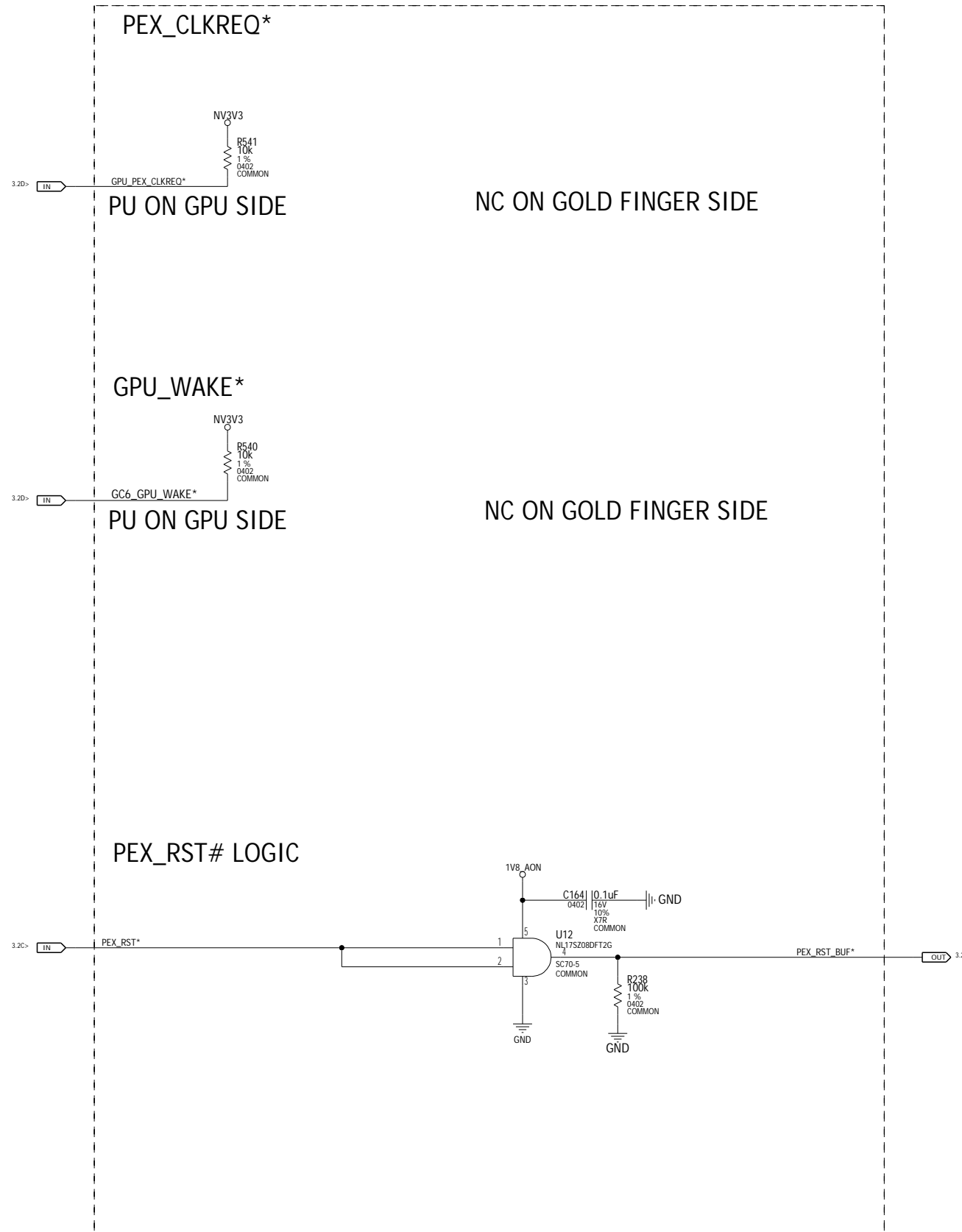


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NV_PN	600-1G161-0021-QS1	PAGE	38 OF 42
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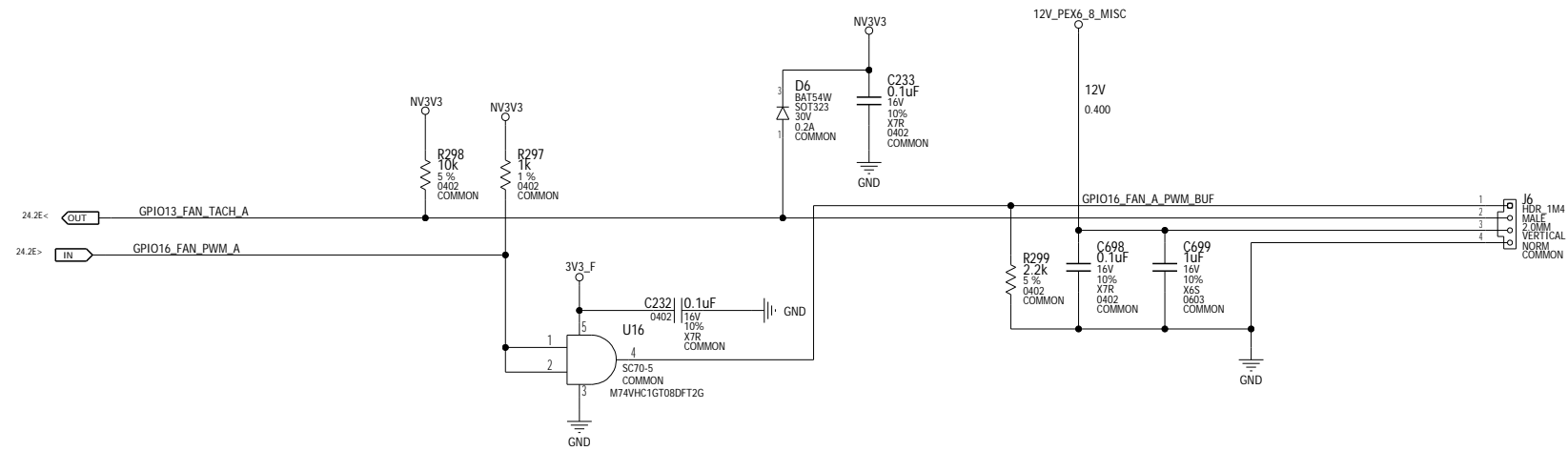




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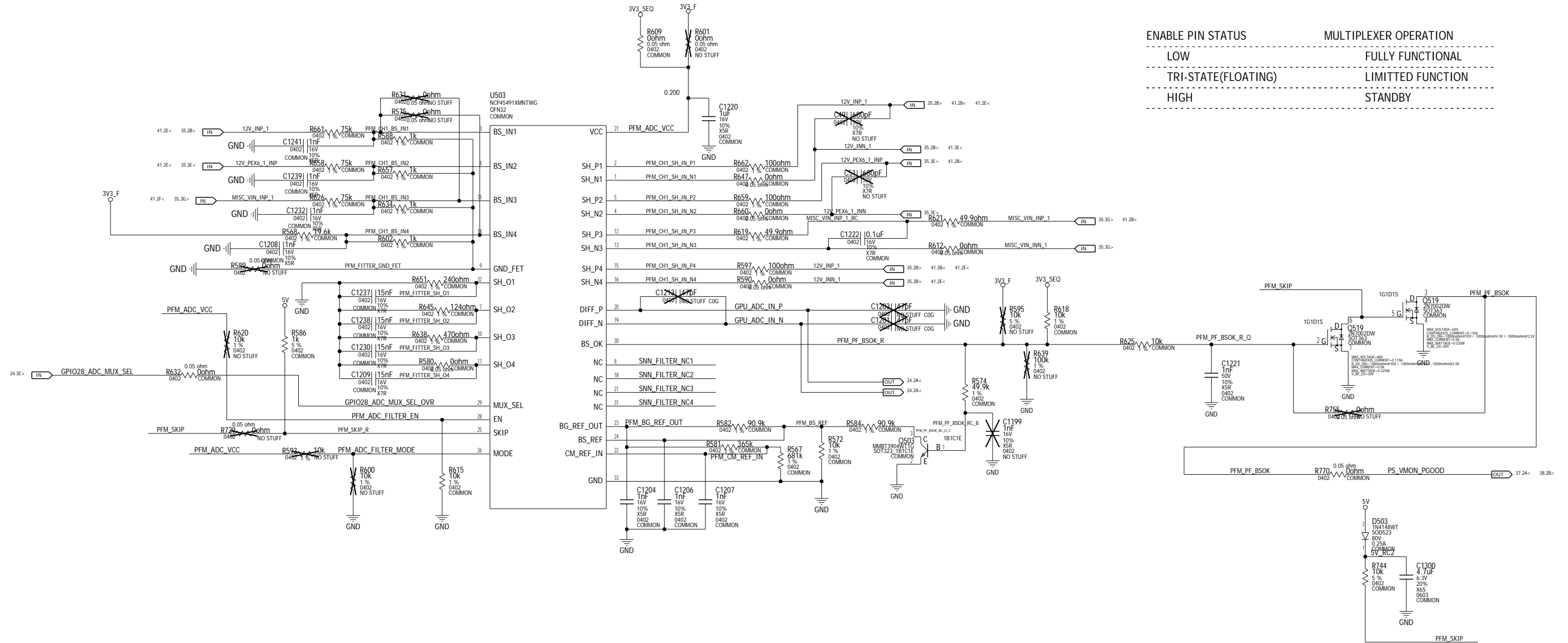


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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

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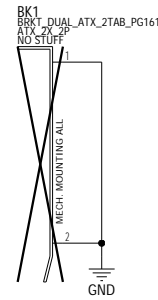
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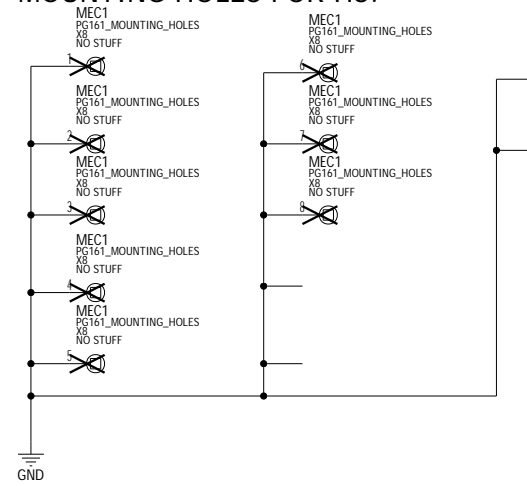
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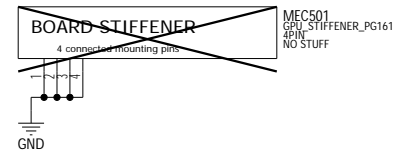
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