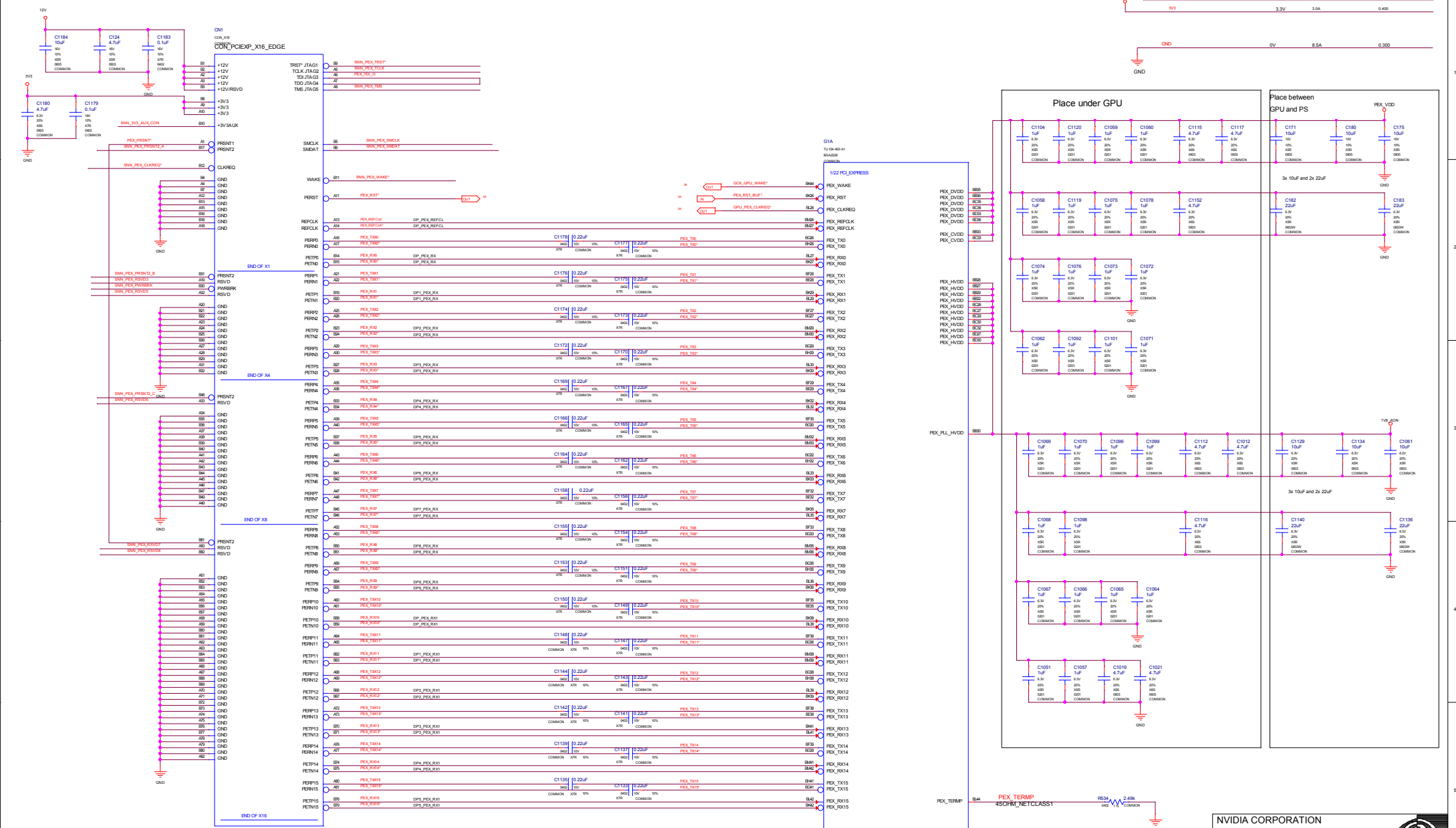


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	Block Diagram

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PCI Express

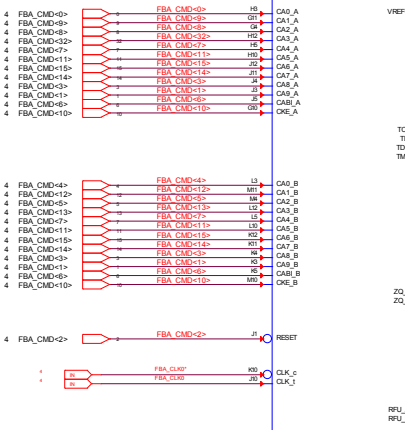
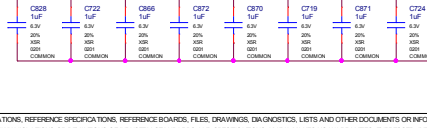
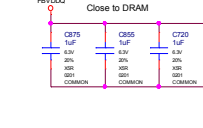
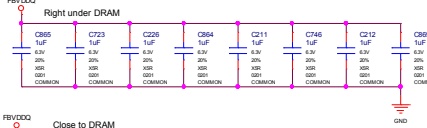
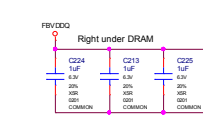
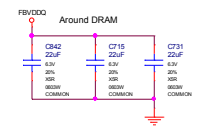
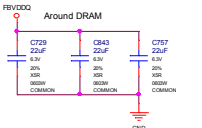
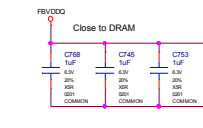
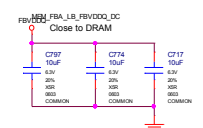
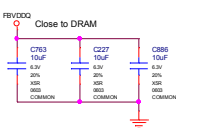
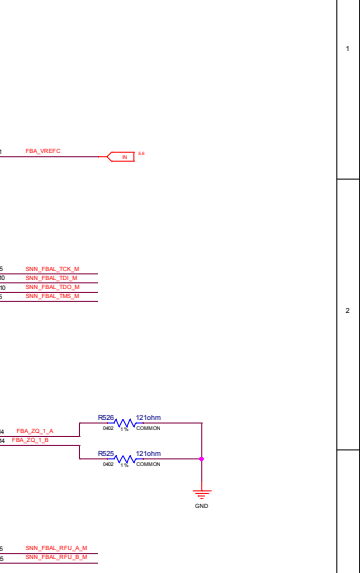
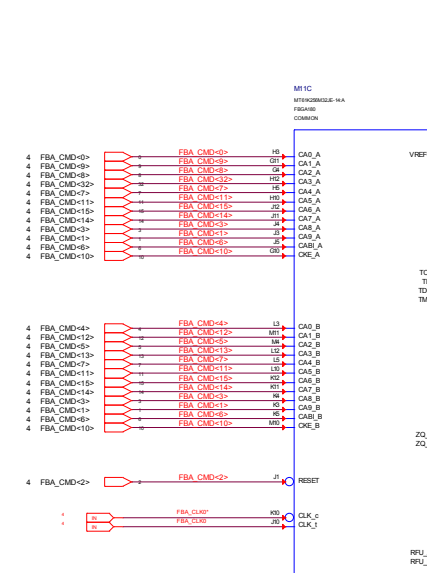
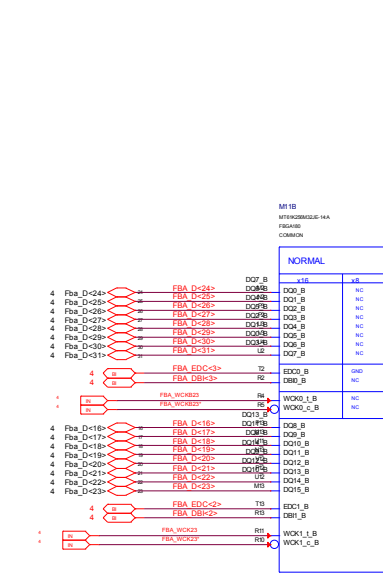
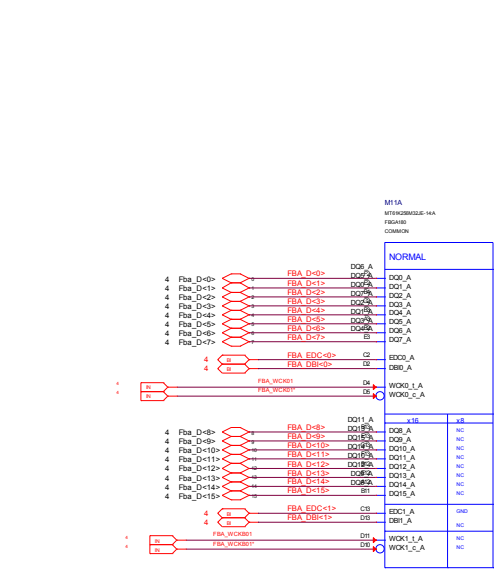
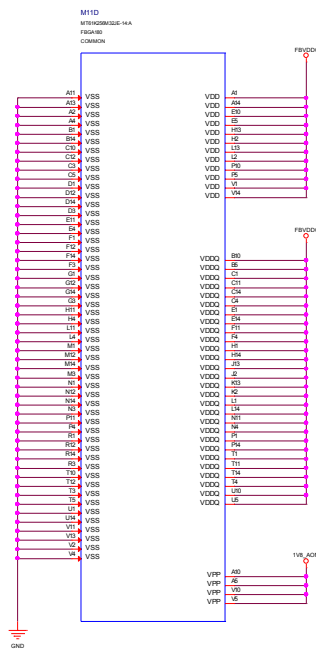
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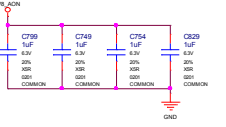
**600-1G161-BASE-100**

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VREFC IS NOT USED IN x16 CONFIGURATION  
1K OHM PULL-DOWNS IN PLACE OF THE 1.33K FOR R106



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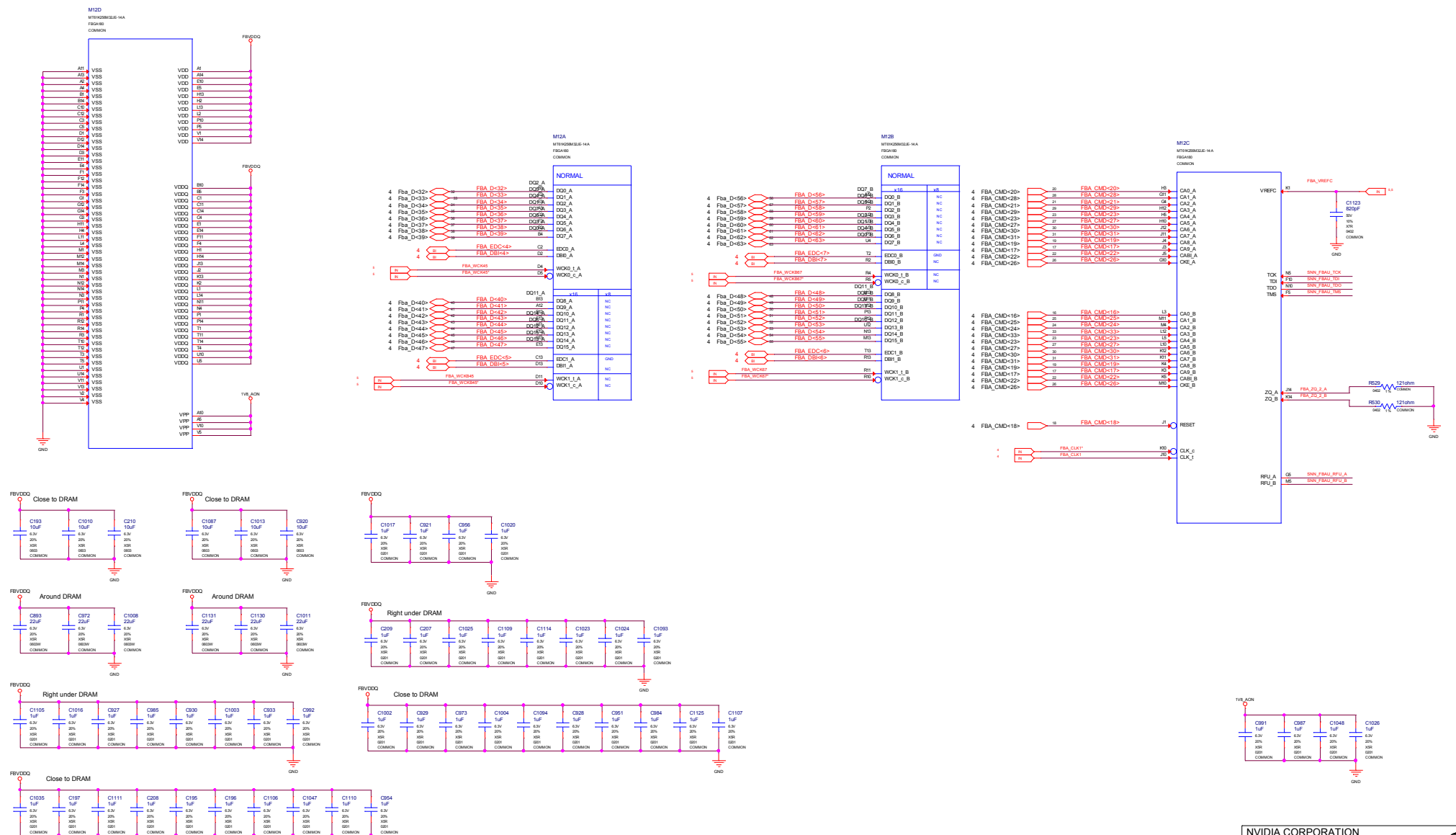
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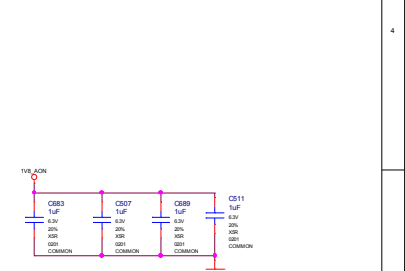
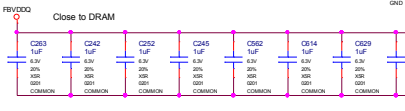
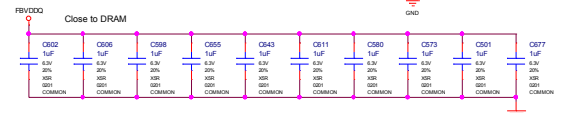
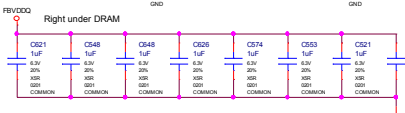
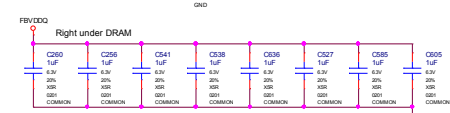
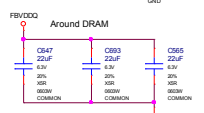
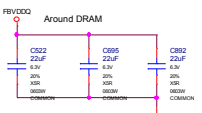
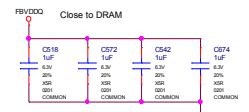
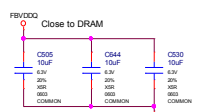
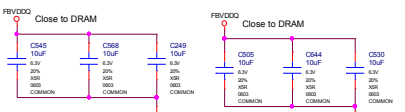
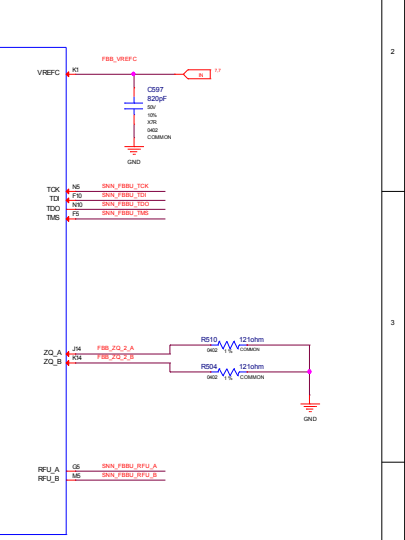
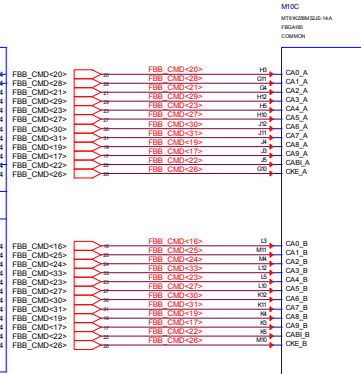
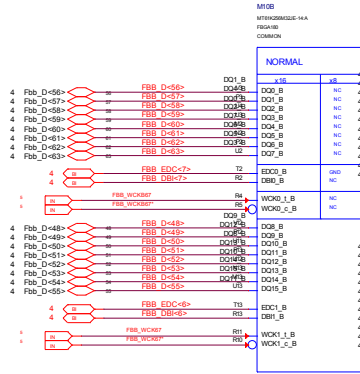
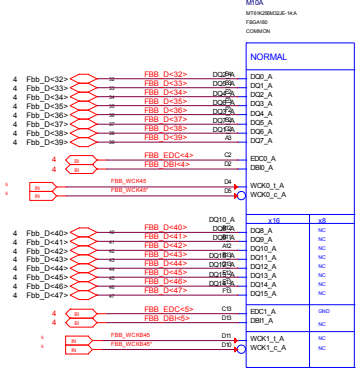
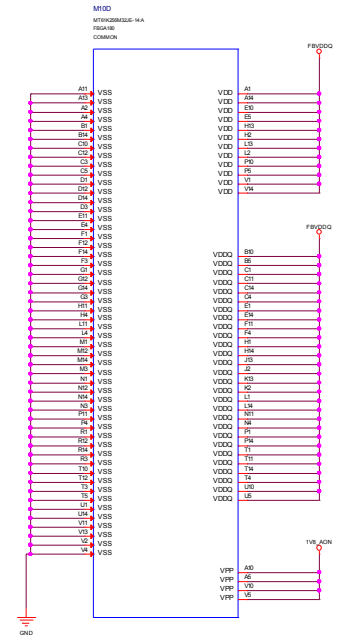
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Part Number: **600-1G161-BASE-100**

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MEMORY: FB63..32

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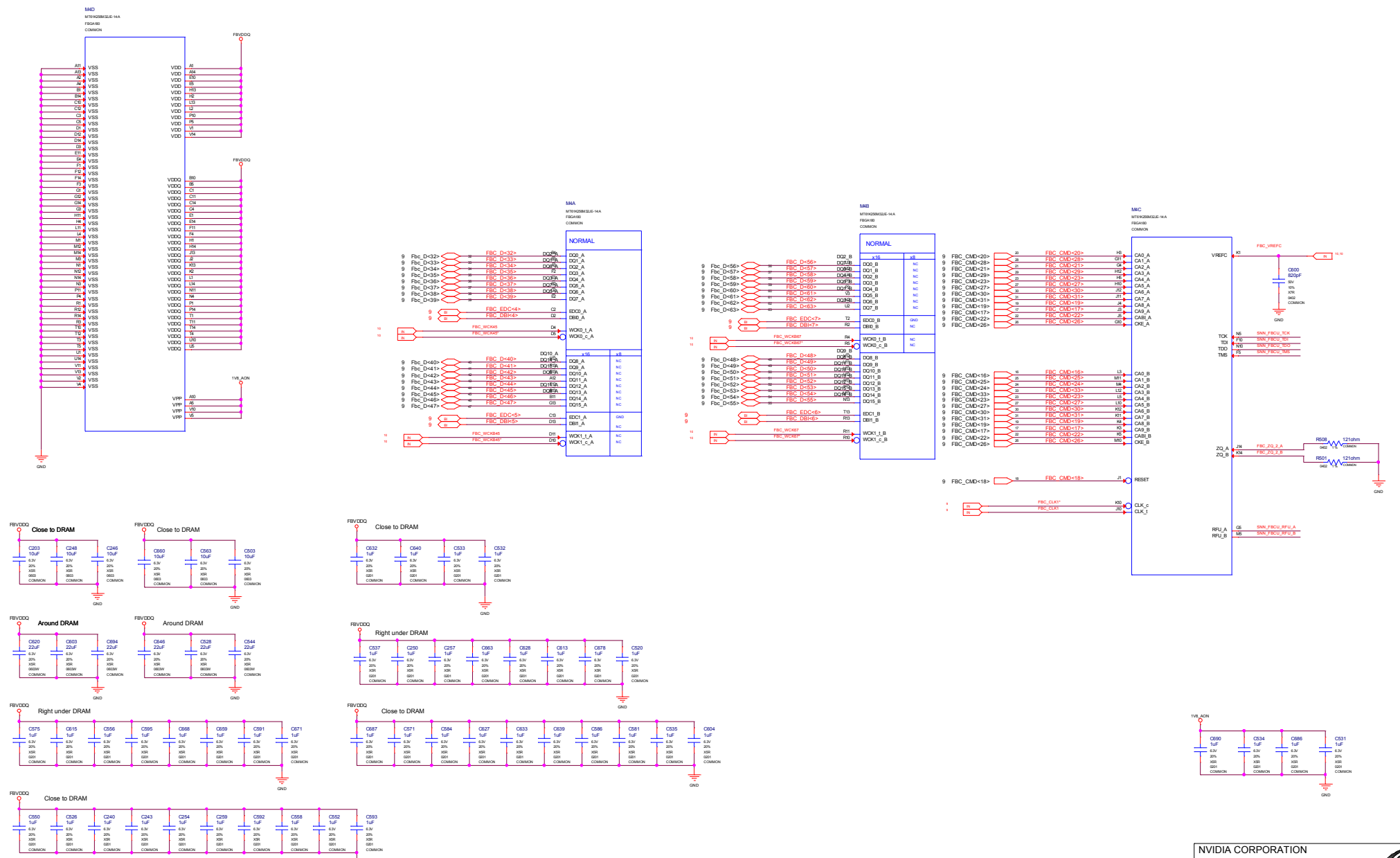
INV\_PN: **600-1G161-BASE-100**

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MEMORY: FRQ63.32

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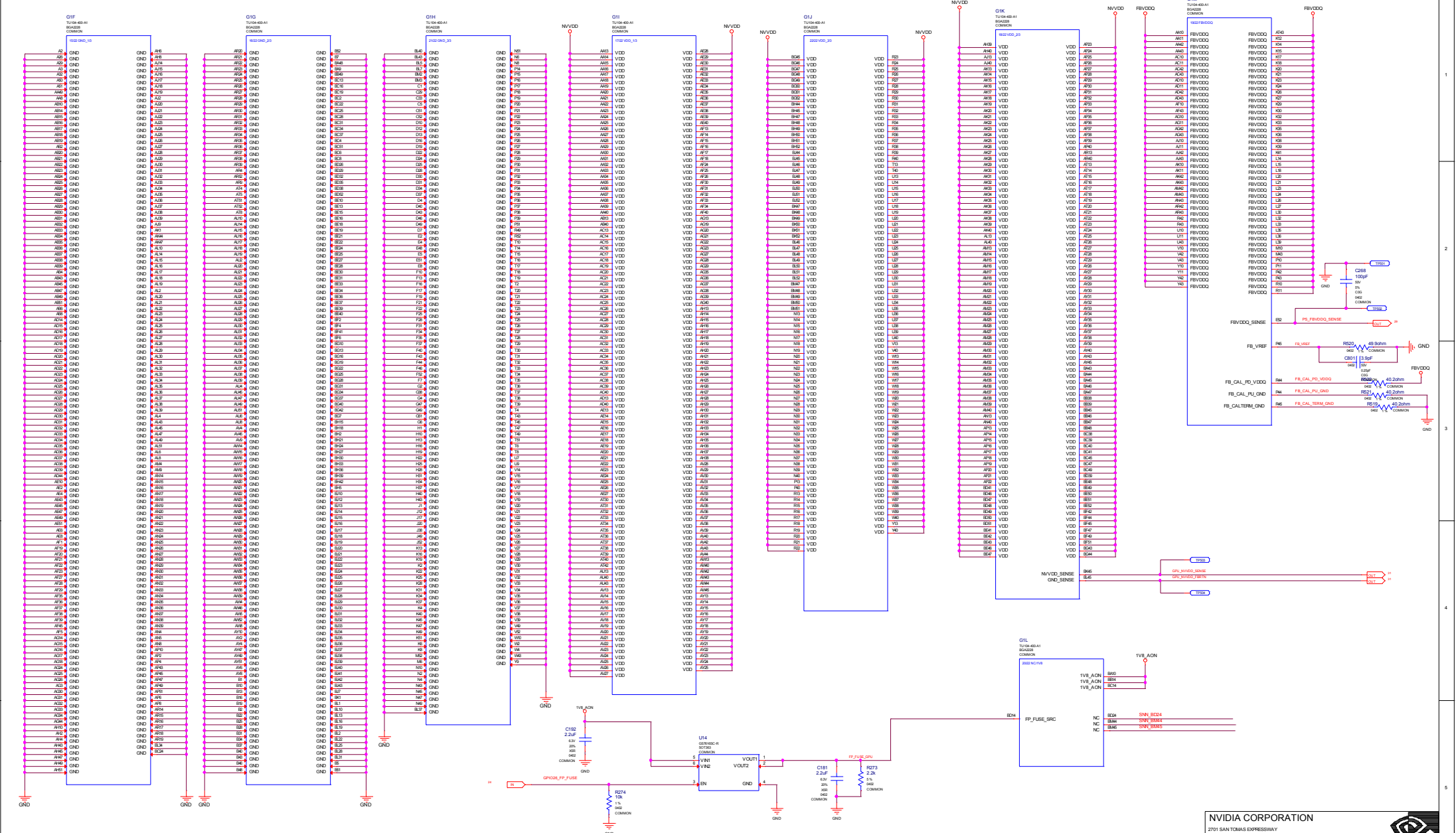
INV\_PN **600-1G161-BASE-100**

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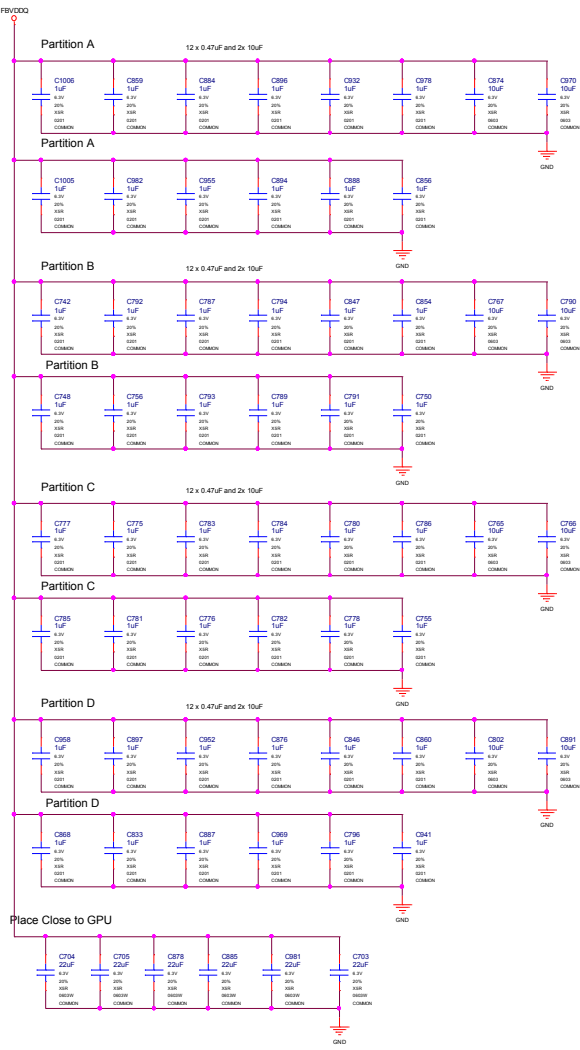
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PAGE DETAIL	GPU PWR & GND

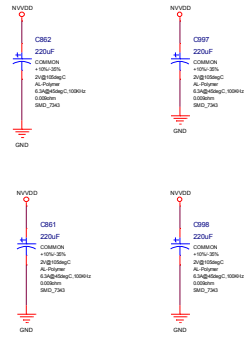
  

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NV_PN	600-G161-BASE-100	PCB REV	P0181A01	PAGE	14 OF 42
RCM REV	B	DATE	19 NOV 2018		

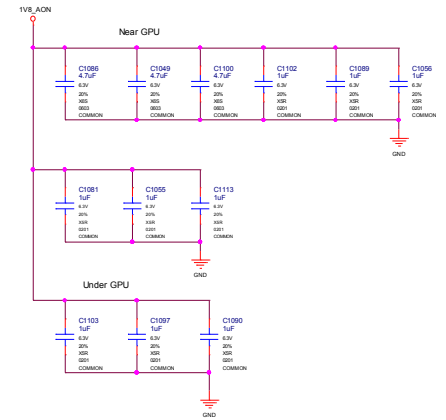
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NVVDD




1V8\_AON

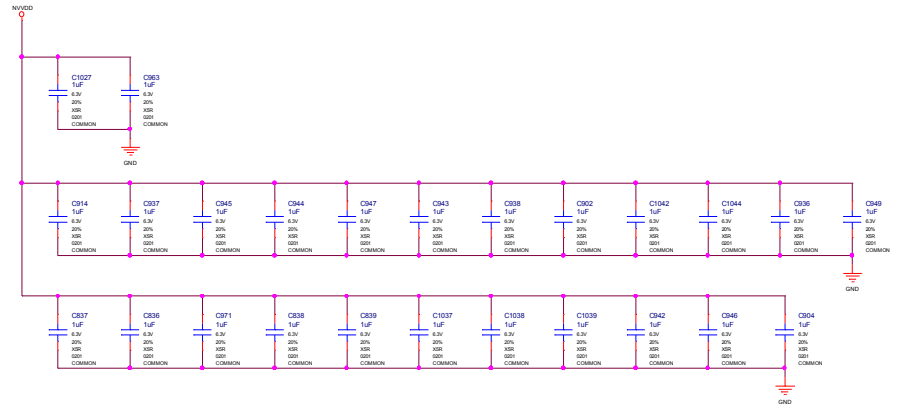
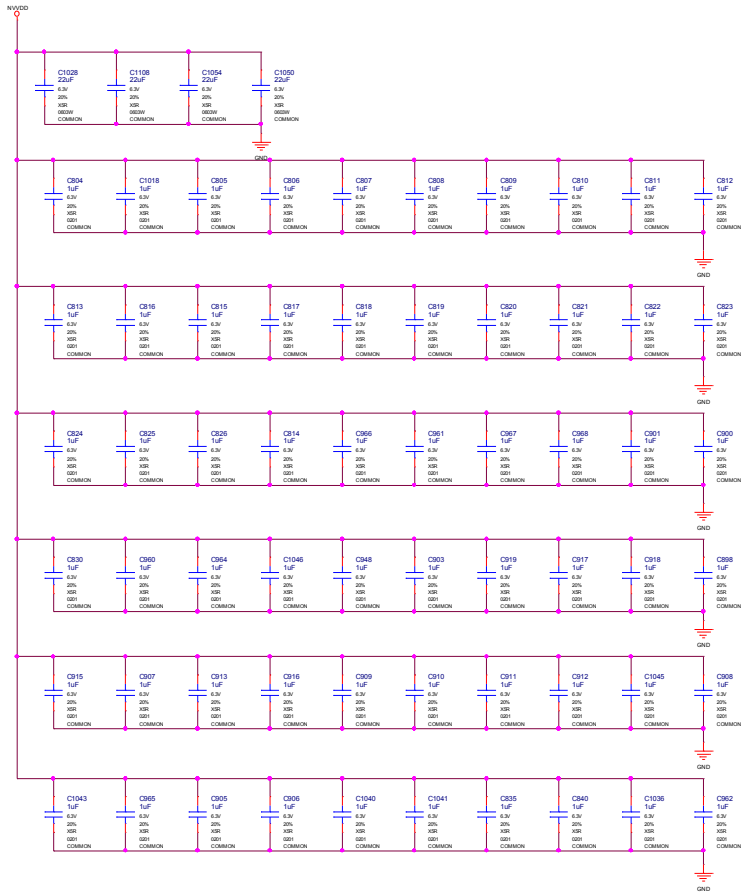


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	GPU Decoupling

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NV_P/N PCB REV BCM REV	600-1G161-BASE-100 PG161-A01 B	
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NVDD



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	GPU Decoupling2

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# IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

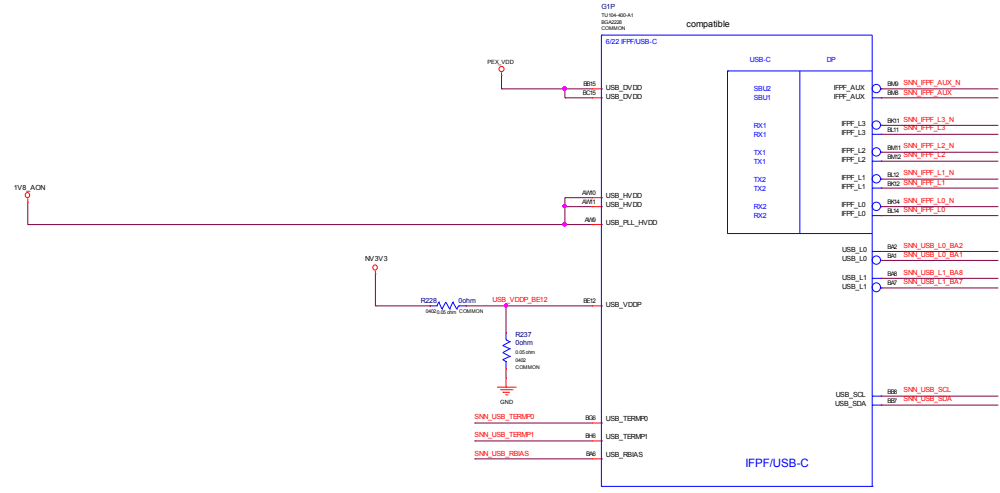
Two cases to be considered:

1. DP ALX to DP connector: ALX AC coupled
2. DP ALX to DP-DVI dongle: ALX pass through

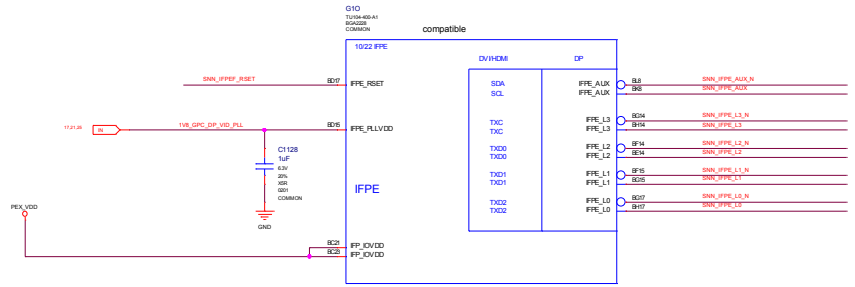
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IC: IFPB DP

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IFPF NC



IFPE NC

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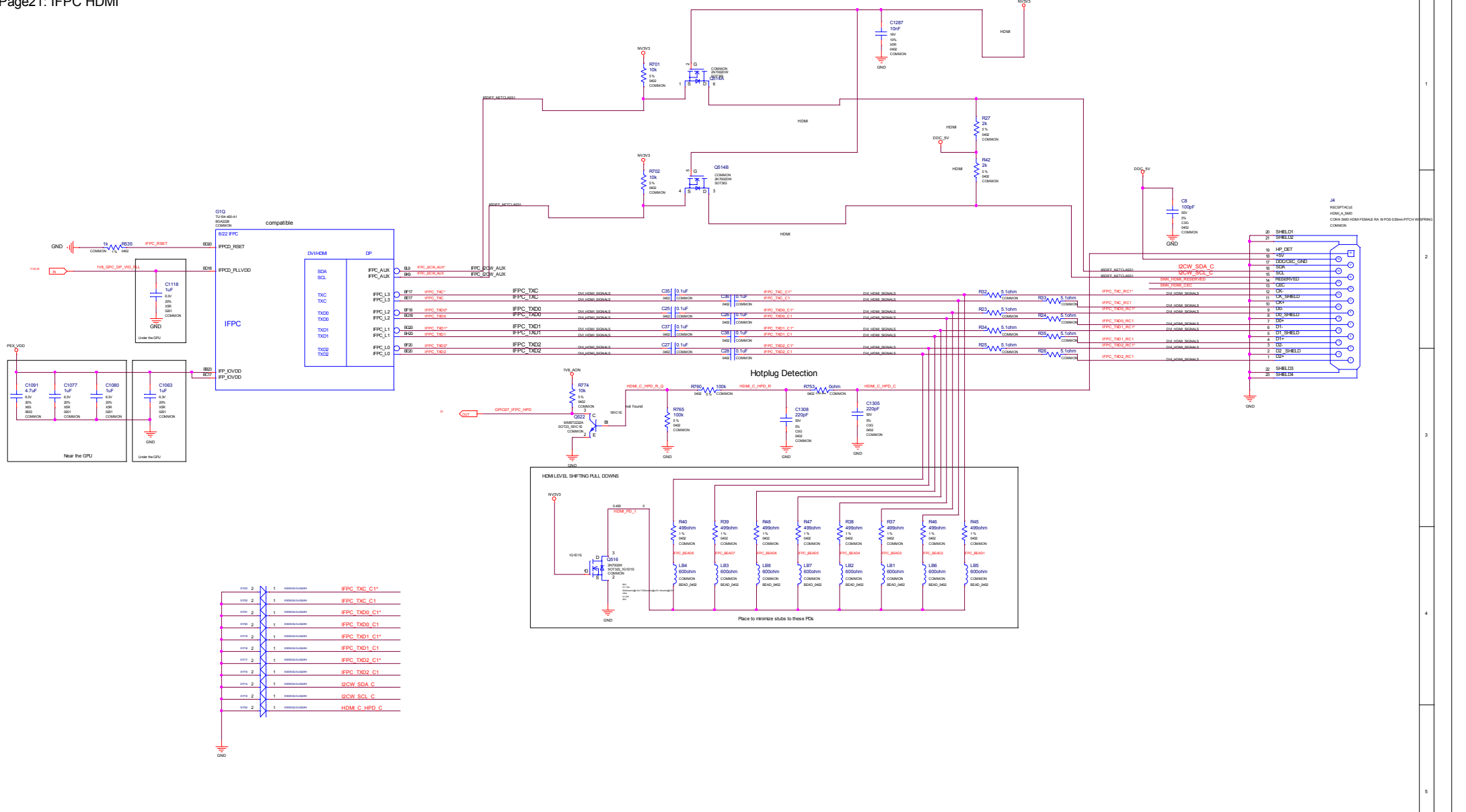


ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	

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ICM REV			

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ID: IFPE & IFPF USB-C NC



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	02 IFPC HDMI

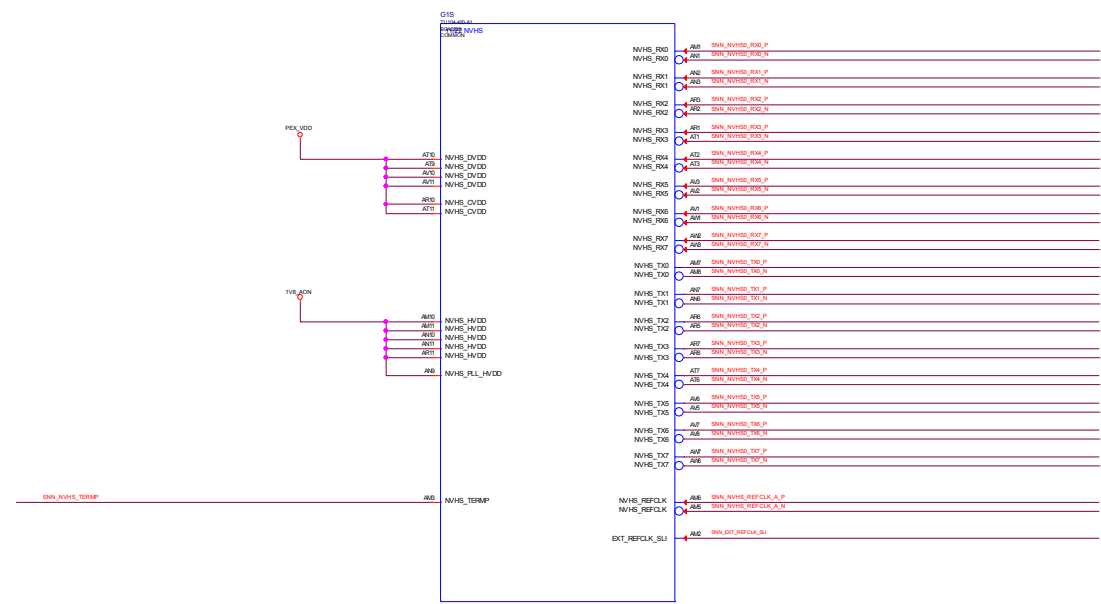
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**NV\_PN 600-IG161-BASE-100**

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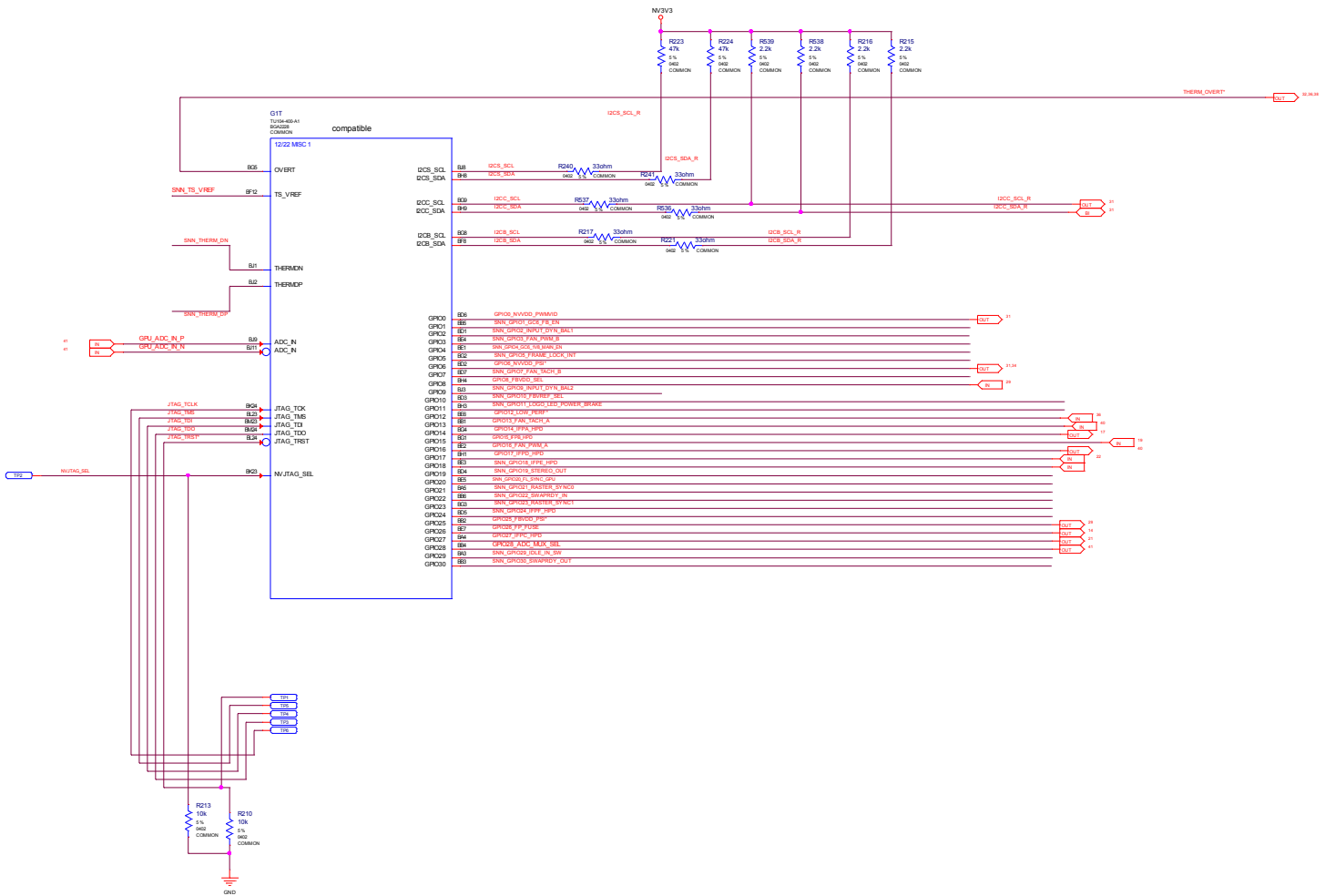
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	ID: NVHS Interface and Frame Lock

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MISC1: Thermal, JTAG, GPIO, STEREO

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

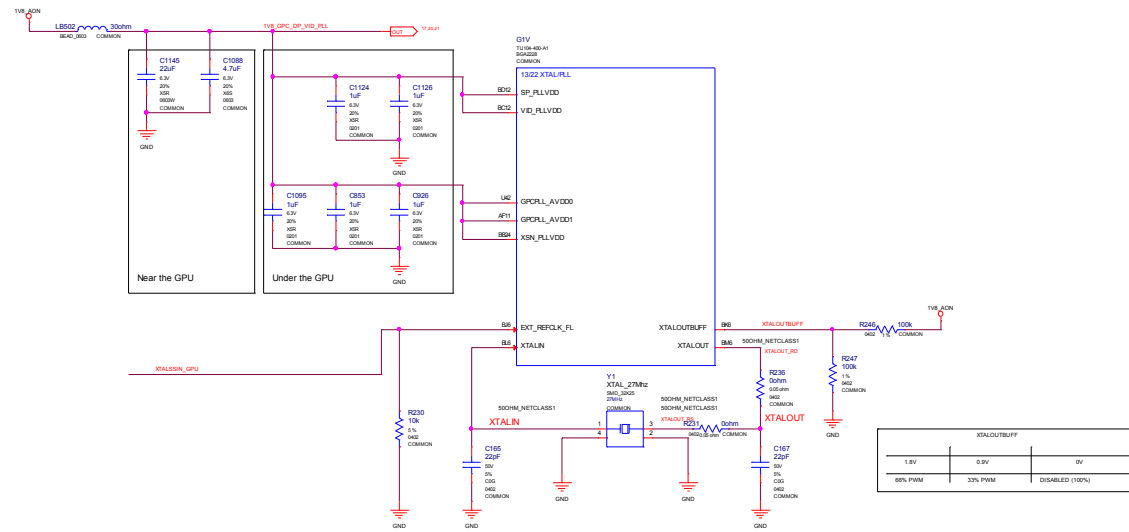
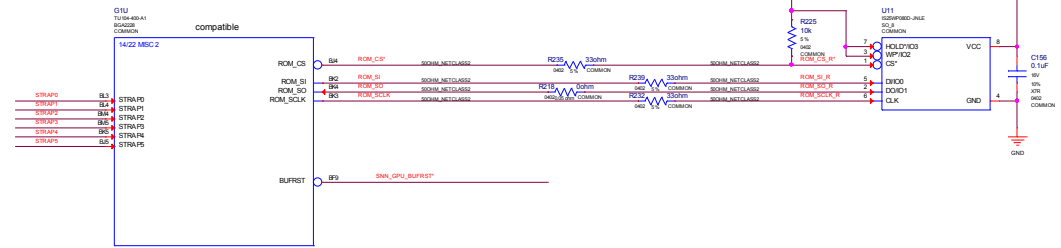
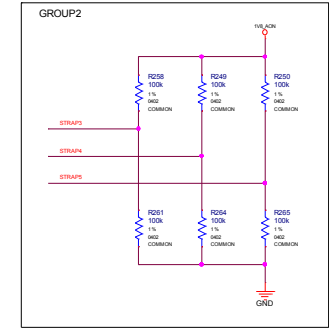
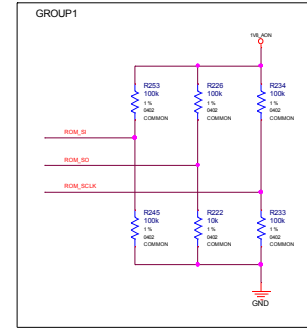
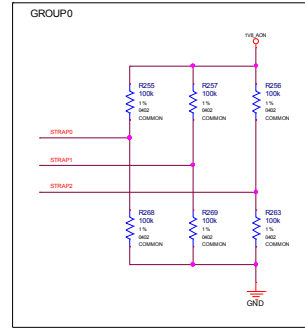
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1.ENABLE 0.DISABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORGNAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



XTALOUTBUFF		
1.8V	0.9V	0V
80% PWM	33% PWM	DISABLED (100%)

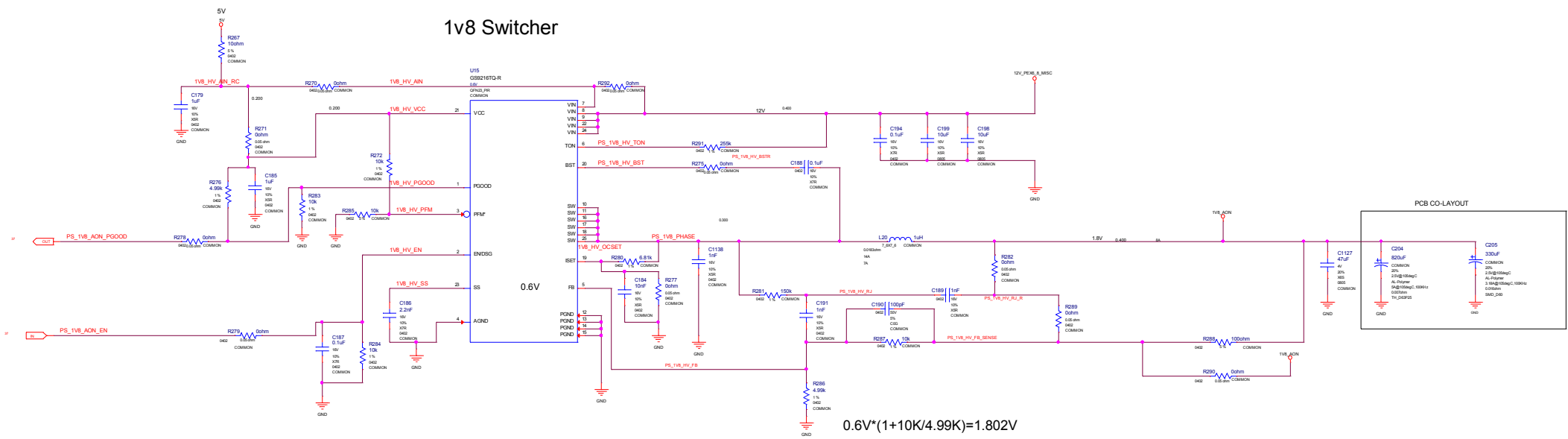
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ASSEMBLY	ASSEMBLY DESCRIPTION	NV_PN	PCB REV	PCB PART	PCB DATE	PAGE	OF
	MISC2: ROM, XTAL, STRAPS	600-1G161-BASE-100	D100	PG161-A01	19 NOV 2018	25	42

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# 1v8 Switcher




$0.6V * (1 + 10K / 4.99K) = 1.802V$

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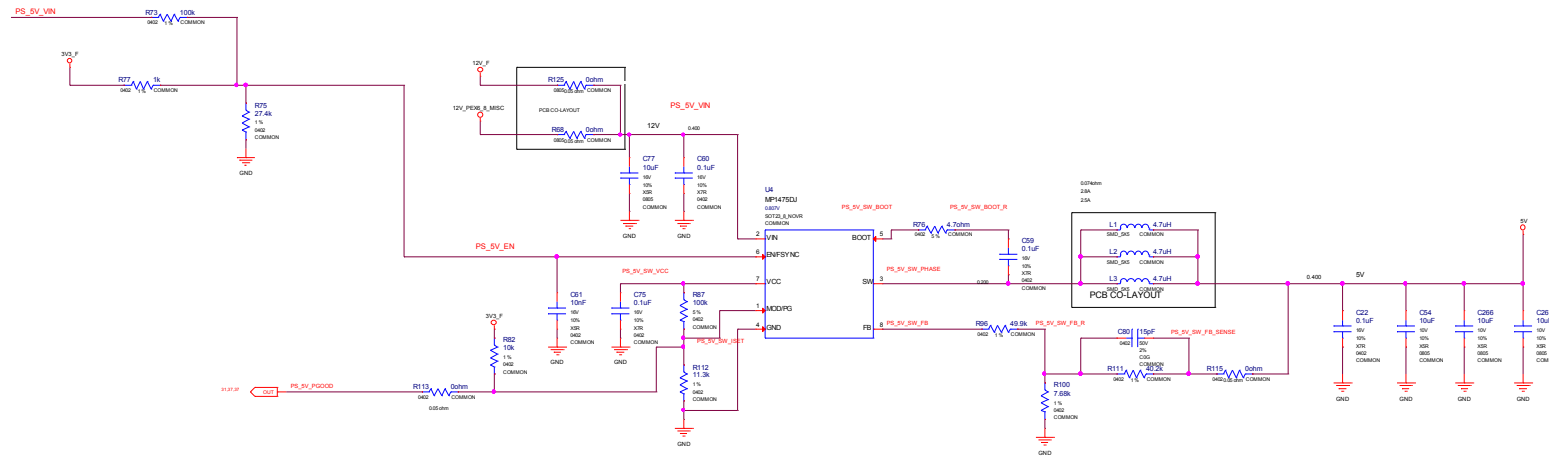
ASSEMBLY	"ASSEMBLY DESCRIPTION"
PAGE DETAIL	PS: 1V8_AON

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$$0.8V \cdot (1 + 40.2K / 7.68K) = 4.9875V$$

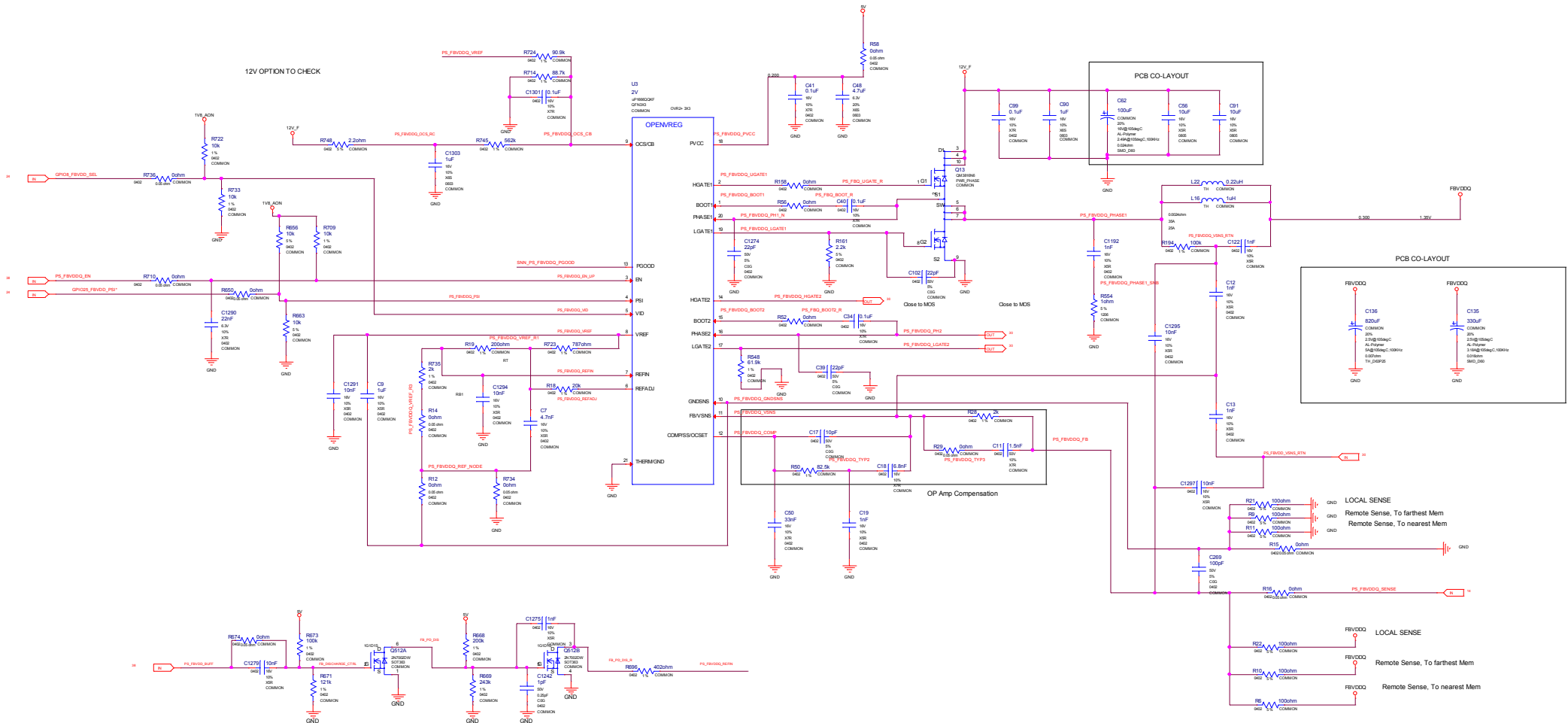
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PAGE: 27/42	PS: 5V

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NV_PN	600-1G161-BASE-100		
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BOM REV	B	DATE	19-NOV-2018







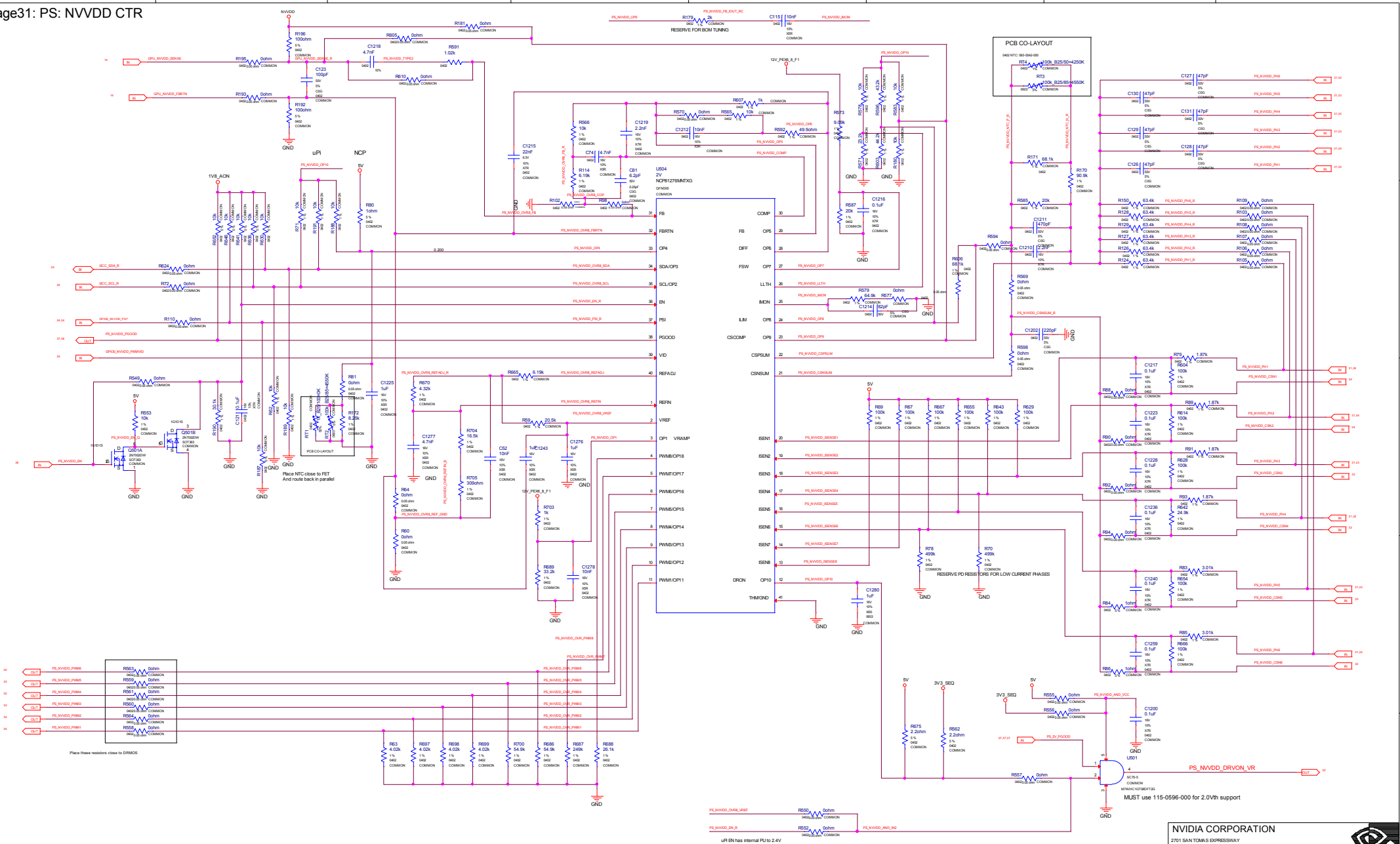
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ASSEMBLY	ASSEMBLY DESCRIPTION	NV_PN	600-1G161-BASE-100
PAGE DETAIL	PS_FBVDDQ	PCB REV	PG181-A01
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Place these resistors close to DRMS

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uP EN has internal PU to 2.4V

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**Nv\_PN 600-1G161-BASE-100**

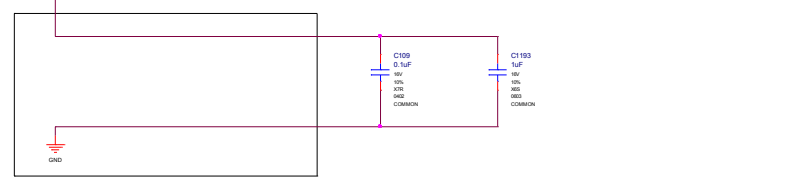
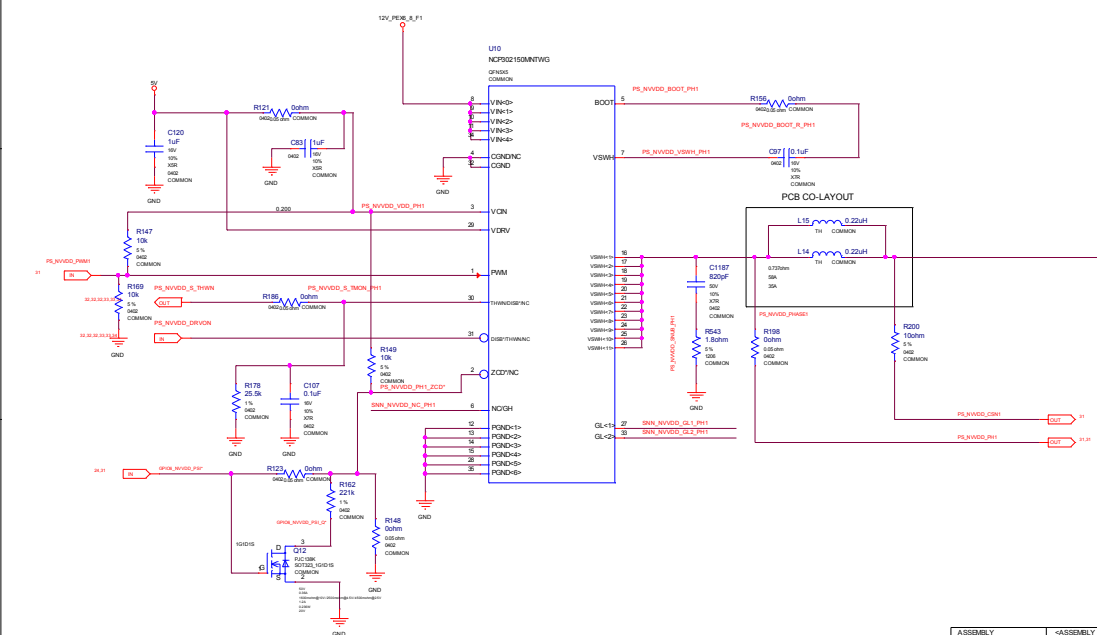
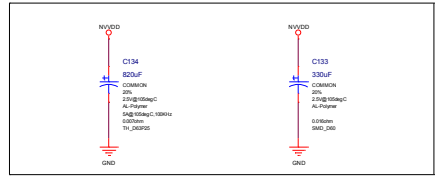
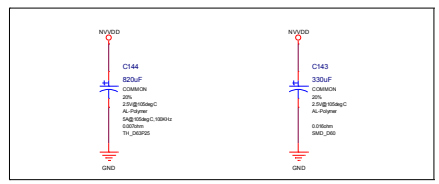
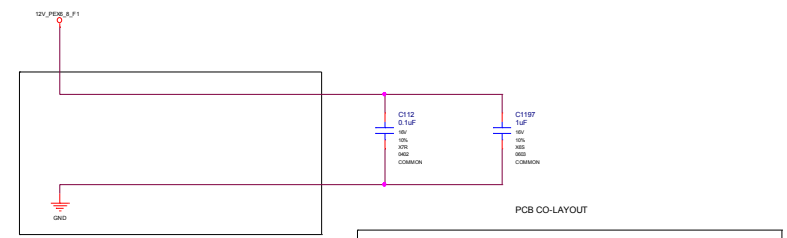
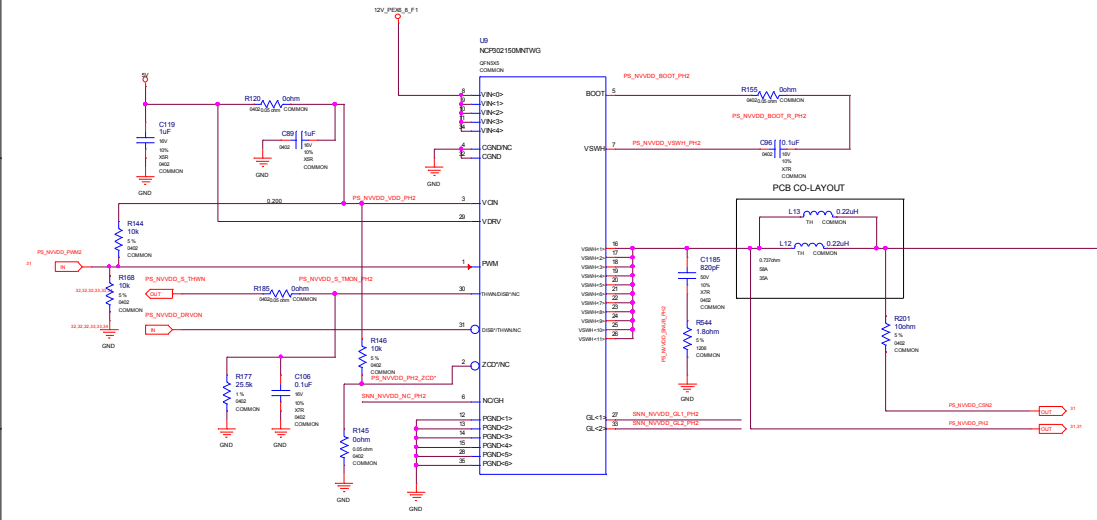
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BCM REV	B	DATE	19-NOV-2018











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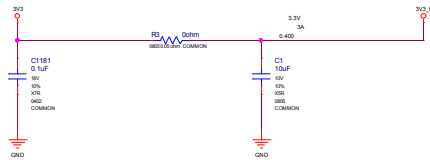


ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: NVVDD Phase 2.1

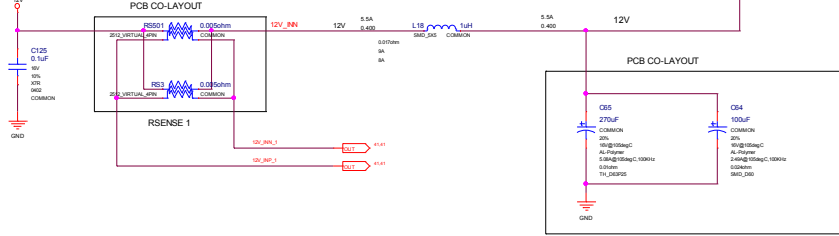
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NV_PN	600-1G161-BASE-100
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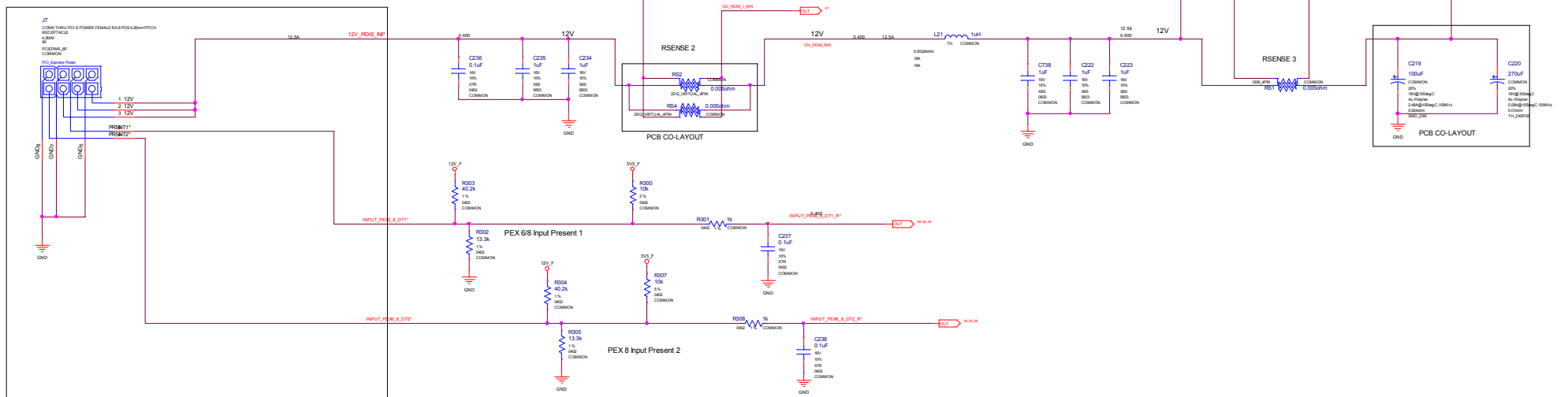
PEX 3V3 INPUT - 10W



PEX\_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



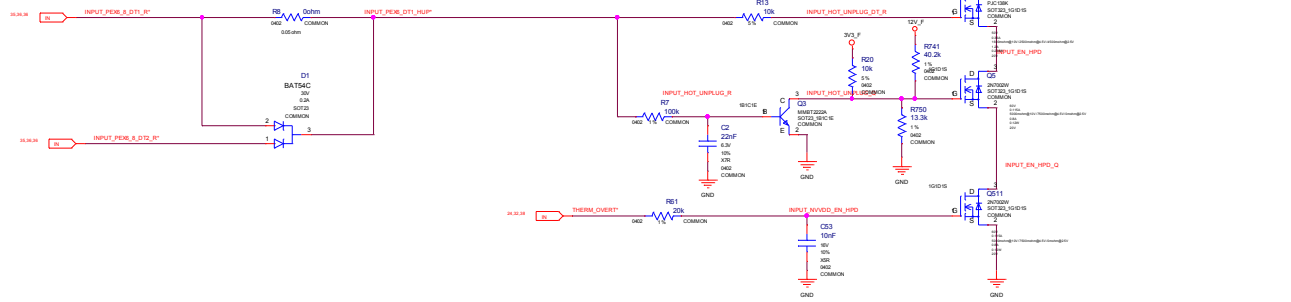
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ASSEMBLY	ASSEMBLY_DESCRIPTION
PAGE:DETAIL	PS: Input, Filtering, and Monitoring

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Nv_PN	600-1G161-BASE-100	PAGE	35 OF 42
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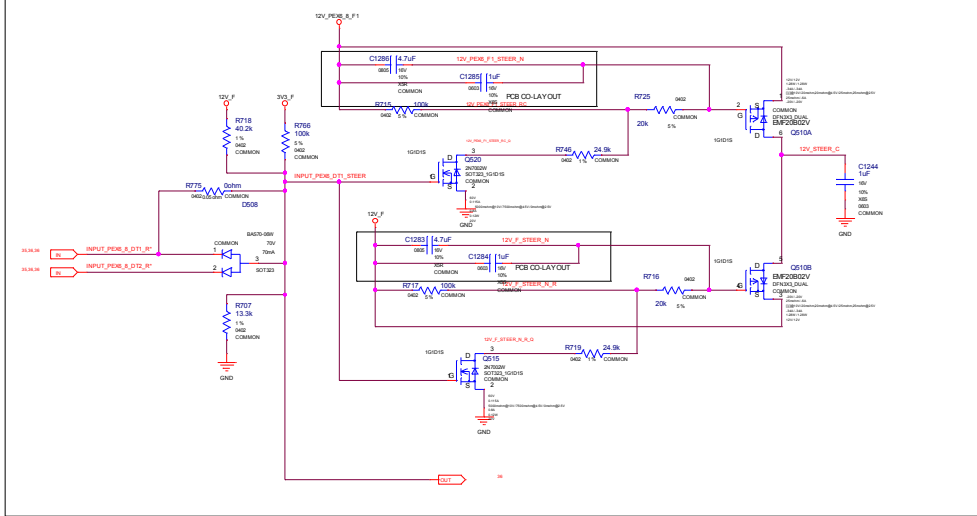
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

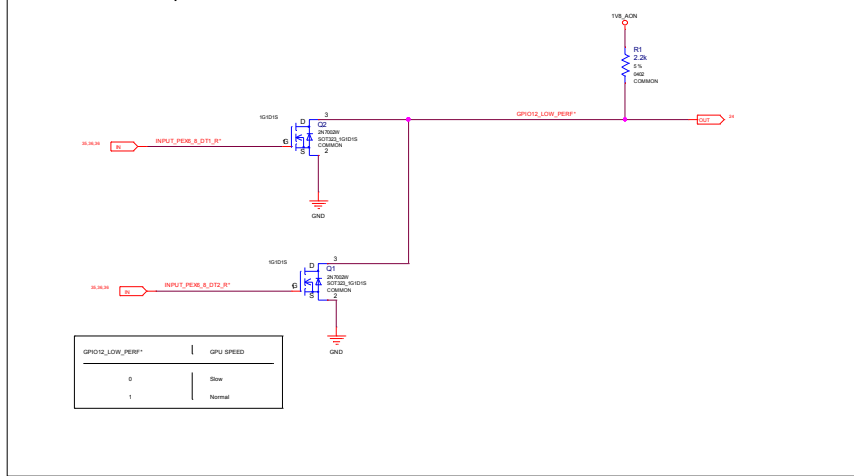


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI\* Control



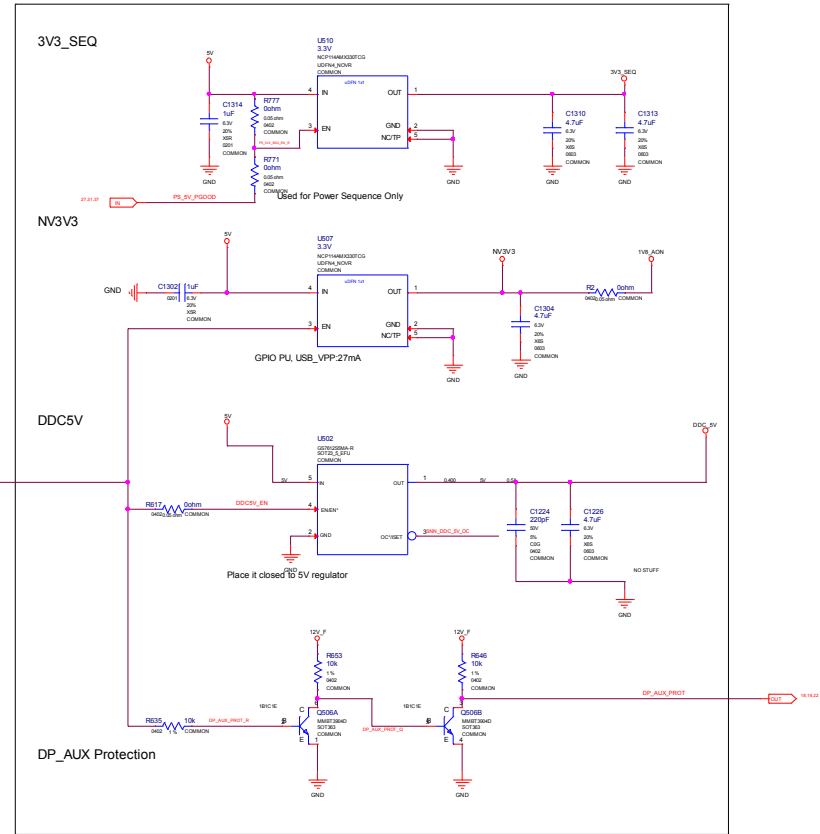
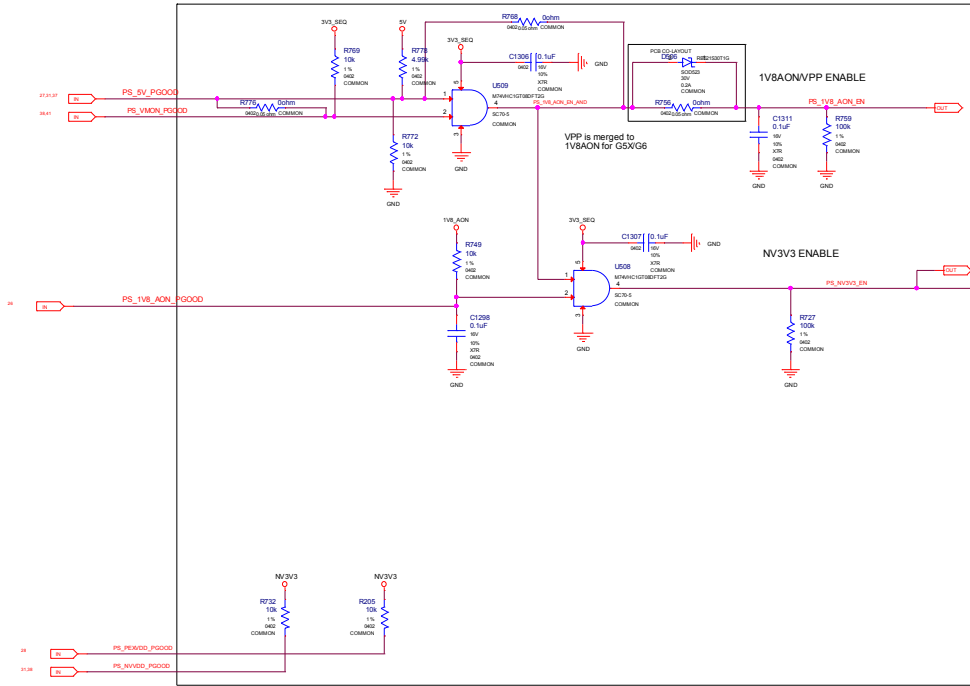
GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: STEERING, LFB & HOT-UNPLUG

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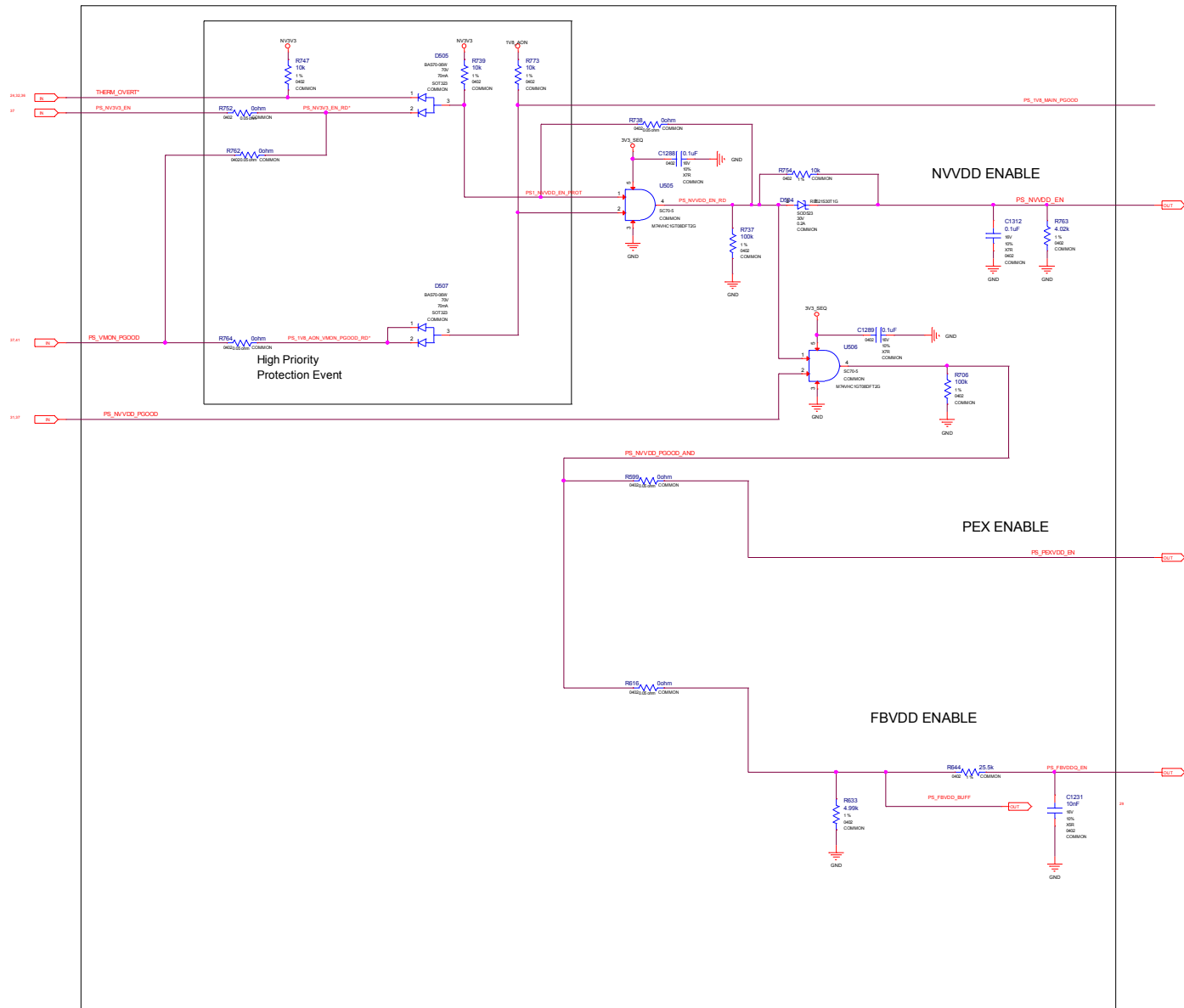


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	SEQ 5V, 1V8, NV3V3 ENABLE

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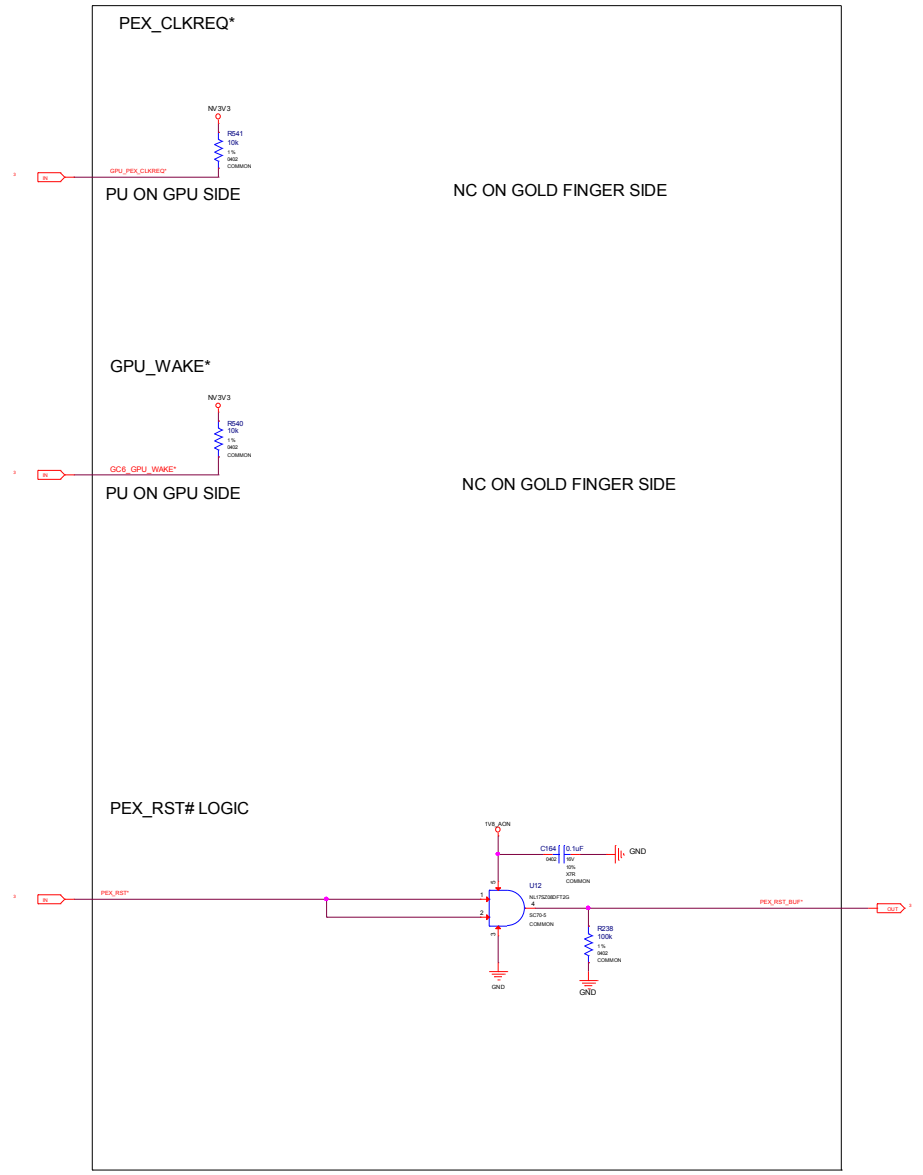
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NV, PEX, FB ENABLE

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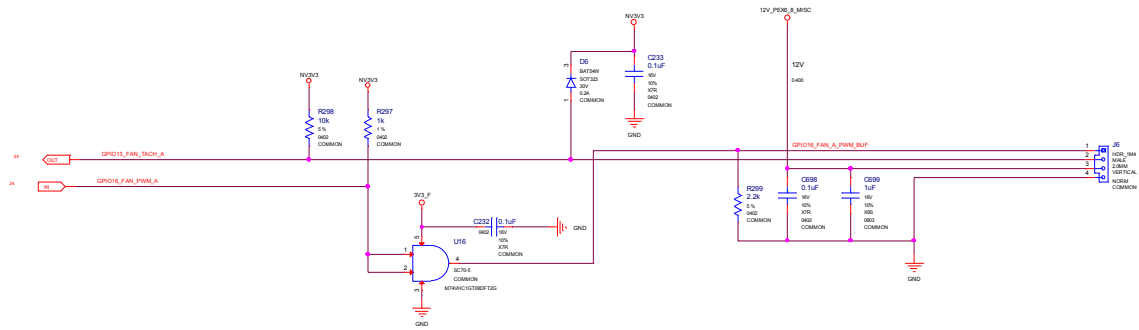
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ASSEMBLY	-ASSEMBLY DESCRIPTION-
PAGE DETAIL	SEQ MISC

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	FAN

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A B C D E F G H



MODE PN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

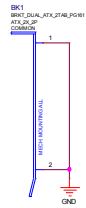
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PCB REV	PG161-A01
BCM REV	B

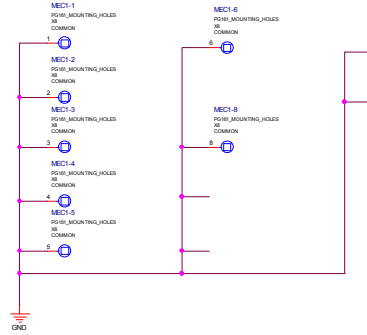
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Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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