

PG160-B03

TU106 6GB GDDR6, 192b, X16 Tall DVI-D + DP + HDMI

TABLE OF CONTENTS


Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCIE RC TERM
5	MEMORY: GPU FB_AB
6	MEMORY: FBA[31:0]
7	MEMORY: FBA[63:32]
8	MEMORY: FBB[31:0]
9	MEMORY: FBB[63:32]
10	MEMORY: GPU FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	GPU PWR & GND
16	GPU Decoupling
17	GPU Decoupling2
18	IO: IFPAB DVI-D-DL
19	IO: IFPE DP
20	IO: IFPF USBC
21	IO: IFPF DP
22	IO: IFPC HDMI/DP
23	IO: IFPD DP
24	IO: NVHS Interface and Frame Lock
25	MISC1: Thermal, JTAG, GPIO,STEREO

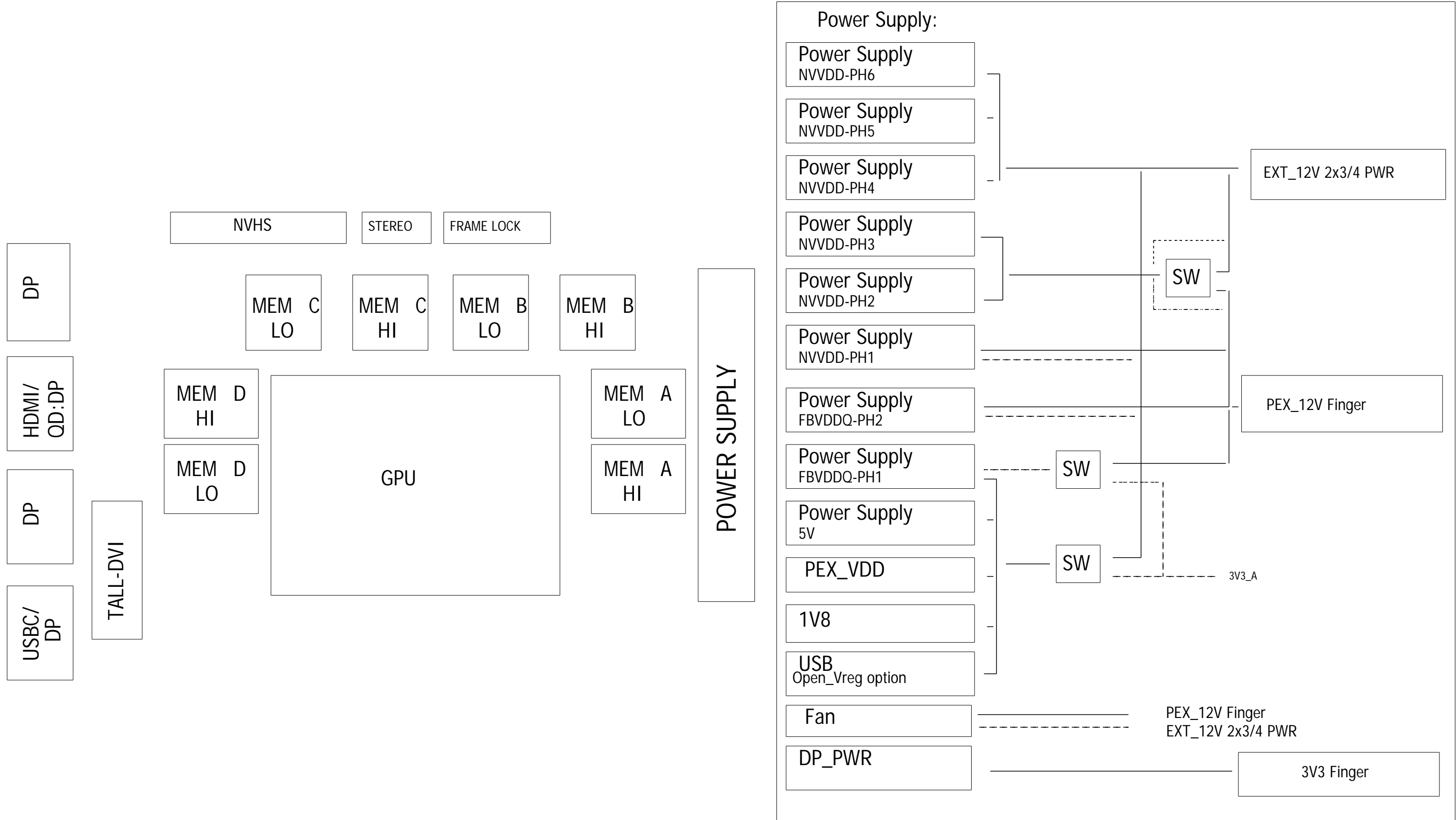
Page	Description
26	MISC2: ROM, XTAL,STRAPS
27	PS: 1V8_PLL, 1V8_AON
28	PS: 5V
29	PS: PEXVDD
30	PS: FBVDDQ
31	PS: FBVDDQ PH2
32	PS: NVVDD Controller
33	PS: NVVDD Controller OVR3i
34	PS: NVVDD Phase 1,2
35	PS: NVVDD Phase 3,4
36	PS: NVVDD Phase 5,6
37	PS: Input Power Balancing Switcher
38	PS: Input, Filtering, and Monitoring
39	PS: STEERING, UPB & HOT-UNPLUG
40	PS: Type-C BuckBoost
41	PD PPC
42	PS: 12V & 3V3_A SWITCHER
43	SEQ: 5V, 1V8, NV3V3 ENABLE
44	SEQ: NV, PEX, FB ENABLE
45	SEQ: VOLTAGE MONITOR
46	SEQ: DISCHARGE
47	SEQ: MISC
48	LOGO LED
49	LED DRIVER & BOOST
50	DUAL FAN

Page	Description
51	PS: Pre-filter
52	MECH
53	PTC

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PAGE DETAIL	Table of Contents

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
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NV_PN	600-1G160-0042-700	PAGE	1 OF 53
PCB REV	PG160-B03	DATE	12-NOV-2018
BOM REV	F		

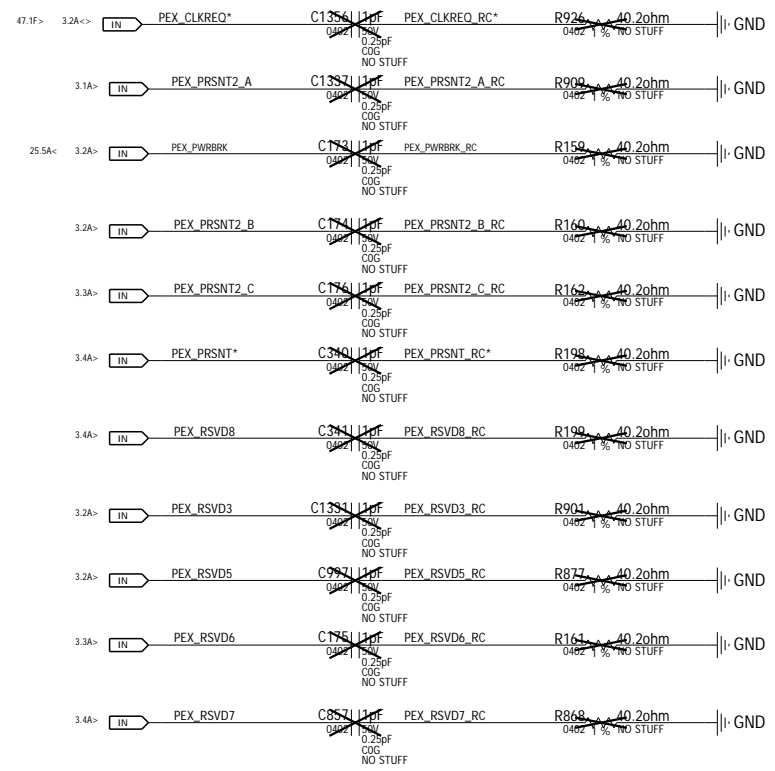


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SANTA CLARA, CA 95050, USA			
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PCB REV	PG160-B03	DATE	12-NOV-2018
BOM REV	F		



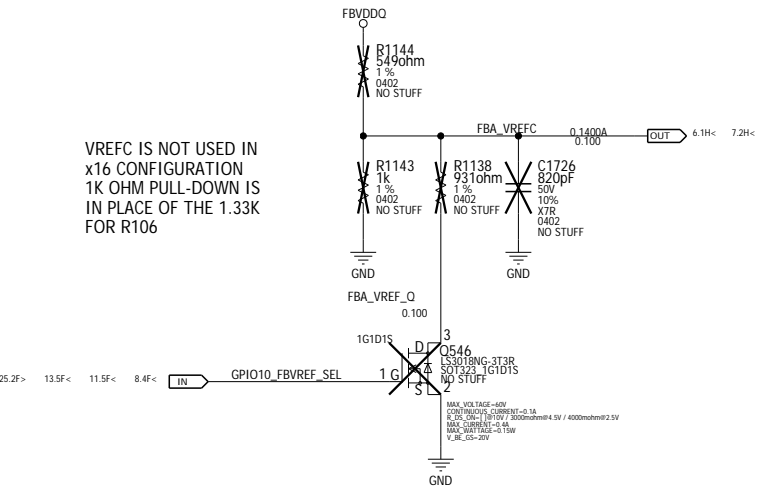
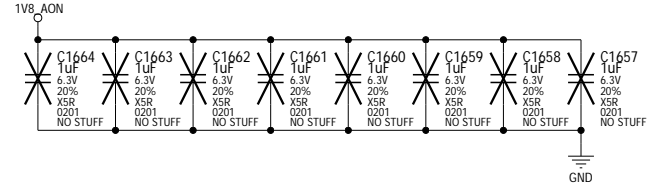
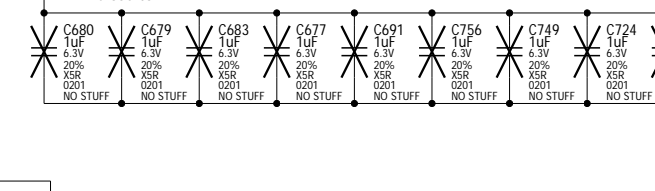
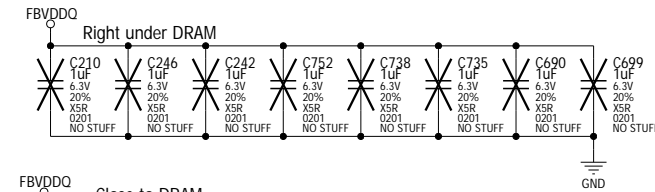
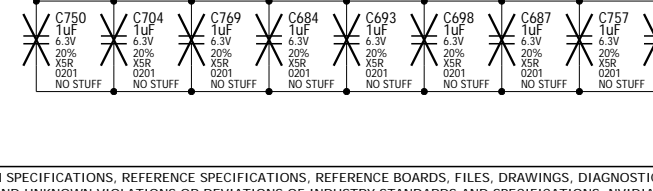
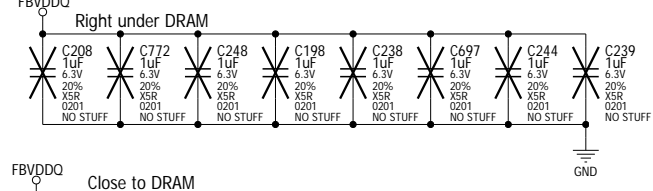
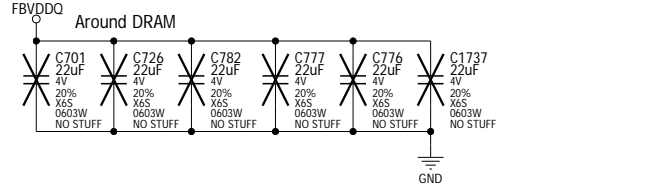
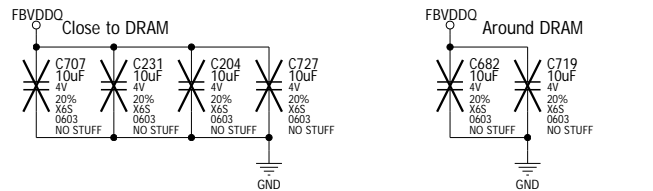
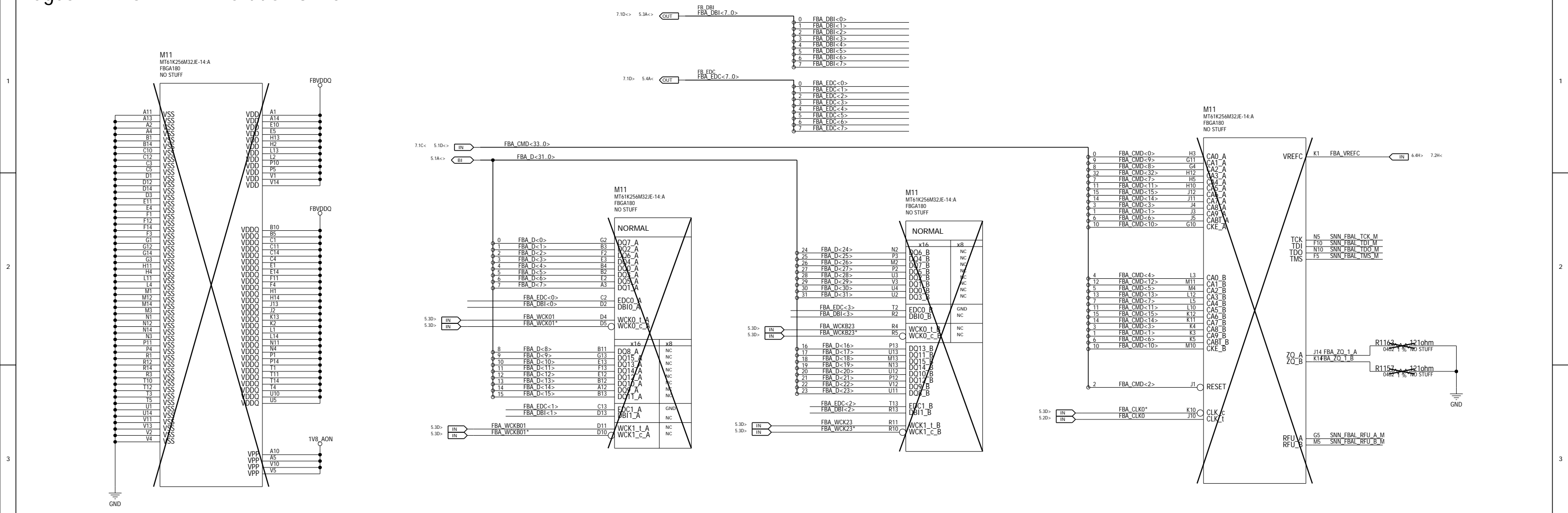


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NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
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PCB REV	PG160-B03	PAGE	4 OF 53
BOM REV	F	DATE	12-NOV-2018



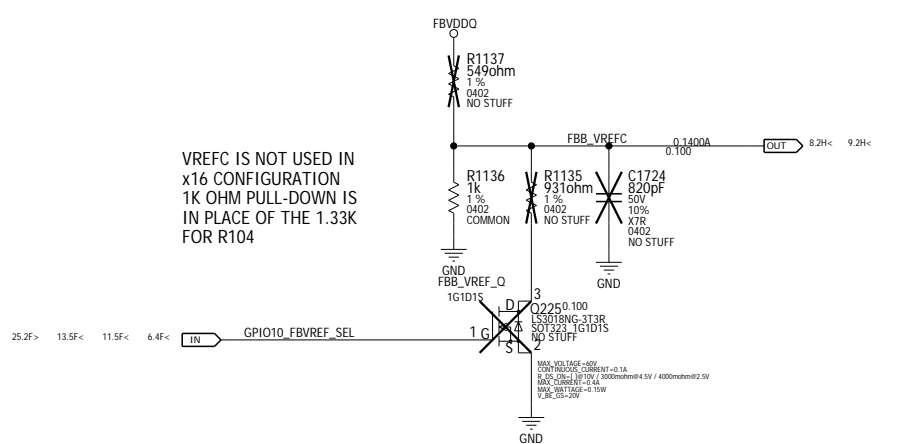
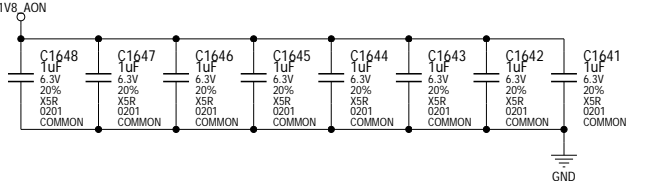
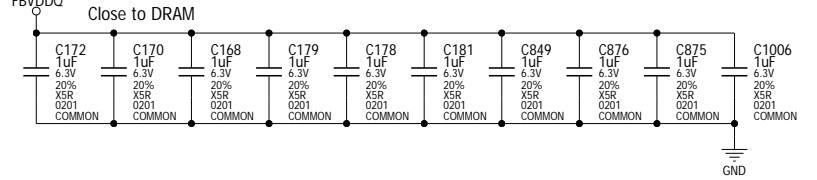
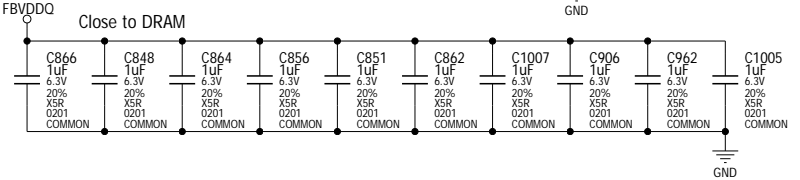
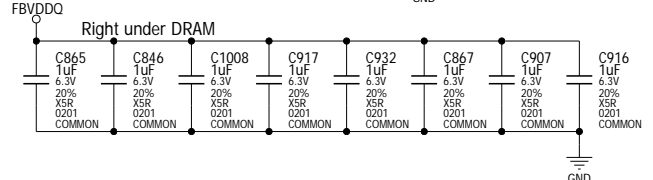
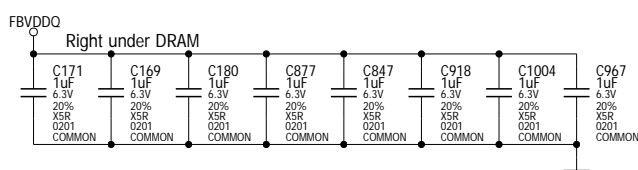
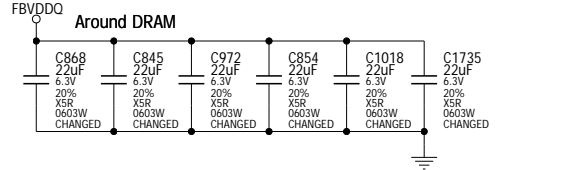
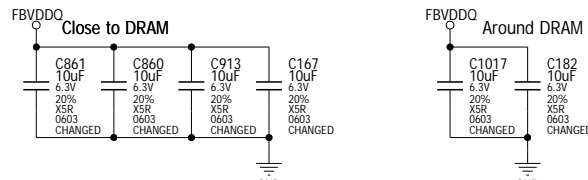
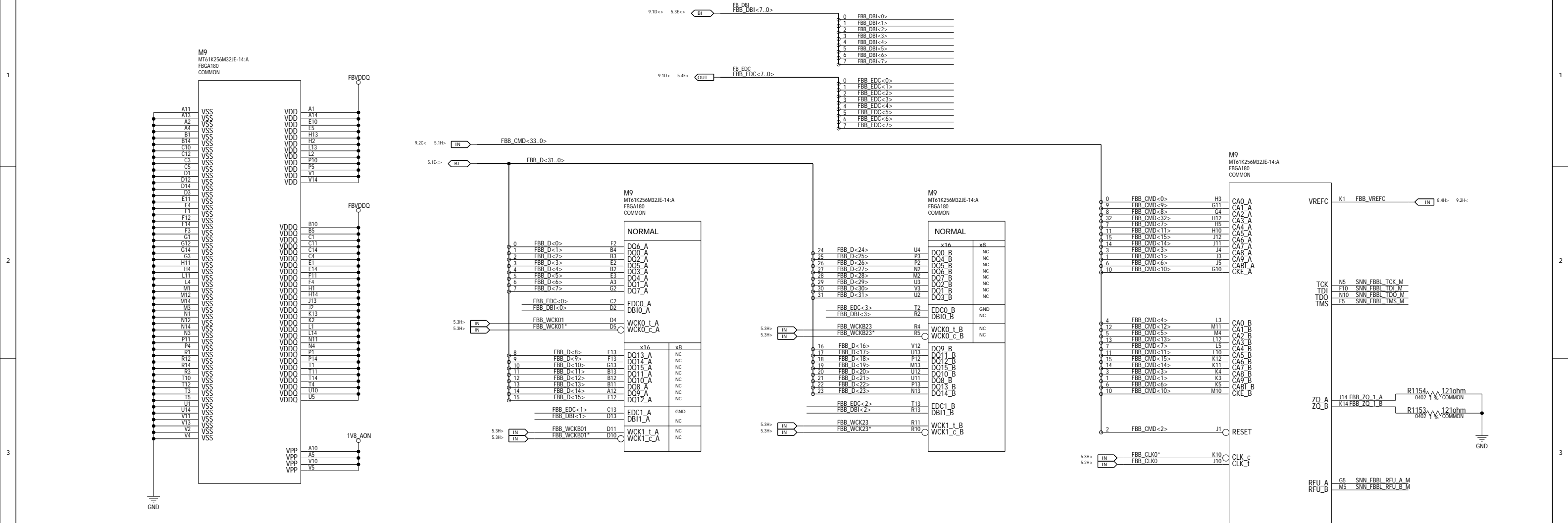


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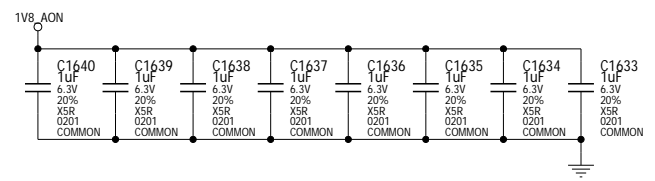
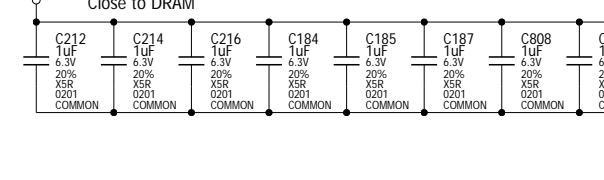
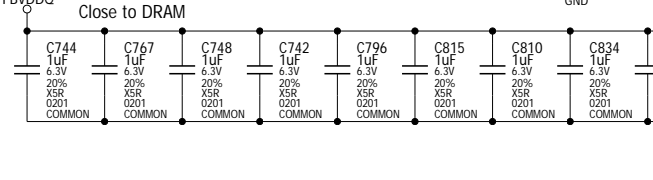
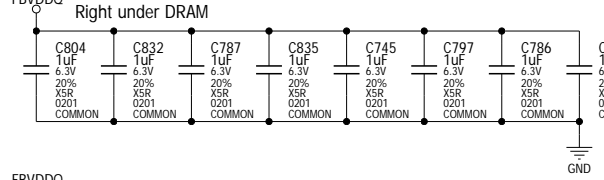
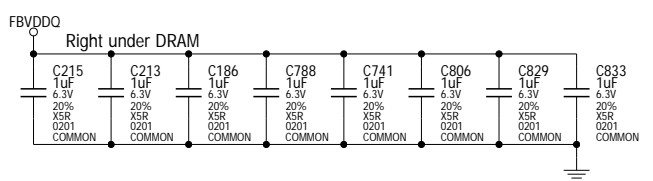
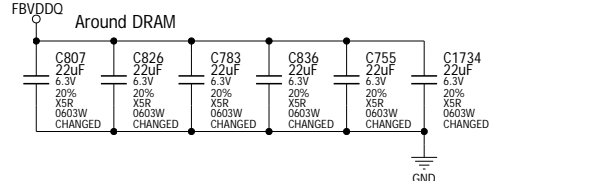
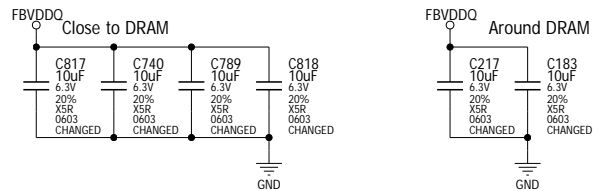
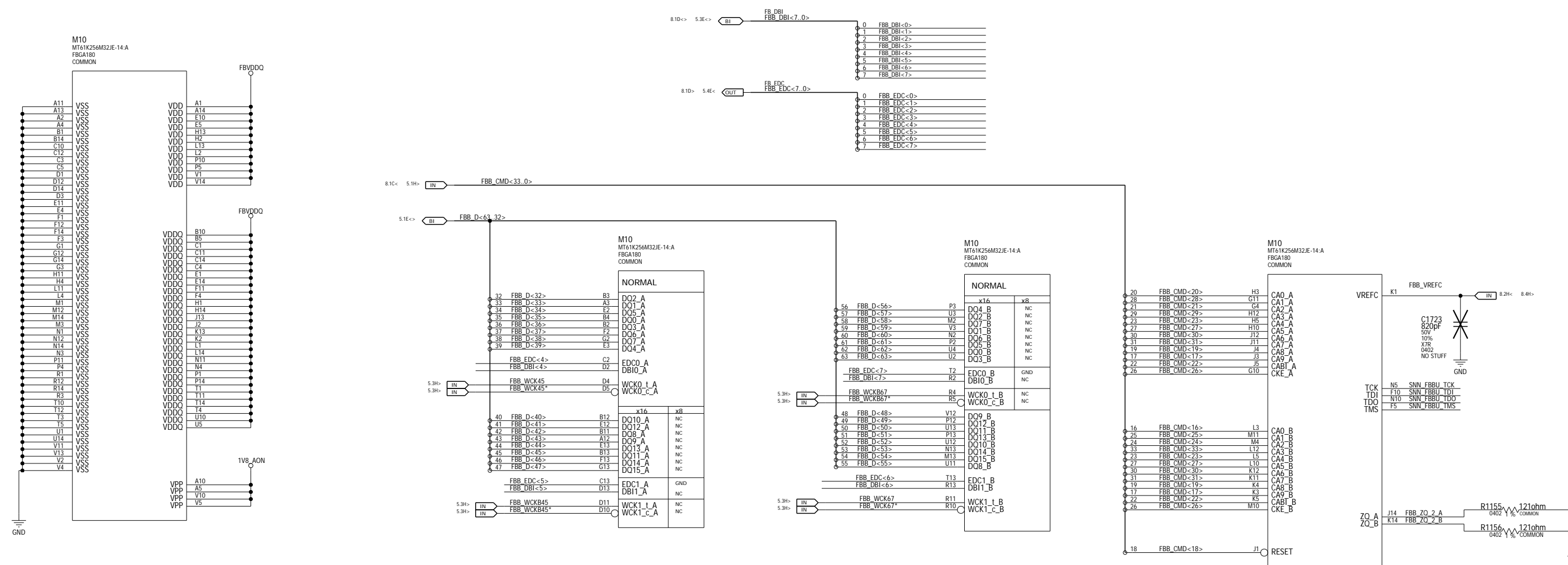
NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F
PAGE	6 OF 53
DATE	12-NOV-2018



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NV_PN	600-1G160-0042-700	PAGE	8 OF 53
PCB REV	PG160-B03	DATE	12-NOV-2018
BOM REV	F		

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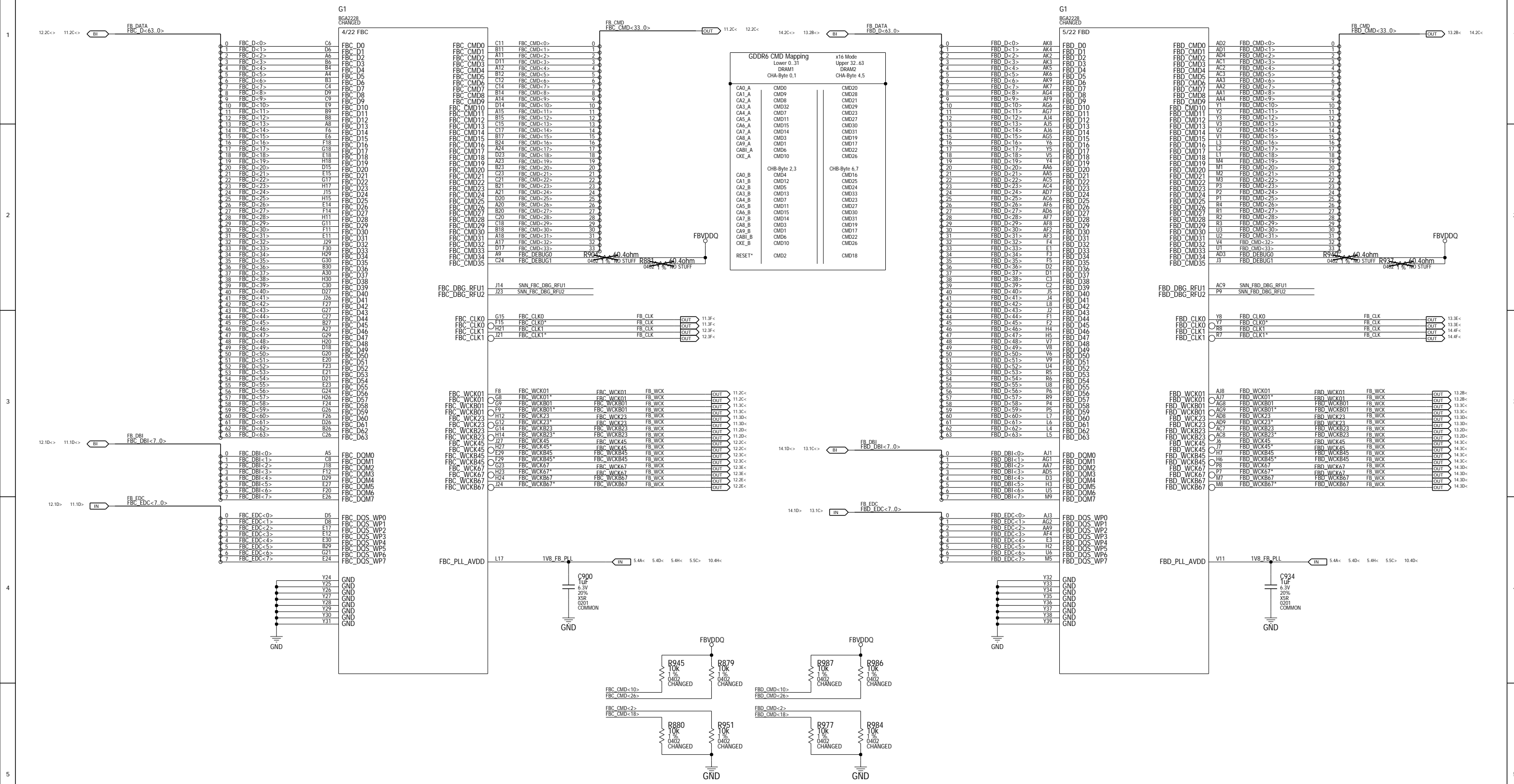
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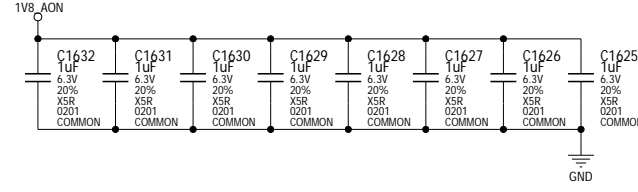
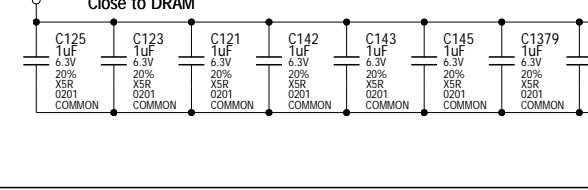
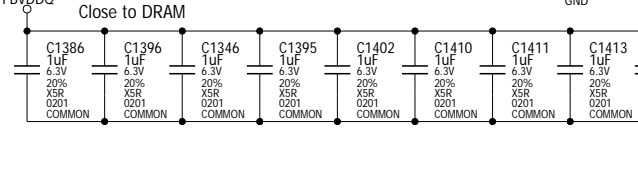
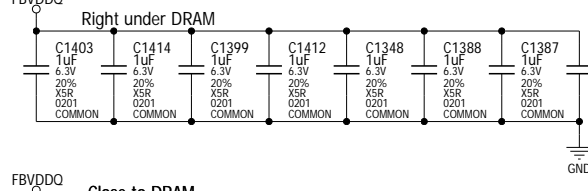
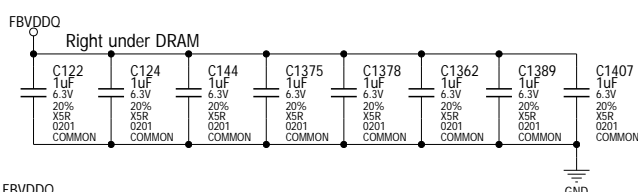
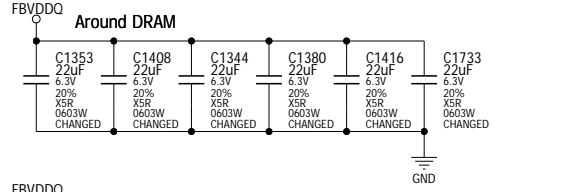
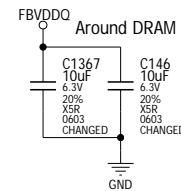
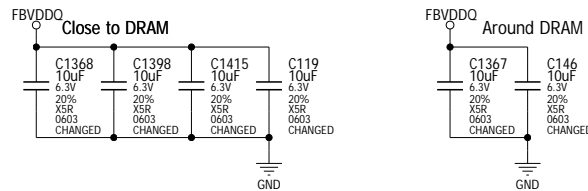
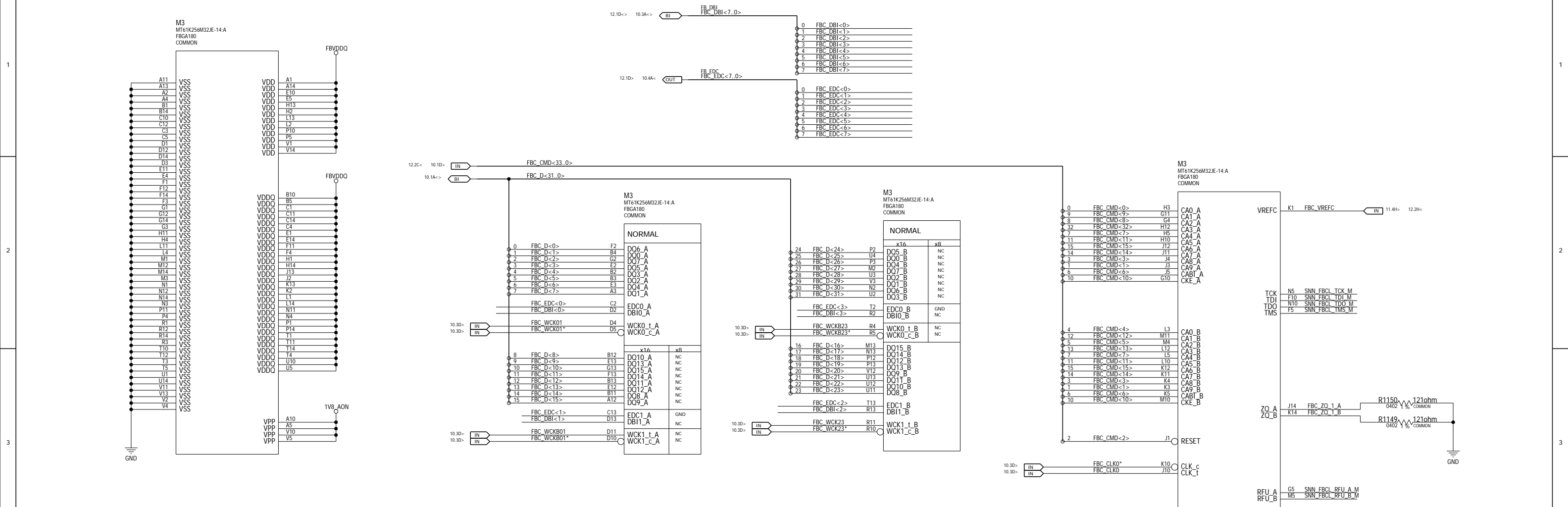
PAGE: 9 OF 53

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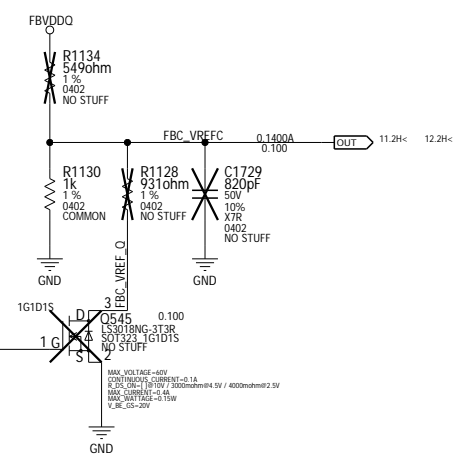
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VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R75



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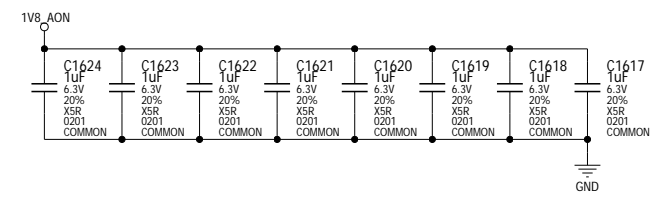
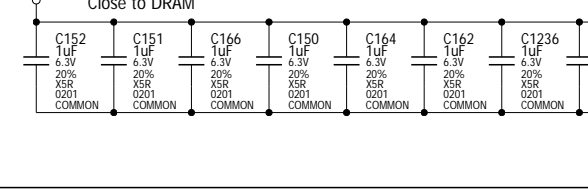
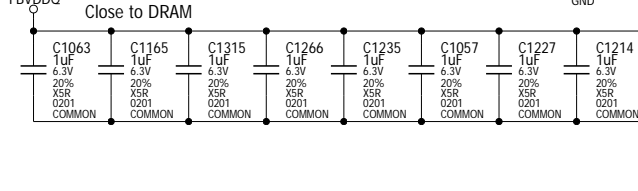
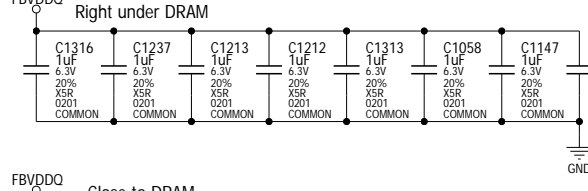
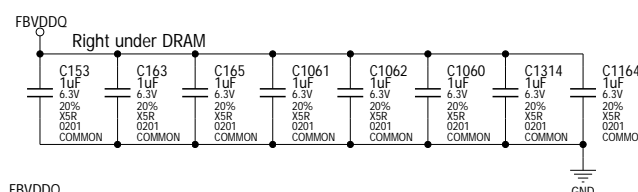
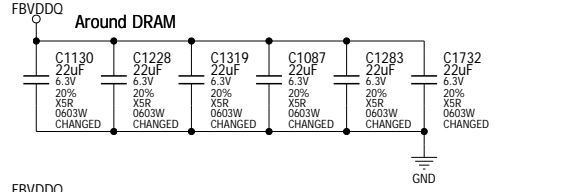
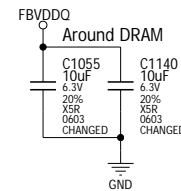
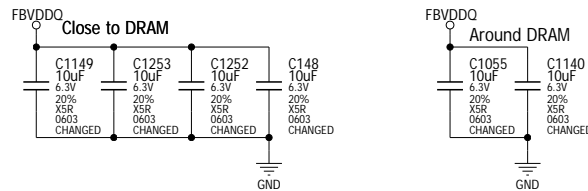
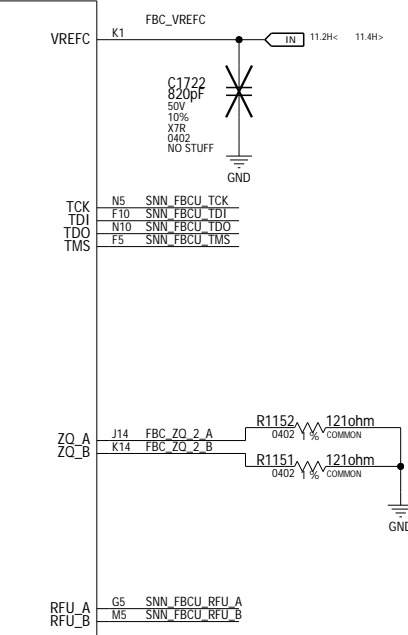
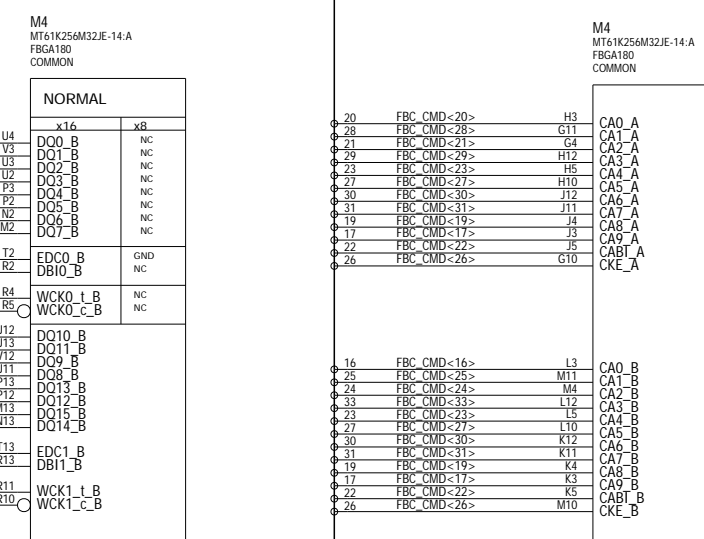
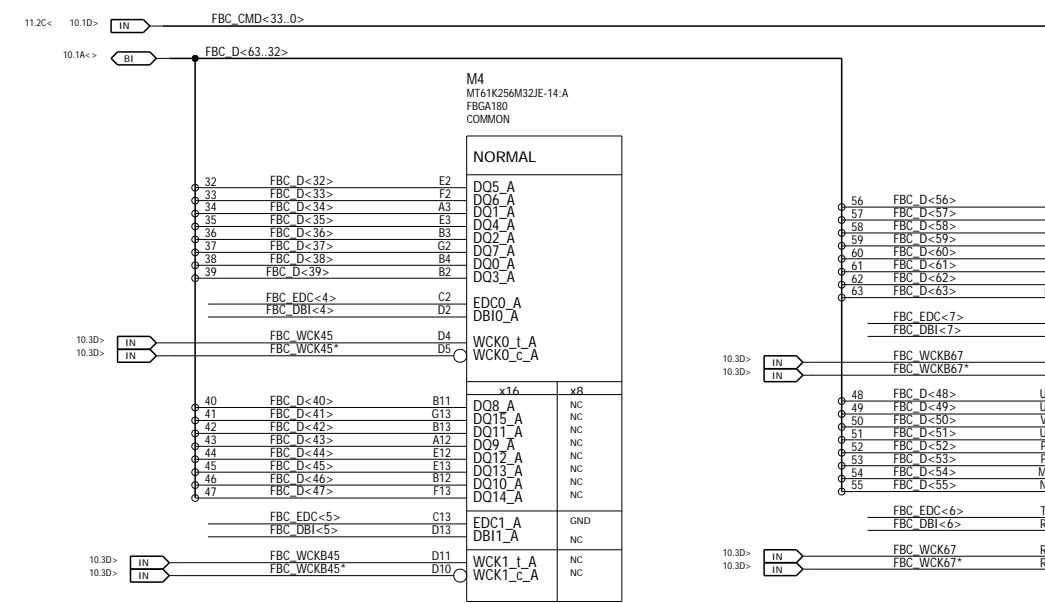
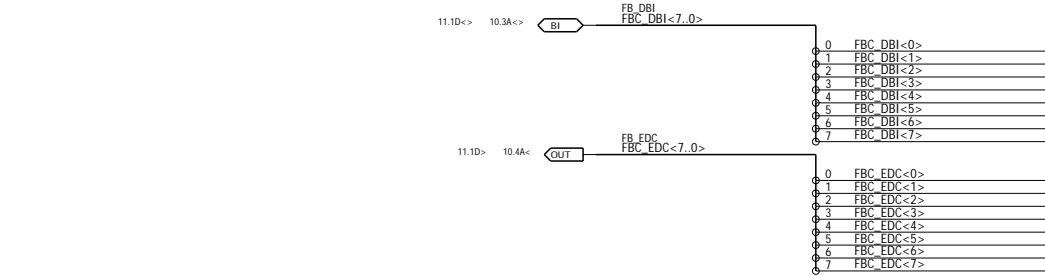
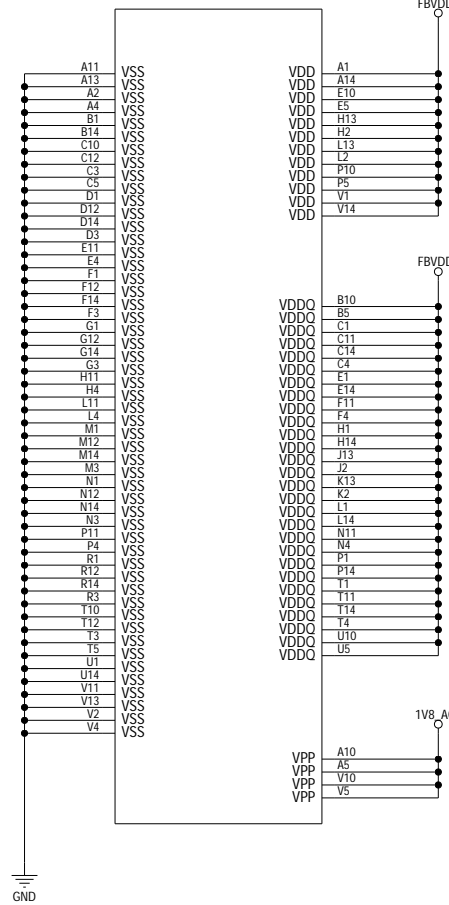
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BOM REV	F

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PAGE	11 OF 53
DATE	12-NOV-2018

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FBGA180
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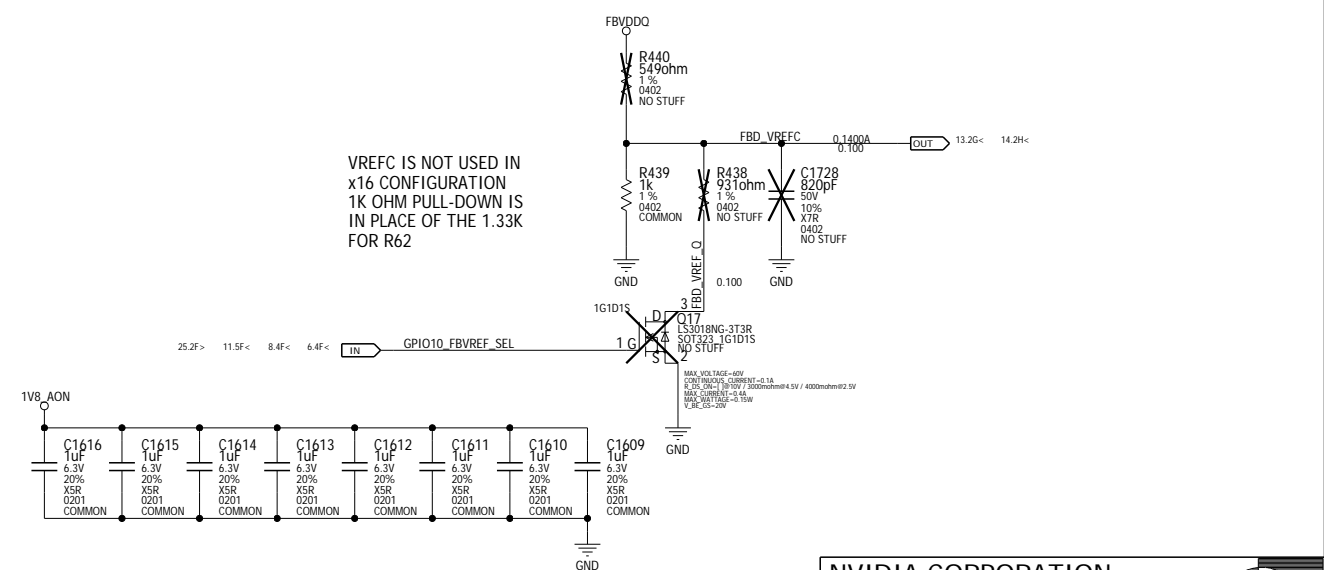
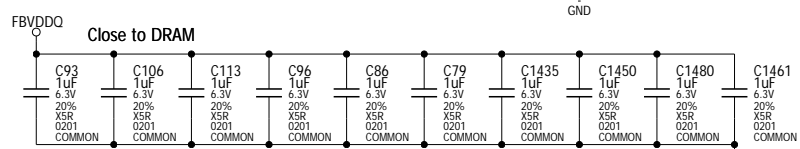
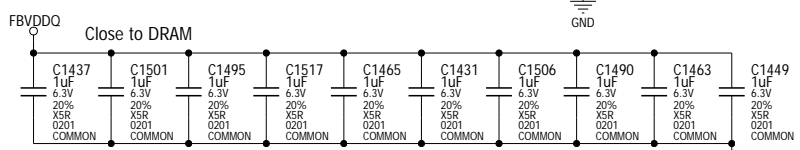
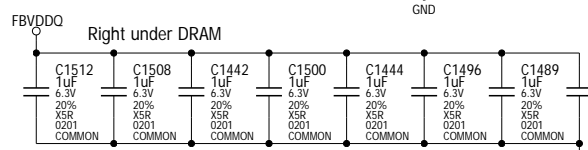
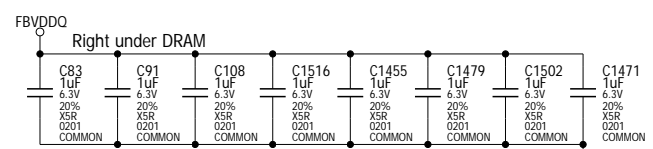
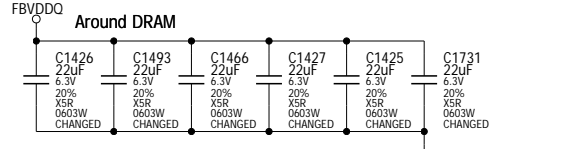
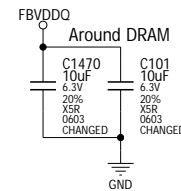
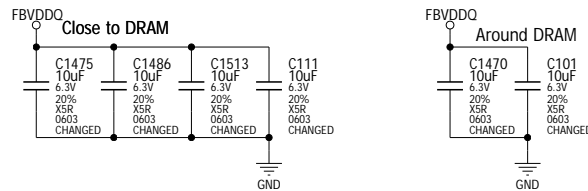
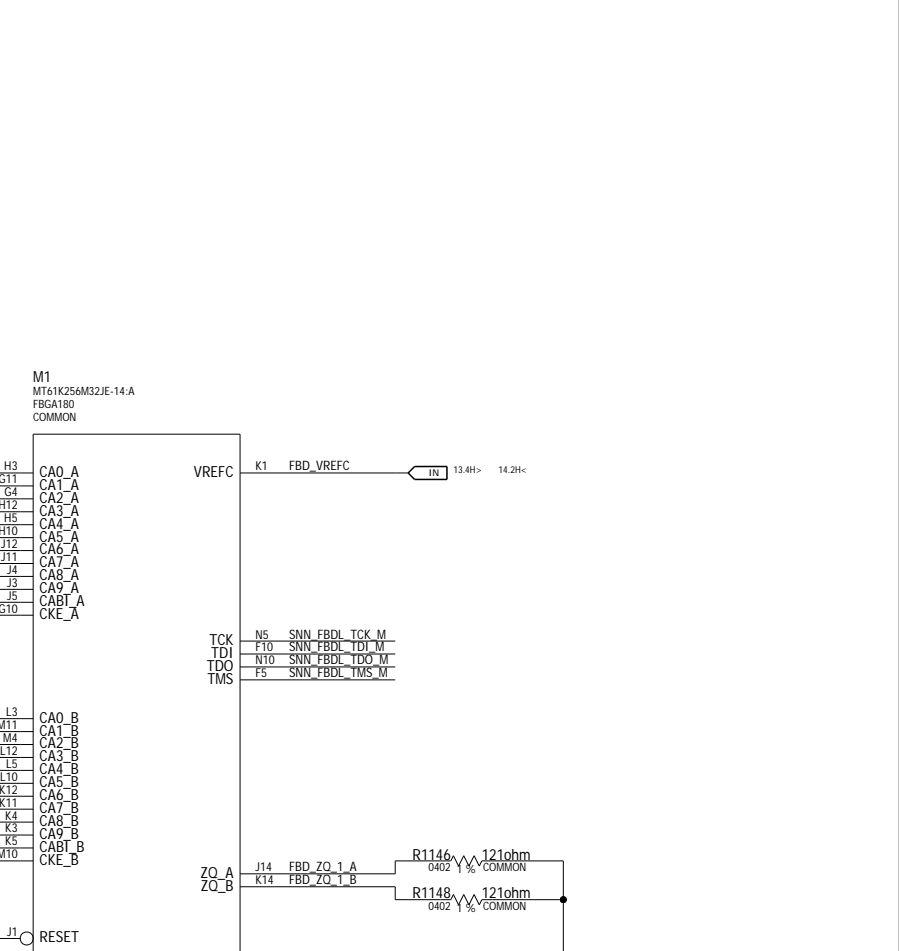
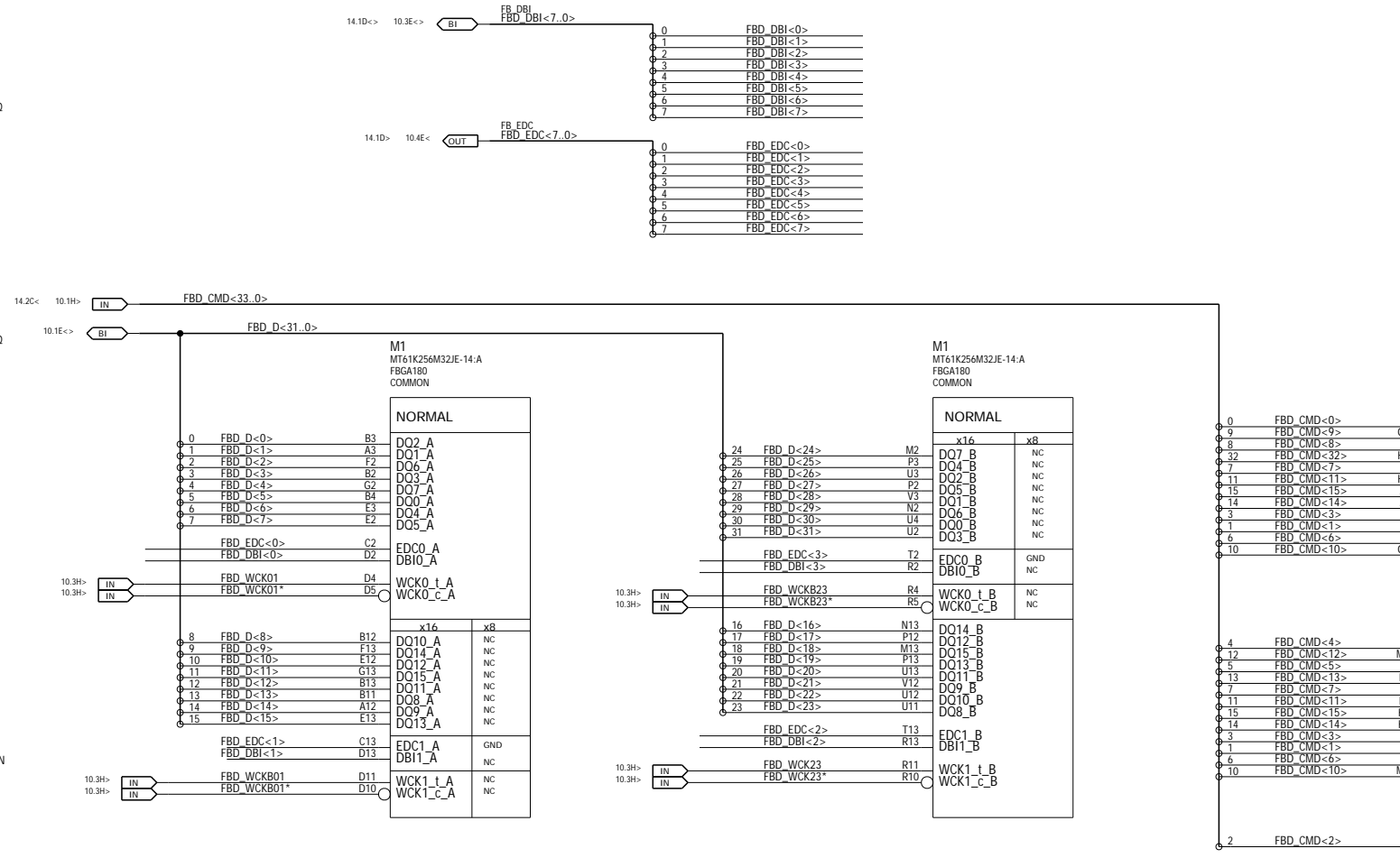
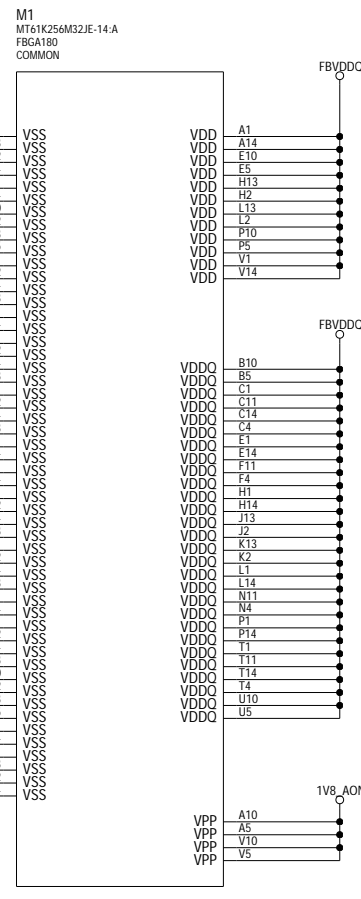
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NV_PN: 600-1G160-0042-700
 PCB REV: PG160-B03
 BOM REV: F

DATE: 12-NOV-2018

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
 PAGE DETAIL: MEMORY: FBC{63:32}

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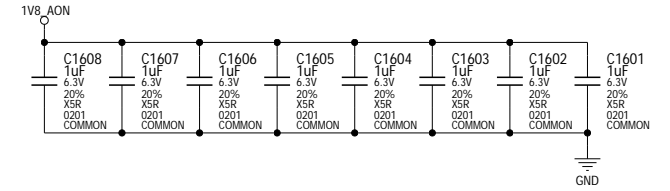
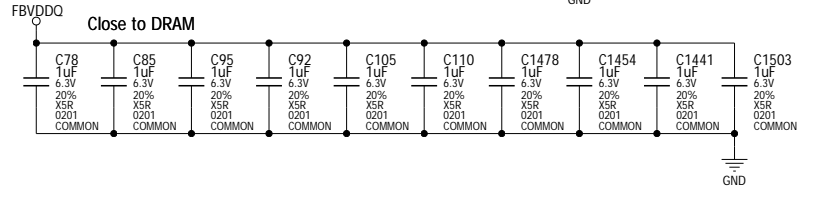
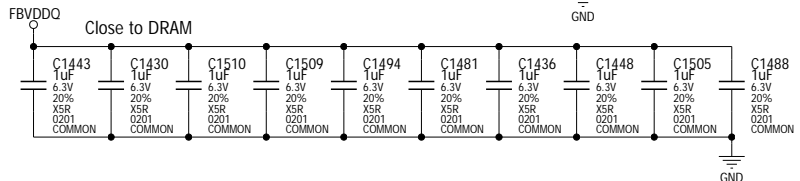
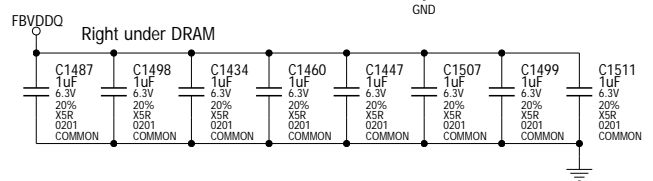
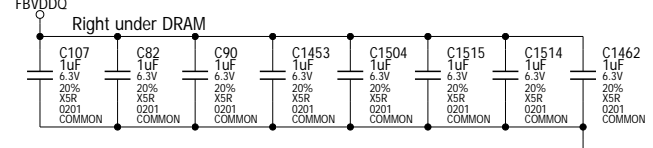
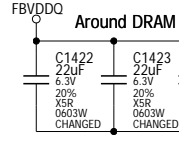
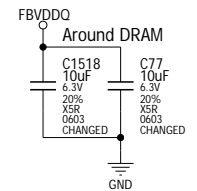
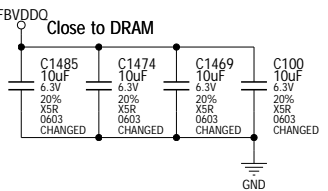
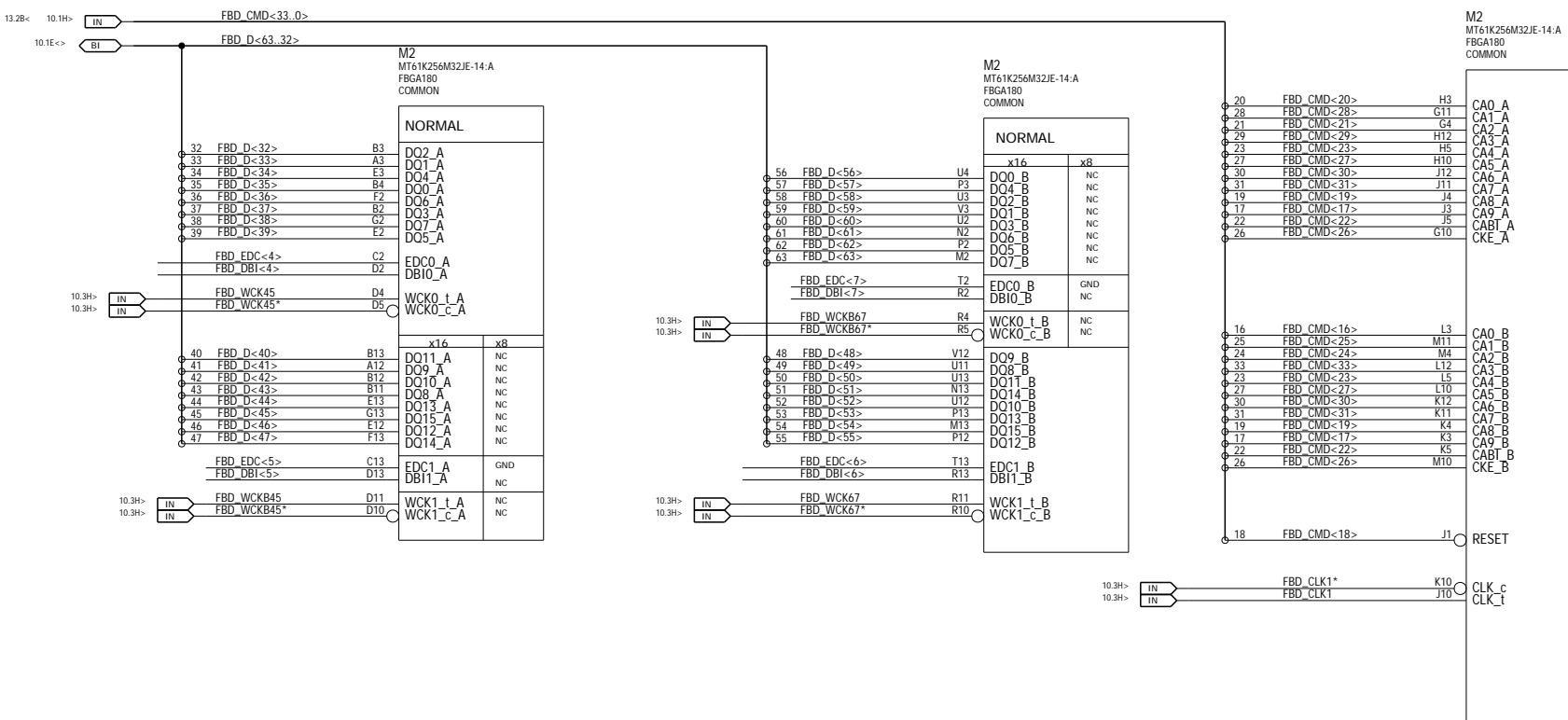
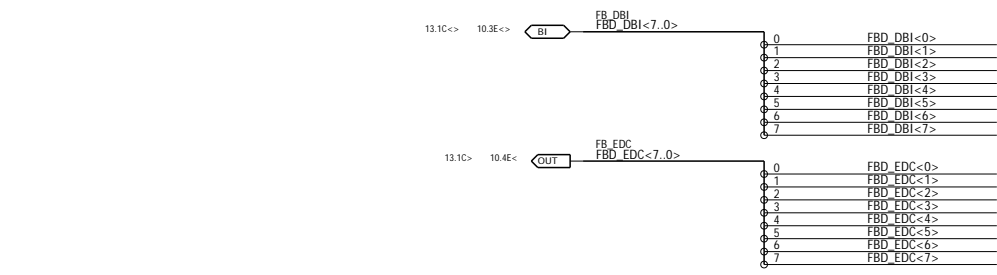
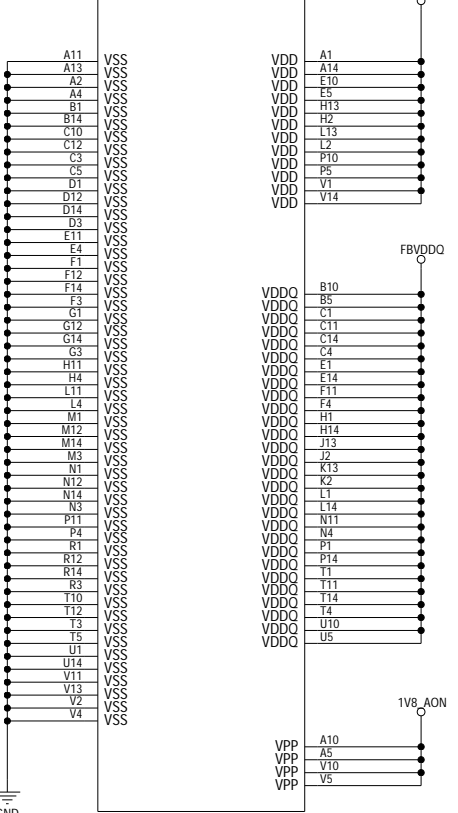
VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R62

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NV_PN	600-1G160-0042-700	
PCB REV	PG160-B03	PAGE 13 OF 53
BOM REV	F	DATE 12-NOV-2018

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PAGE DETAIL MEMORY: FBD[31..0]

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M2
MT61K256M32JE-14-A
FBGA180
COMMON

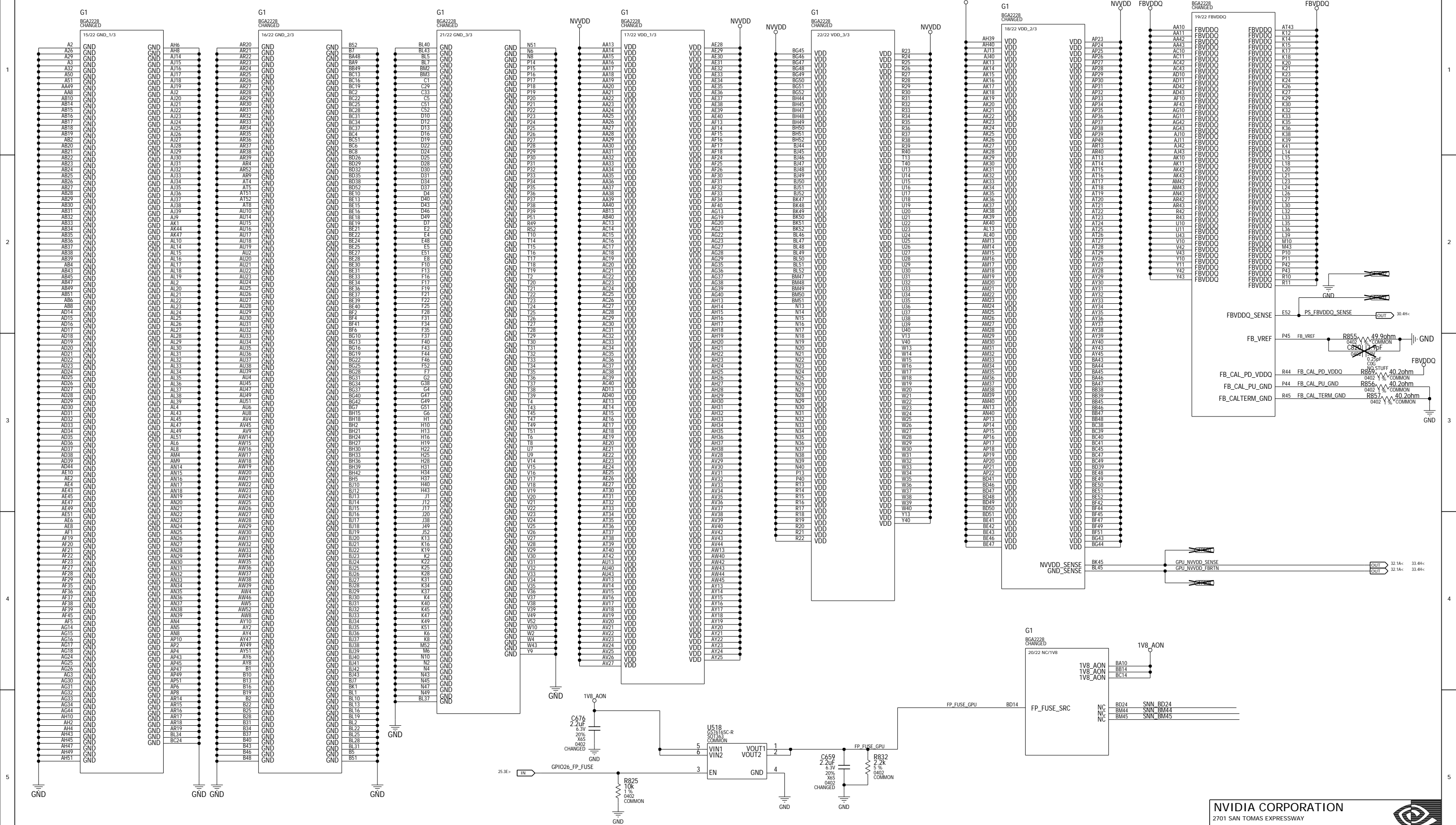


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PAGE DETAIL: MEMORY: FBD[63:32]

NV_PN: 600-1G160-0042-700
PCB REV: PG160-B03
BOM REV: F

REVISION HISTORY:
PAGE: 14 OF 53
DATE: 12-NOV-2018



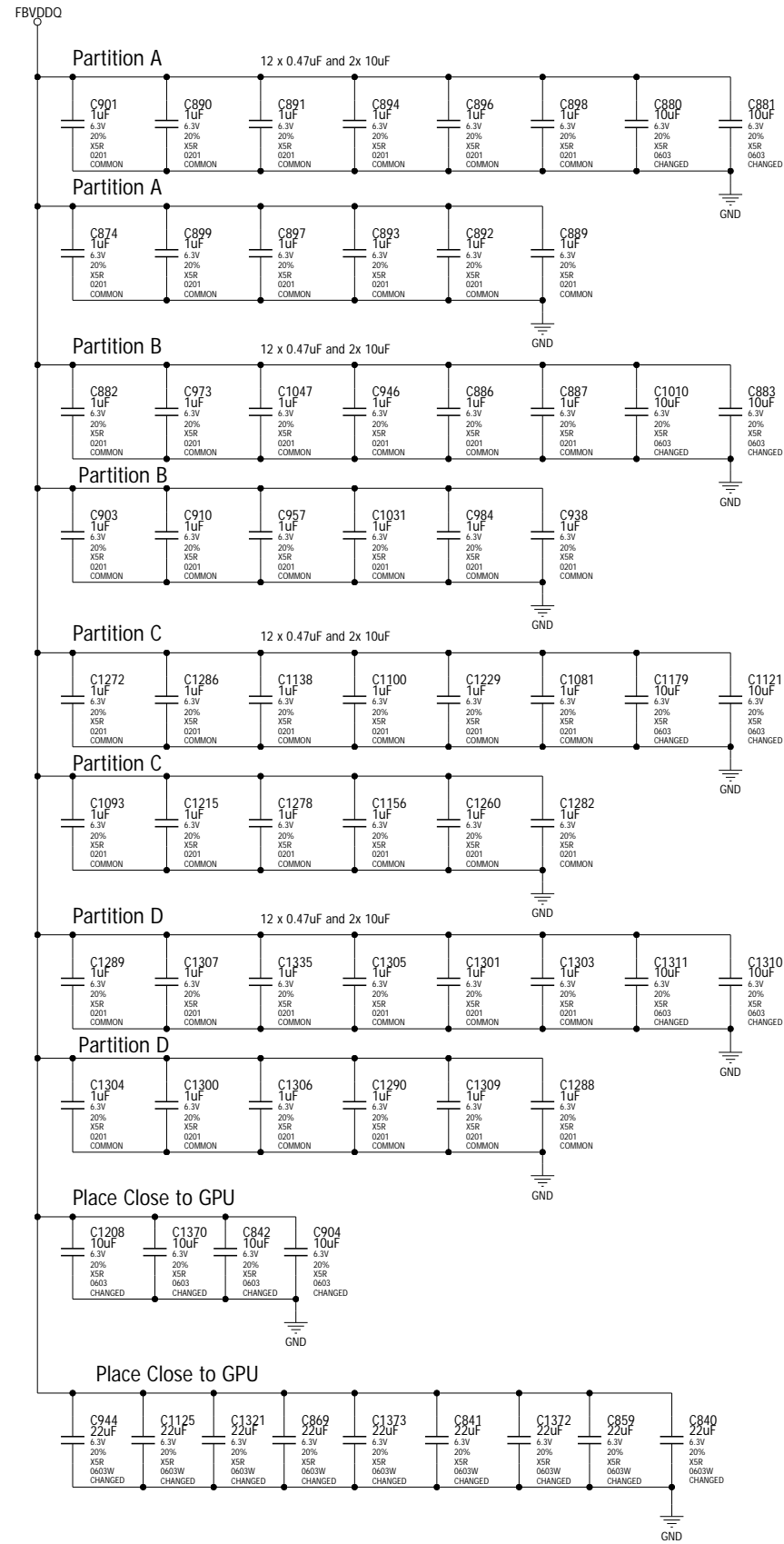
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NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F
PAGE	15 OF 53
DATE	12-NOV-2018

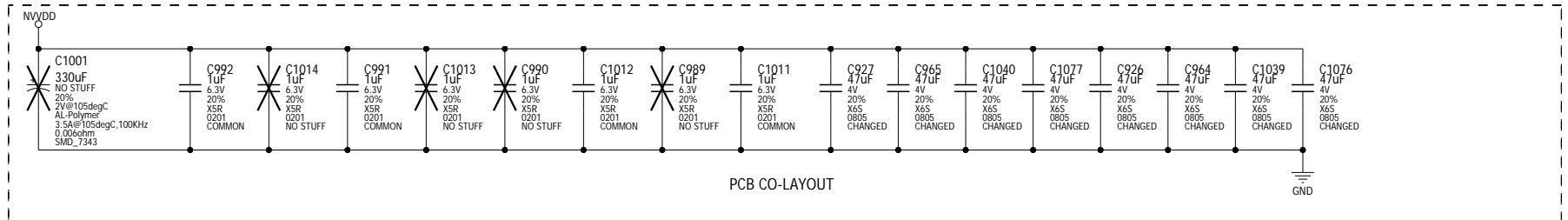
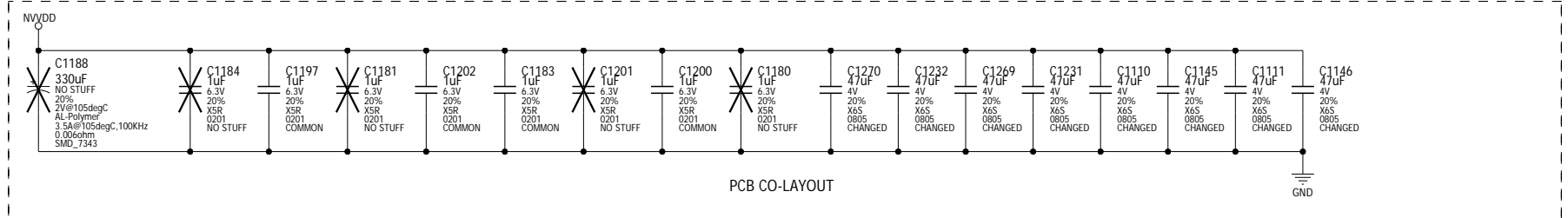
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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

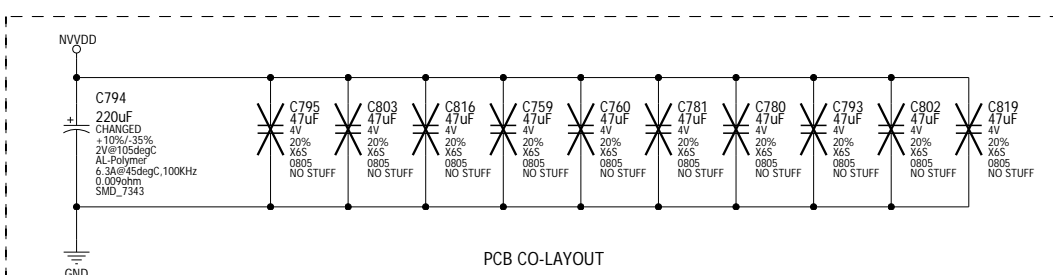
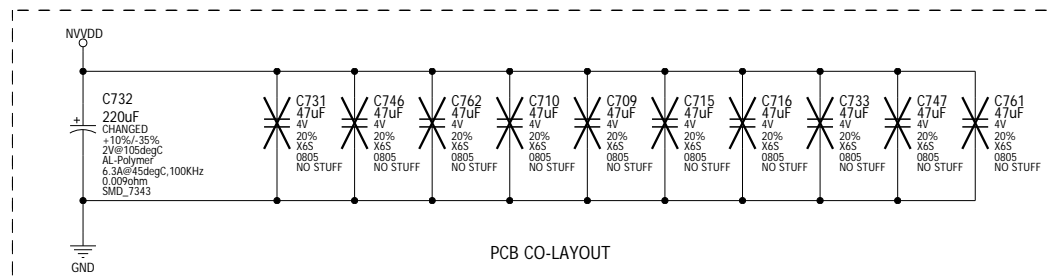
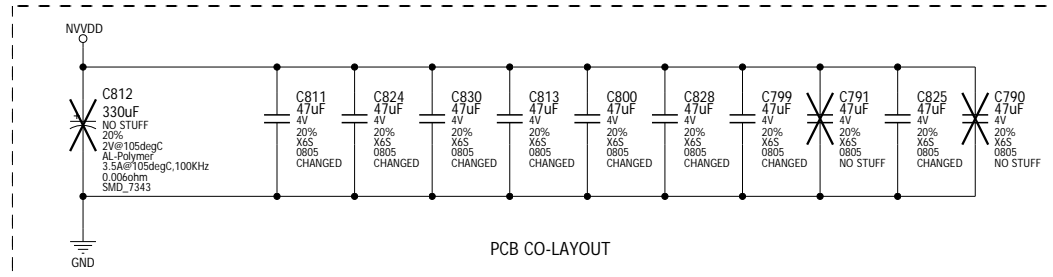
FBVDDQ



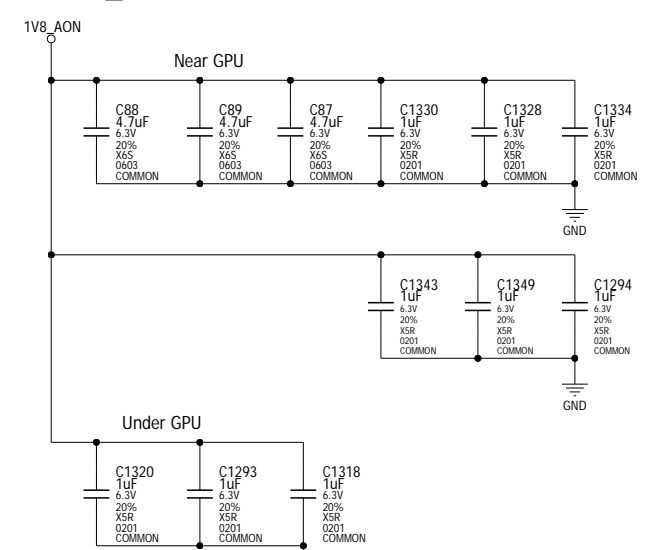
Under GPU



Near GPU



1V8_AON



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU Decoupling

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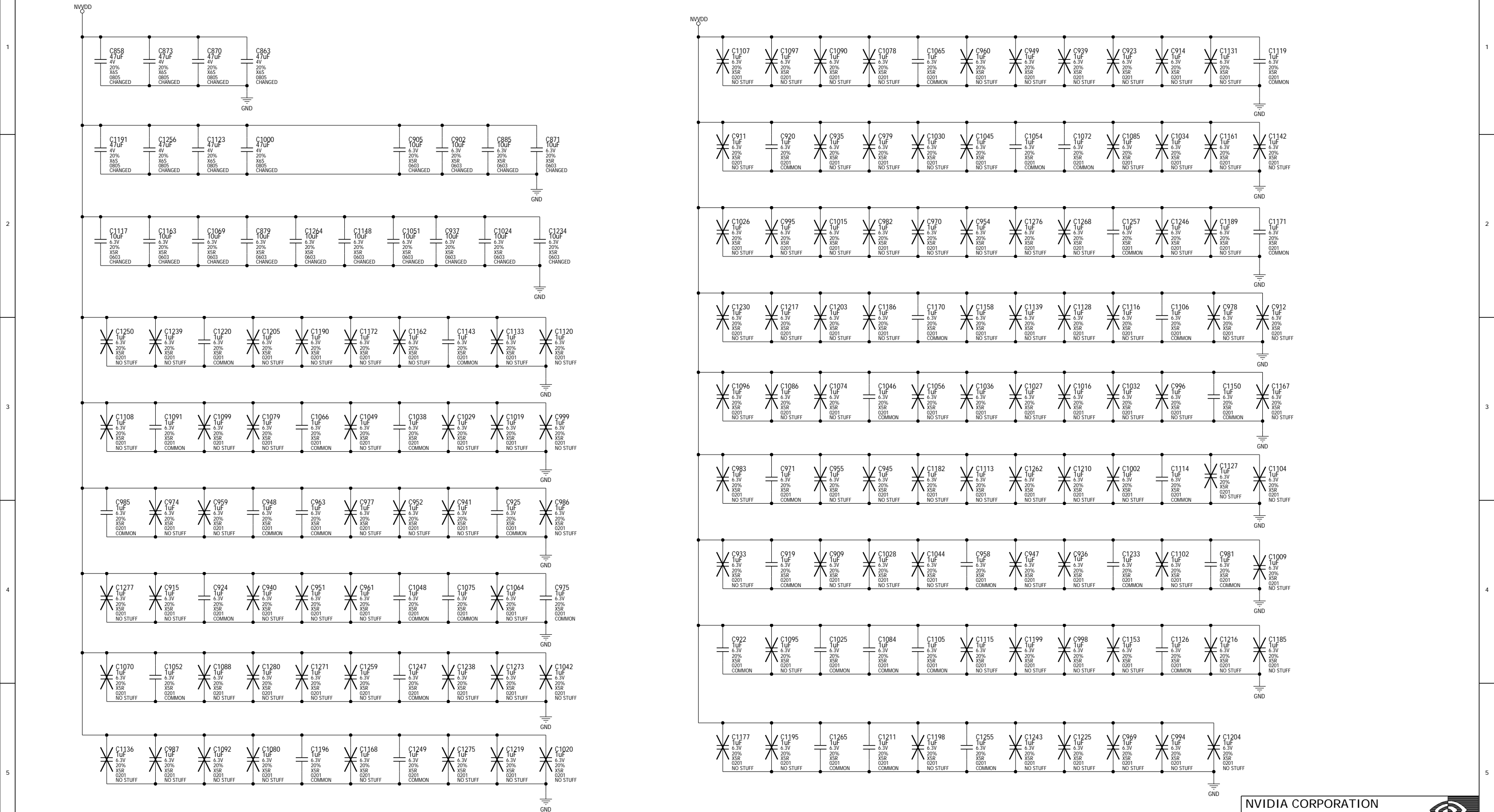
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NV_PN 600-1G160-0042-700

PCB REV	PG160-B03	PAGE	16 OF 53
BOM REV	F	DATE	12-NOV-2018

NVVDD



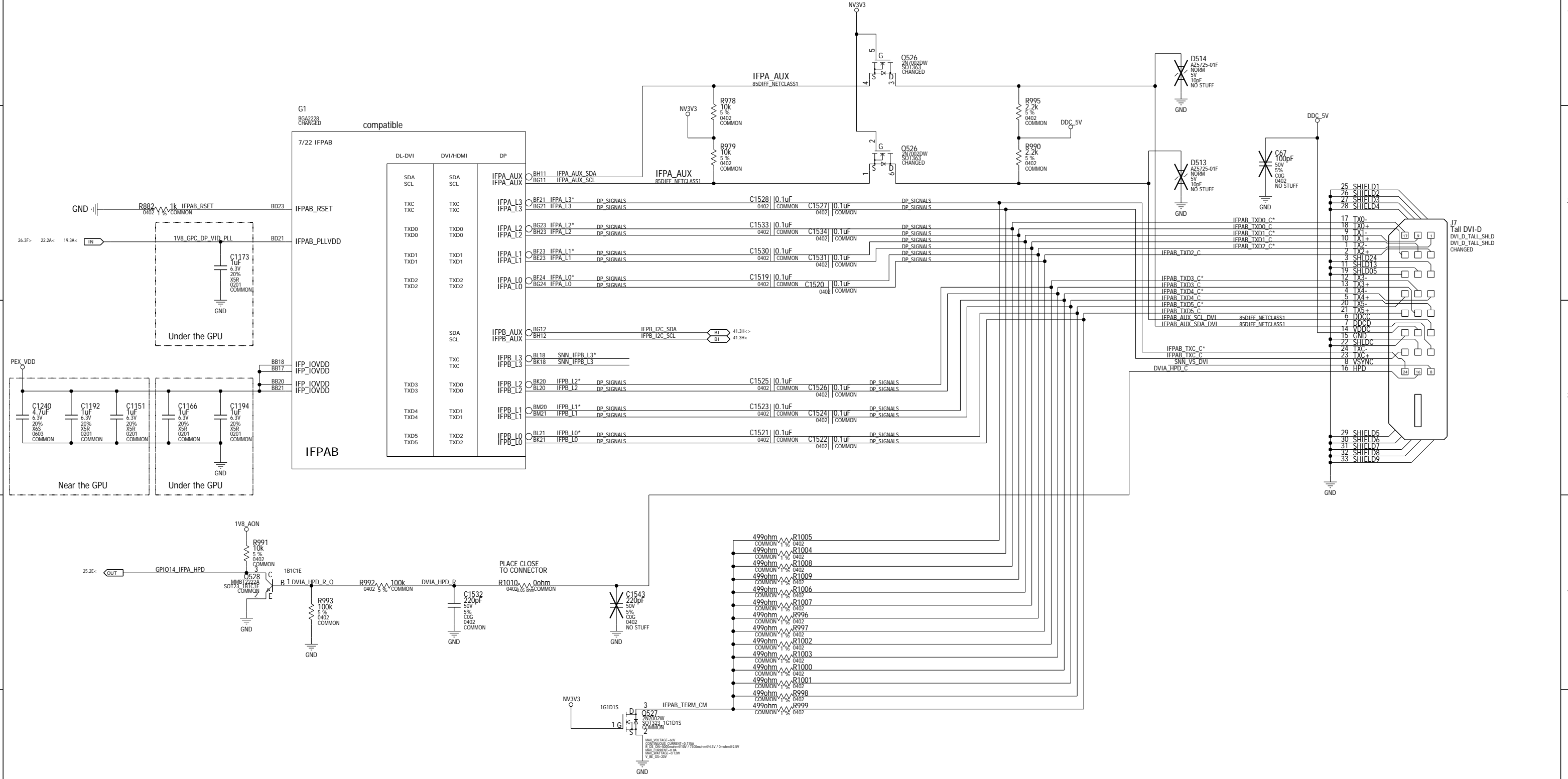
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PAGE DETAIL	GPU Decoupling2

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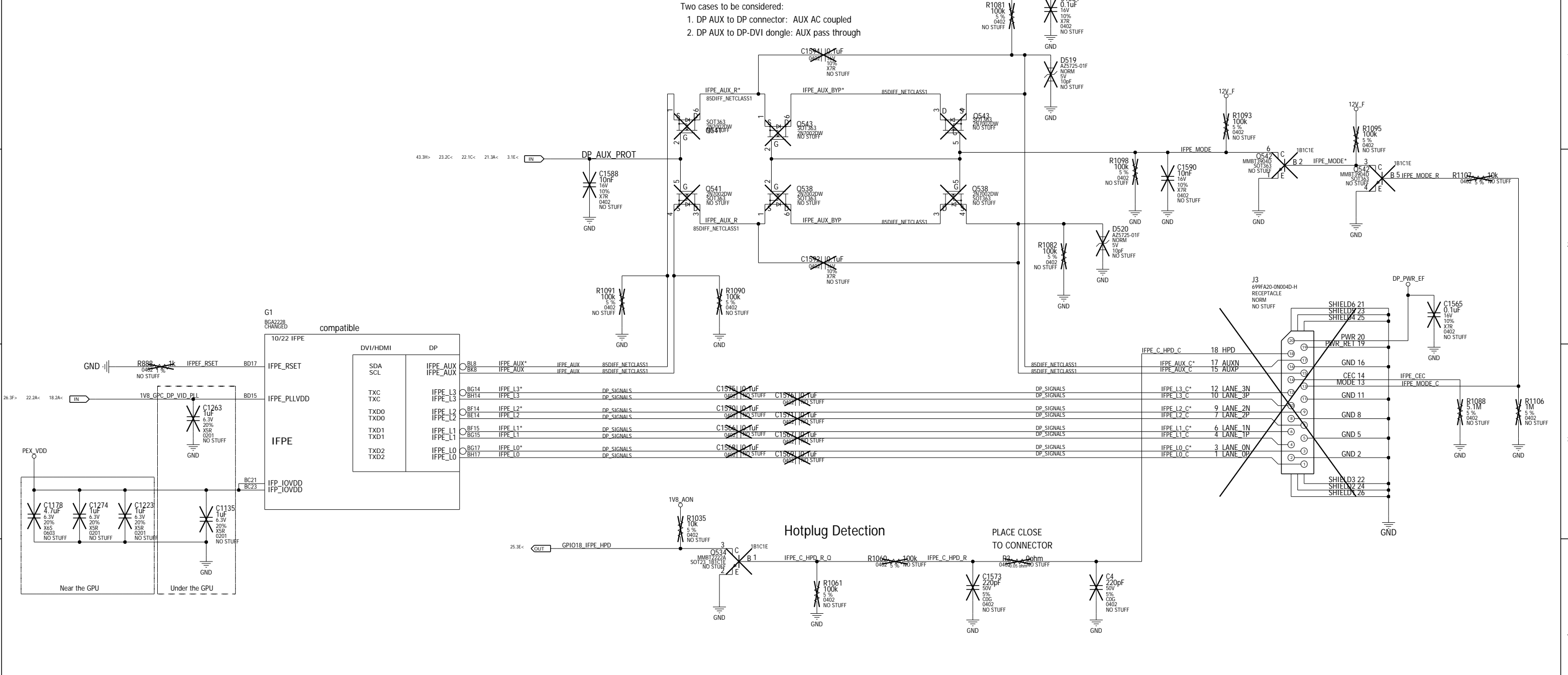
NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F

PAGE 17 OF 53
 DATE 12-NOV-2018

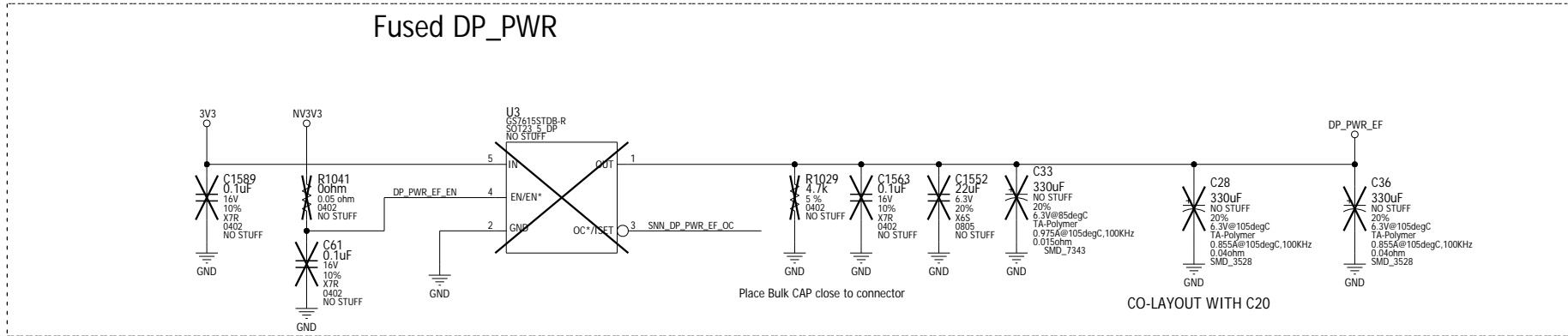
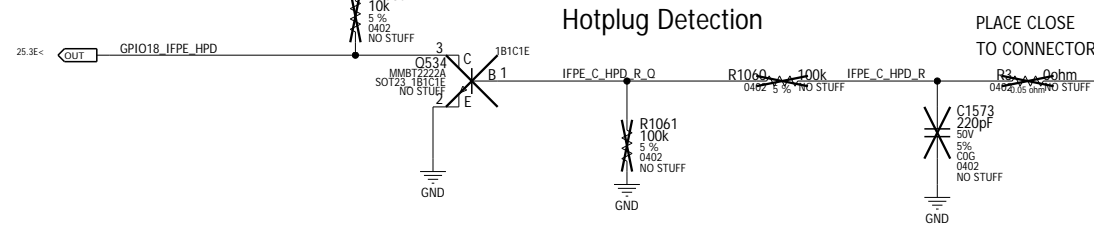
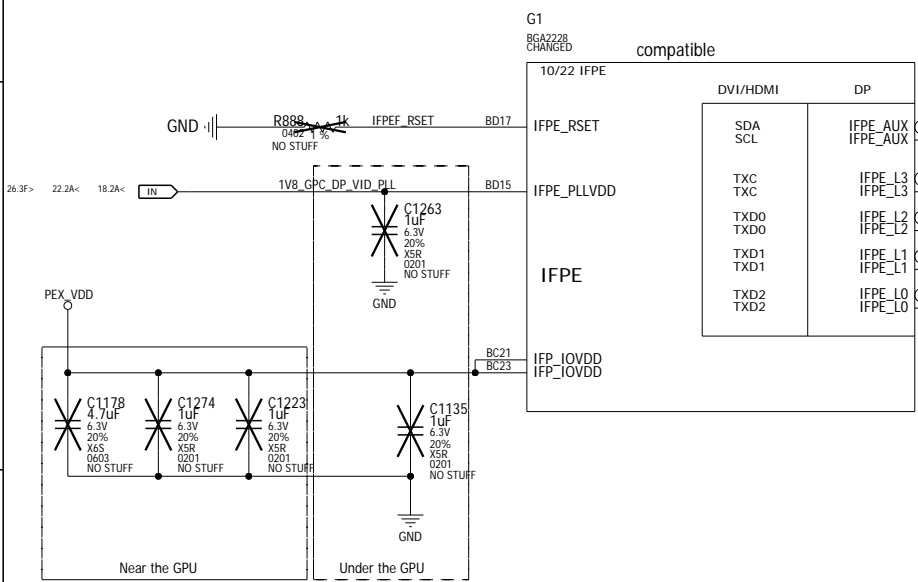
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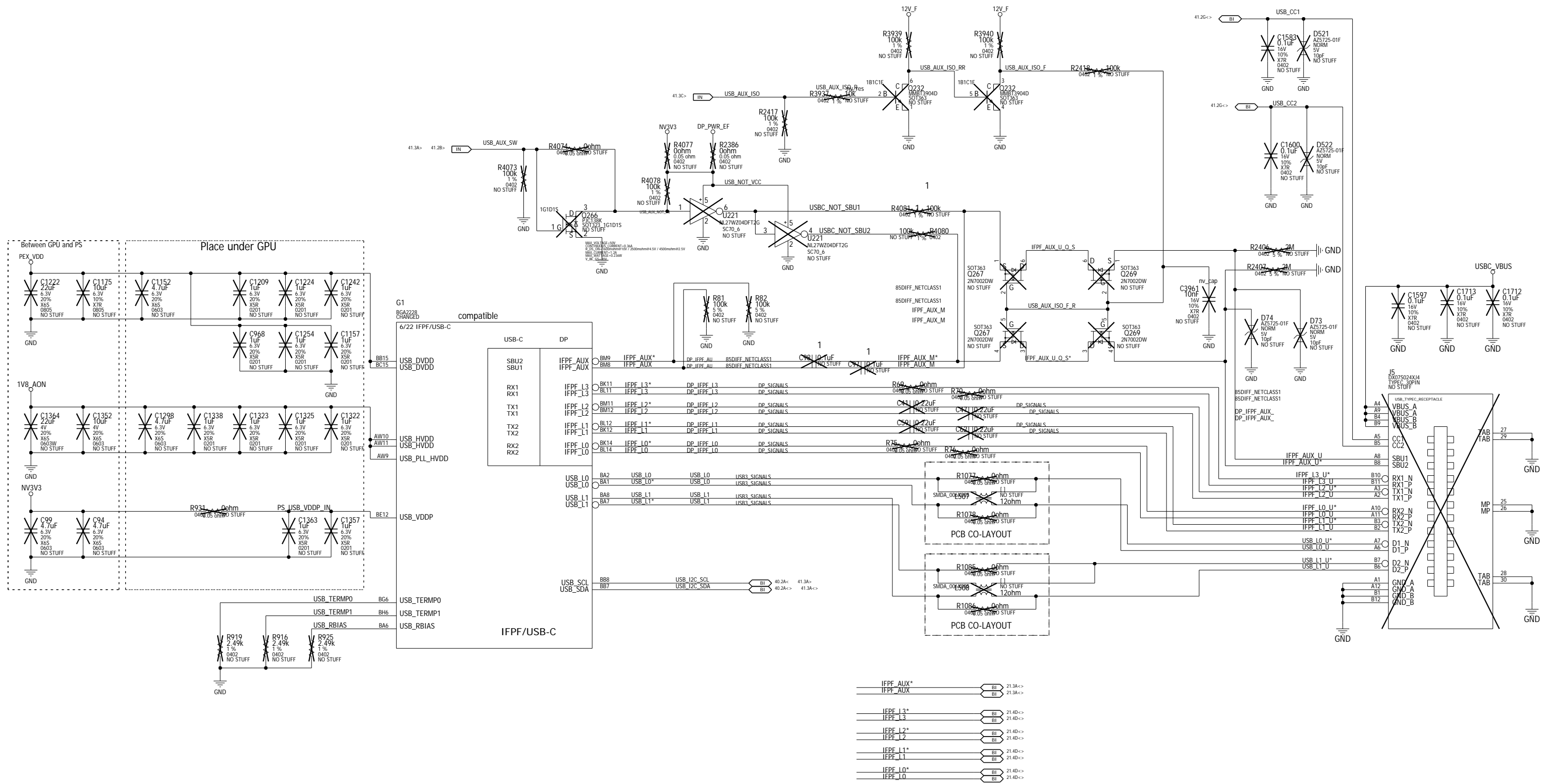
Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



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NV_PN	600-1G160-0042-700		
PCB REV	PG160-B03	PAGE	19 OF 53
BOM REV	F	DATE	12-NOV-2018

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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL IO: IFPE DP



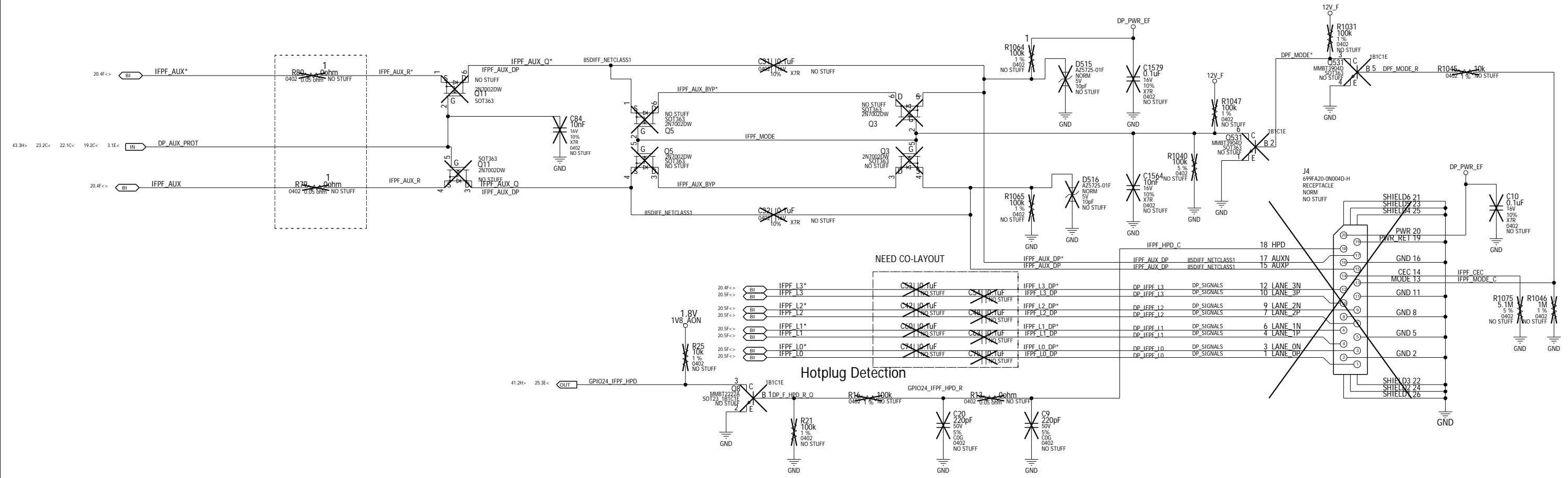
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 PCB REV: PG160-B03
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PAGE: 20 OF 53
 DATE:

ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

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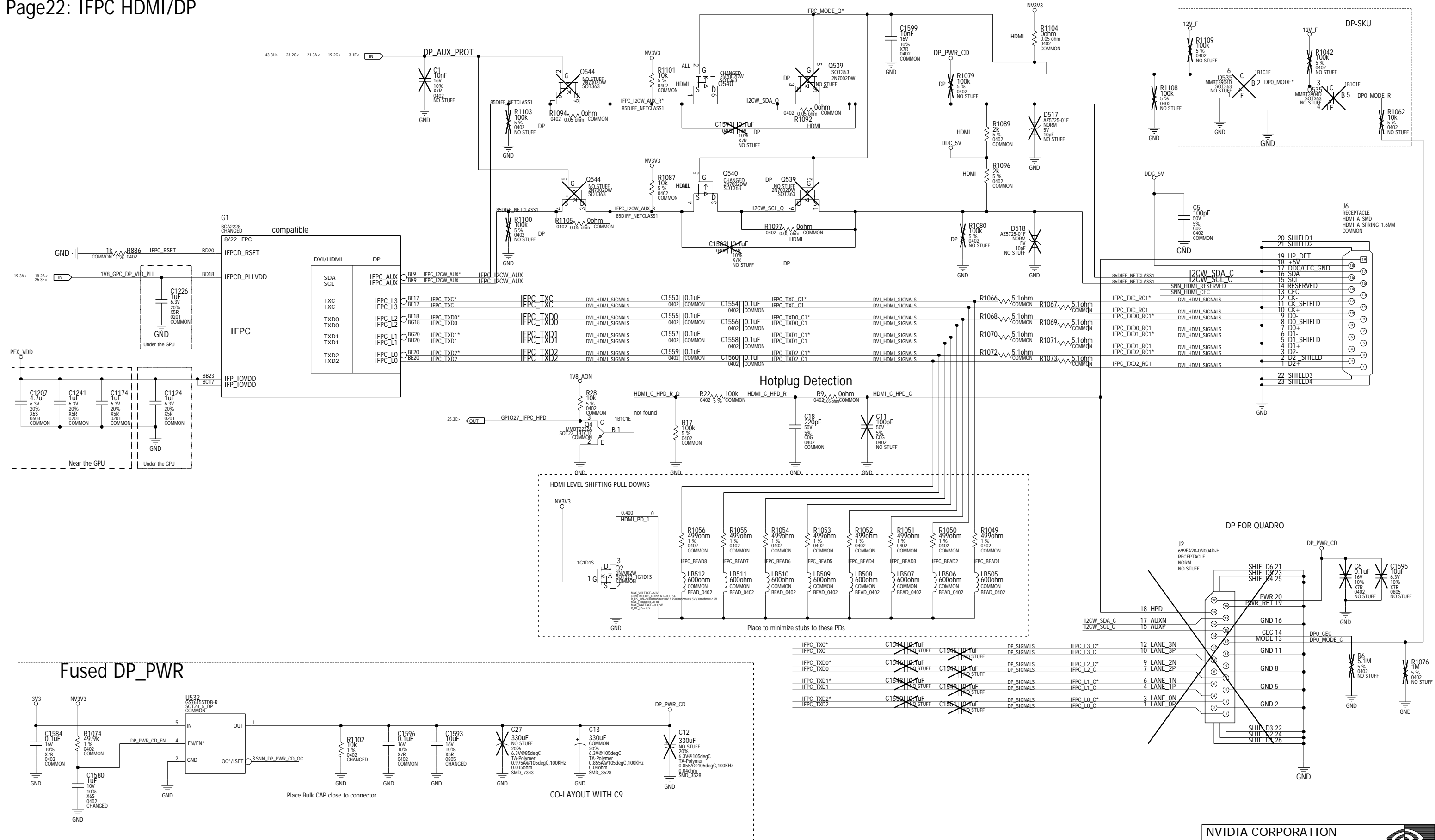
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IO: IFPF DP

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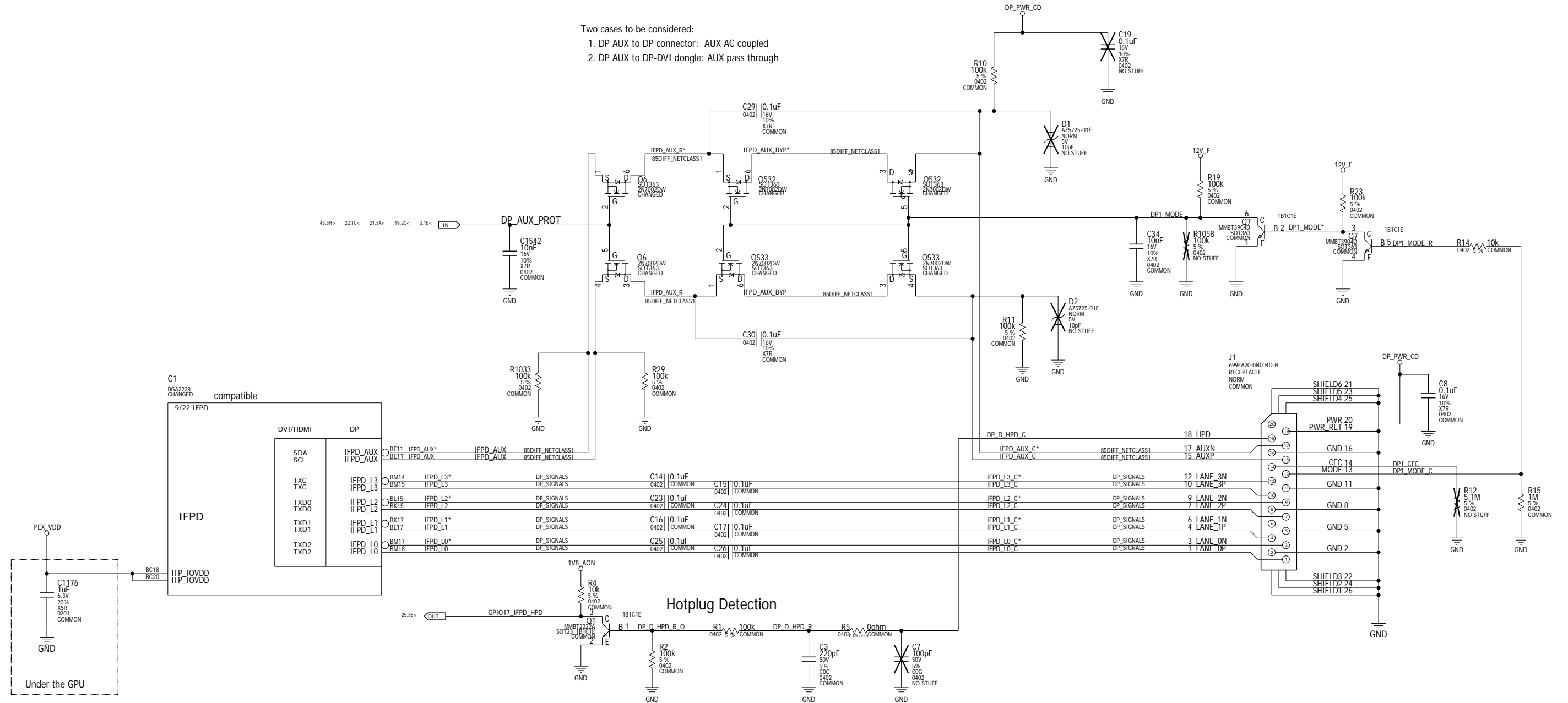
NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F

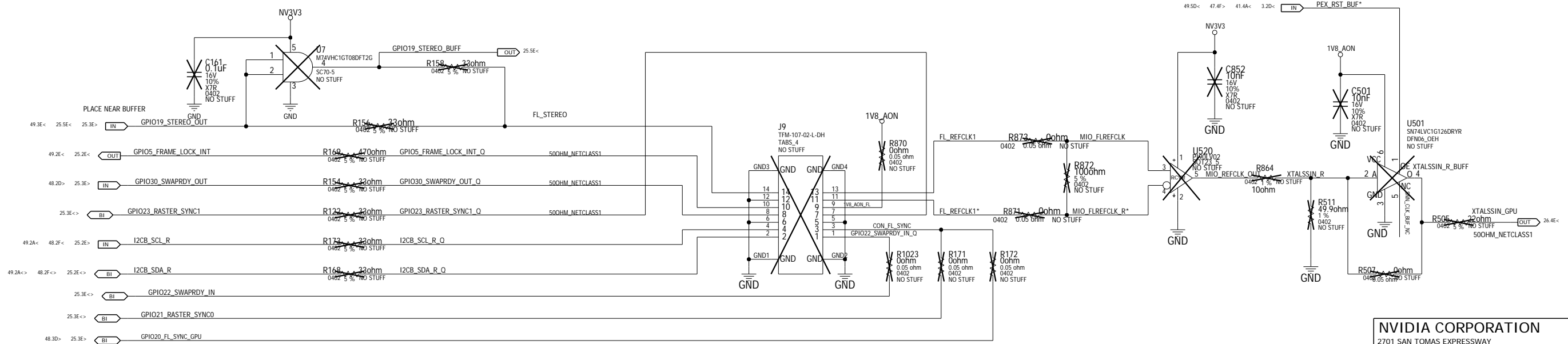
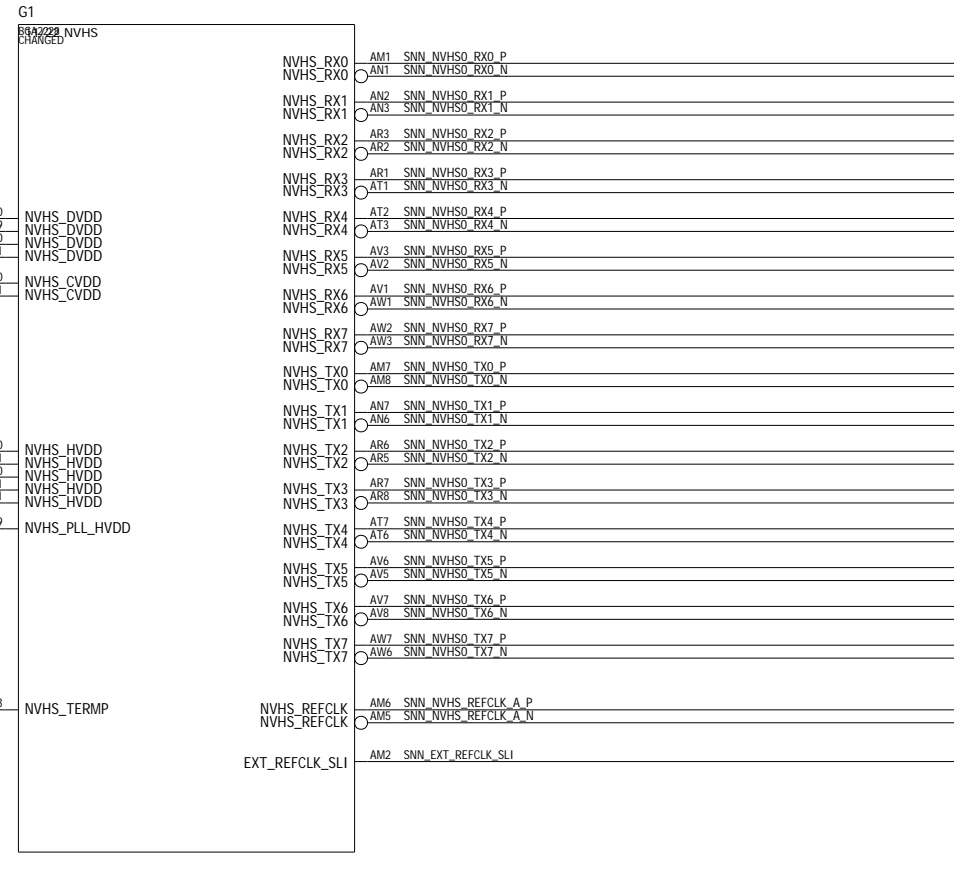
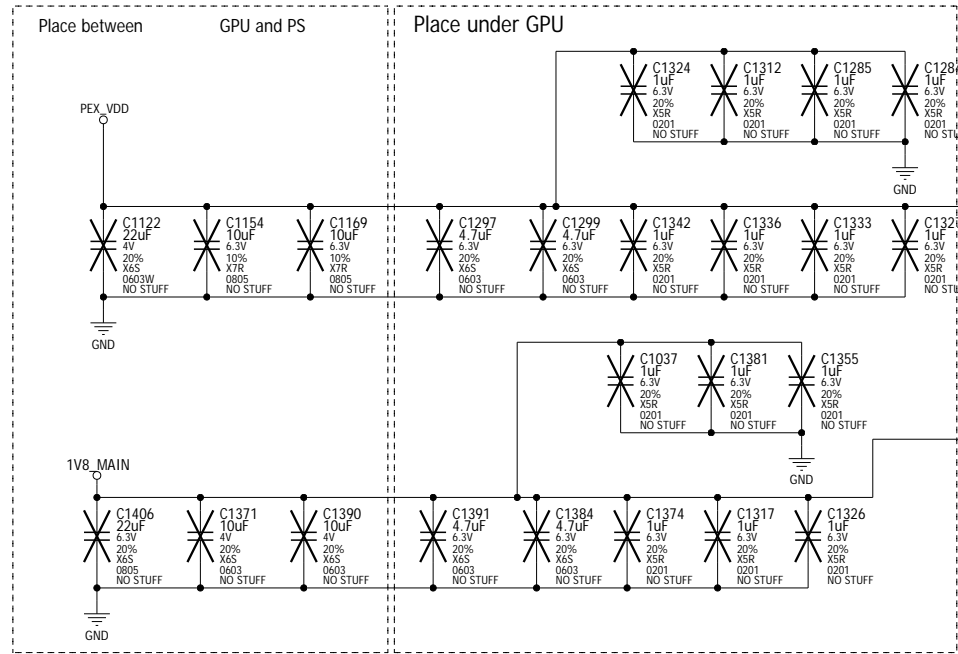
PAGE 21 OF 53
 DATE 12-NOV-2018



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- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

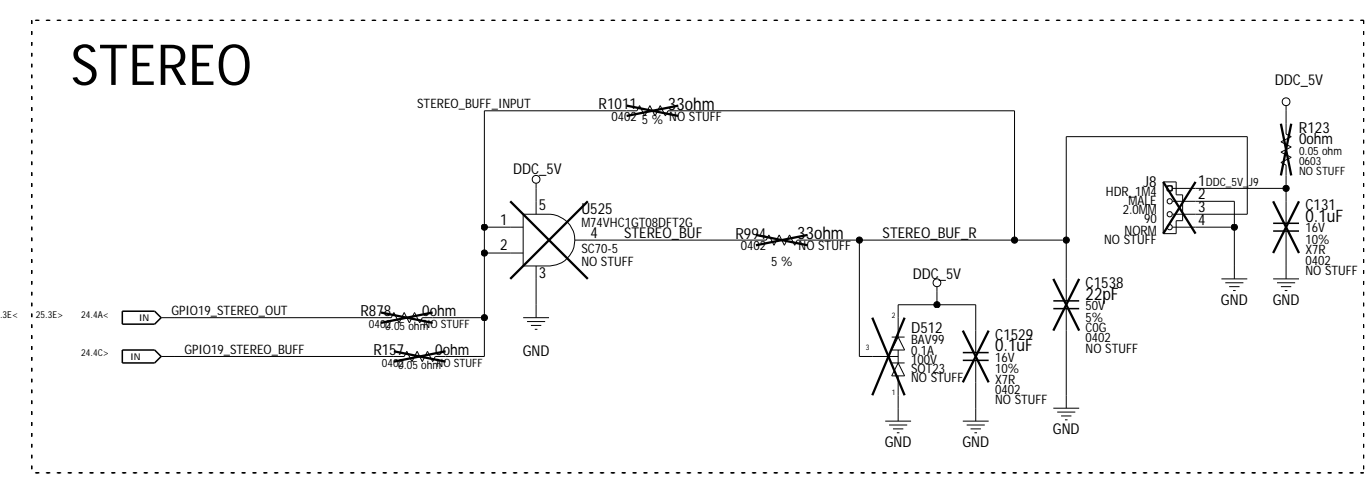
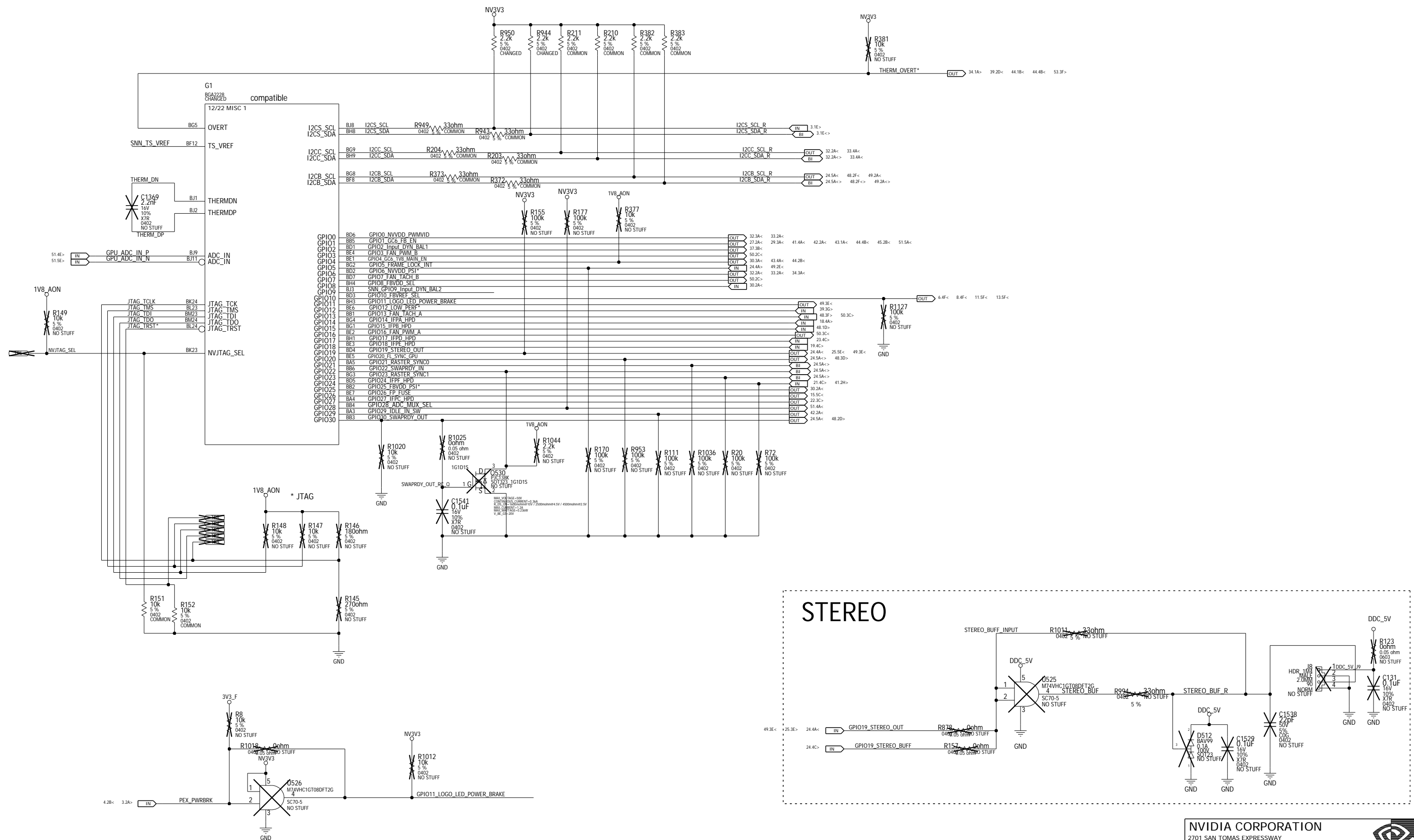




ASSEMBLY		BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL	
PAGE DETAIL		IO: NVHS Interface and Frame Lock	
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PCB REV	PG160-B03	PAGE	24 Of 53
BOM REV	F	DATE	12-NOV-2018

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PAGE DETAIL	MISC1: Thermal, JTAG, GPIO, STEREO

Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

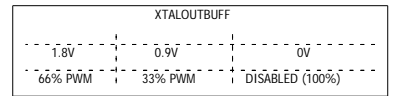
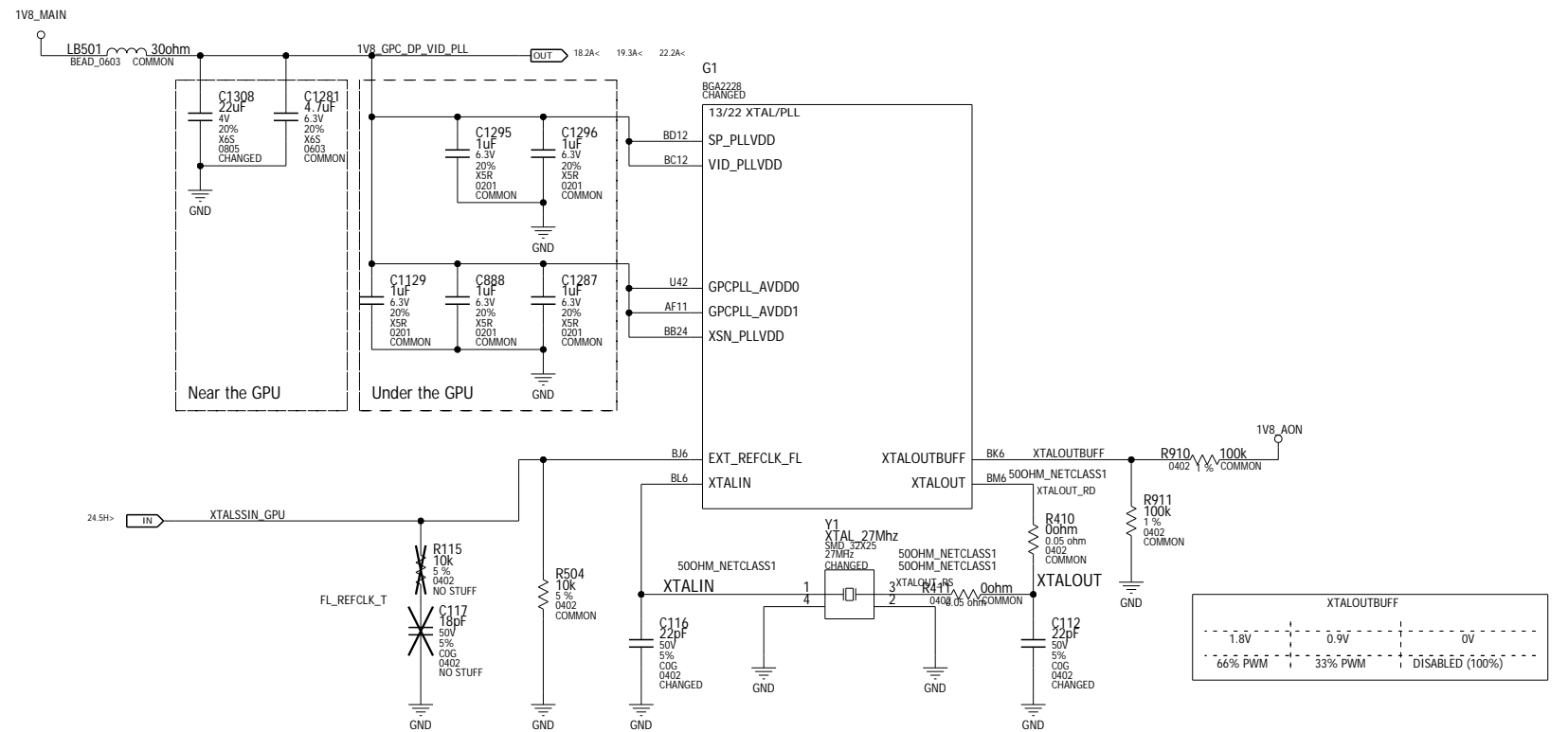
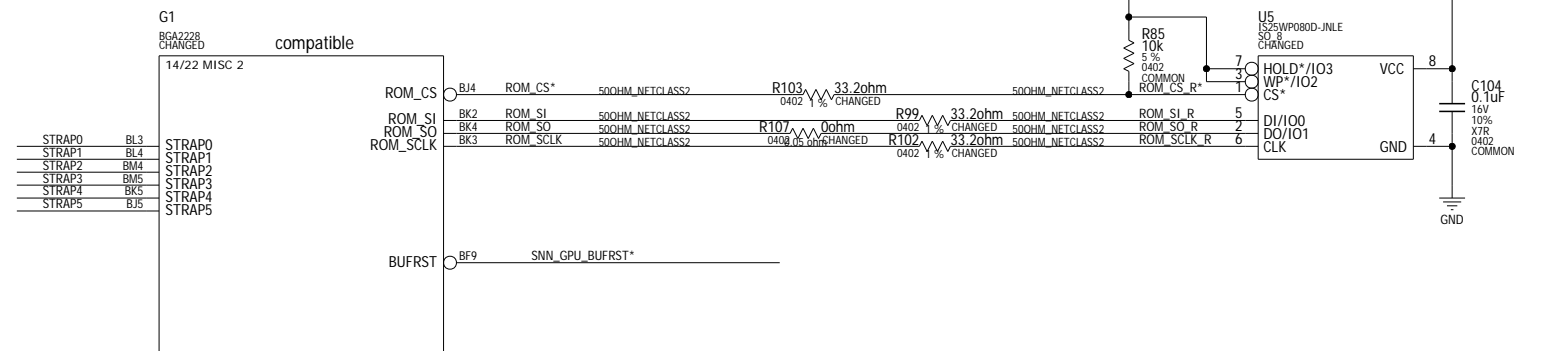
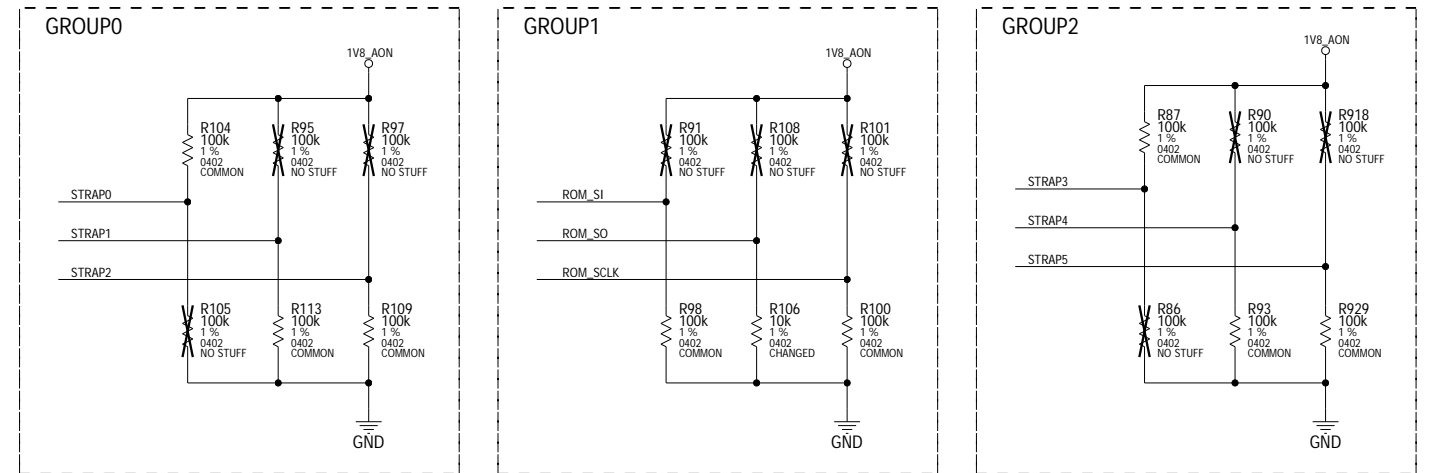
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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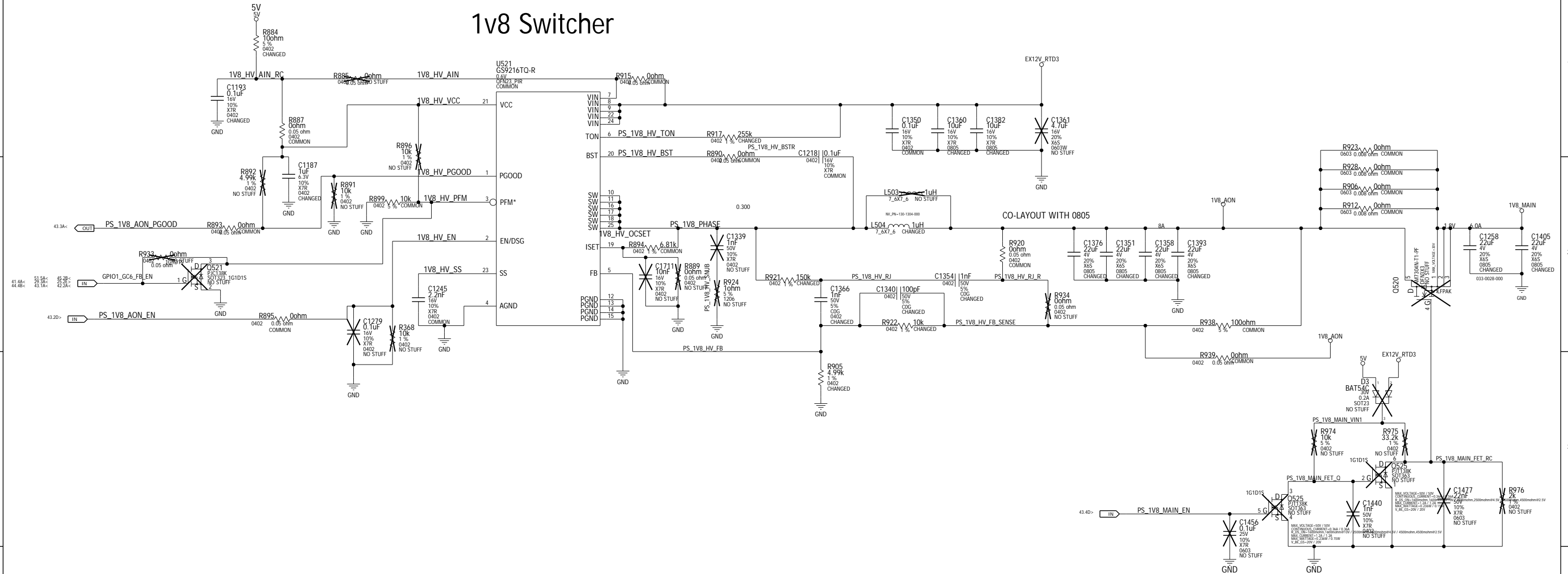
NV_PN 600-1G160-0042-700

PCB REV PG160-B03 PAGE 26 OF 53
BOM REV F DATE 12-NOV-2018

ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL MISC2: ROM, XTAL, STRAPS

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1v8 Switcher

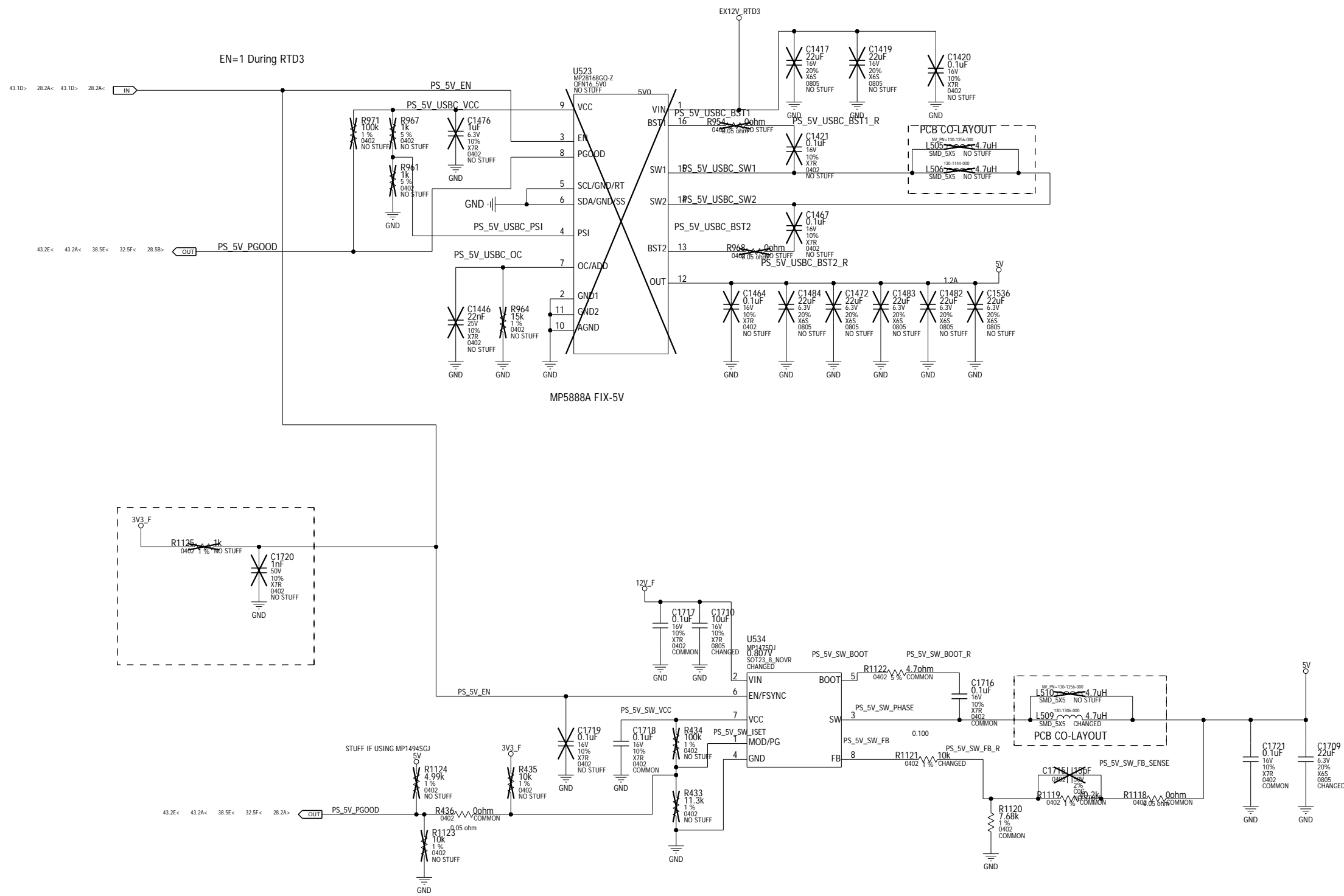


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PAGE DETAIL	PS: 1V8_PLL, 1V8_AON

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SANTA CLARA, CA 95050, USA		PAGE 27 OF 53	
NV_PN	600-1G160-0042-700	DATE	12-NOV-2018
PCB REV	PG160-B03		
BOM REV	F		





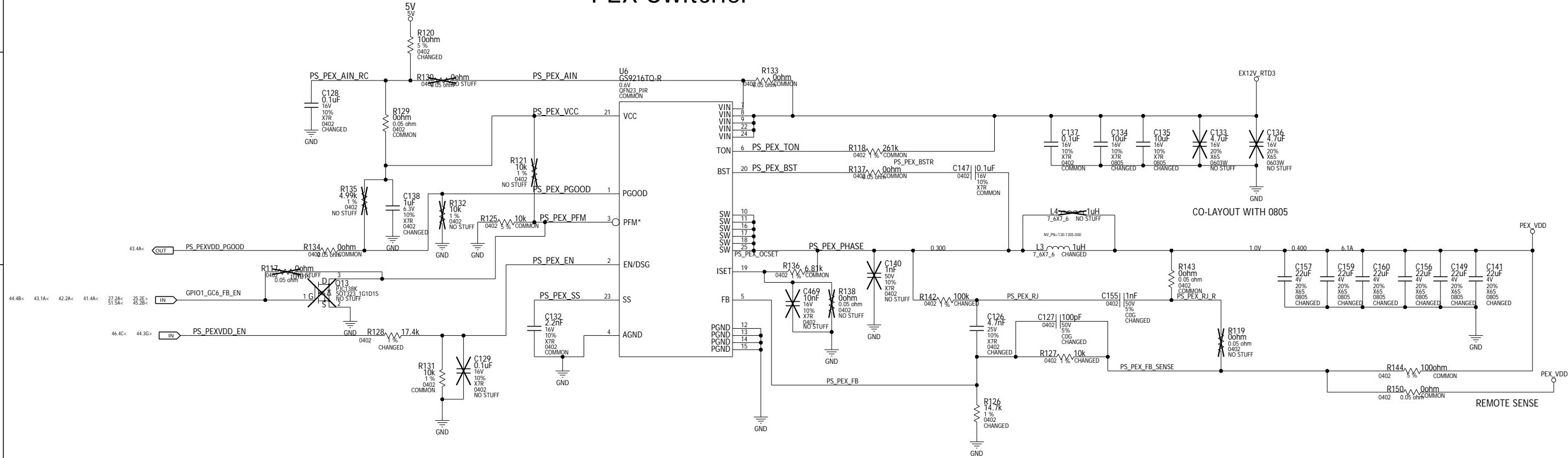
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PAGE DETAIL	PS: 5V

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NV_PN	600-1G160-0042-700		
PCB REV	PG160-B03	PAGE	28 OF 53
BOM REV	F	DATE	12-NOV-2018

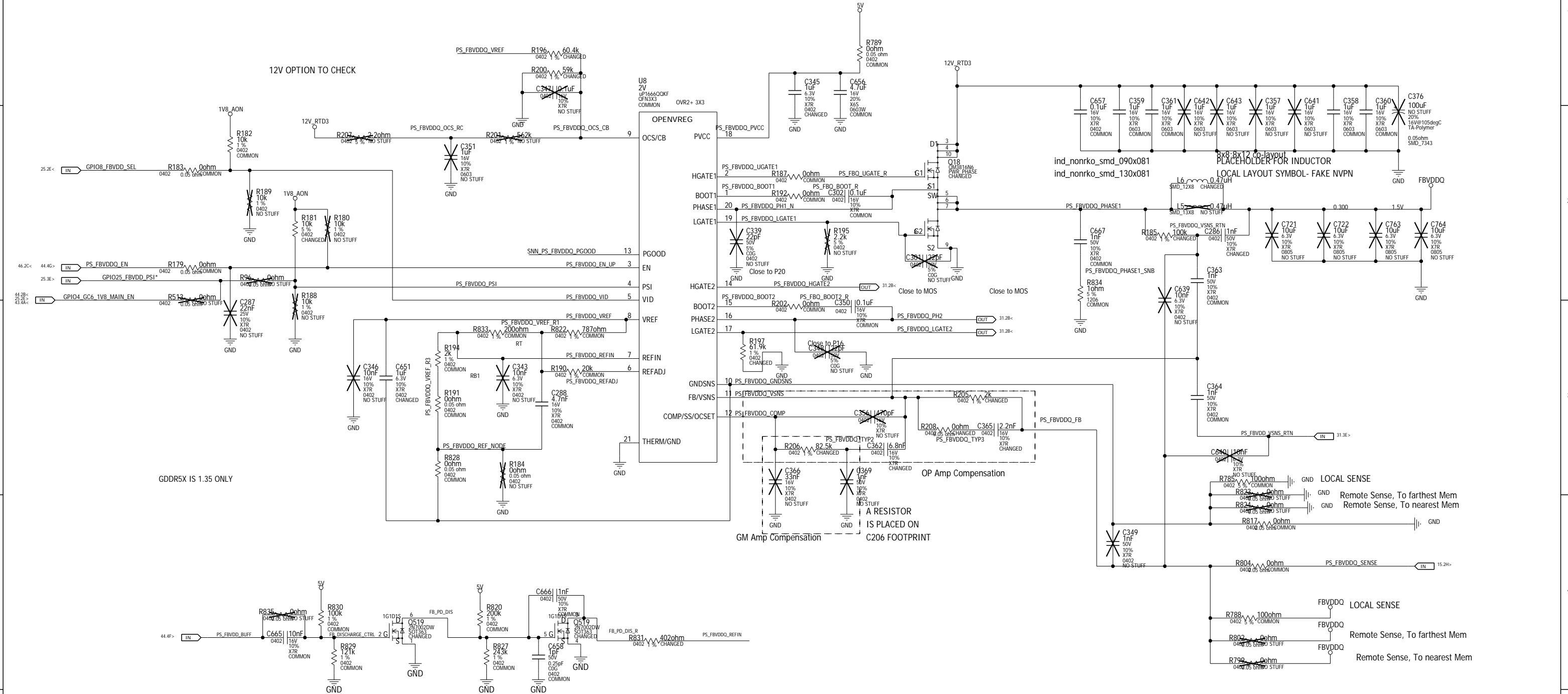
PEX Switcher



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NV_PN	600-1G160-0042-700	PAGE	29 OF 53		
PCB REV	PG160-B03	DATE	12-NOV-2018		
BOM REV	F				

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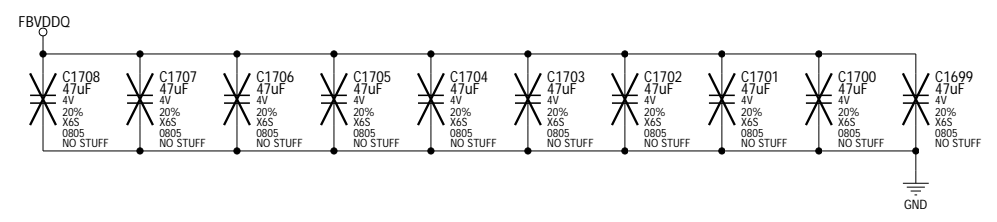
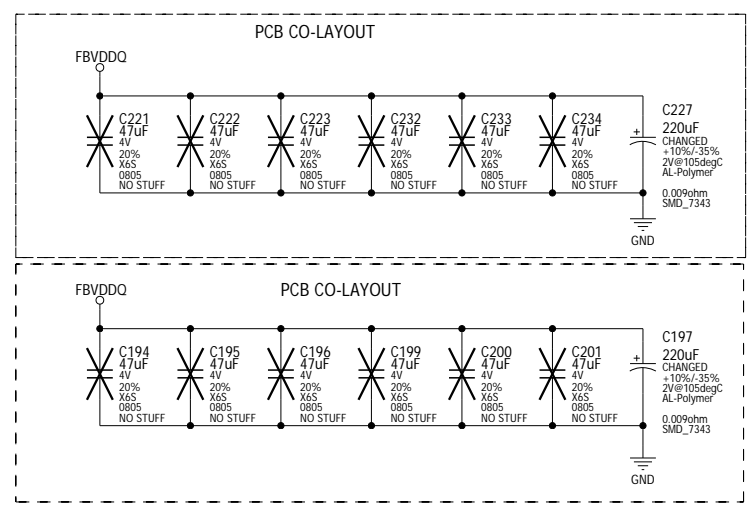
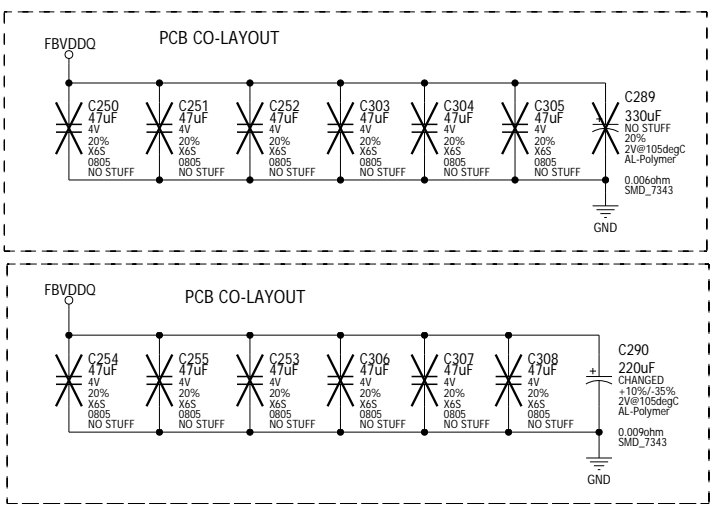
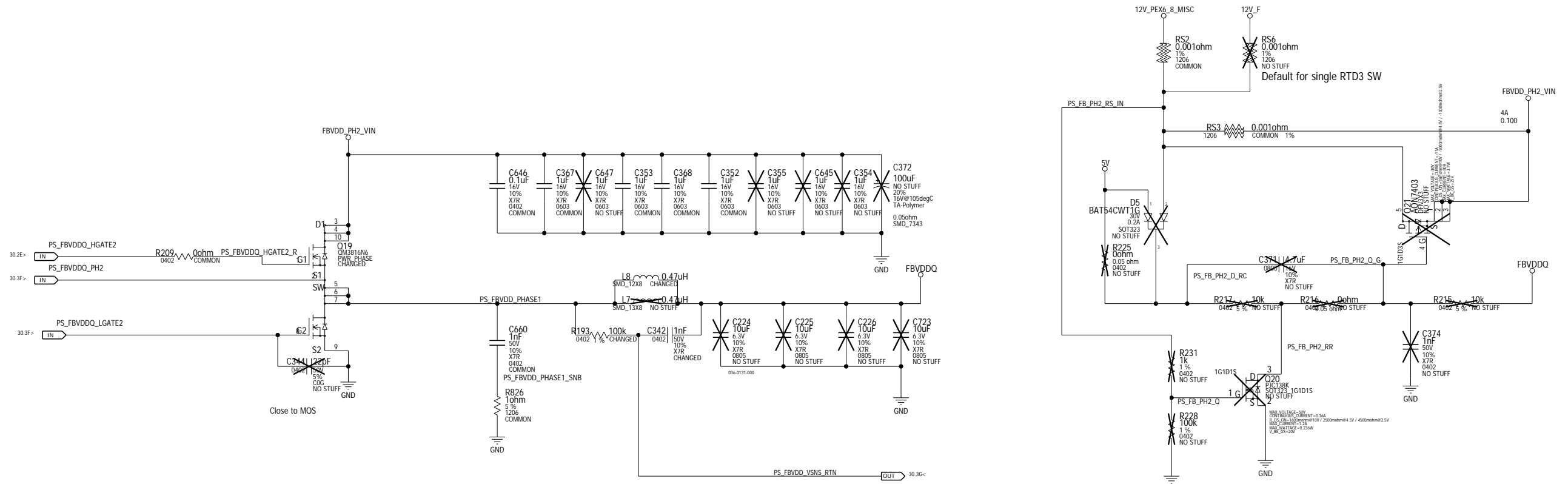


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 PCB REV: PG160-B03
 BOM REV: F

PAGE: 30 OF 53
 DATE: 12-NOV-2018

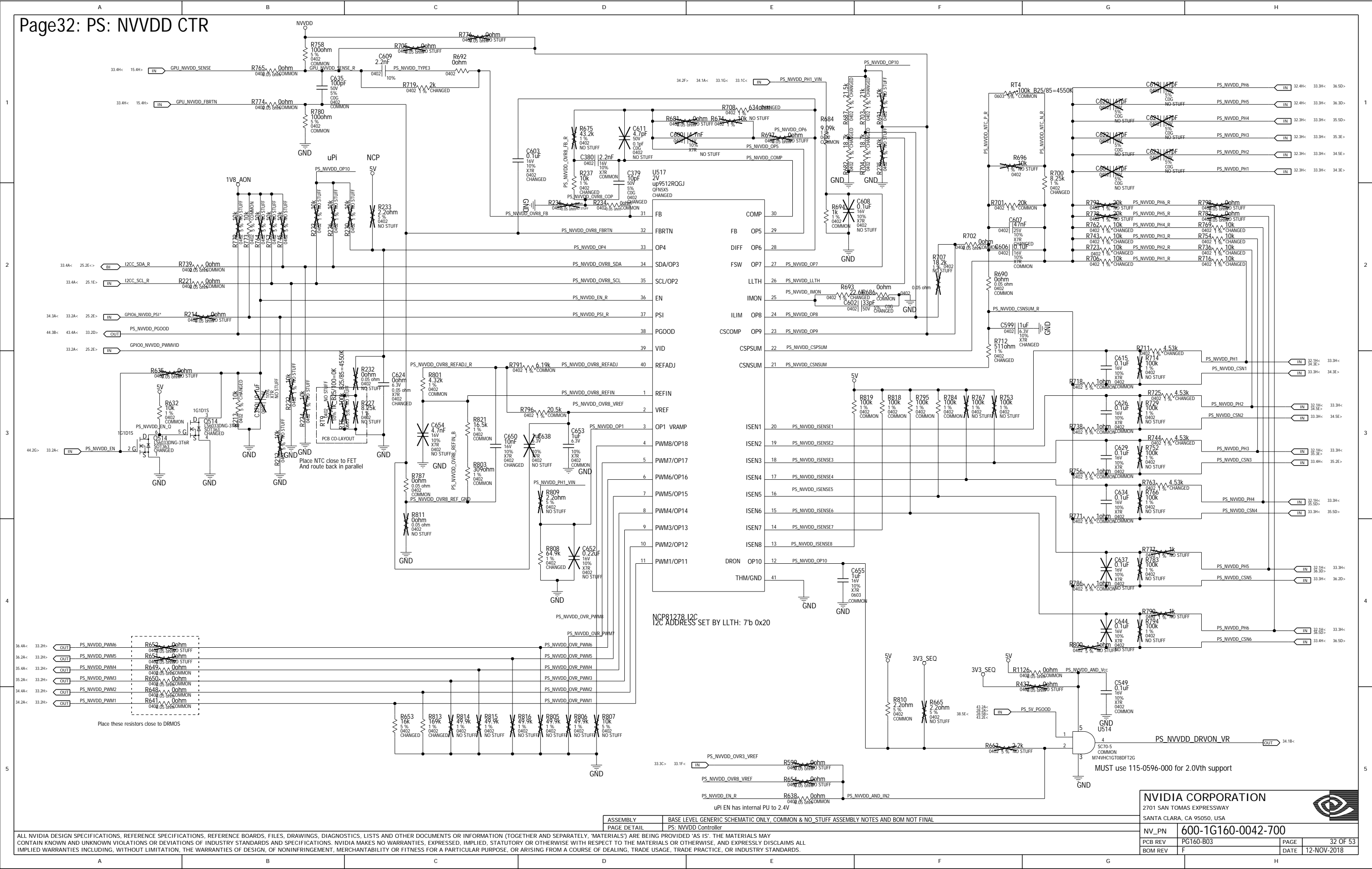
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PAGE DETAIL	PS: FBVDDQ



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PAGE DETAIL		PS: FBVDDQ PH2	
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PCB REV	PG160-B03	PAGE	31 OF 53
BOM REV	F	DATE	12-NOV-2018

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NCP1278 I2C ADDRESS SET BY LLTH: 7'b 0x20

Place these resistors close to DRMOS

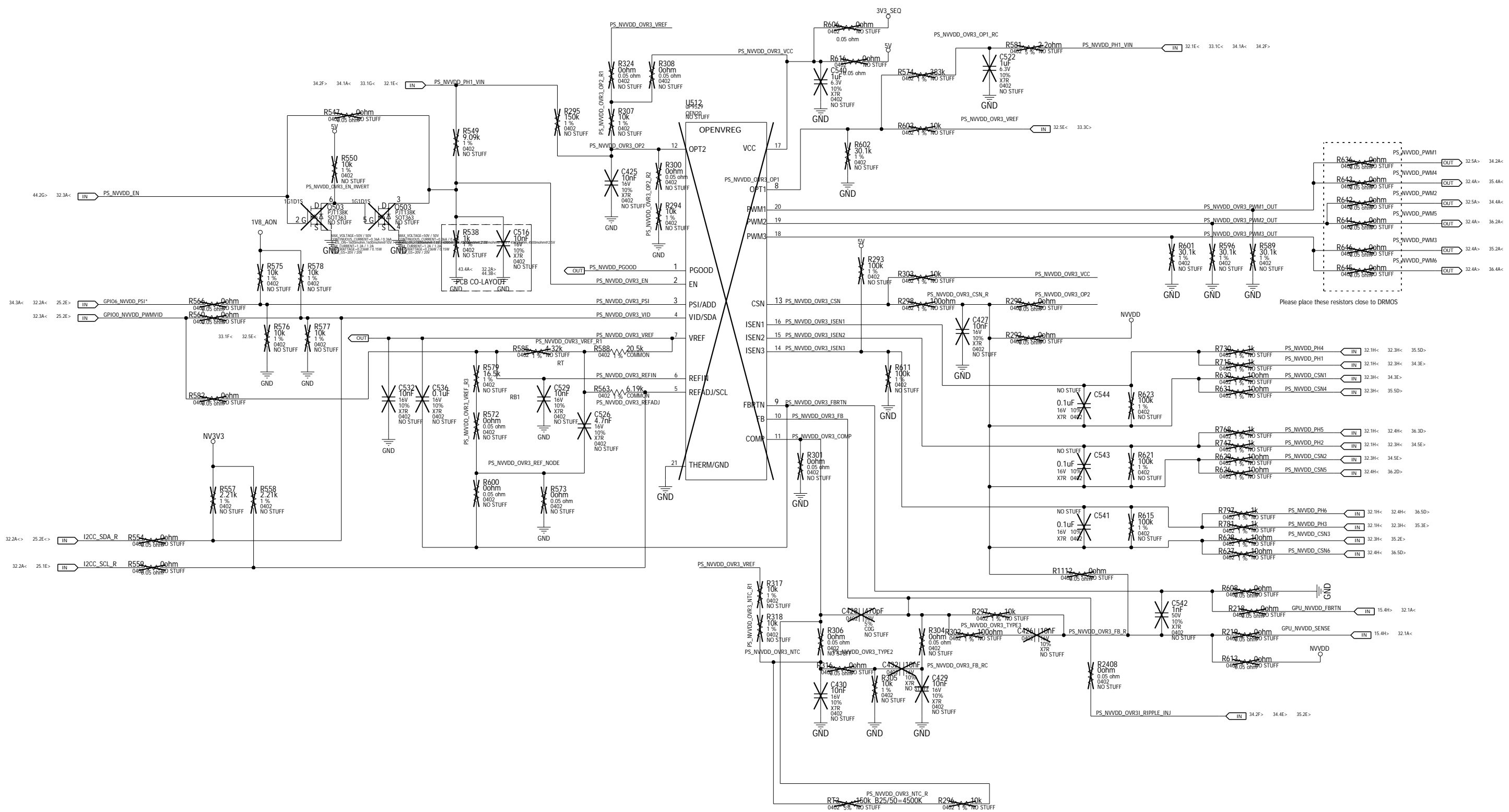
MUST use 115-0596-000 for 2.0Vth support

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD Controller

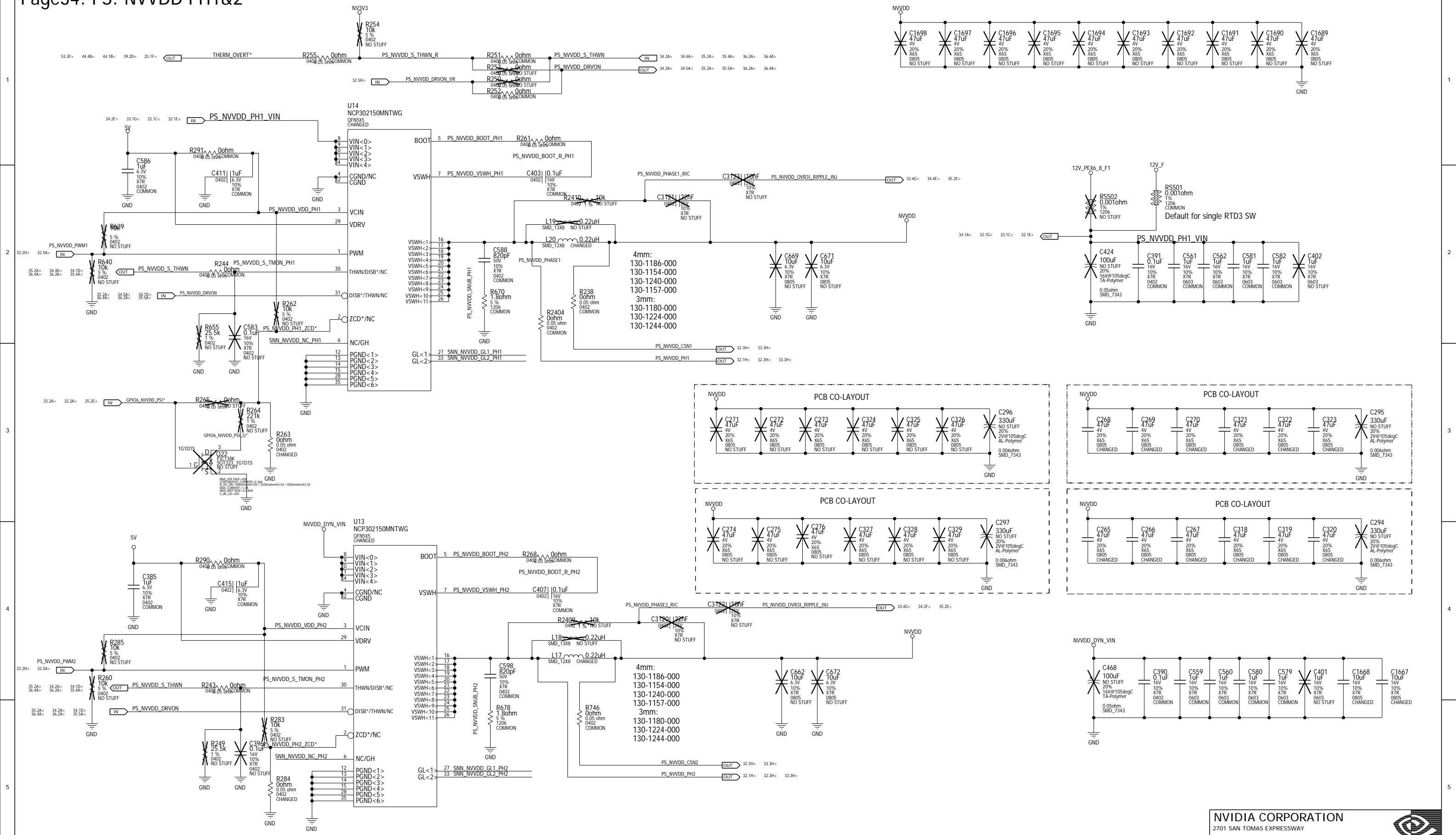
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BOM REV	F
PAGE	32 OF 53
DATE	12-NOV-2018



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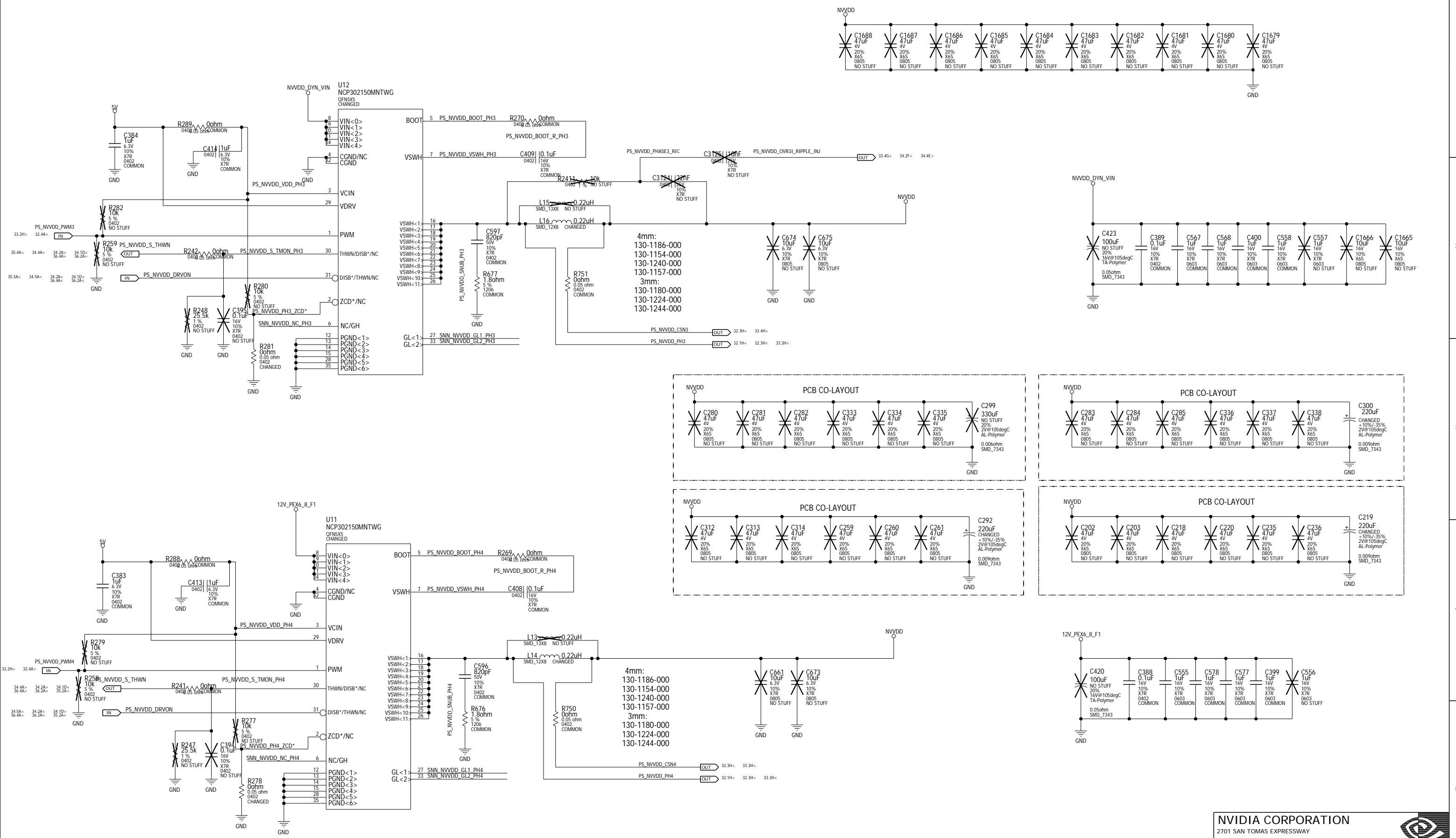
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PAGE DETAIL	PS: NVVDD Phase 1,2

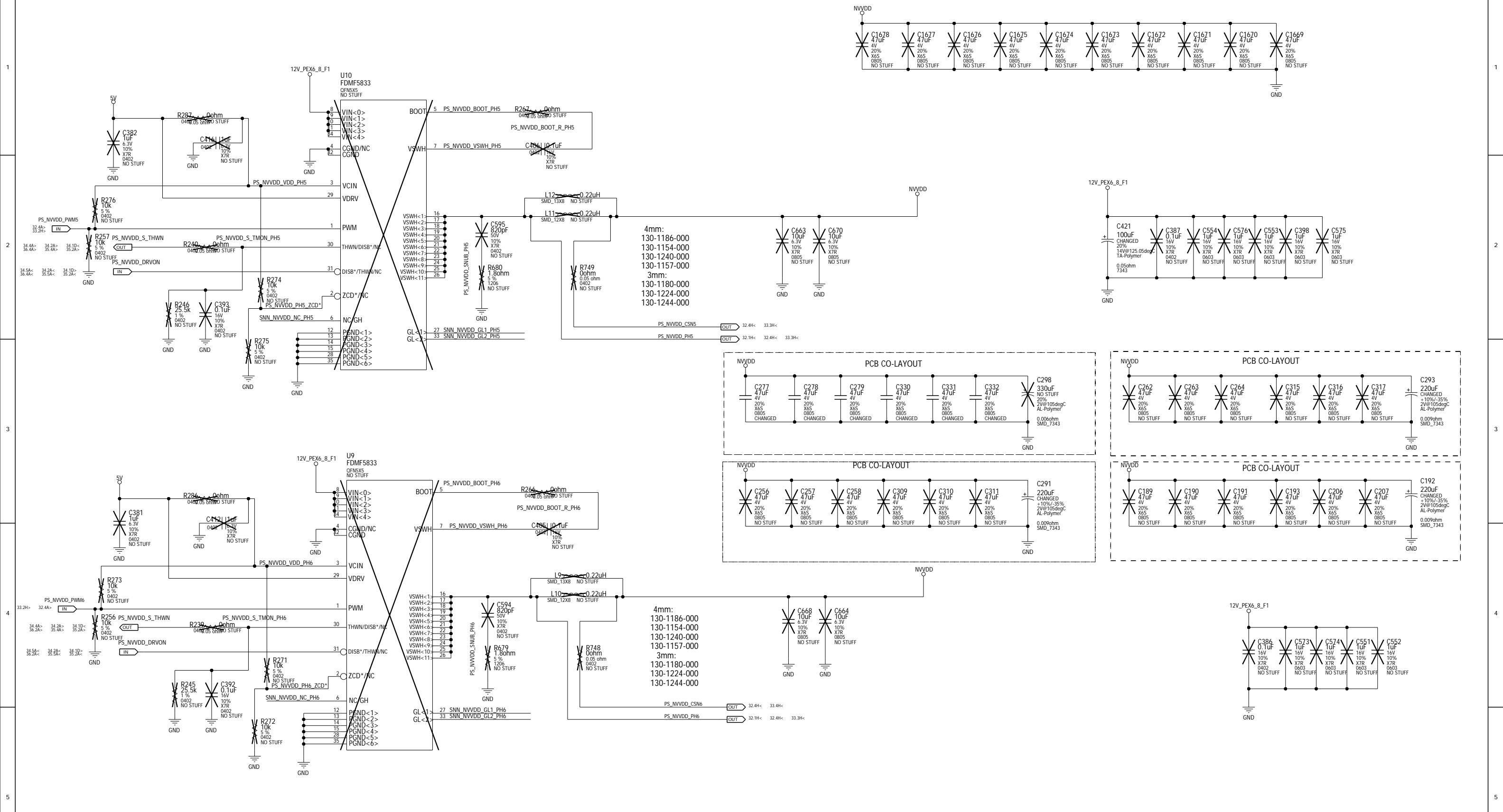
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NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F

PAGE 34 OF 53
 DATE 12-NOV-2018





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PAGE DETAIL	PS: NVVDD Phase 5,6

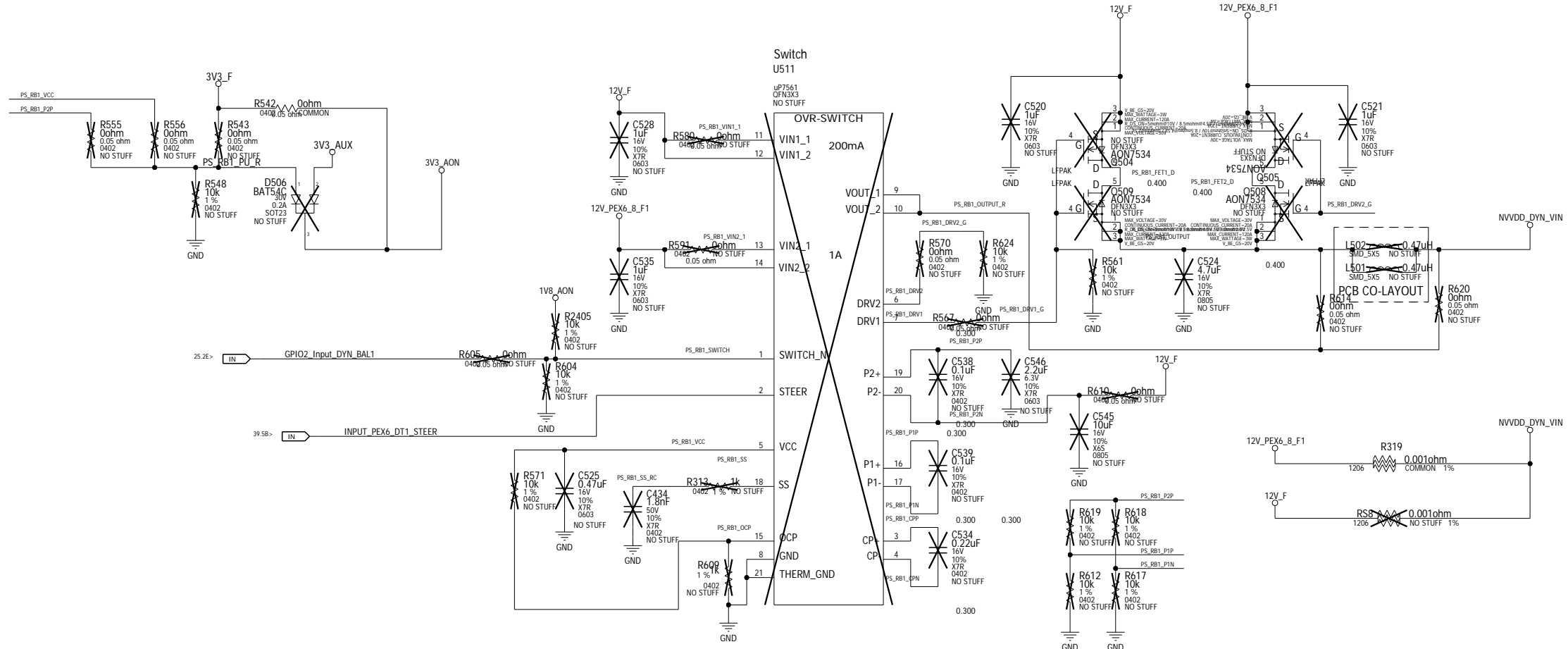
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NV_PN	600-1G160-0042-700	PAGE	36 Of 53
PCB REV	PG160-B03	DATE	12-NOV-2018
BOM REV	F		

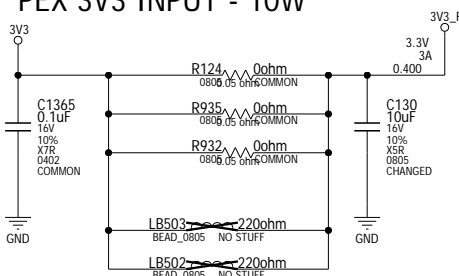


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PAGE DETAIL	PS: Input Power Balancing Switcher

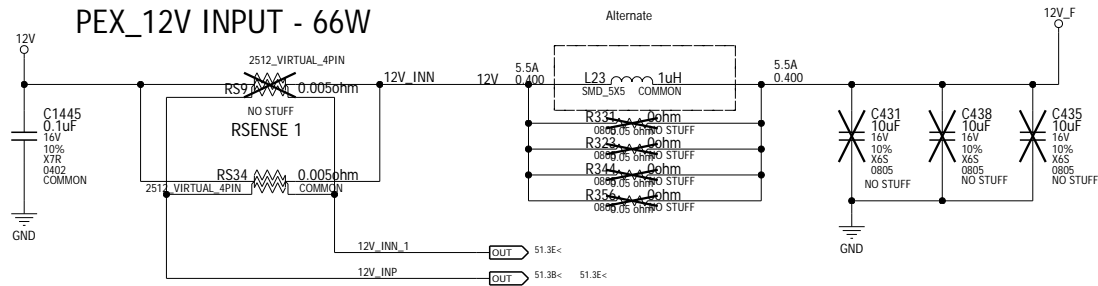
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NV_PN	600-1G160-0042-700	PAGE	37 OF 53
PCB REV	PG160-B03	DATE	12-NOV-2018
BOM REV	F		

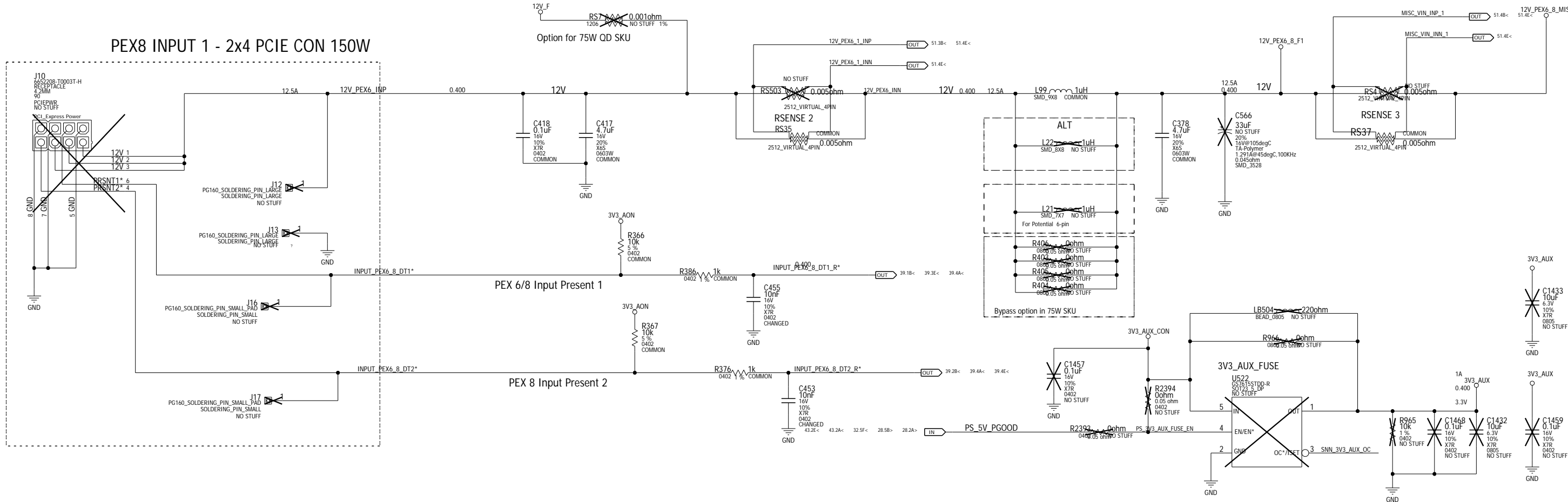
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W

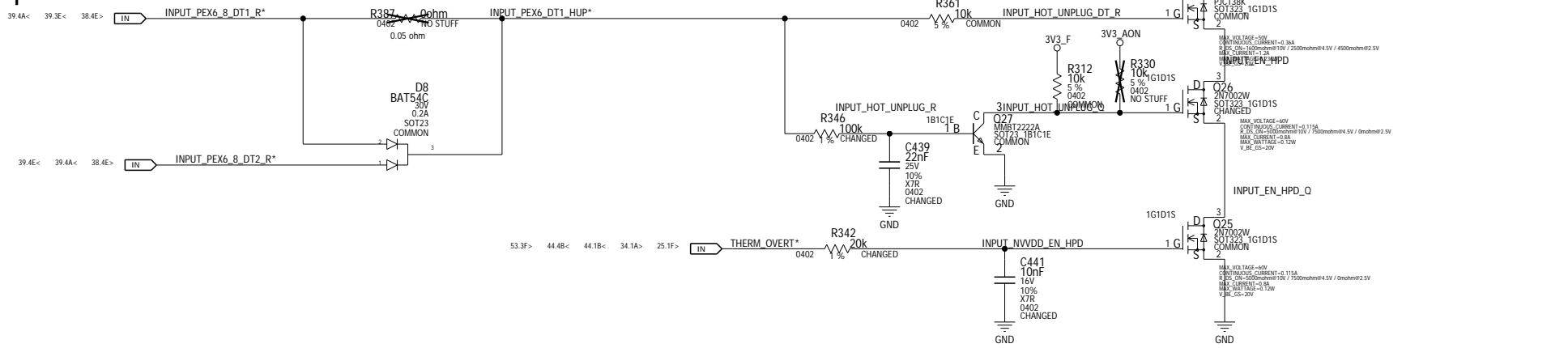


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PAGE DETAIL	PS: Input, Filtering, and Monitoring

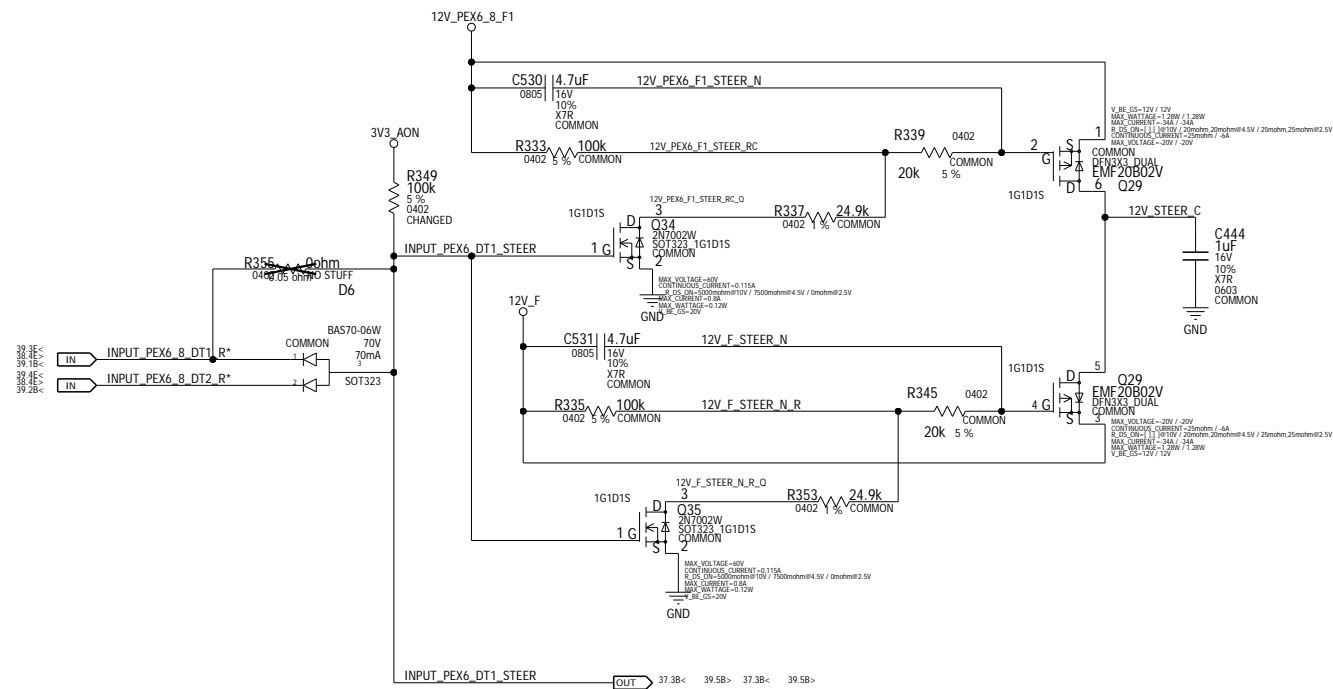
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

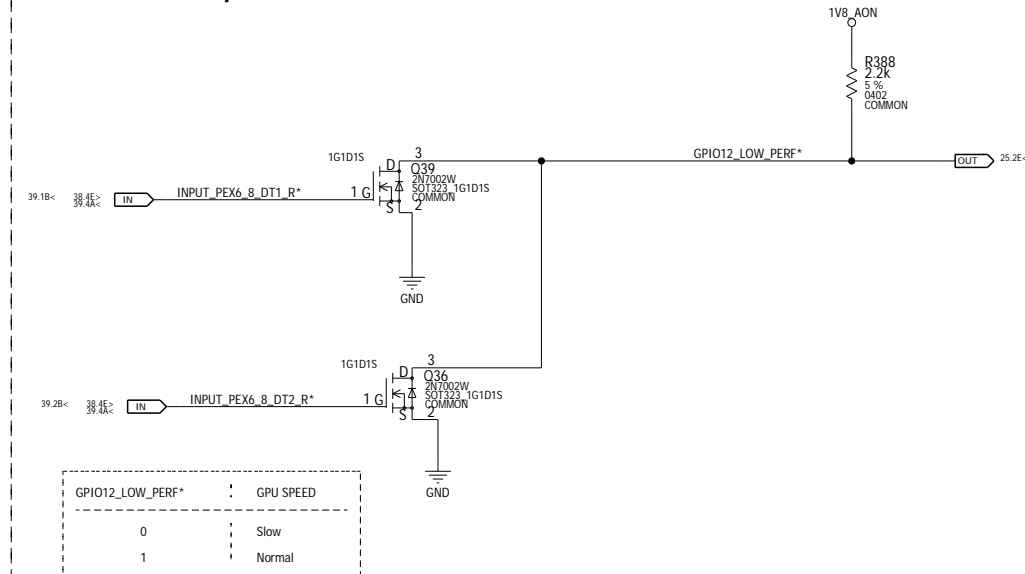


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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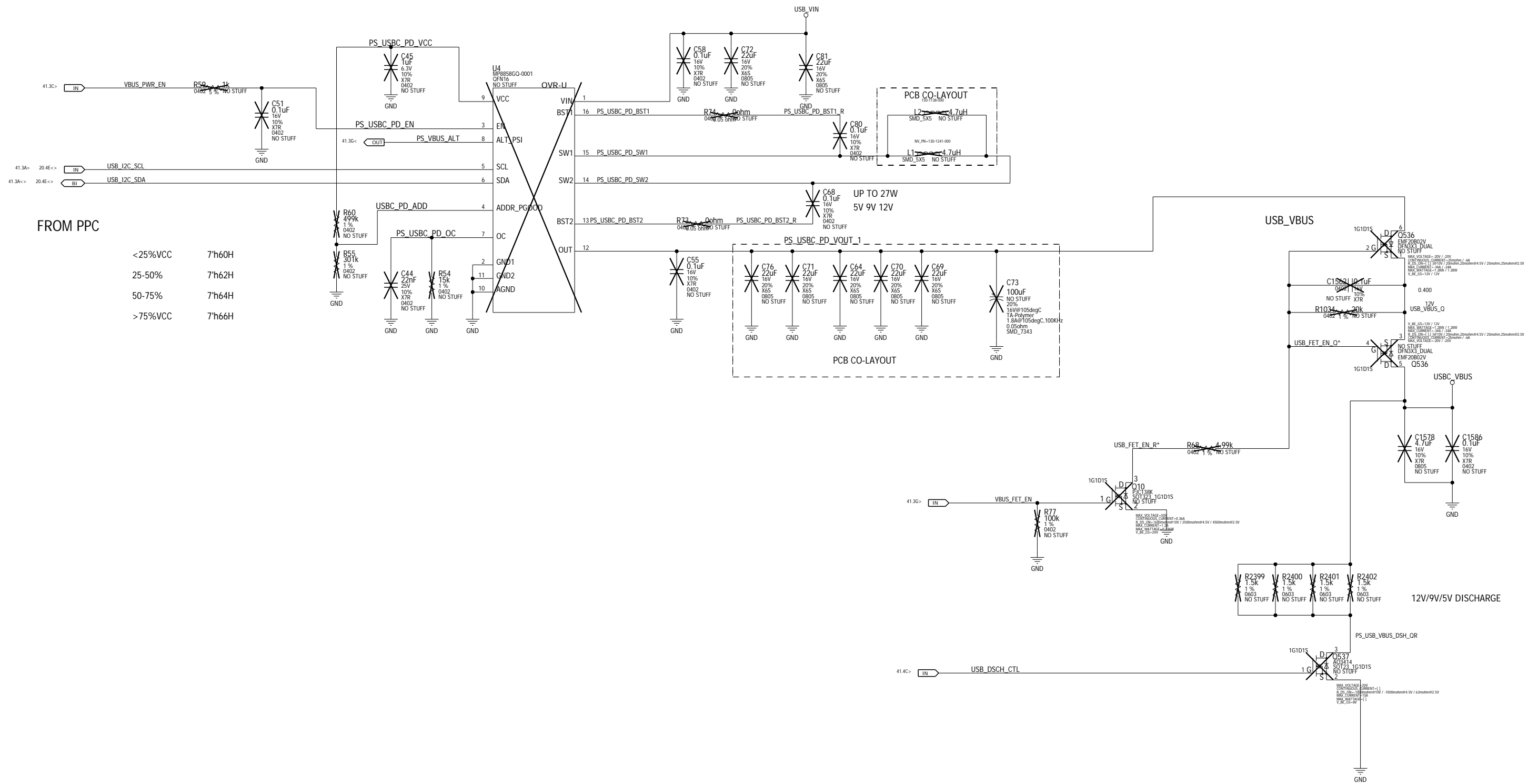
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PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

NV_PN	600-1G160-0042-700	PAGE	39 OF 53
PCB REV	PG160-B03	DATE	12-NOV-2018
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FROM PPC

<25%VCC	7'h60H
25-50%	7'h62H
50-75%	7'h64H
>75%VCC	7'h66H

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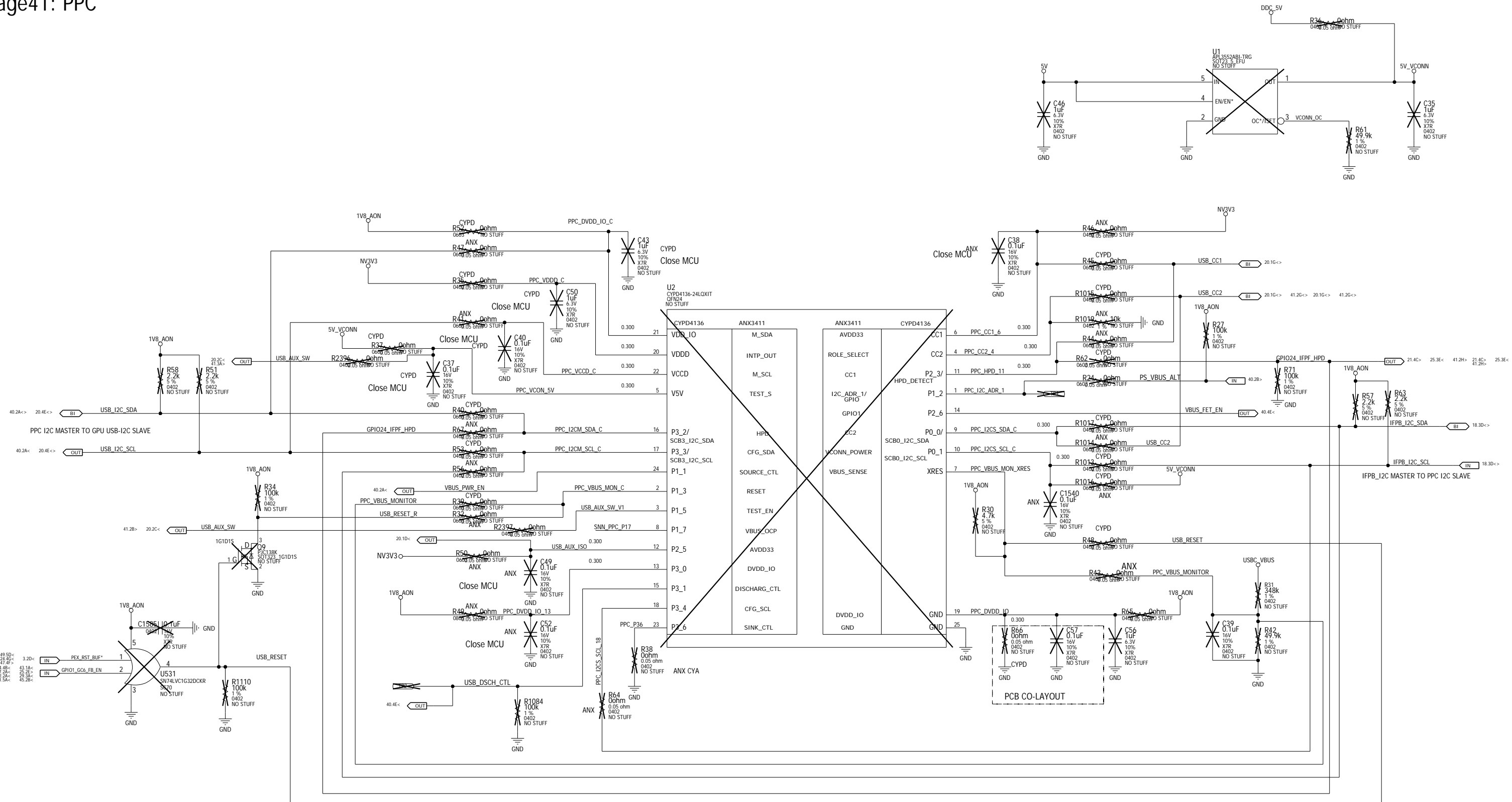


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BOM REV	F	DATE	12-NOV-2018

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PAGE DETAIL	PS: Type-C BuckBoost



	SCL	SDA
CYPD I2C SLAVE	PIN 10	PIN 9
CYPD I2C MASTER	PIN 17	PIN 16
ANX I2C SLAVE	PIN 18	PIN 17
ANX I2C MASTER	PIN 22	PIN 21


ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL PD PPC

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 PCB REV: PG160-B03
 BOM REV: F

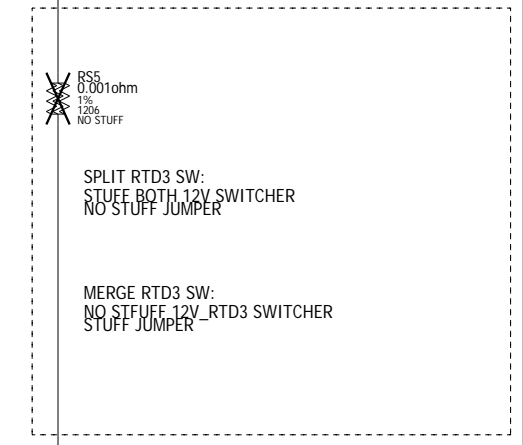
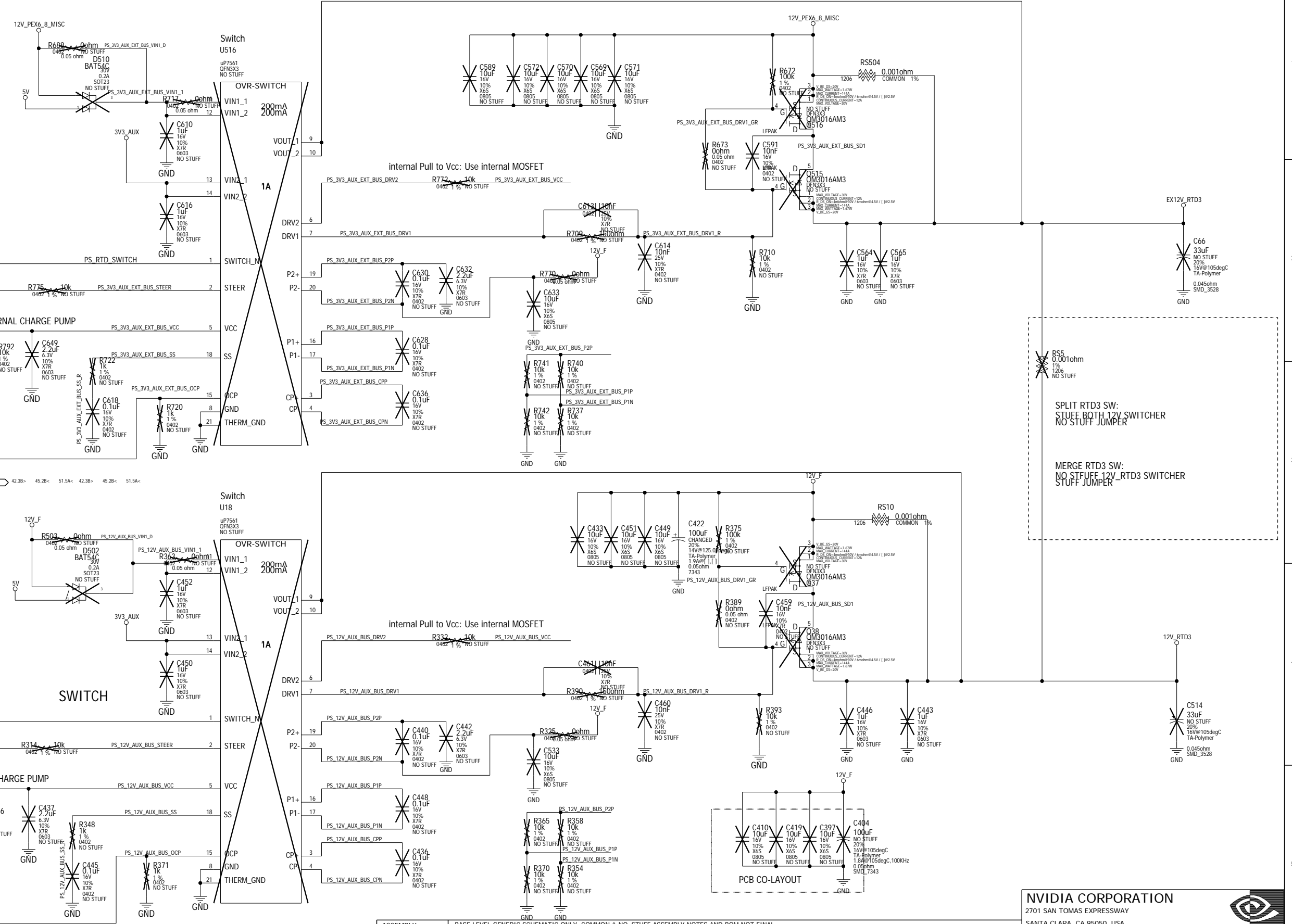
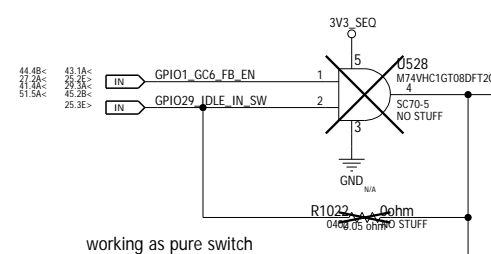
PAGE: 41 OF 53
 DATE: 12-NOV-2018



Page42: 12V & 3V3_A SWITCHER

SWITCH		VOUT
0		VOUT = VIN1
1		VOUT = VIN2

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

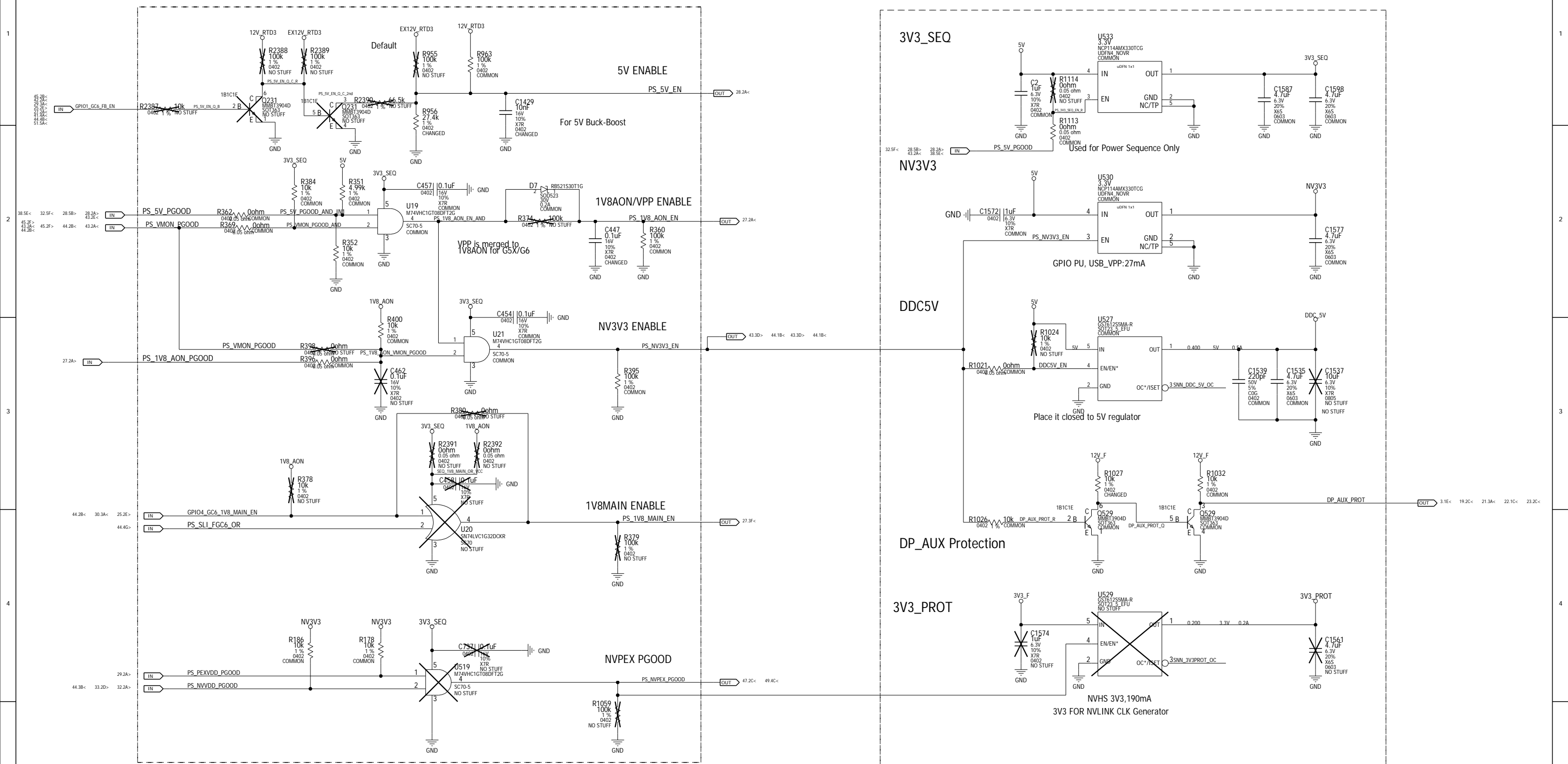


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PAGE DETAIL	PS: 12V & 3V3_A SWITCHER

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PCB REV	PG160-B03
BOM REV	F
PAGE	42 OF 53
DATE	12-NOV-2018

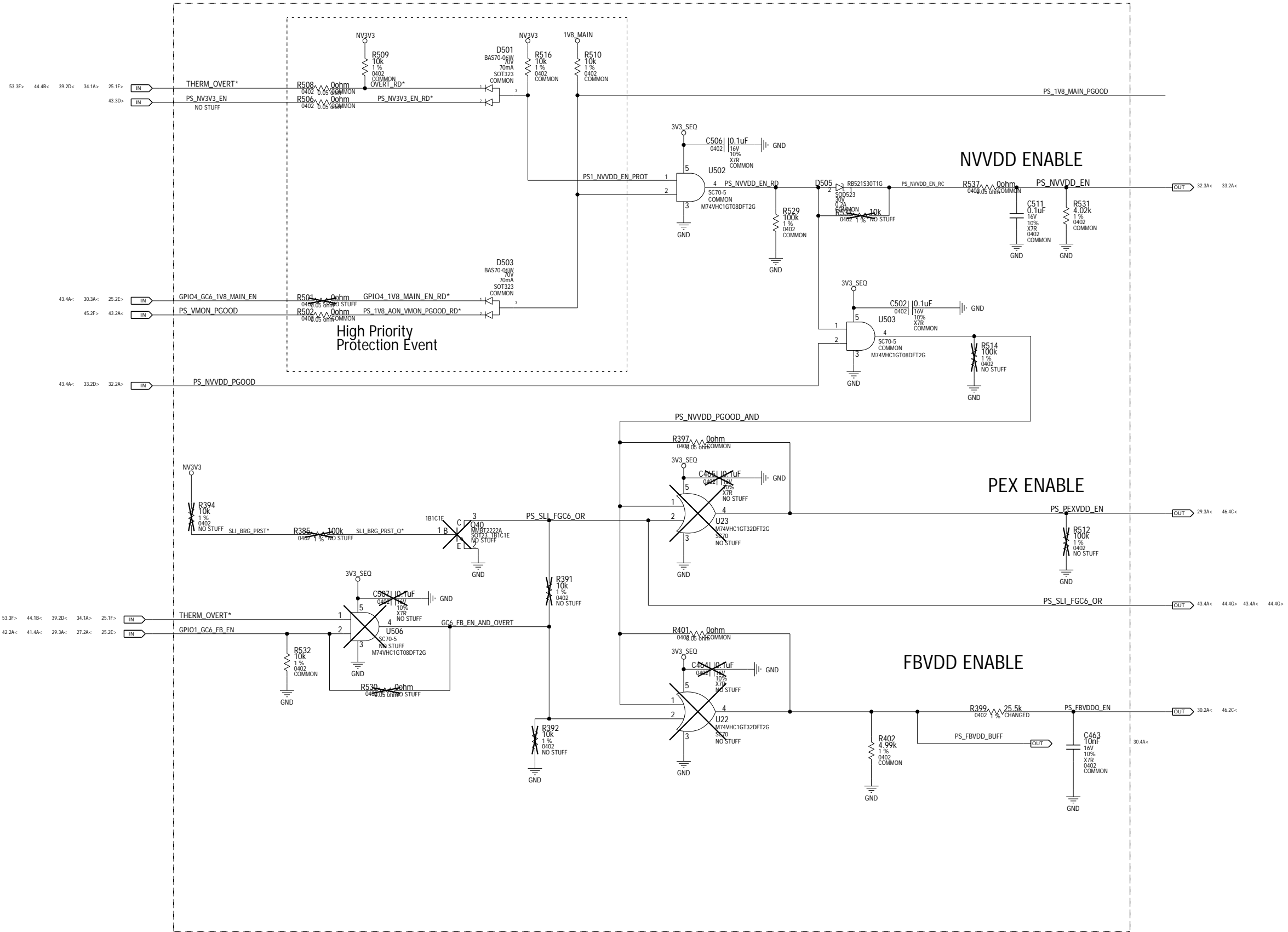


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PAGE DETAIL	SEQ: 5V, 1V8, NV3V3 ENABLE

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PCB REV	PG160-B03
BOM REV	F
PAGE	43 OF 53
DATE	12-NOV-2018



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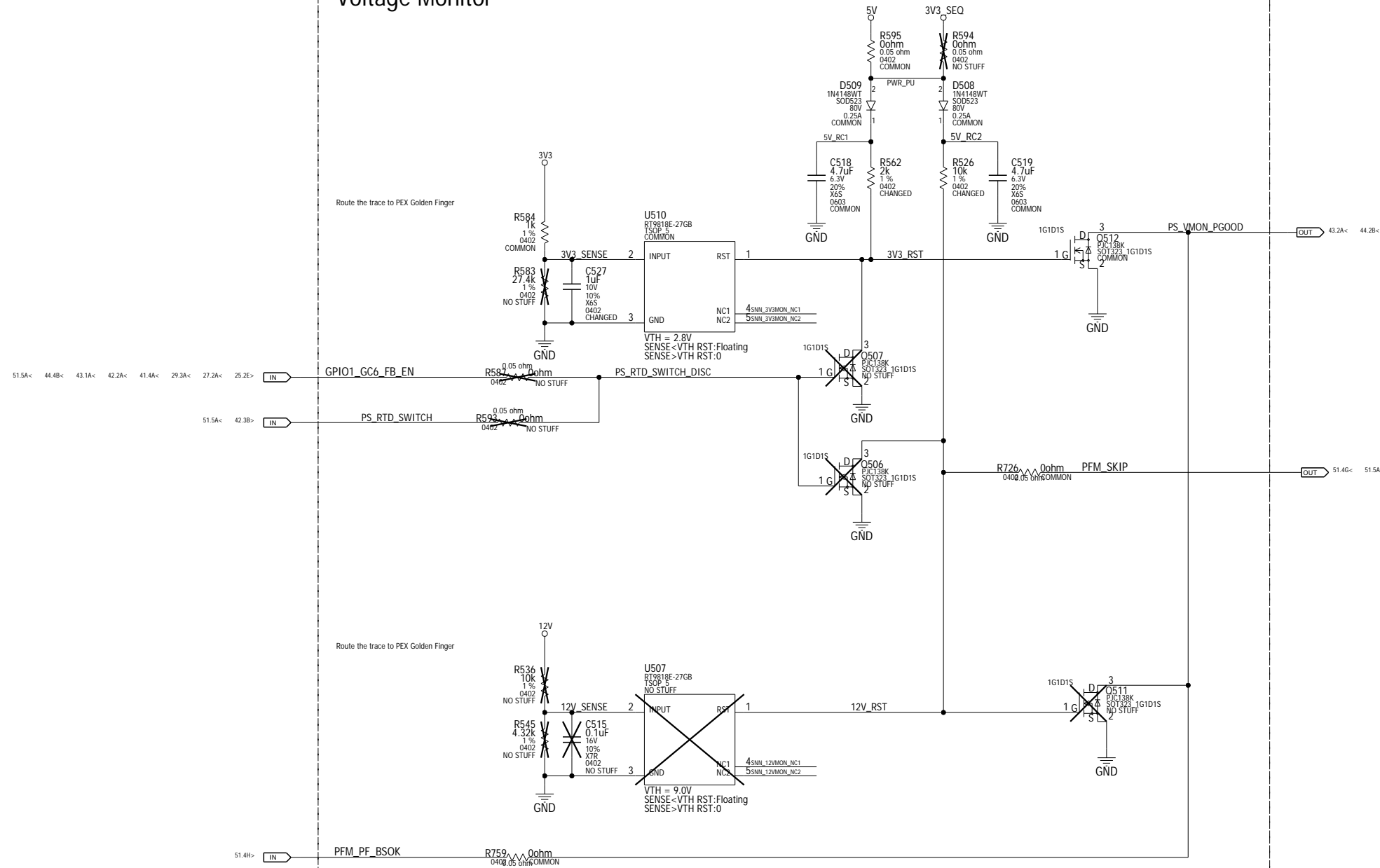
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NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F

PAGE 44 OF 53
 DATE 12-NOV-2018

Voltage Monitor



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

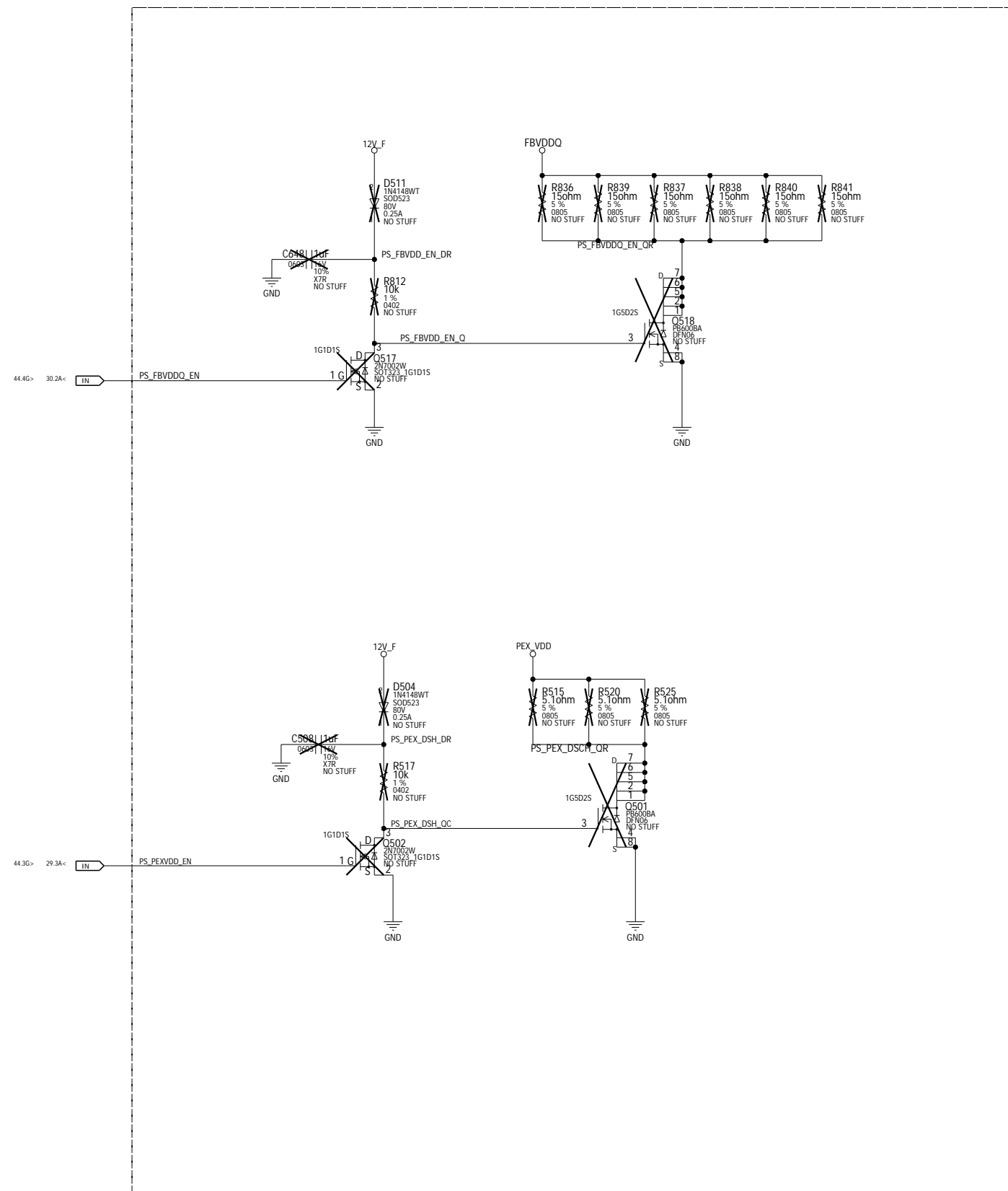
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence, Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

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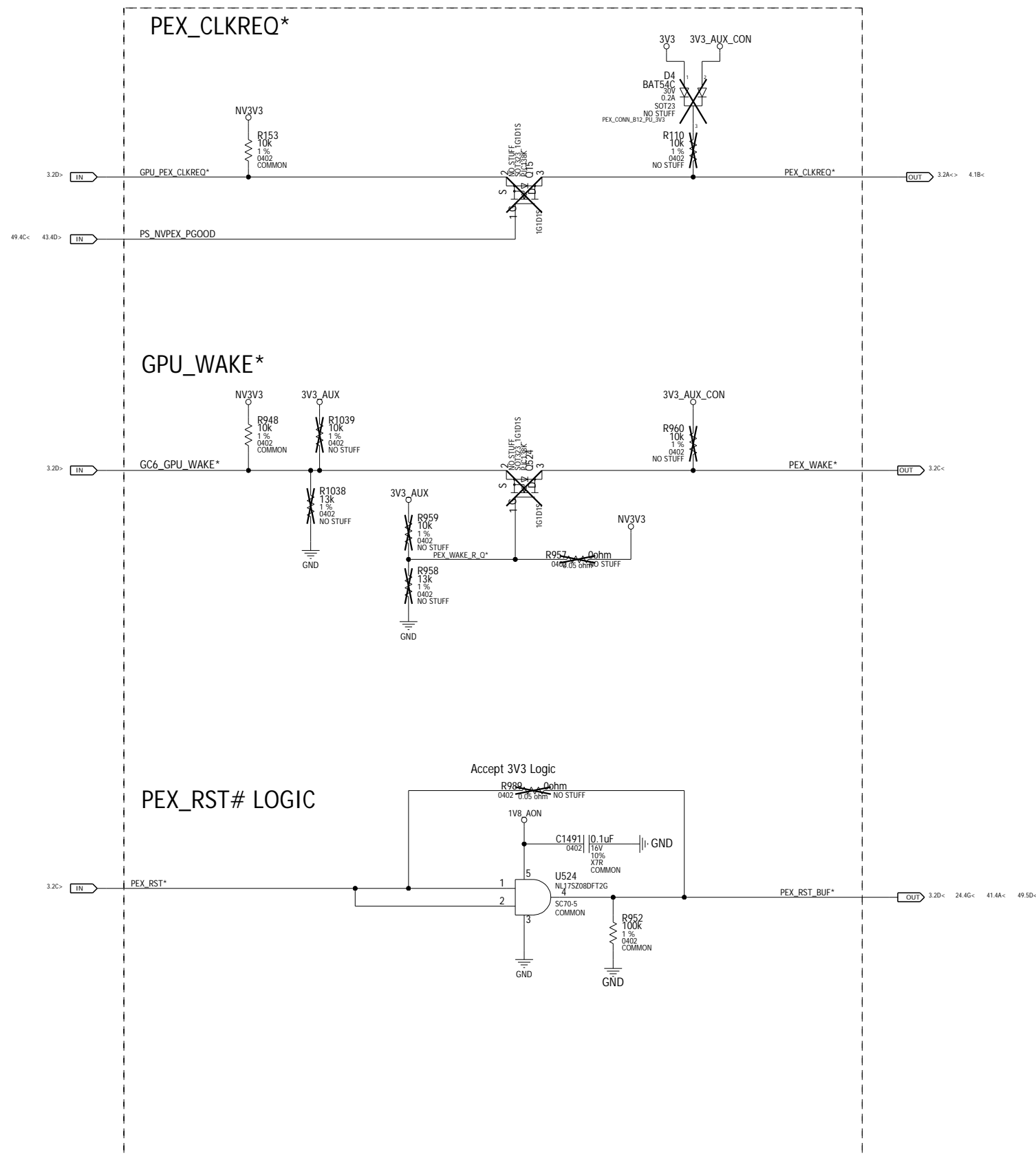
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BOM REV	F	DATE	12-NOV-2018



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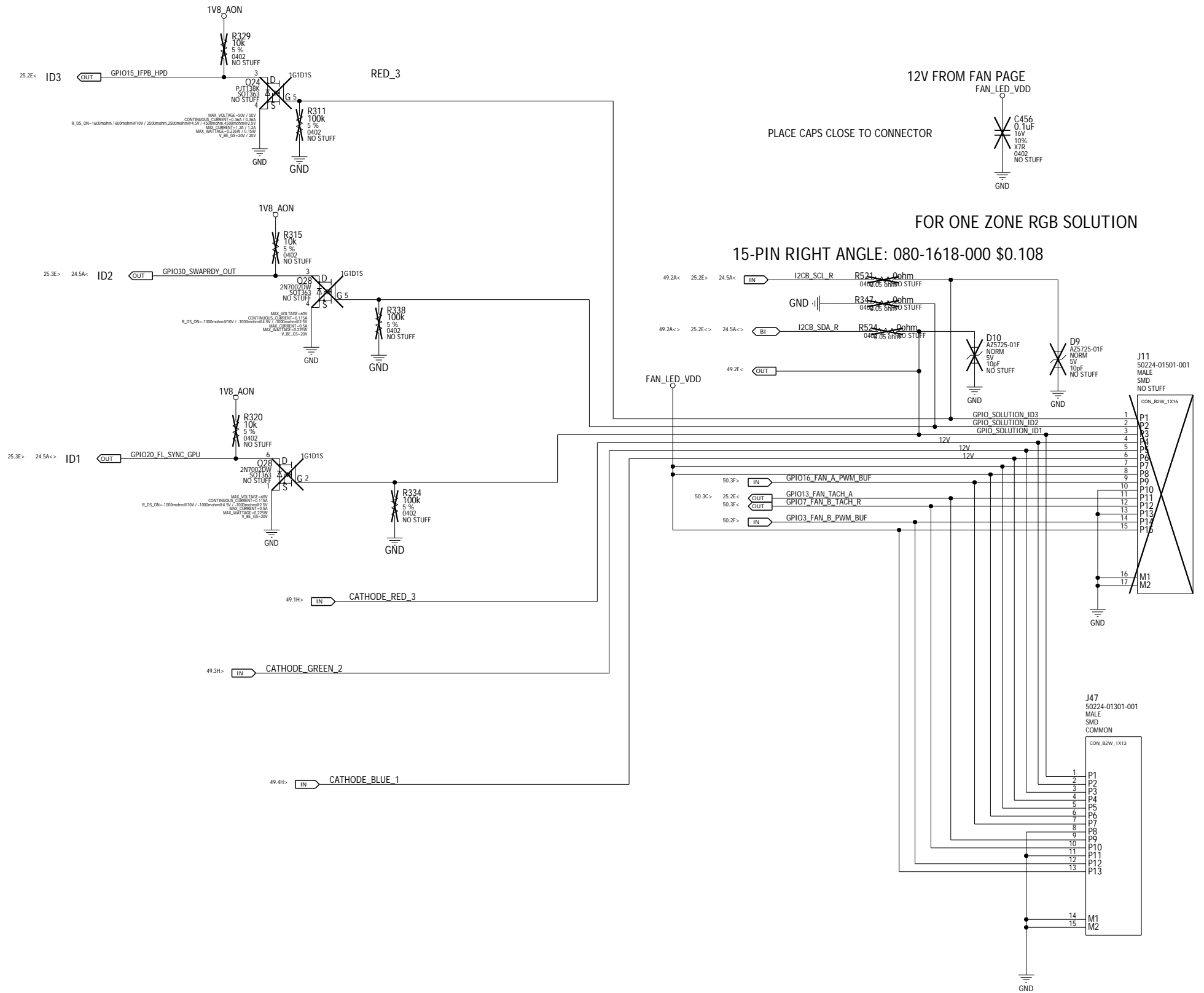
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PCB REV	PG160-B03	DATE	12-NOV-2018
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NV_PN	600-1G160-0042-700	PAGE	47 OF 53		
PCB REV	PG160-B03	DATE	12-NOV-2018		
BOM REV	F				



For ONE ZONE RGB/cable	
PIN SEQ	Pin Name
1	ID3
2	ID2
3	ID1
4	DRIVE3/R
5	DRIVE2/G
6	DRIVE1/B
7	12V
8	12V
9	FAN_PWM1
10	GND
11	FAN_TACH1
12	FAN_TACH2
13	GND
14	FAN_PWM2
15	12V

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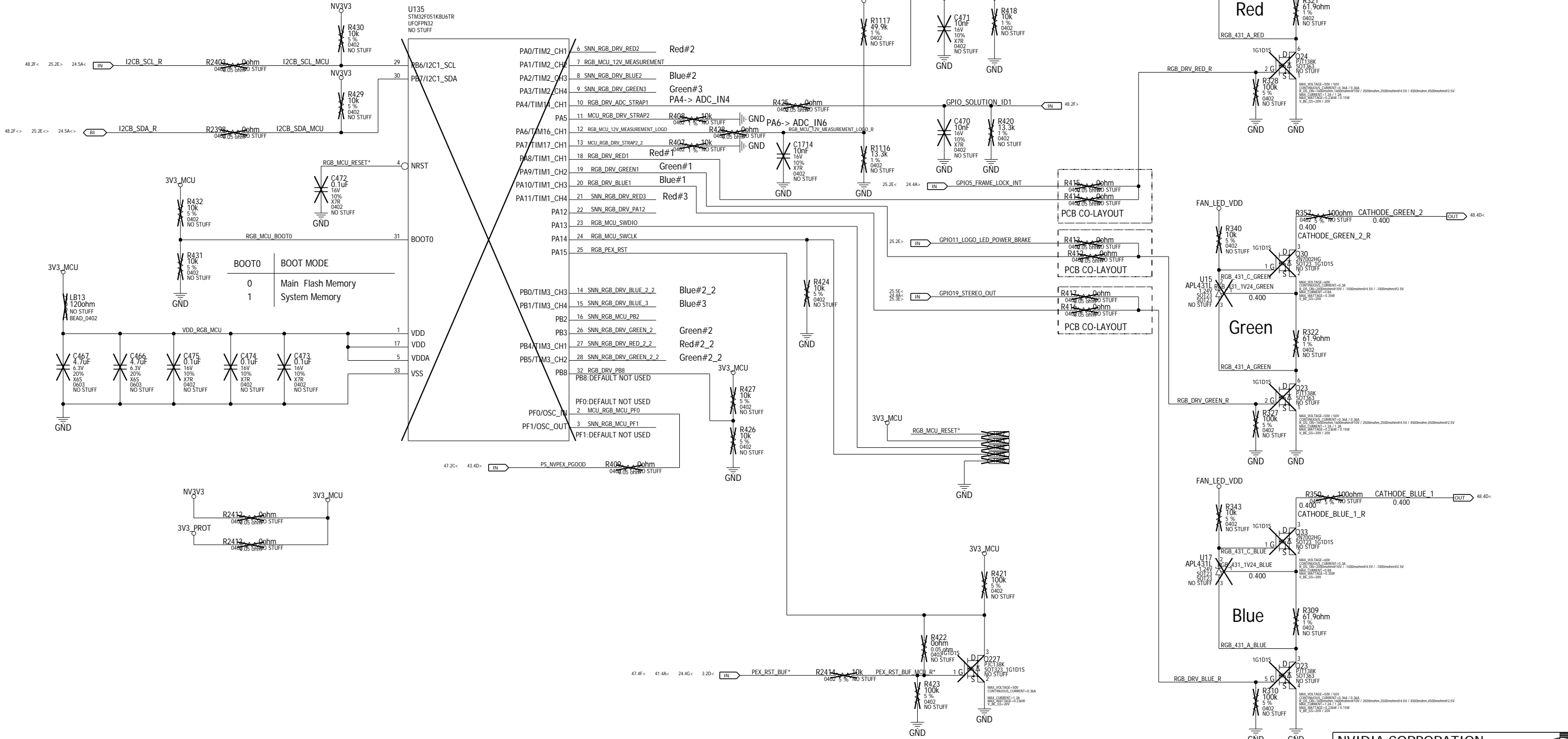
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NV_PN 600-1G160-0042-700
 PCB REV PG160-B03 PAGE 48 OF 53
 BOM REV F DATE 12-NOV-2018

8-bit I2C Address of MCU on GPU BOARD: 0x92

INPUT LEAKAGE CURRENT OF ADC_INx PINS: -0.2uA-0.2uA(max)



BOOT0	BOOT MODE
0	Main Flash Memory
1	System Memory

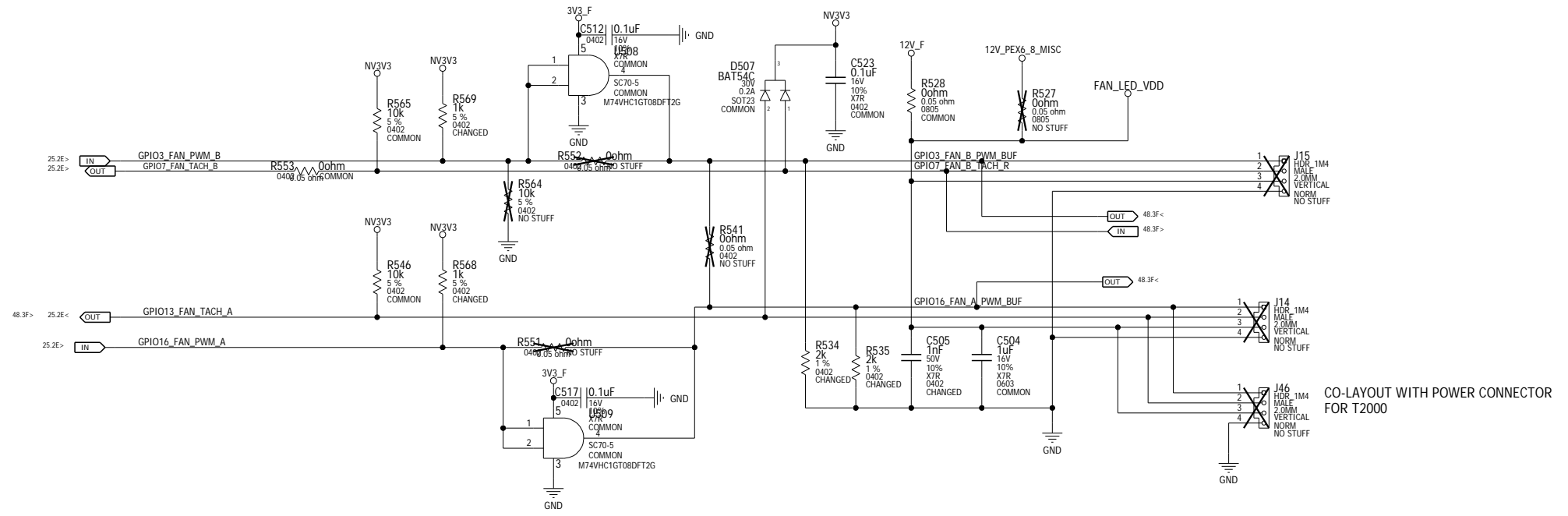
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PAGE DETAIL	LED DRIVER & BOOST

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NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F

PAGE 49 OF 53
 DATE 12-NOV-2018



CO-LAYOUT WITH POWER CONNECTOR FOR T2000

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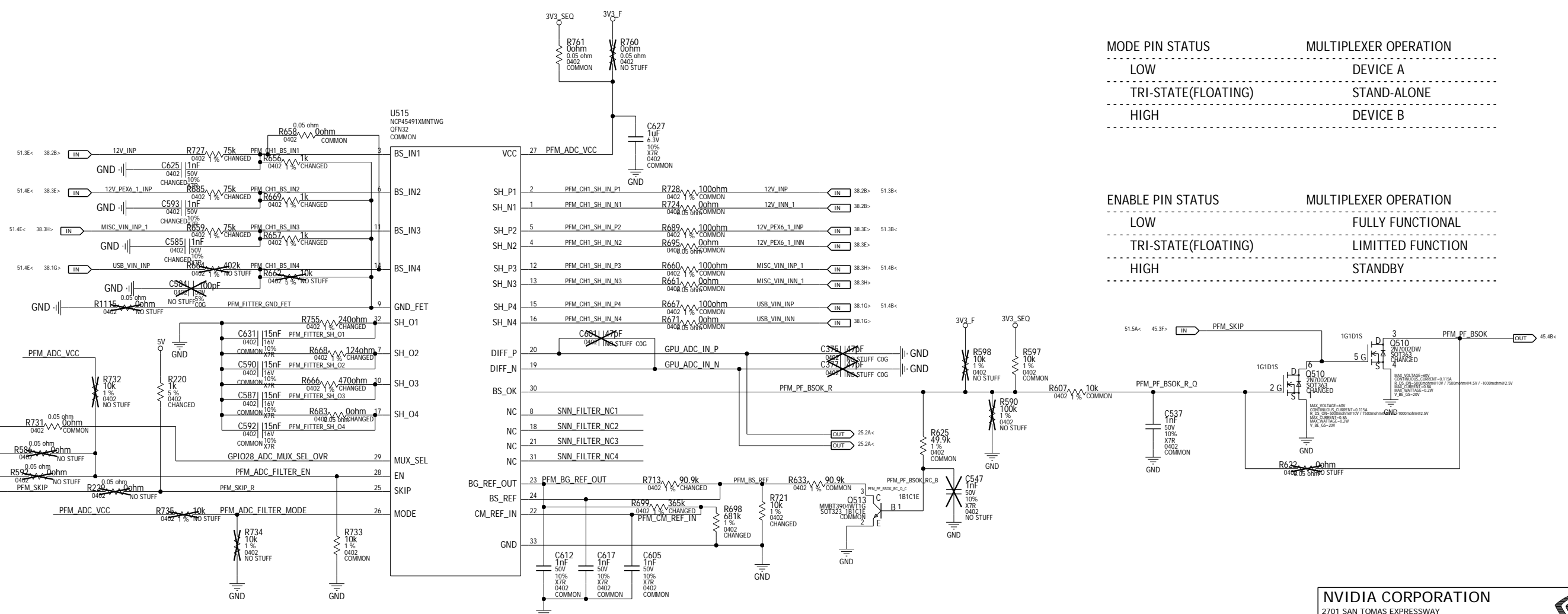


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PCB REV	PG160-B03	PAGE	50 OF 53
BOM REV	F	DATE	12-NOV-2018

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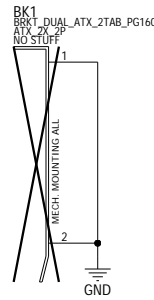
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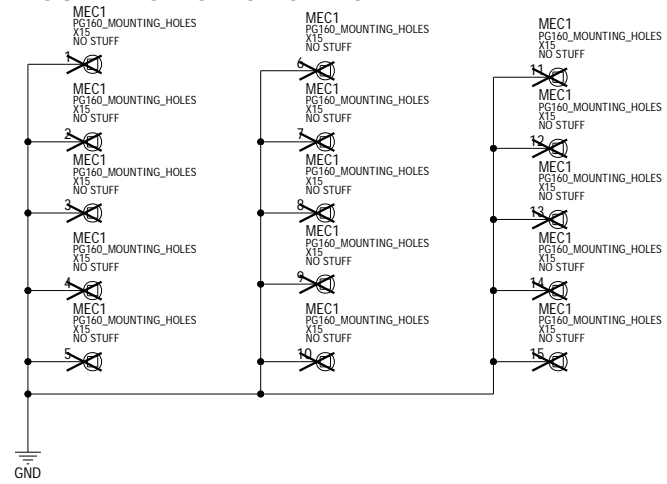
NV_PN	600-1G160-0042-700
PCB REV	PG160-B03
BOM REV	F

PAGE	51 Of 53
DATE	12-NOV-2018

Brackets:



MOUNTING HOLES FOR HS:



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NV_PN	600-1G160-0042-700	PAGE	52 OF 53
PCB REV	PG160-B03	DATE	12-NOV-2018
BOM REV	F		

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