

PG160-B02

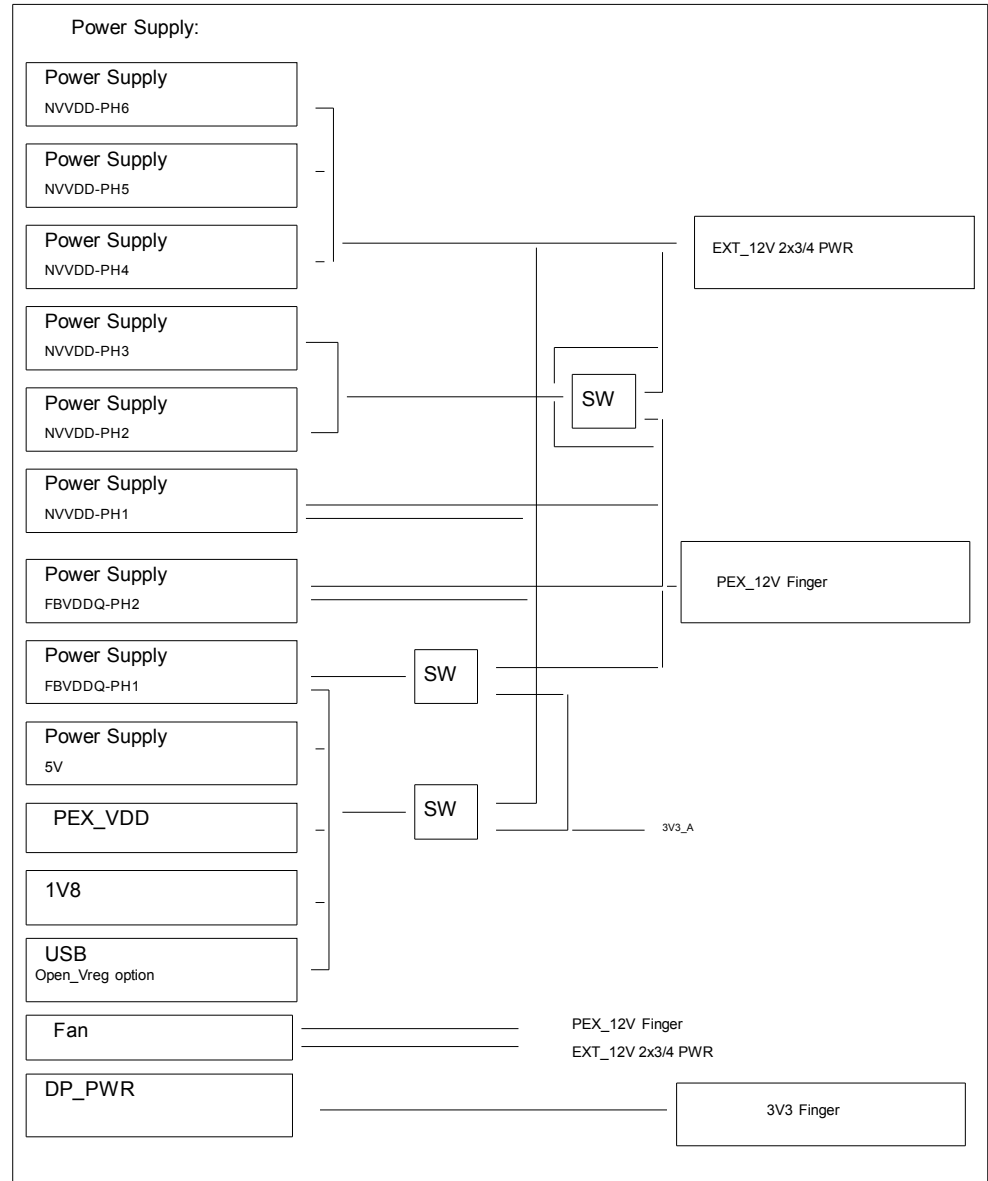
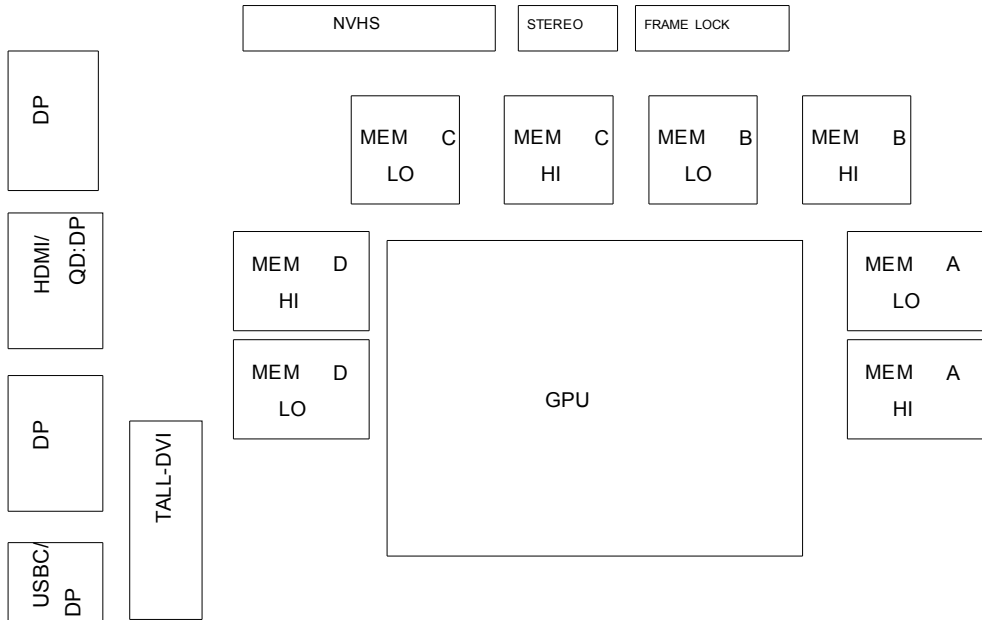
8GB GDDR6, 256b, X16 Tall DVI-D + USBC/DP + DP + HDMI/DP + DP

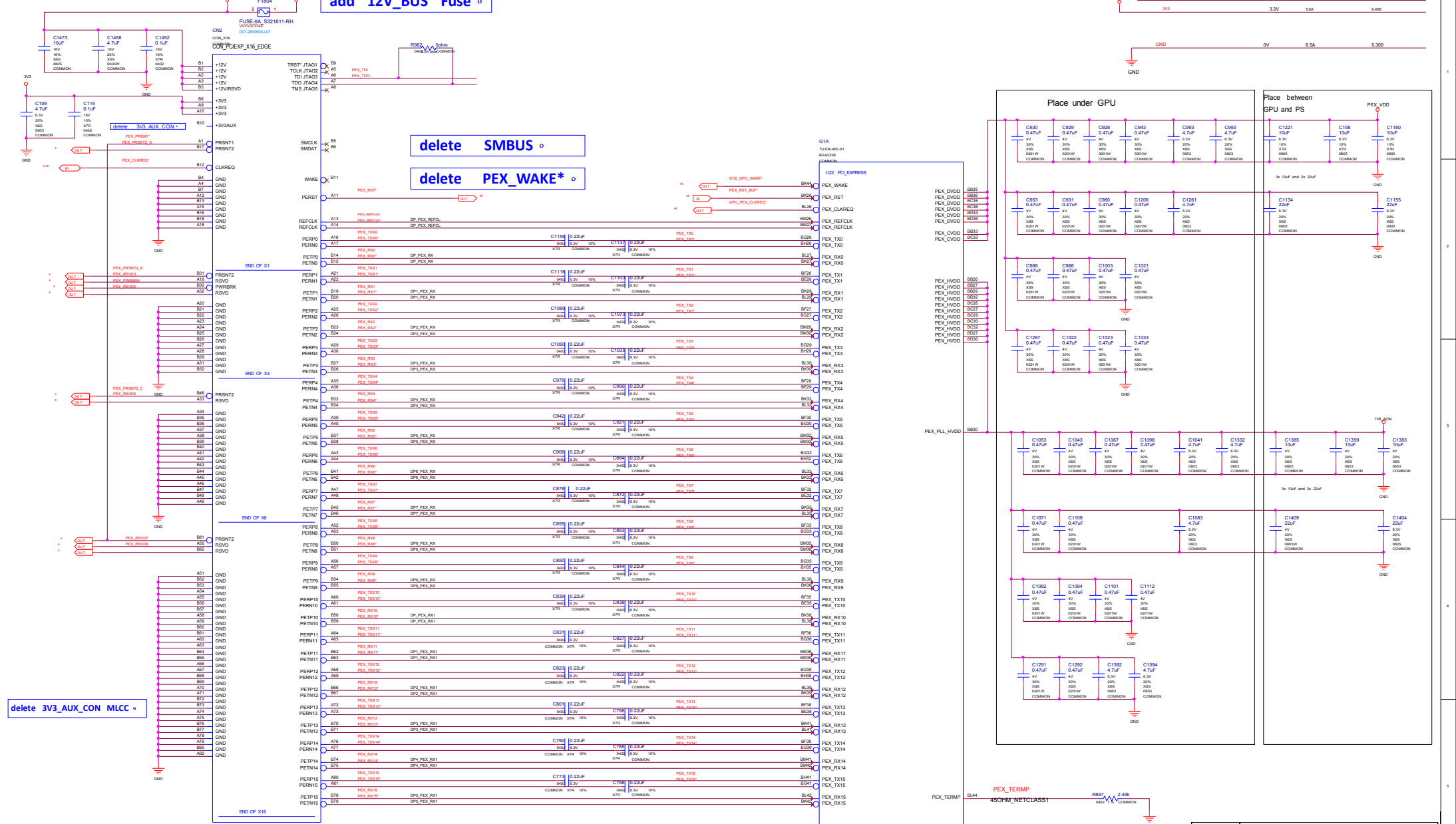
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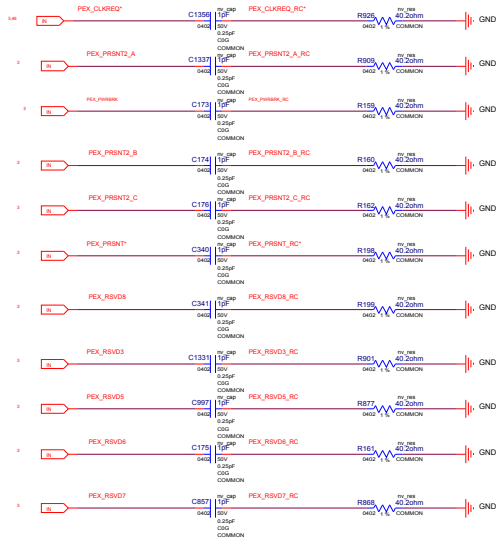
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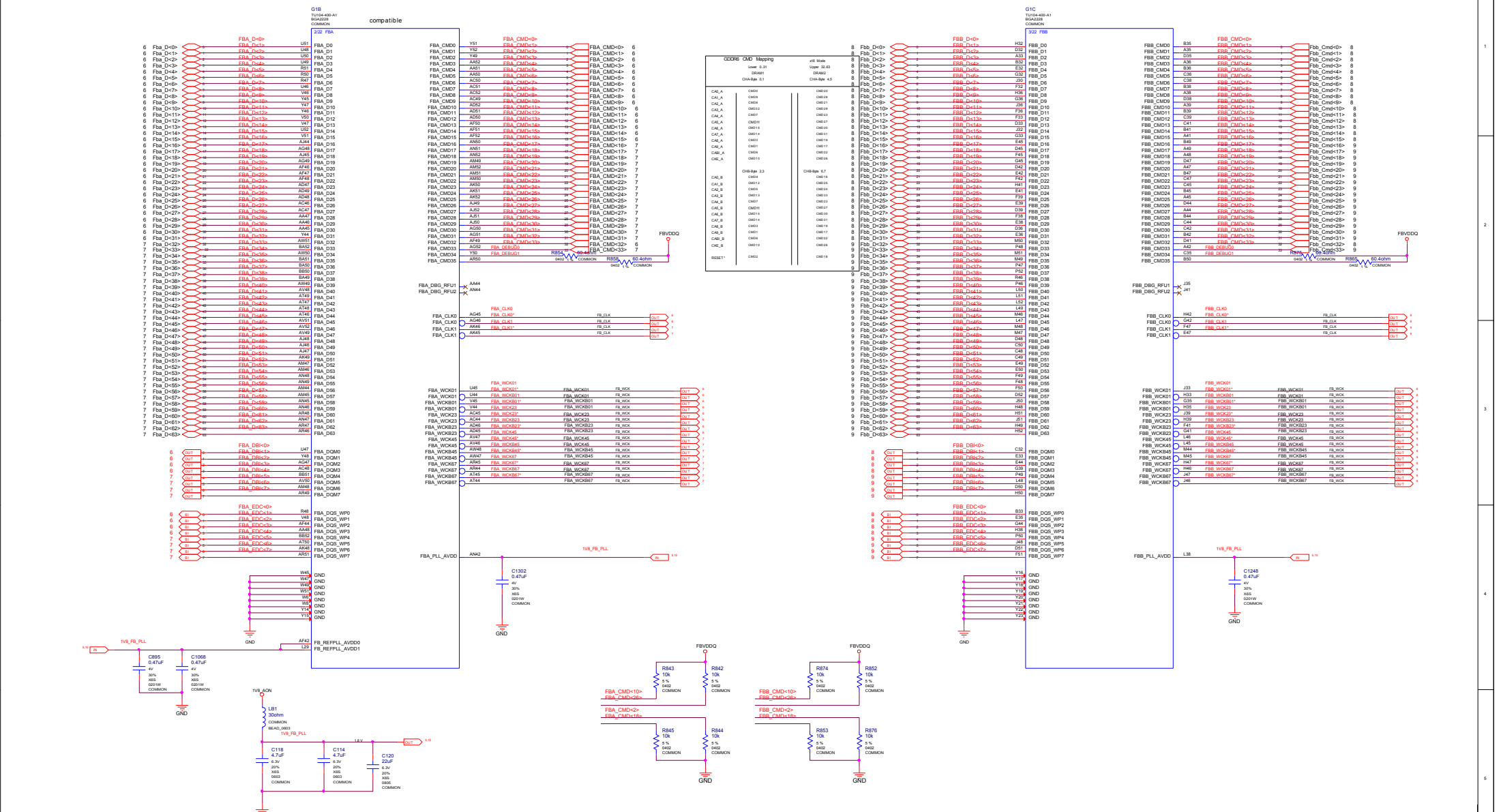
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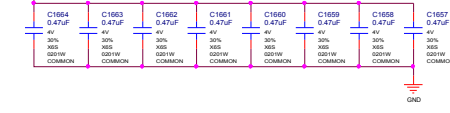
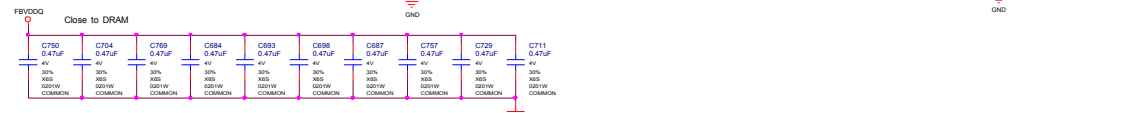
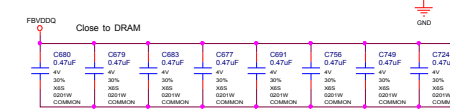
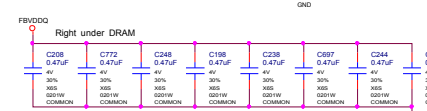
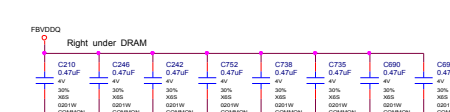
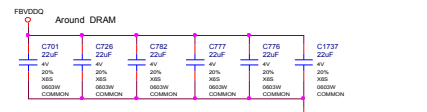
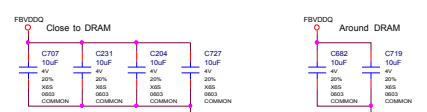
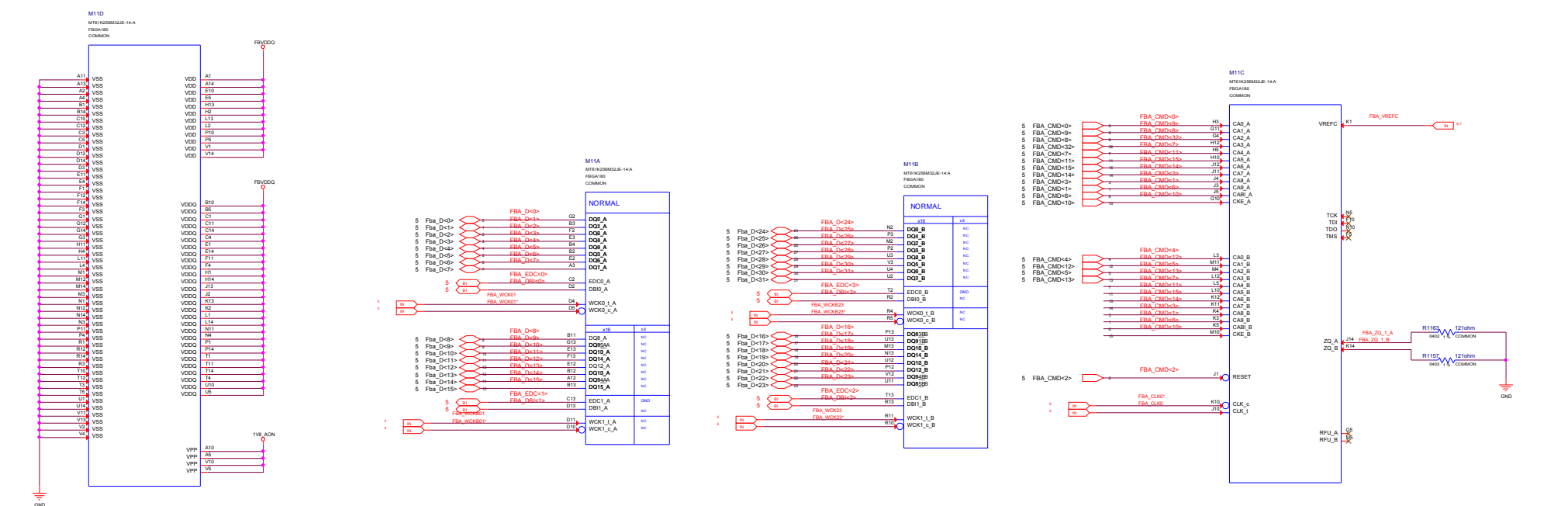




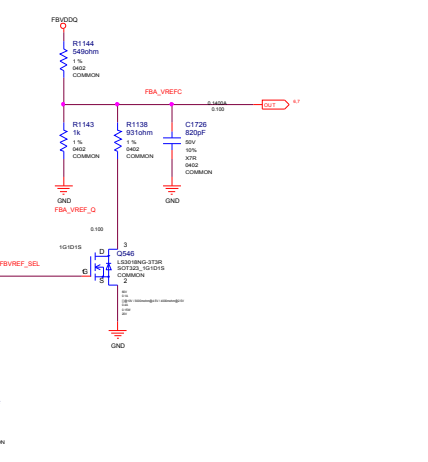


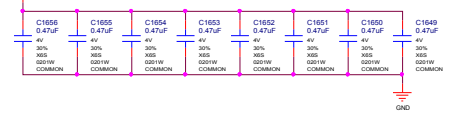
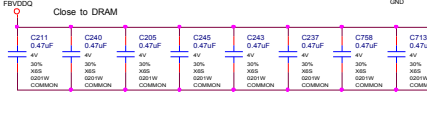
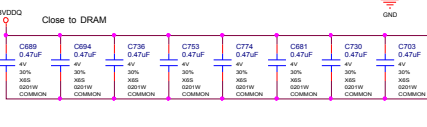
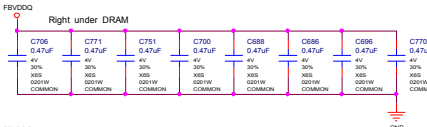
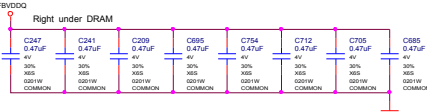
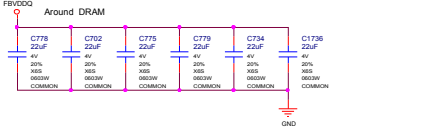
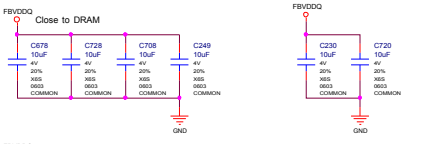
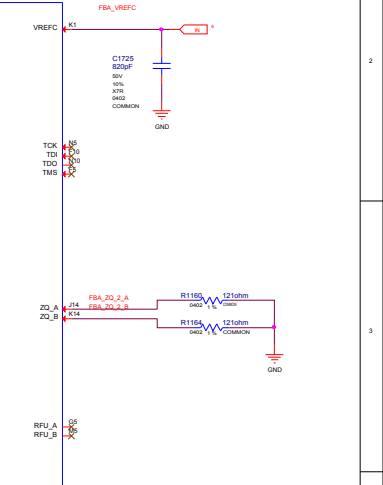
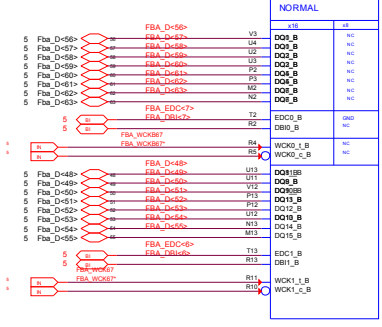
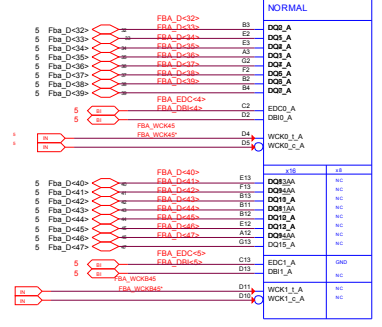
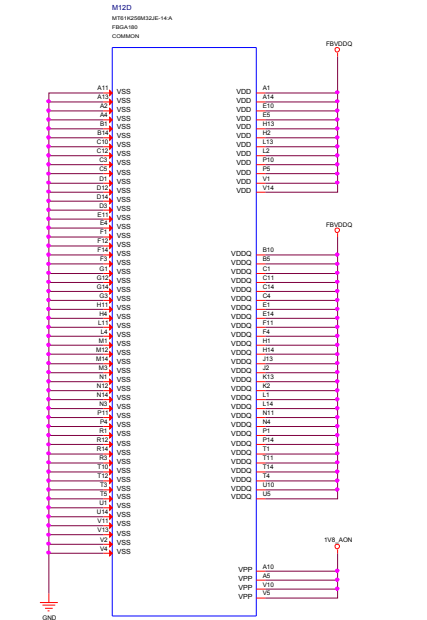
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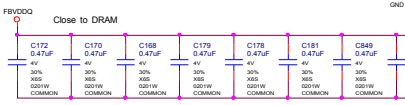
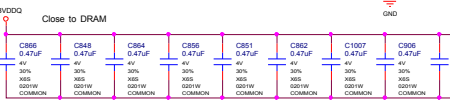
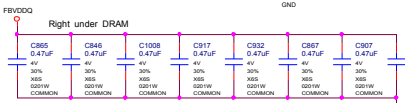
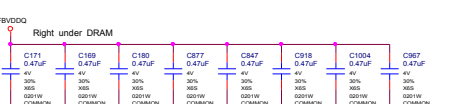
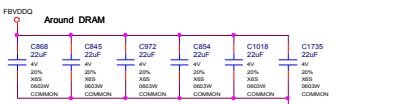
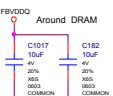
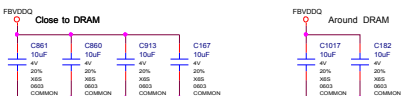
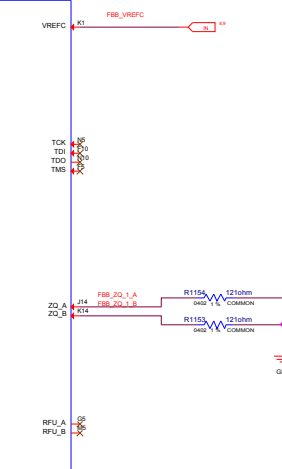
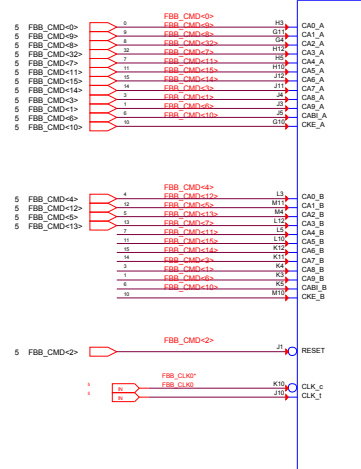
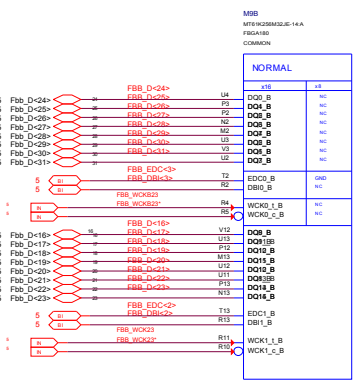
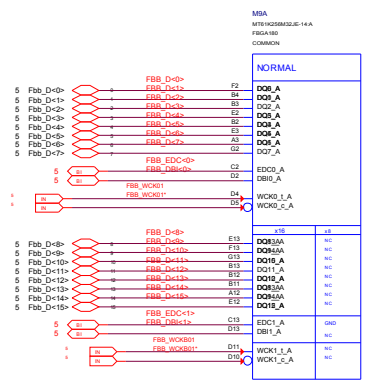
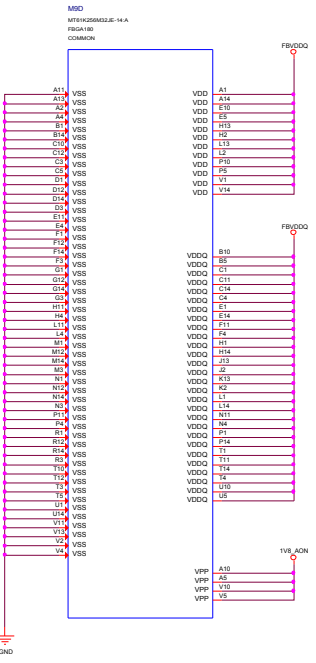
VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R106



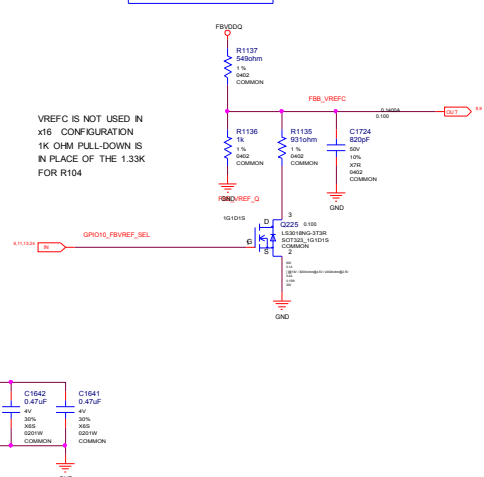


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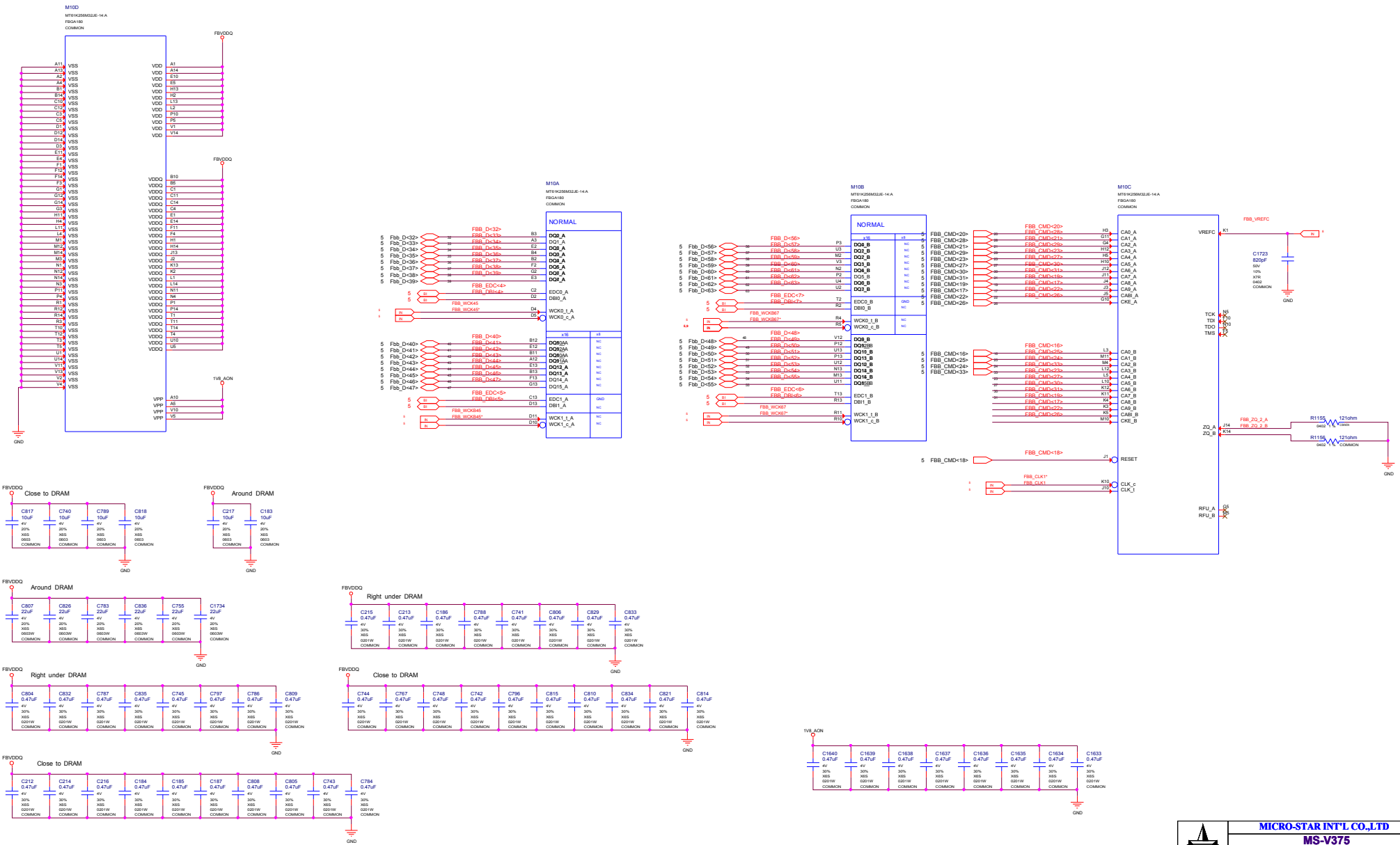
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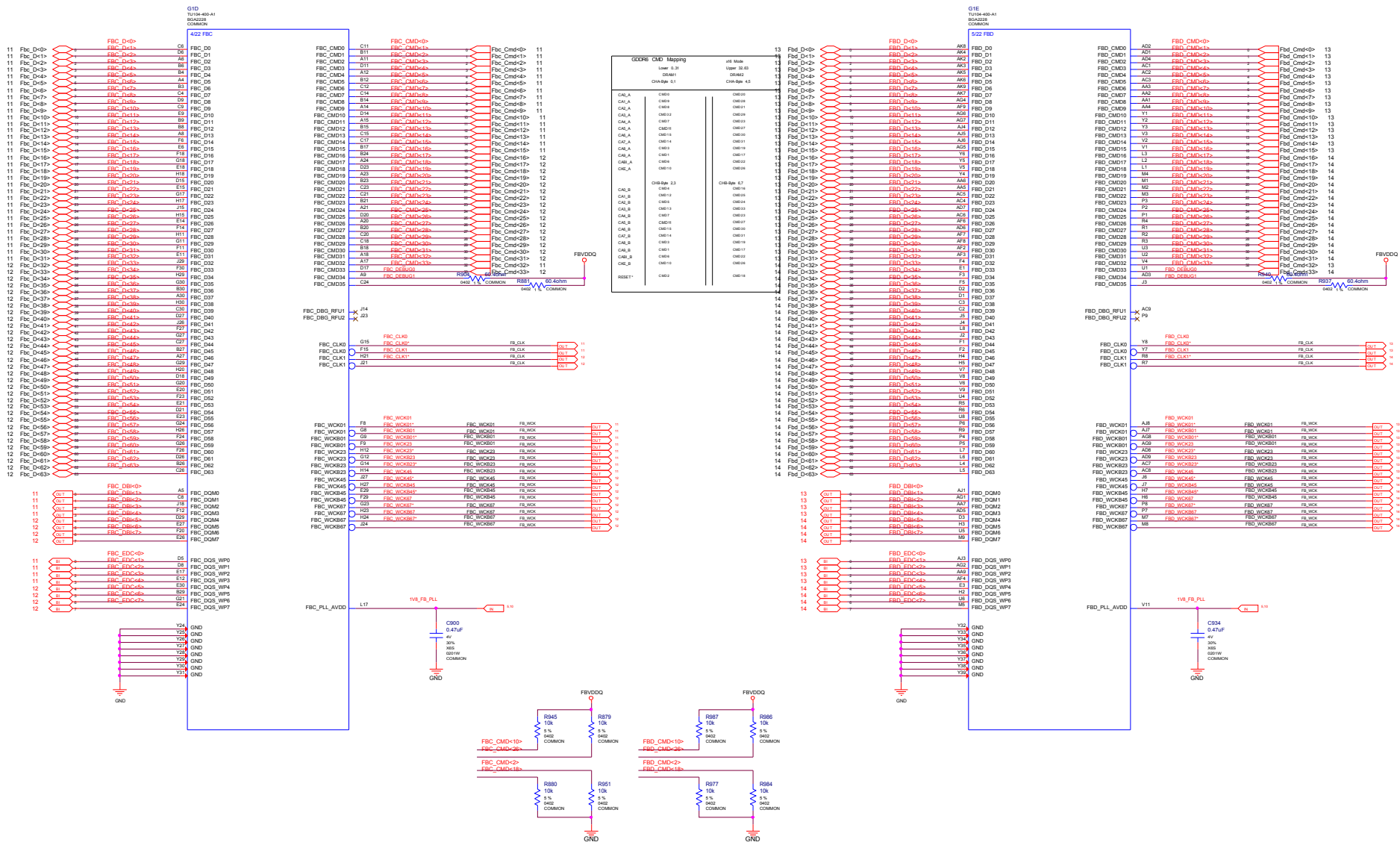


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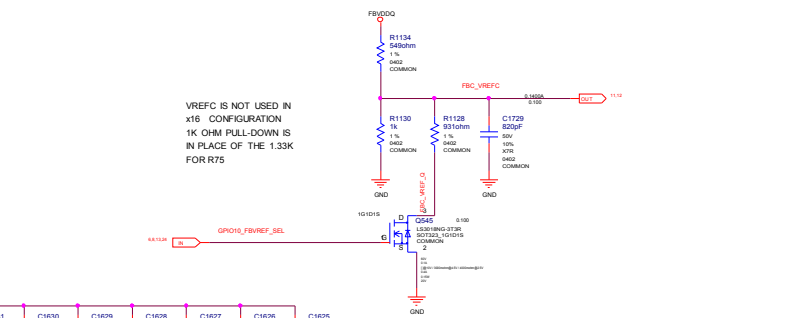
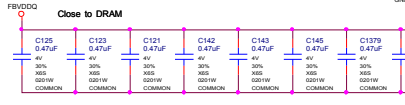
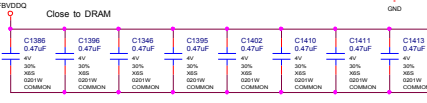
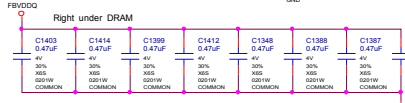
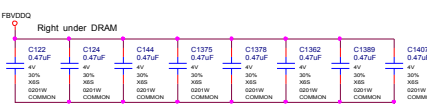
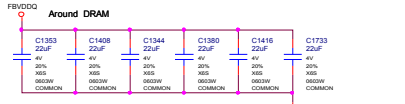
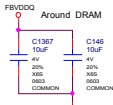
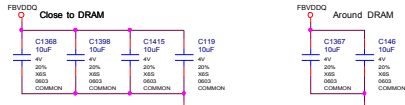
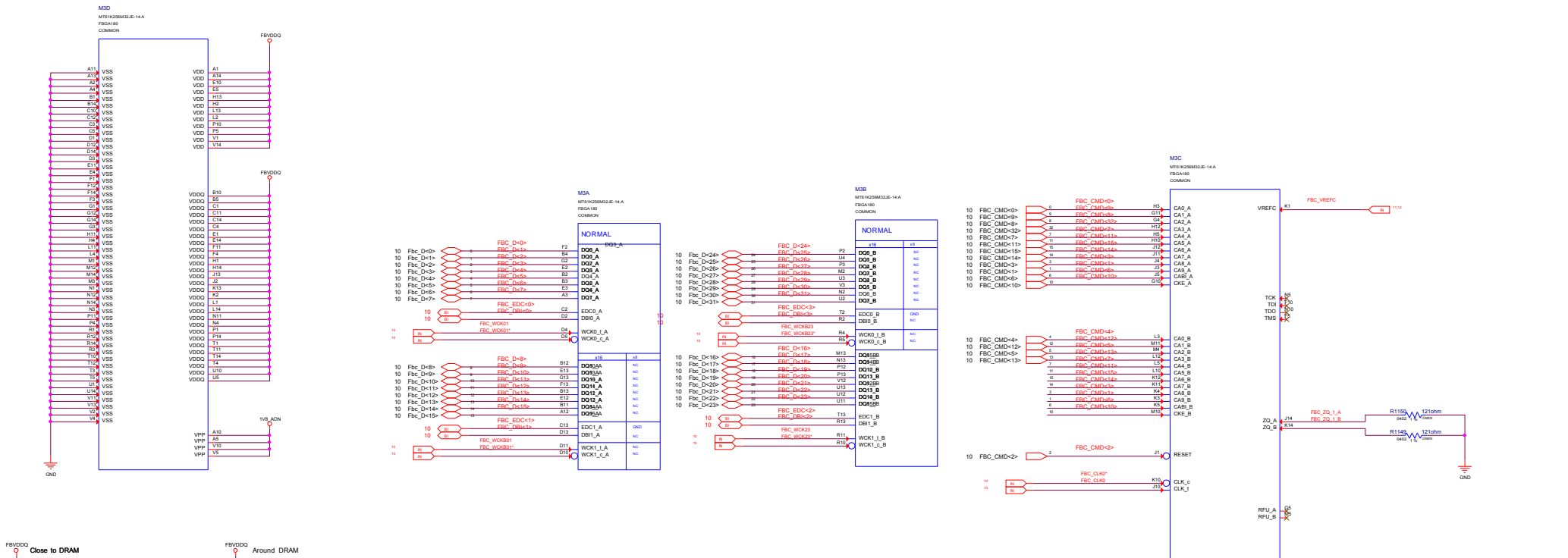
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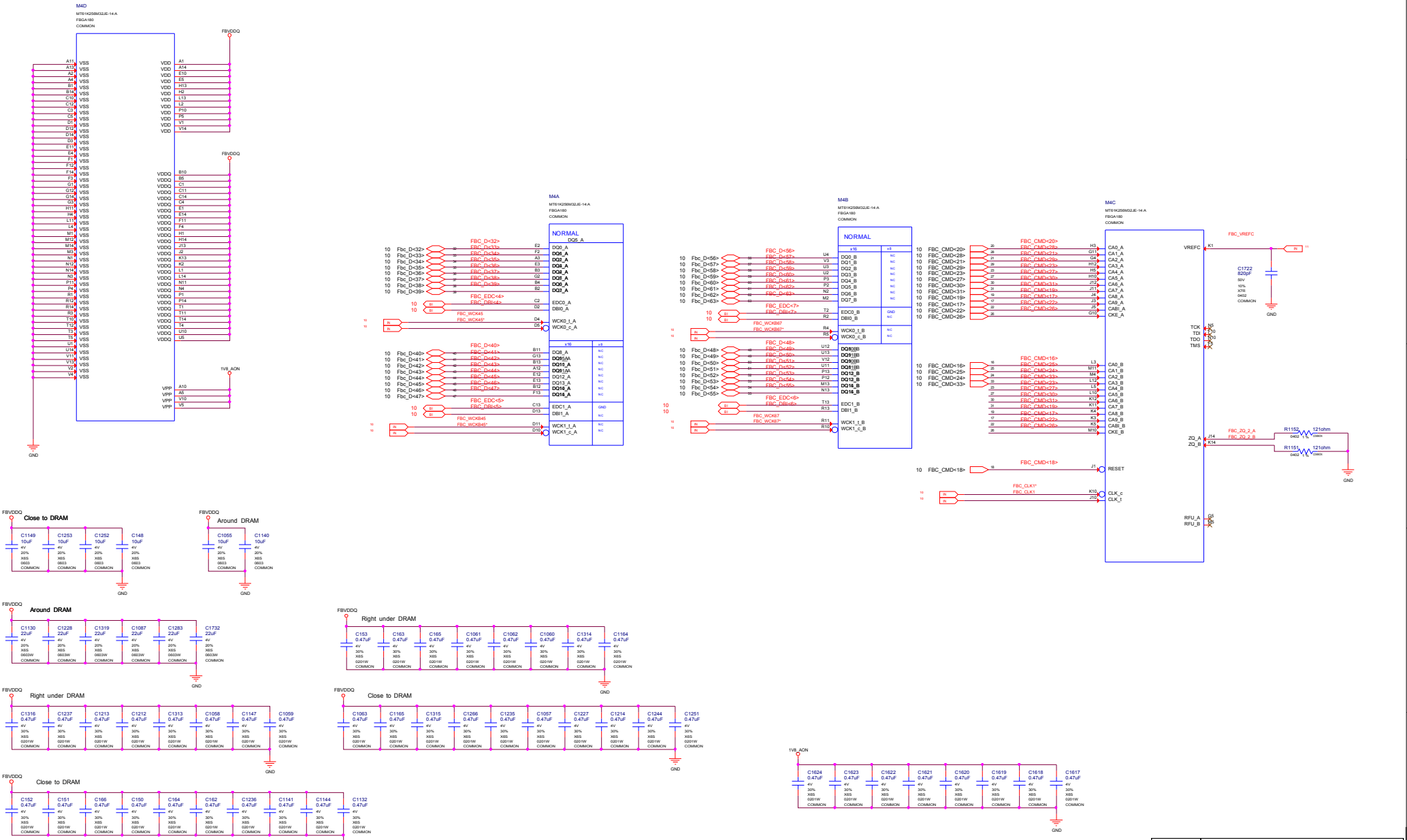


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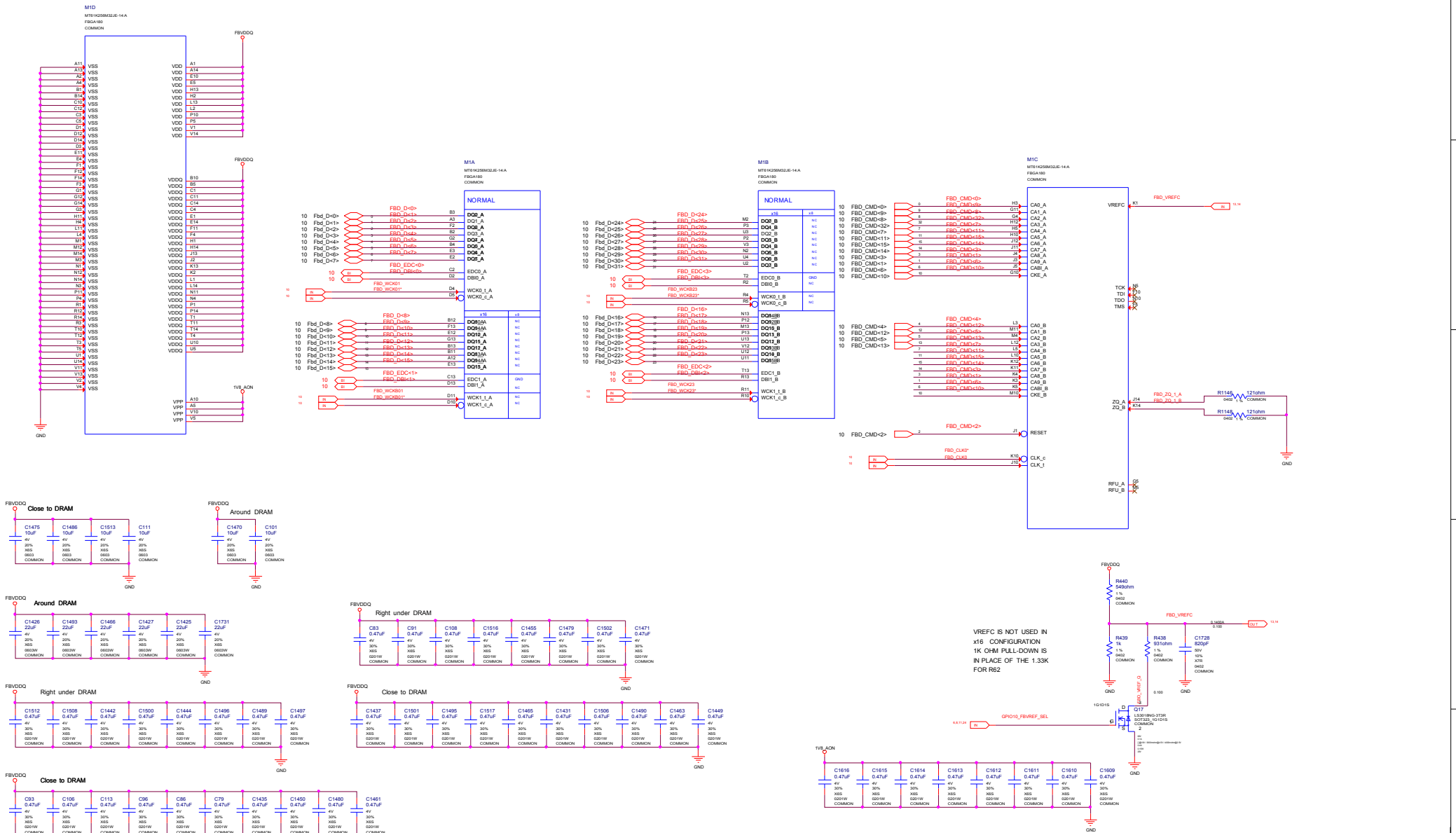
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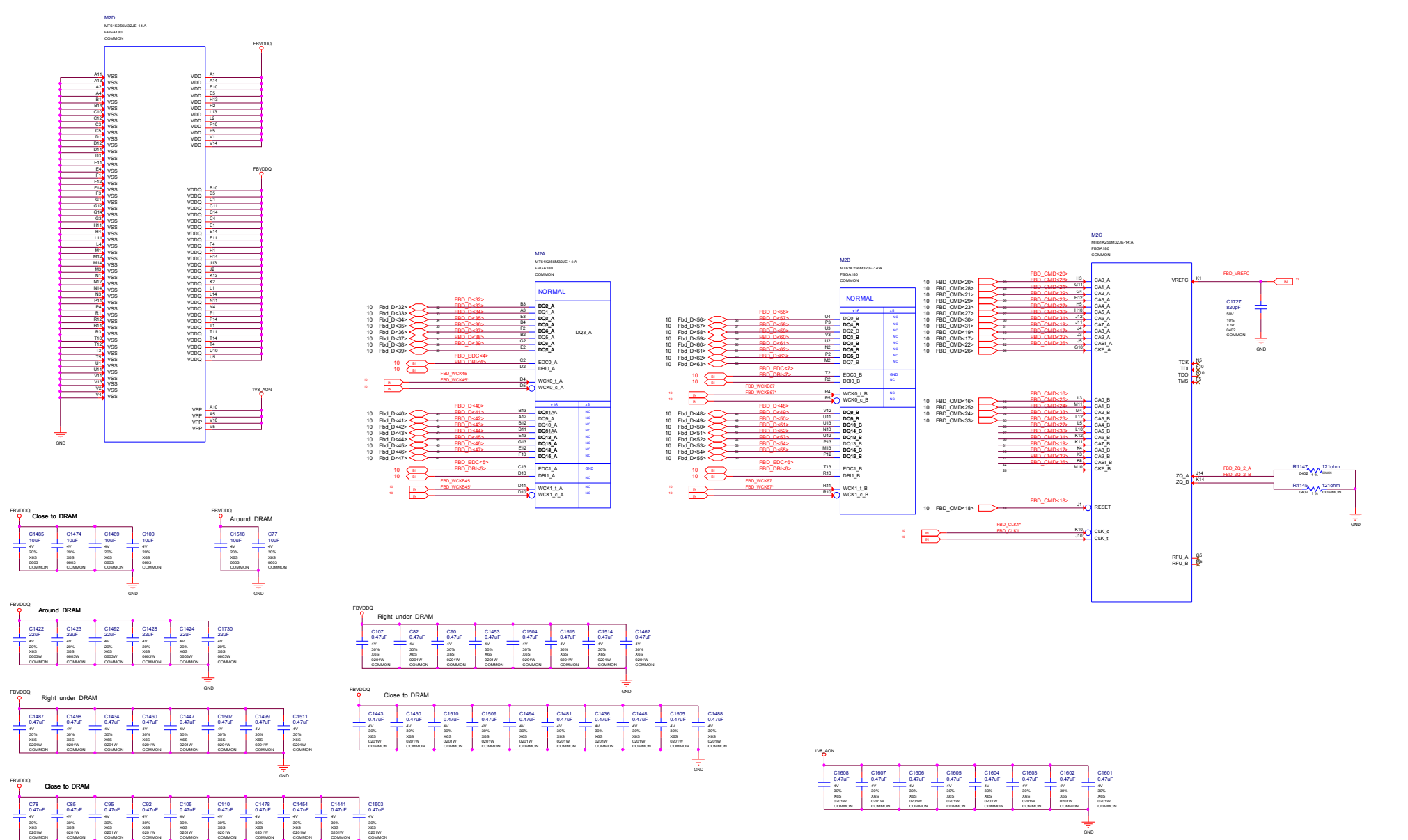


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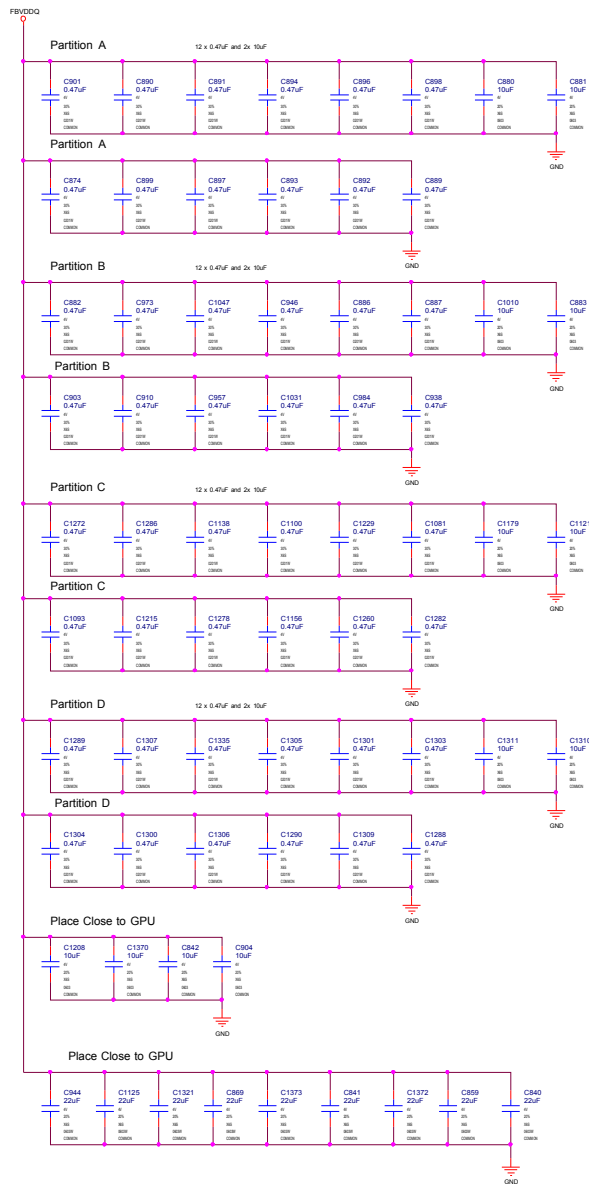


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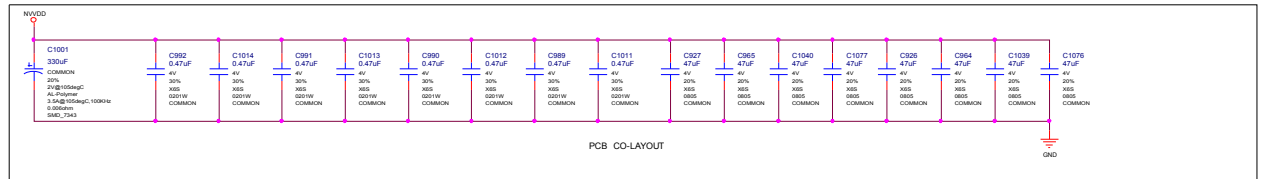
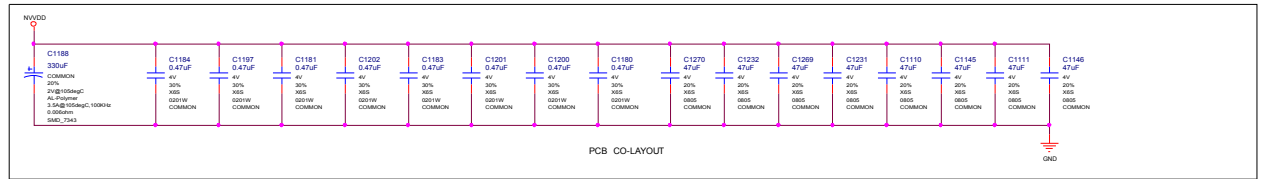
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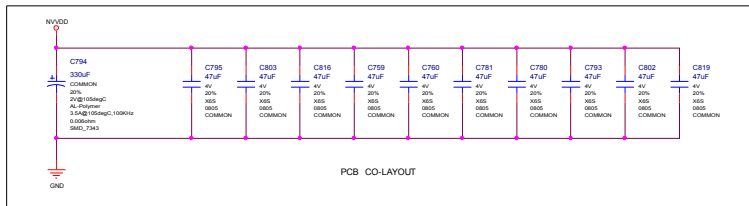
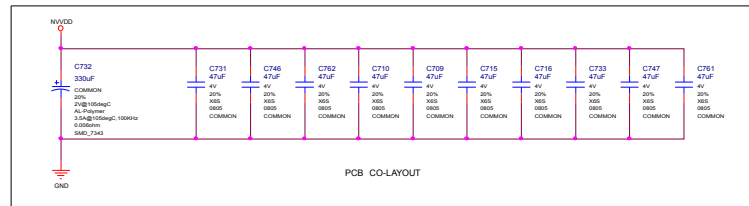
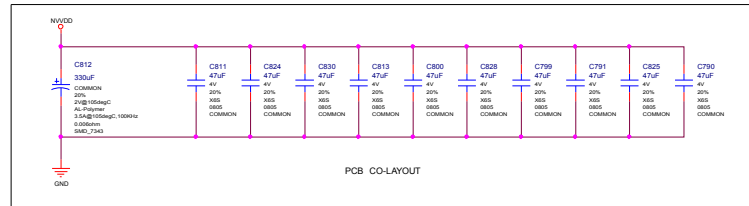
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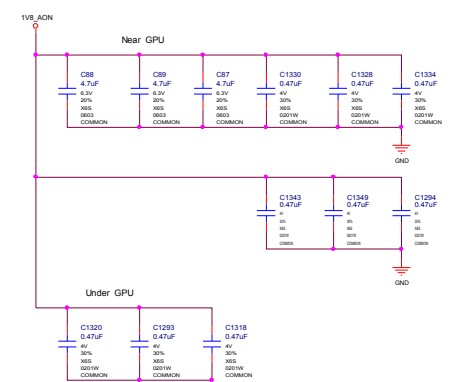
Under GPU



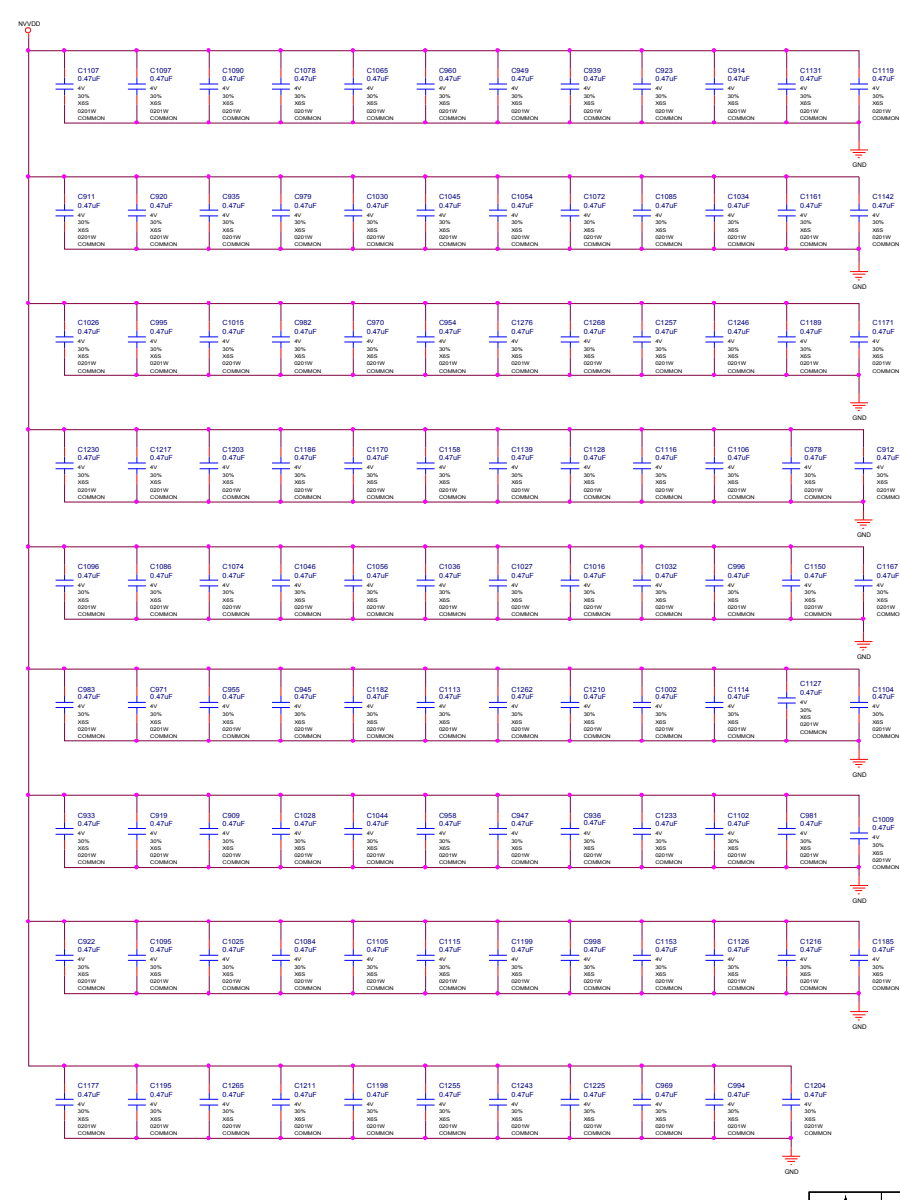
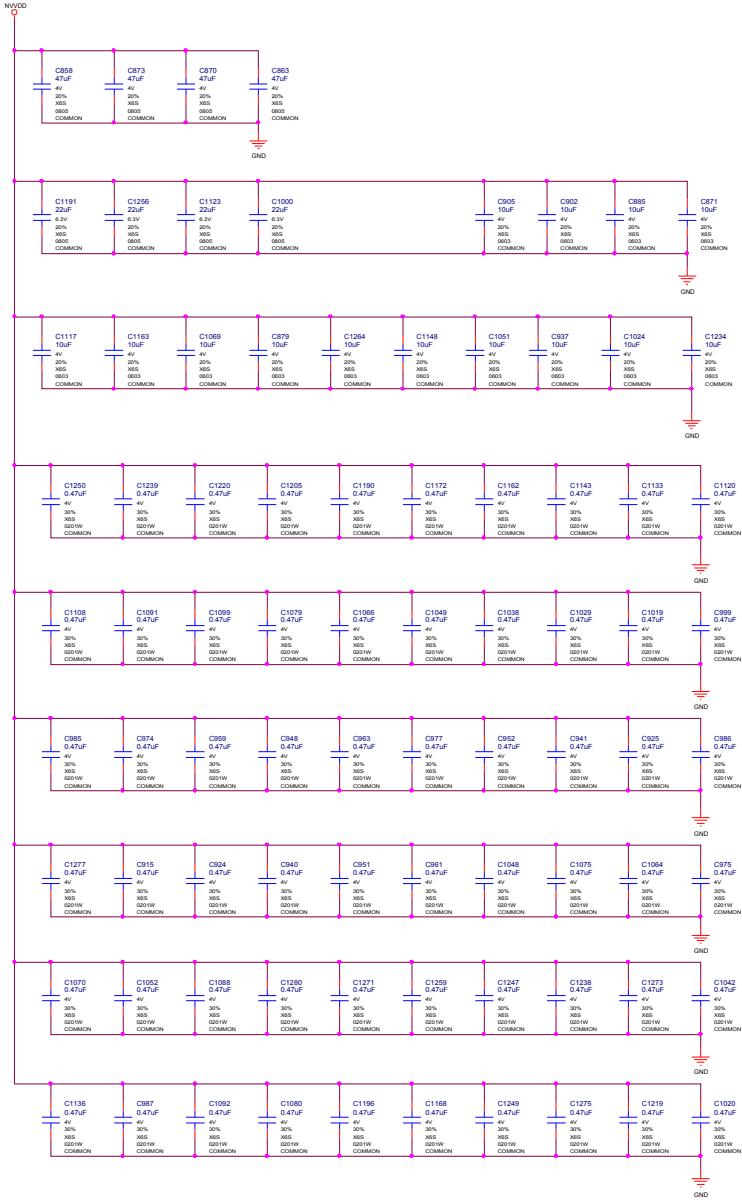
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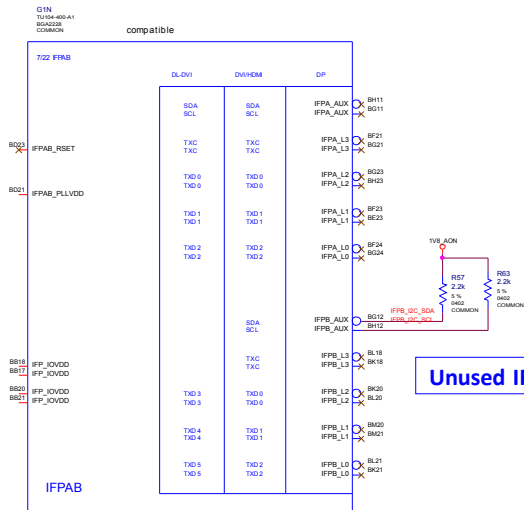
1V8_AON



NVDD



delete Link AB ◦

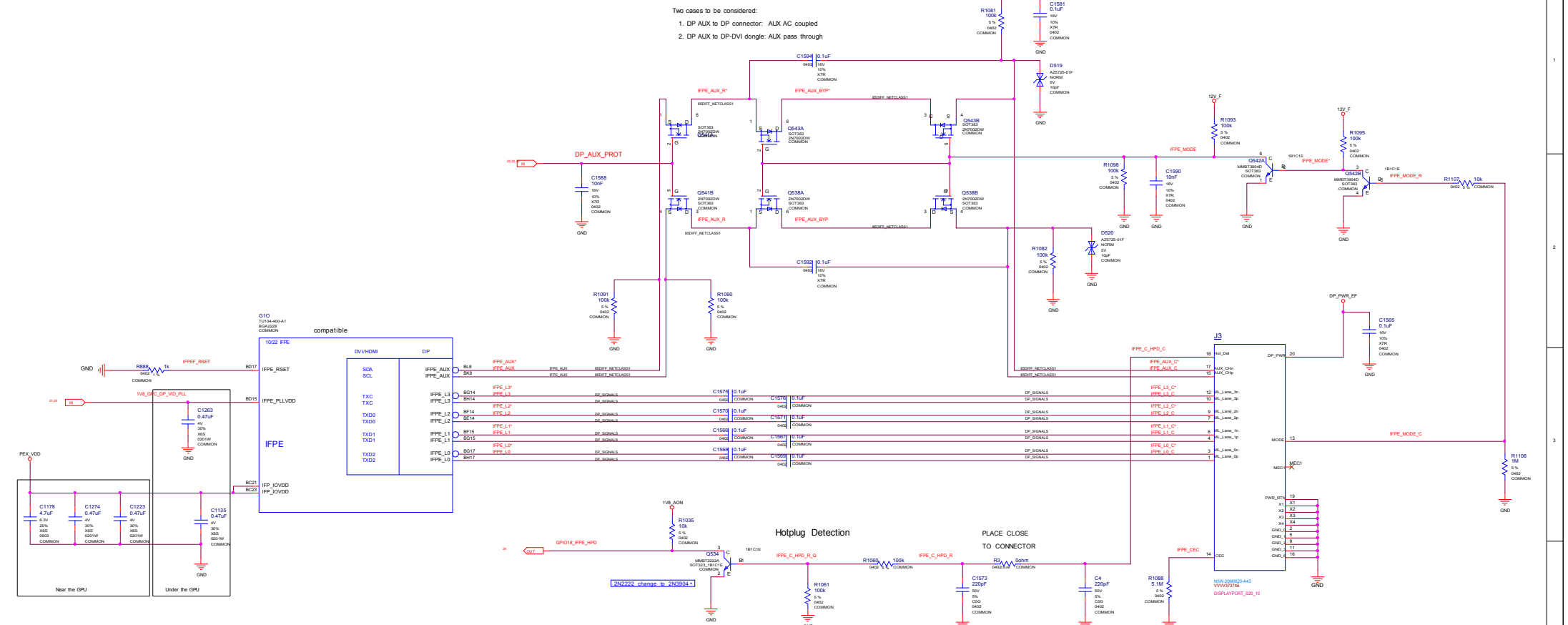


9.3 UNUSED PINS

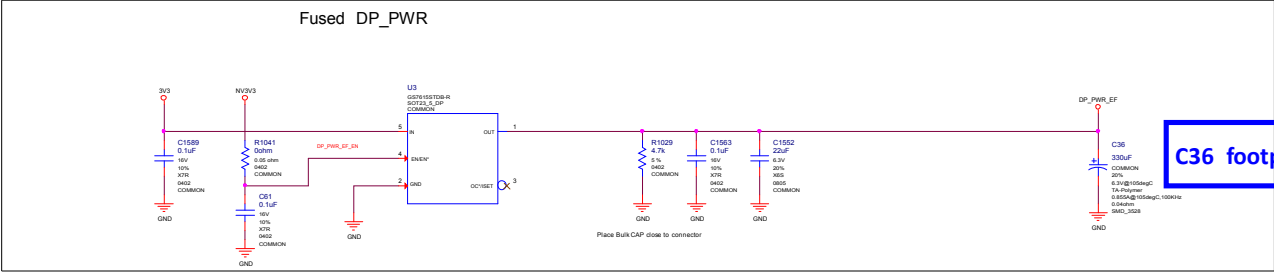
If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use. For example, **If neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD and IFPAB_RSET should be left disconnected, and all signals and references associated with Link A and Link B should also be left unconnected.**

IFP_IOVDD rail can be unconnected if no IFP link is used. If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

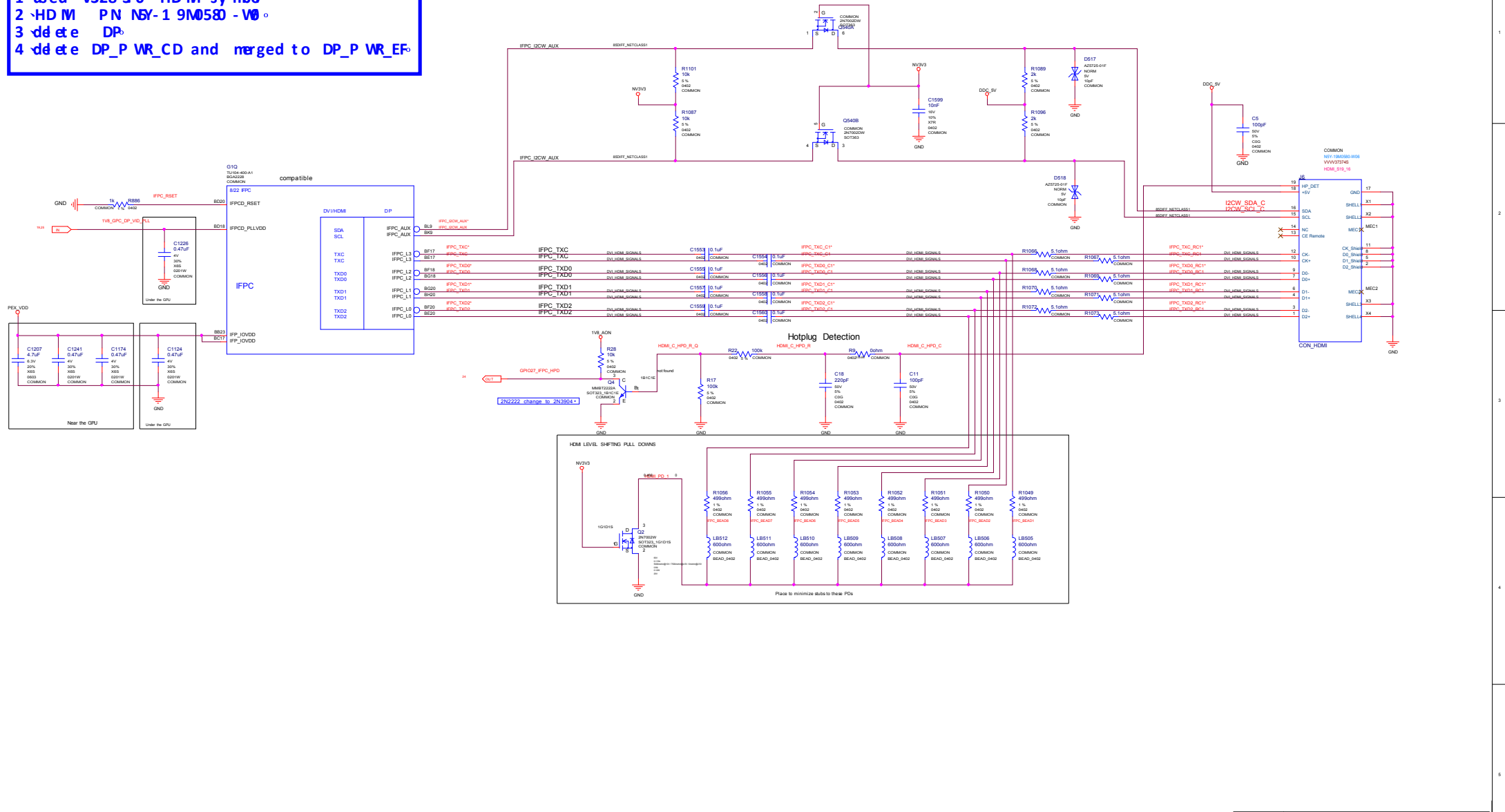
Unused IFPB_I2C* leaving Pull high resistor to 1.8V ◦



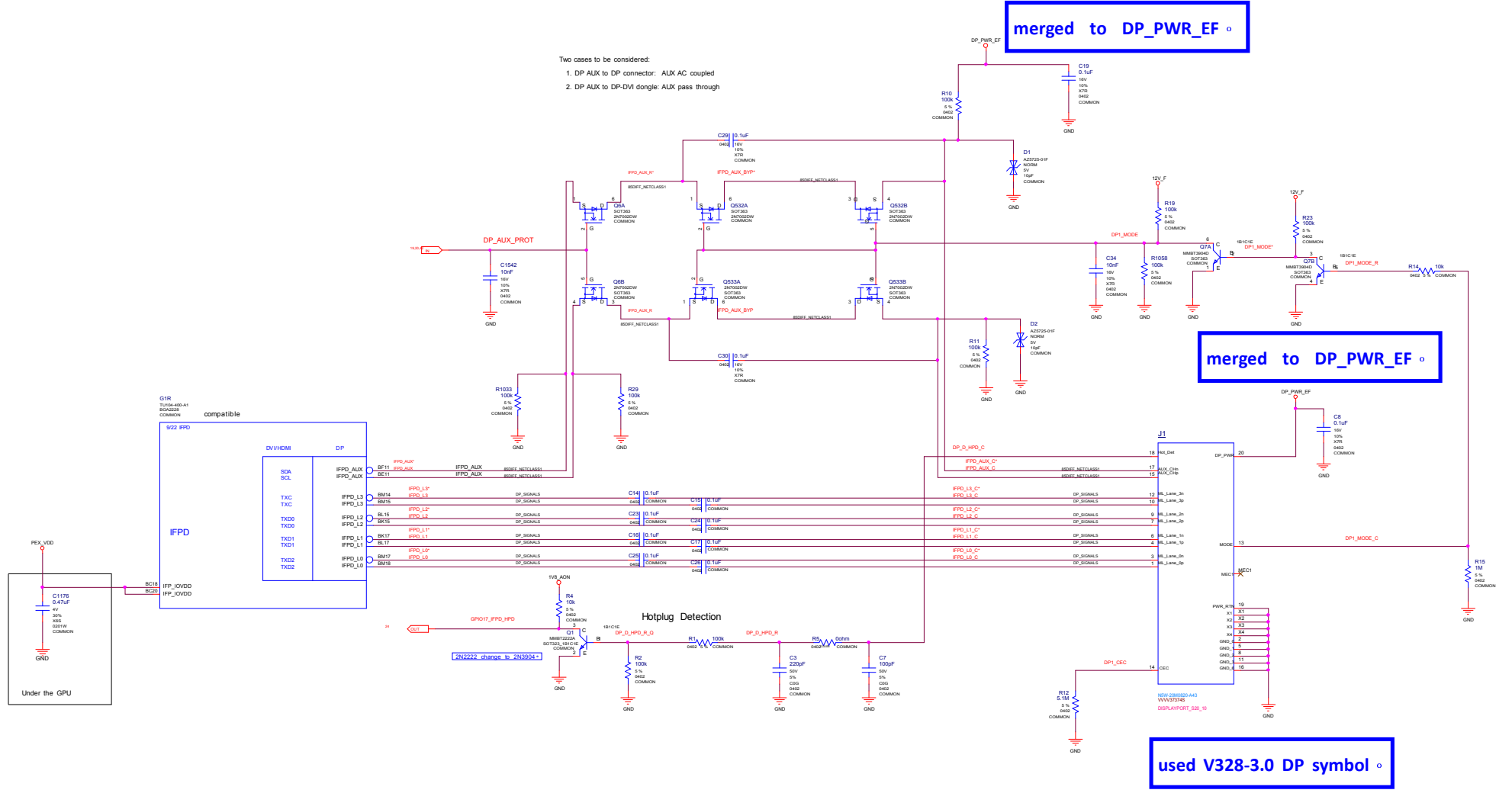
used V328-3.0 DP symbol

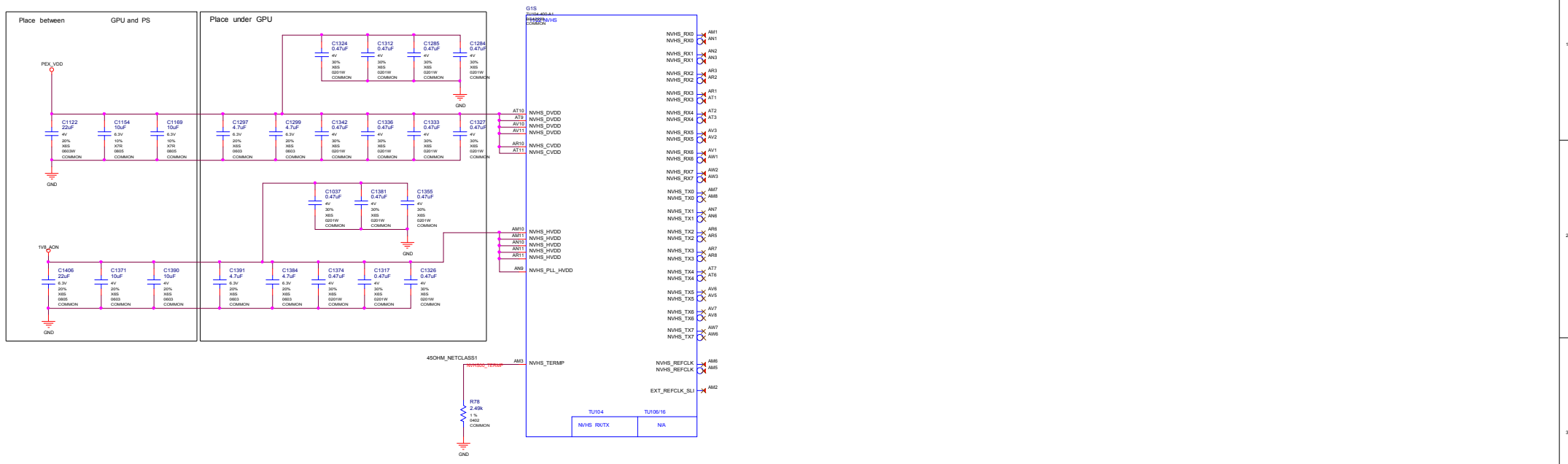


- 1 used V328-3 0 HD M sy mbd
- 2 HD M PN N5Y-1 9M058D - V0
- 3 ddt e DP
- 4 ddt e DP_P WR_CD and merged to DP_P WR_EF



- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

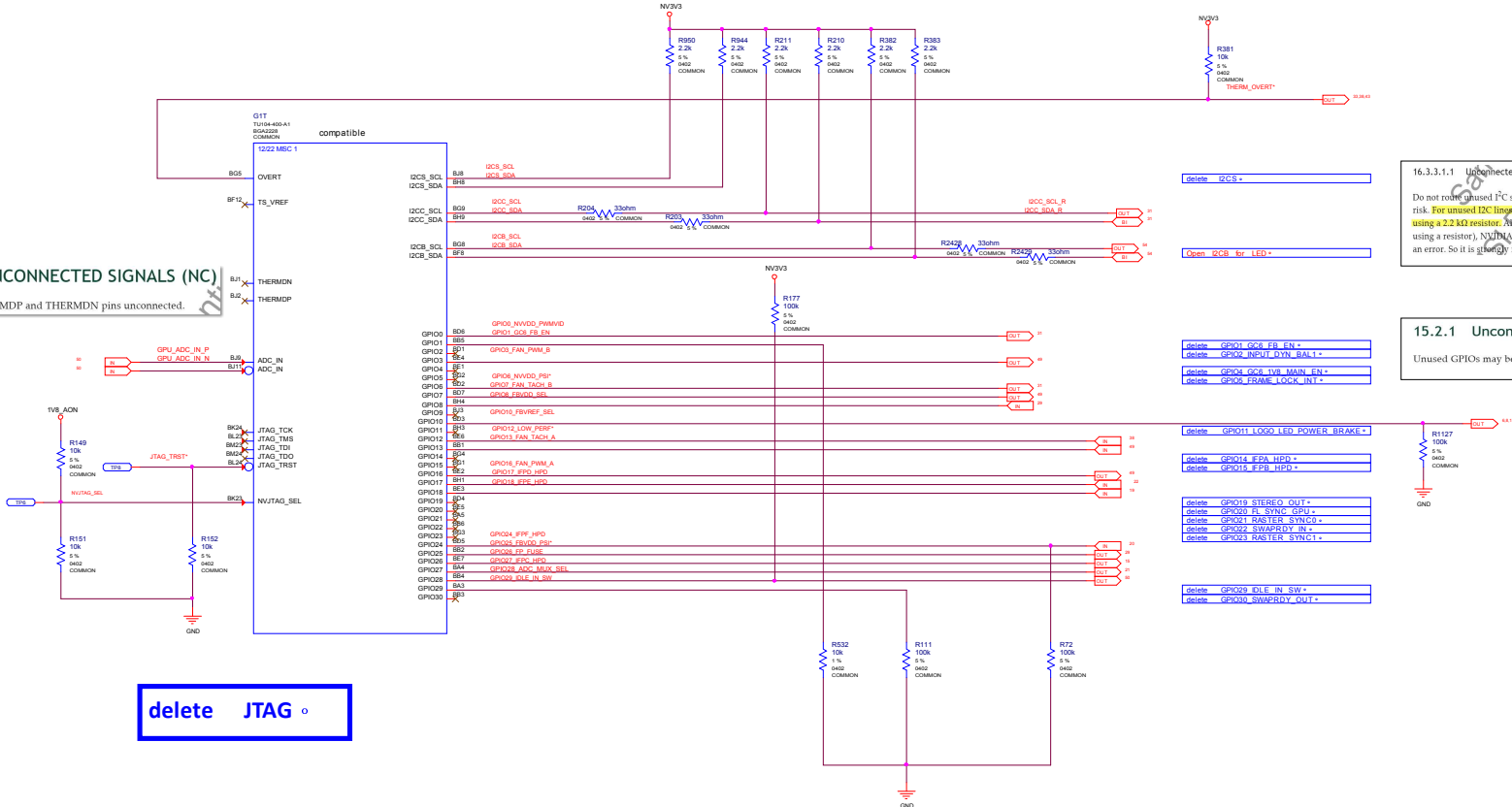




delete Frame Lock ◦

14.5 UNCONNECTED SIGNALS (NC)

Leave the THERMDP and THERMDN pins unconnected.



delete JTAG

Unused delete GPIO11_LOGO_LED_POWER_BRAKE

16.3.3.1.1 Unconnected I2C Pins
Do not route unused I2C signals on the PCB in order to protect the GPU from outside ESD risk. For unused I2C signals, pull both the I2C_SCL and I2C_SDA lines to 1.8V or 3.3V using a 2.2 kΩ resistor. Although unused I2C lines can be soft-grounded (that is, grounded using a resistor), NVIDIA's diagnostic program expects them to be pulled up and will flag an error. So it is strongly recommended that unused I2C lines be pulled up.

15.2.1 Unconnected Signals
Unused GPIOs may be left floating (NC) on the board design.

Unused delete STEREO

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

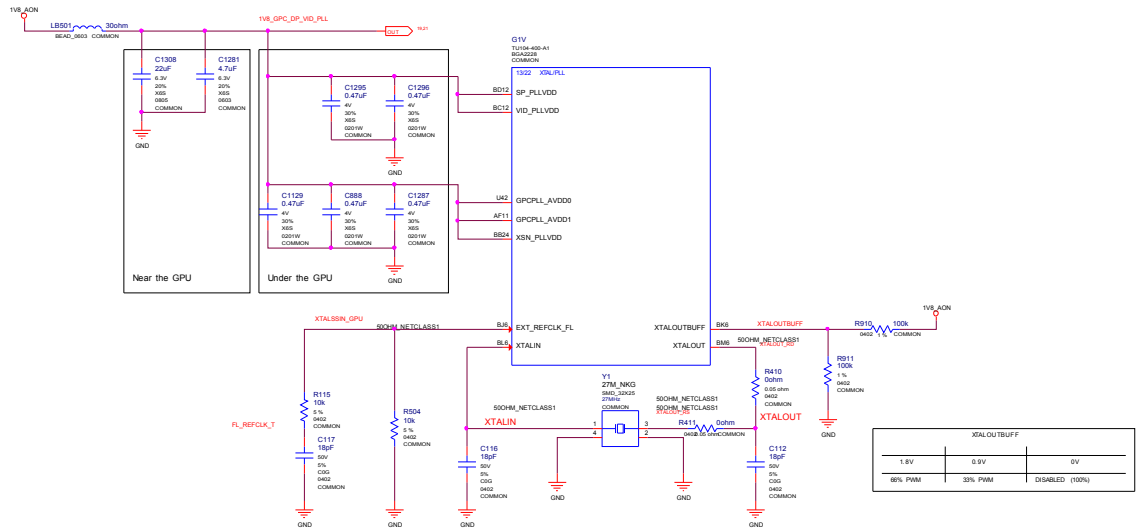
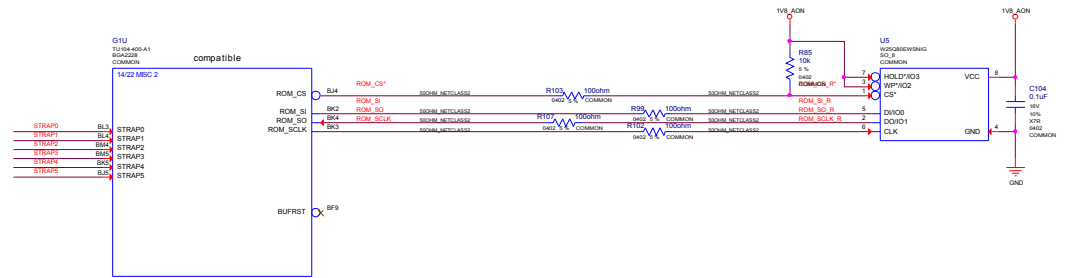
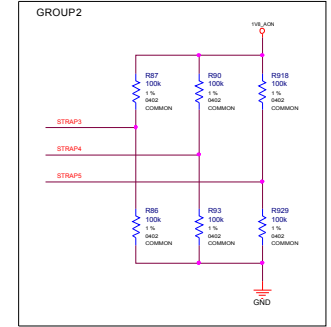
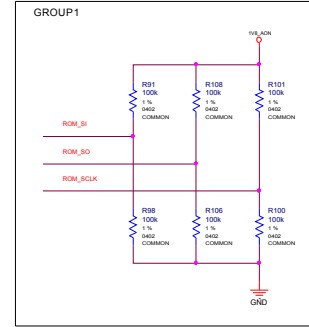
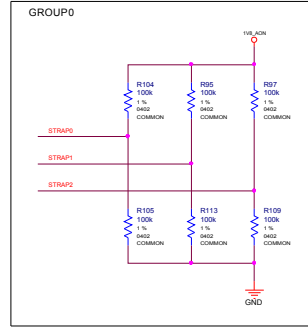
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]	FS_OVERT	1.ENABLE 0.DISABLE	DEFAULT
L	L	L	XXX1		FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0		FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCI_E_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

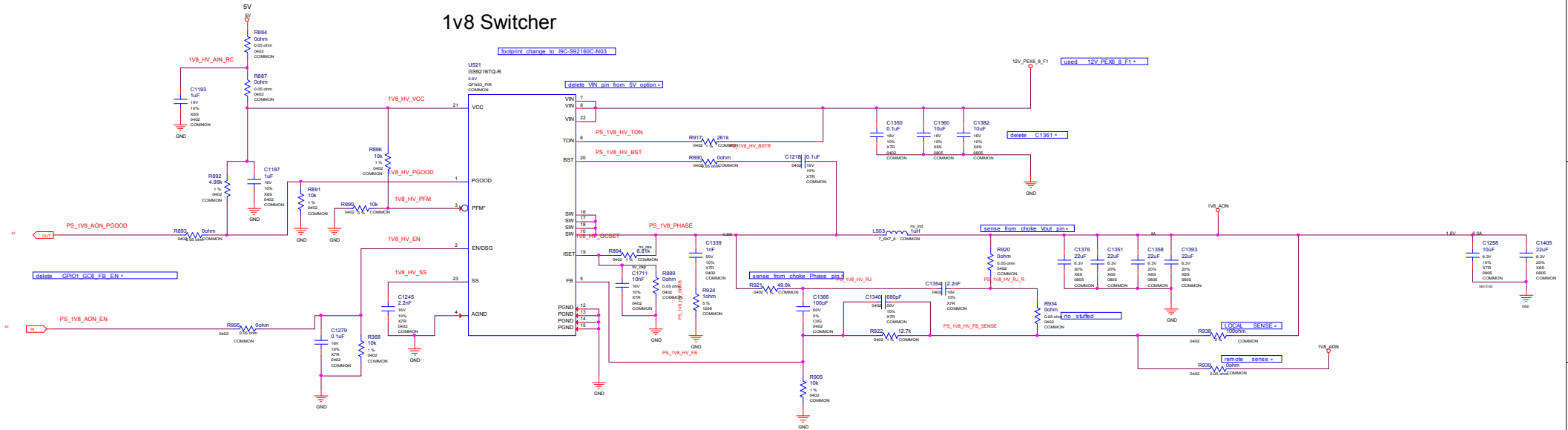
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCI_E_CFG LOW POWER
0:PCI_E_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



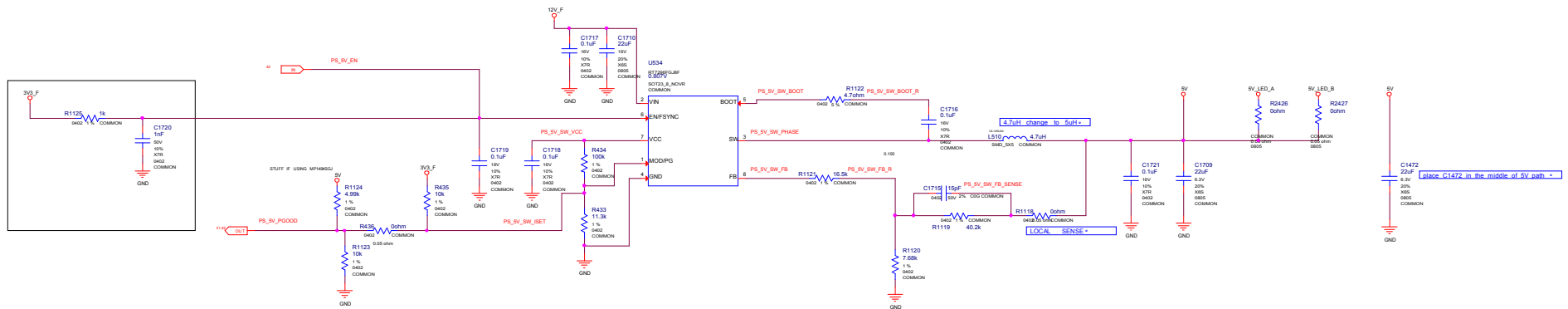
XTALOUTBUFF		
1.8V	0.9V	0V
86% PWM	33% PWM	DISABLED (100%)


1v8 Switcher



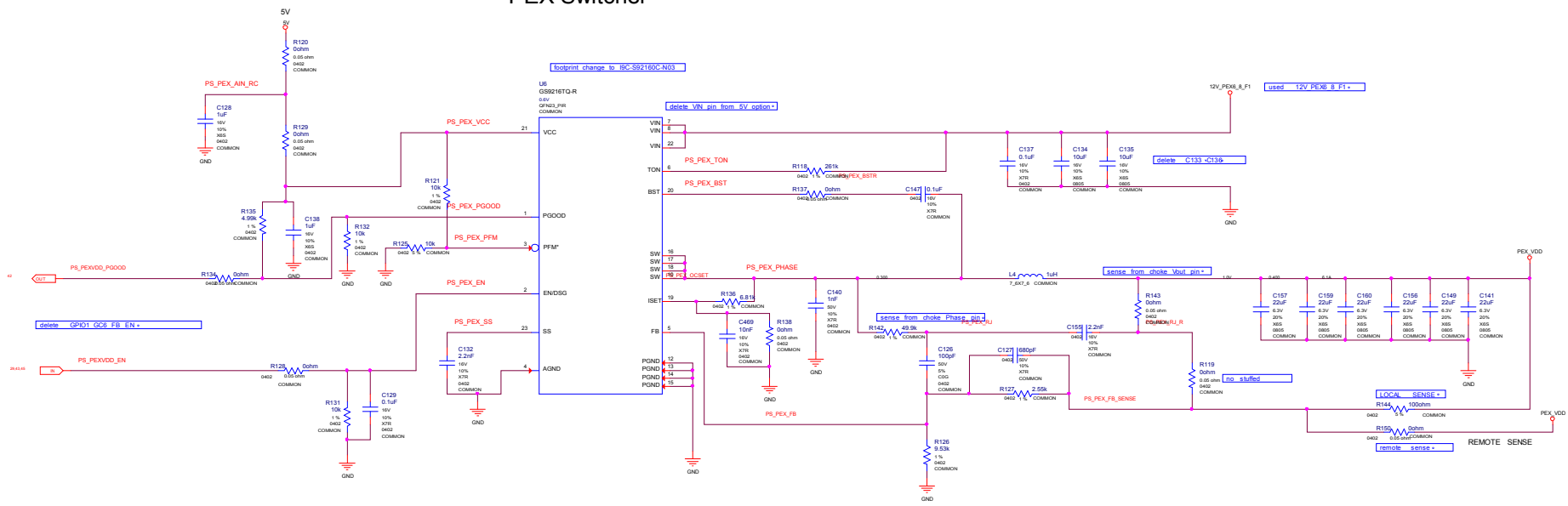
- 1 L503 PNL04-01074K0-L65 / footprint : CHK_S2_7_3X6_61
- 2 delete colayout PWM output choke
- 3 delete 1V8_MA N and merged to 1V8_AON

- 1 L510 P N L04-0507010-L65 / footprint : CHK_S2_5_4X5_23
- 2 d d e colayout P WM output choke
- 3 unused RTD3 d d e Buck Boost regulat or

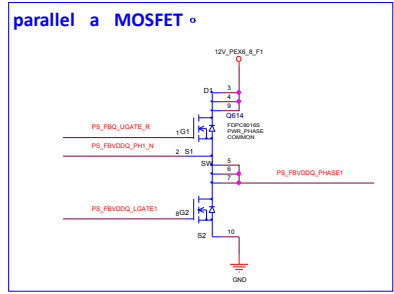
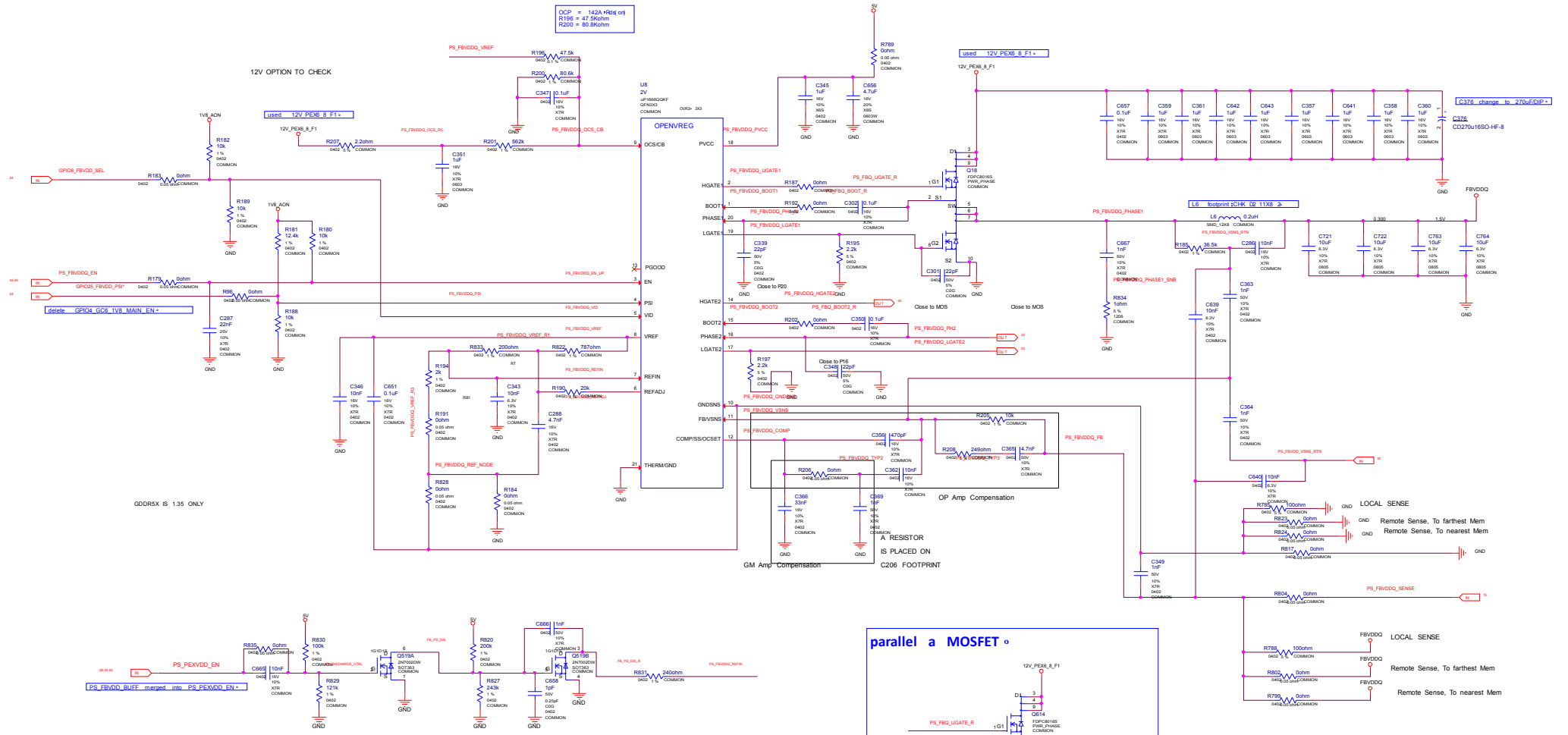


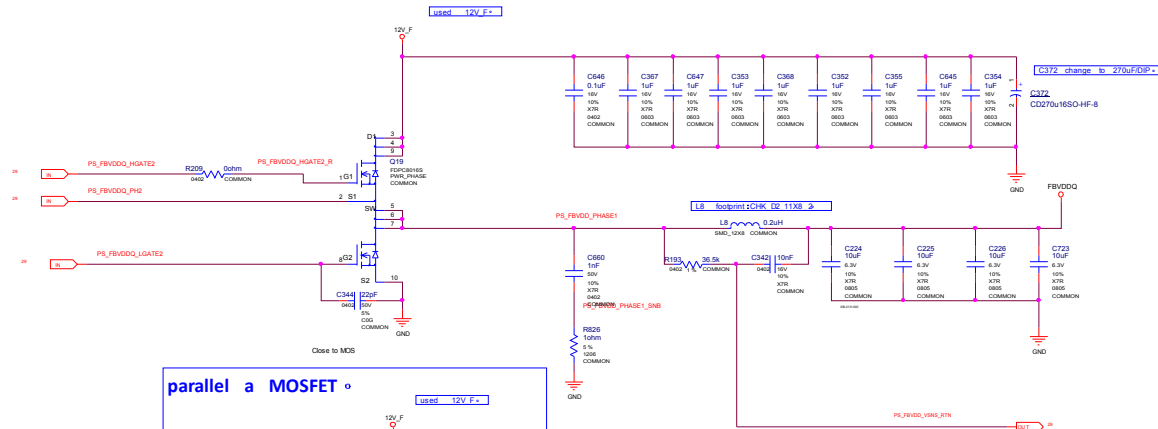
				MICRO-STAR INT'L CO.,LTD		
				MS-V375		
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PEX Switcher

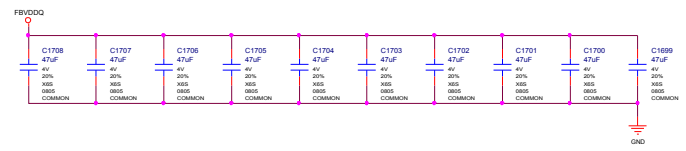
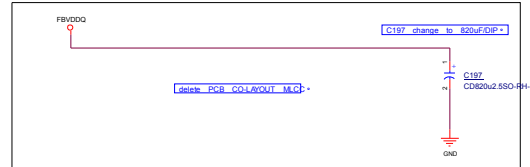
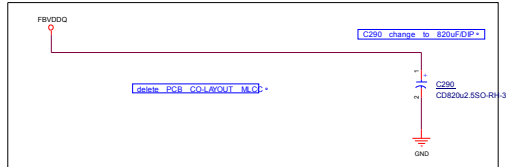
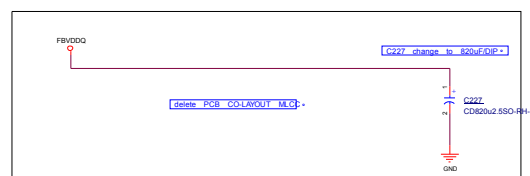
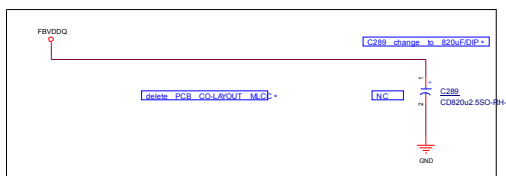
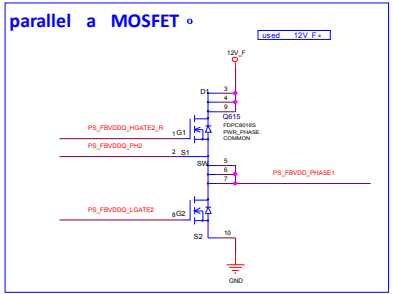


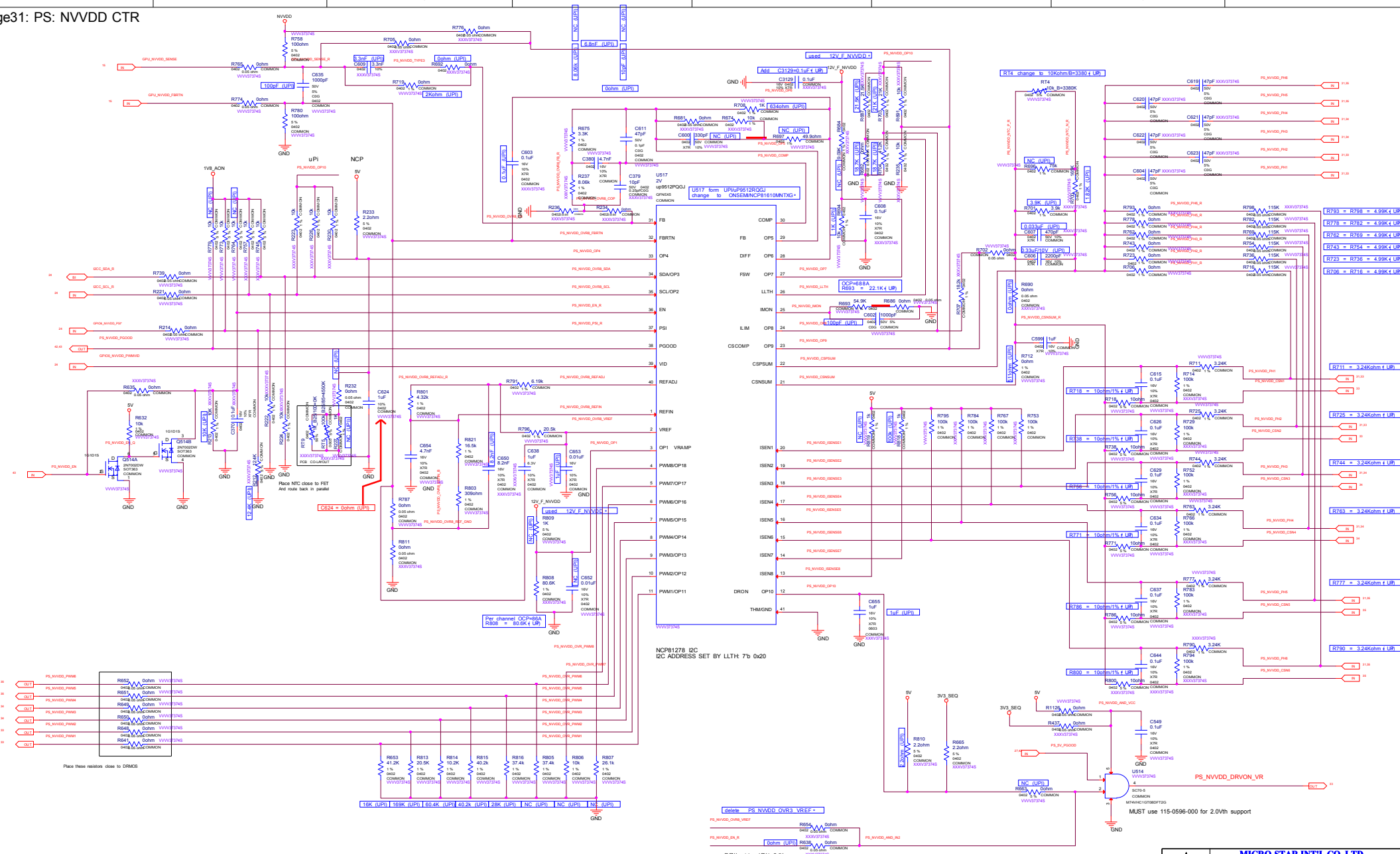
1 L4 PN L04-0107410-L65 / footprint : CHK_S2_7_3X6_61
 2 delete colayout PWM output choke






delete RTD3 backdrive ◦

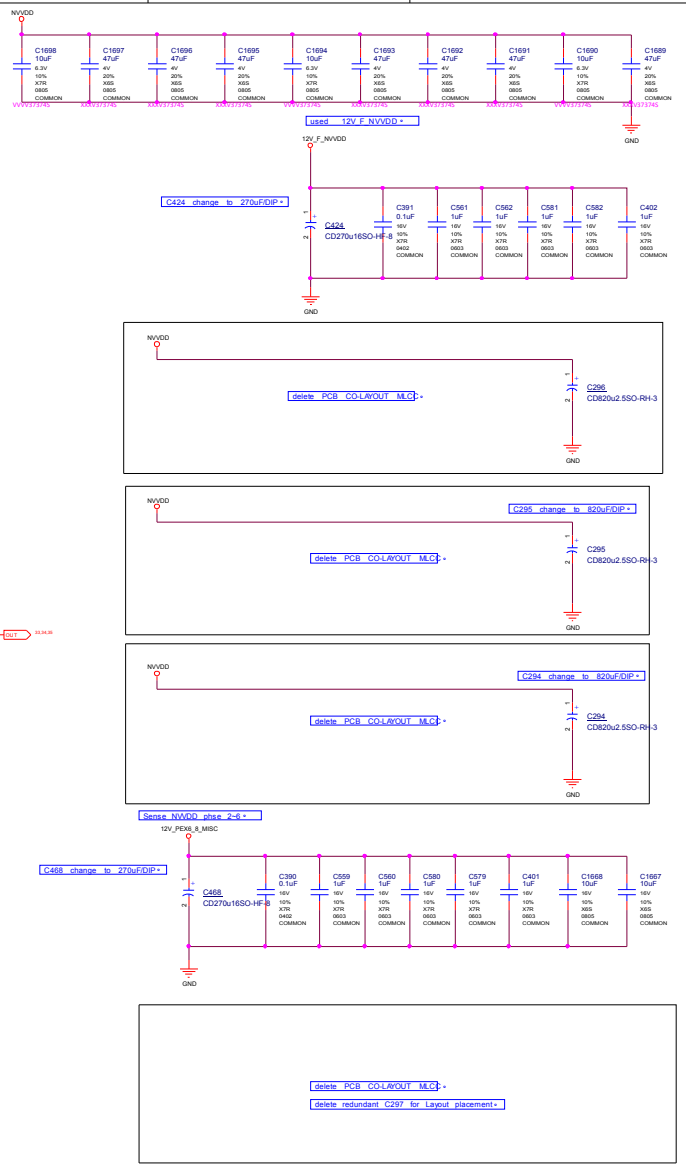
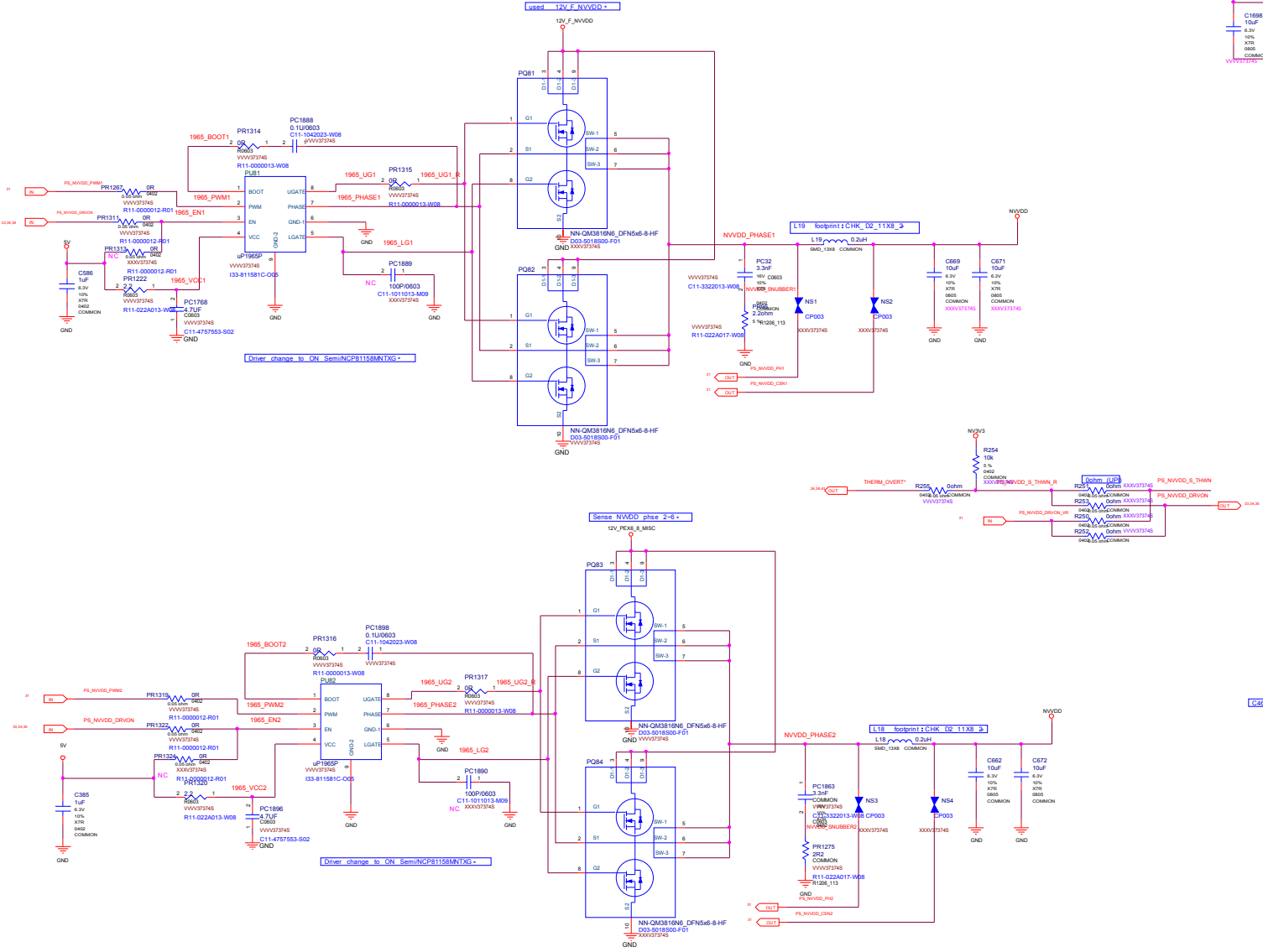


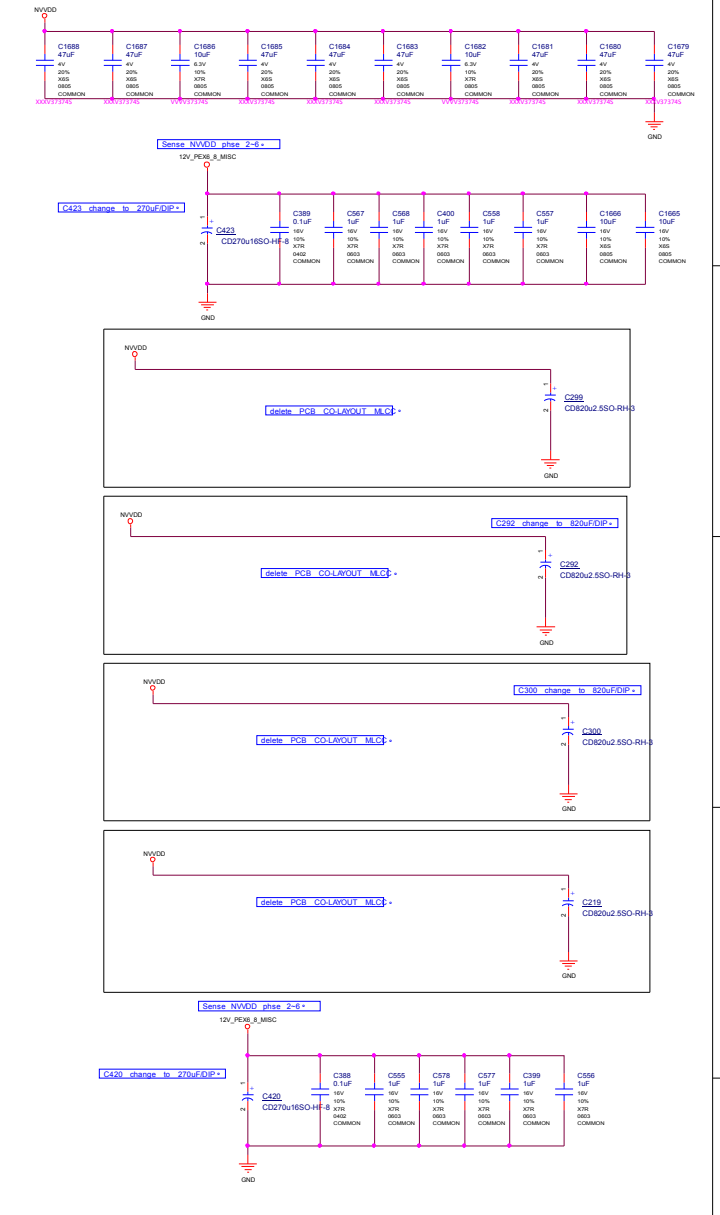
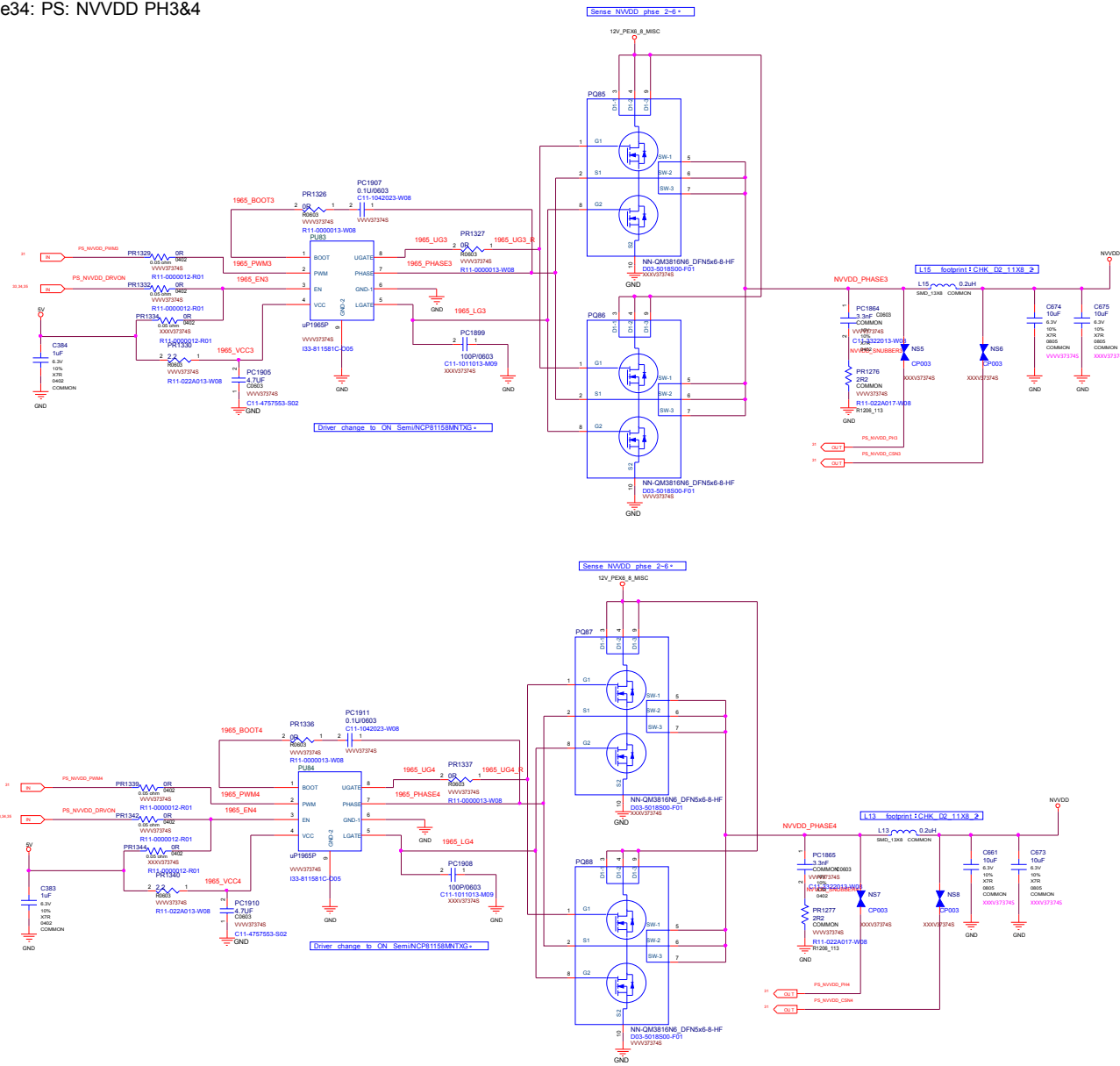


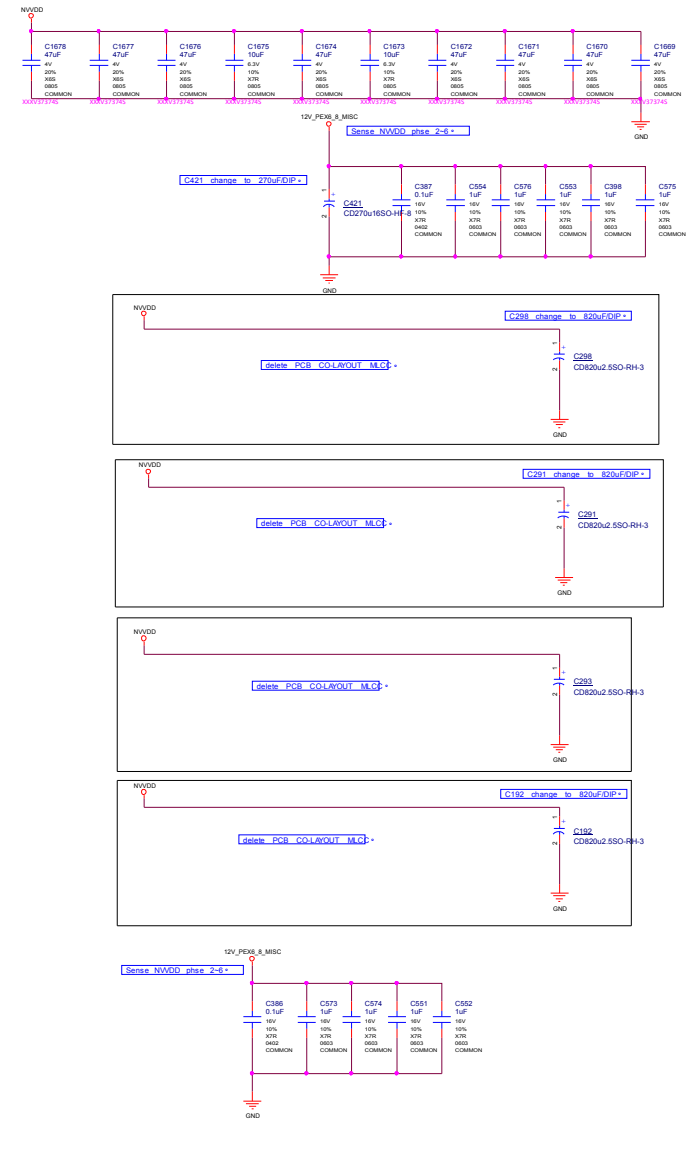
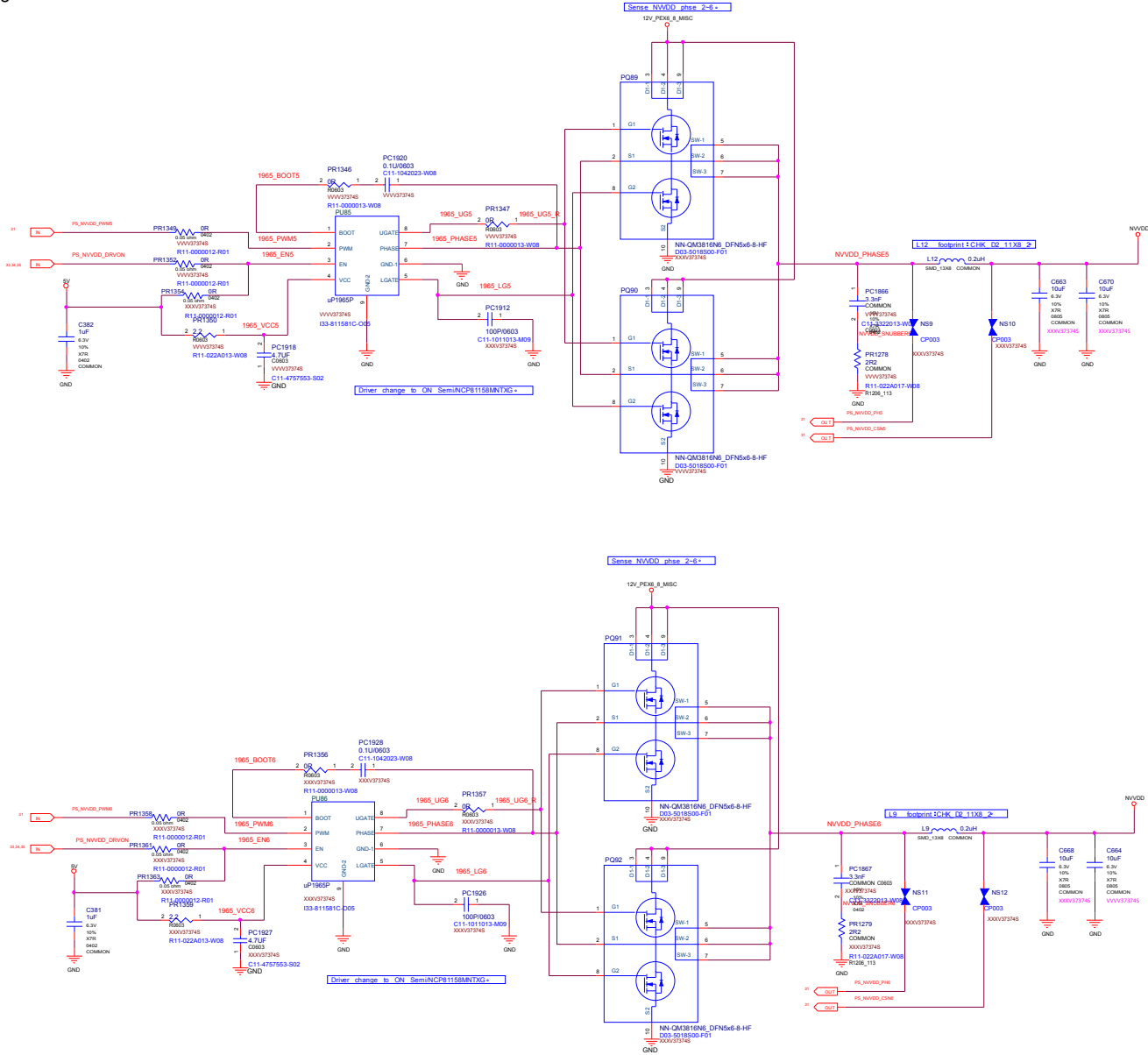
- Place these resistors close to DRMS
- R852 10k
- R853 41.2k
- R854 10k
- R855 10k
- R856 10k
- R857 10k
- R858 10k
- R859 10k
- R860 10k
- R861 10k
- R862 10k
- R863 10k
- R864 10k

delete all unused

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removed U511 for fixed NVVDD 12V input:
1 merged 3V3_AON to 3V3_F
2 unused and delete 3V3_AUX
3 unused and delete 3V3_AUX_CON
4 NVVDD_DYN_VIN merged to 12V_PEX6_8_F1

delete GPDI2_INOUT_DYN_BAL1

delete INPUT_PEX6_D11_STEER

- 1 changed EXT 12V 8pin PN and footprint
- 2 add EXT 12V 8pin Fuse
- 3 delete unused parts
- 4 RSENSE 3 change to sense NVVDD PEX 12V
- 5 RSENSE 4 change to sense NVVDD EXT 12V
- 6 change RSENSE parts and footprint

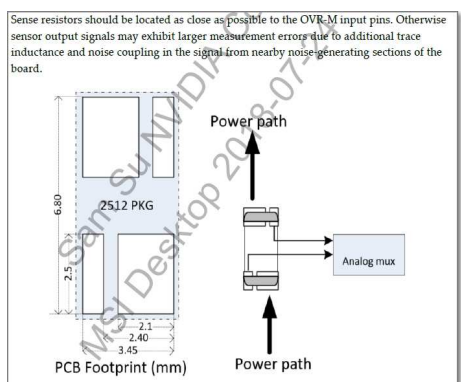
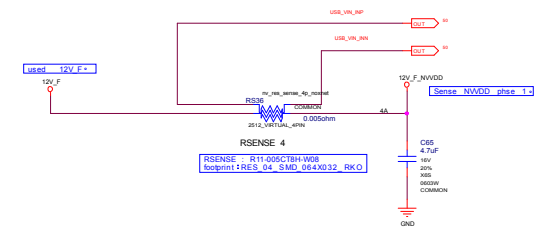
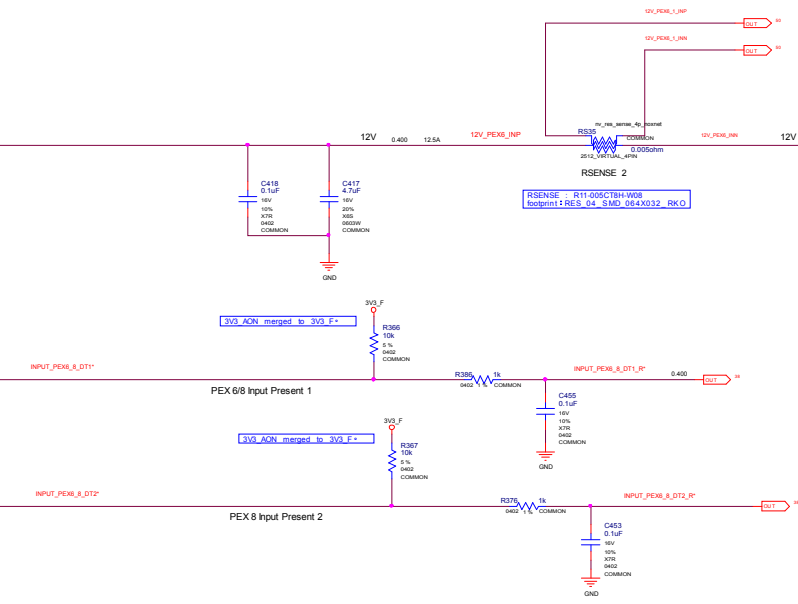
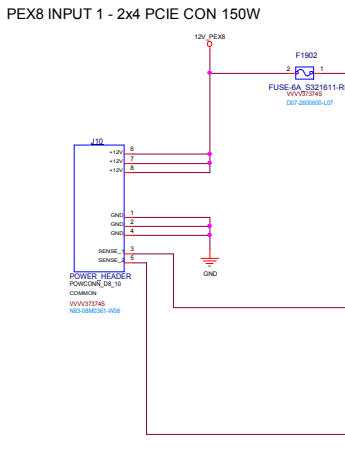
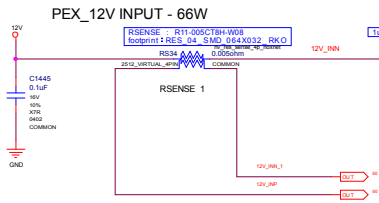
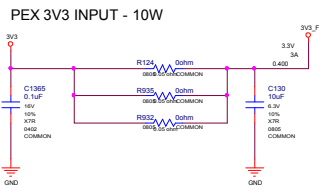
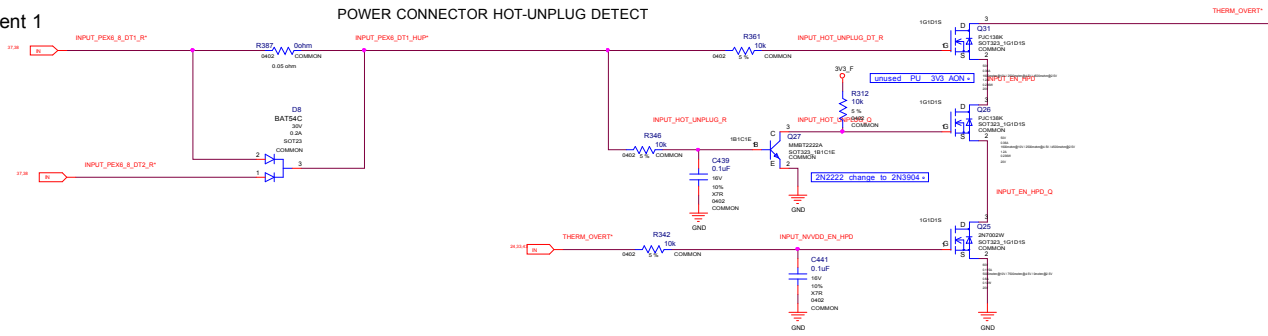


Figure 5.10 Connection for 2-Pin Sense Resistor (2512 Package)
 If customer prefers using a 2-pin sense resistor instead, we recommend implementing a 4-pin footprint with two large PADS for the high current path and two small PADS for sensing line, to emulate the functionality of a 4-pin resistor.

Note: Two-pin sense resistor can be used, but the sensing signal MUST connect to resistor pad directly. Connect the sensing signal to nearby power plane may cause large measurement error.

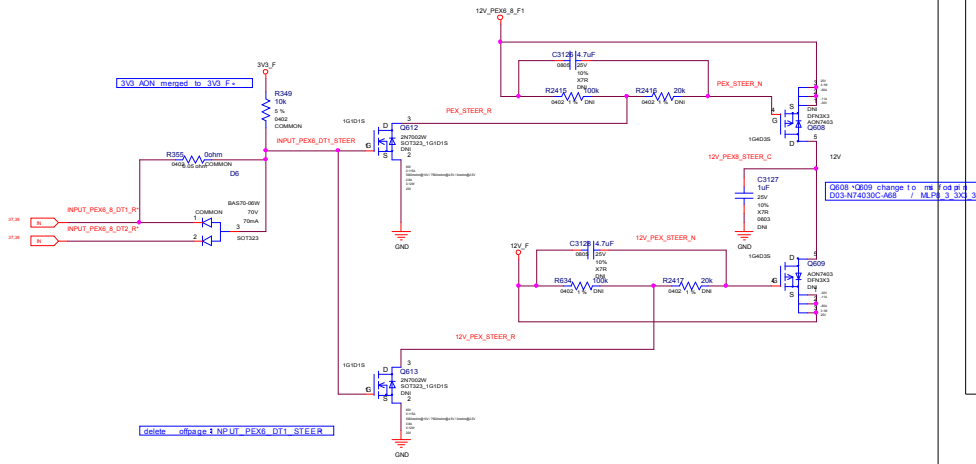
PEX Input Present 1



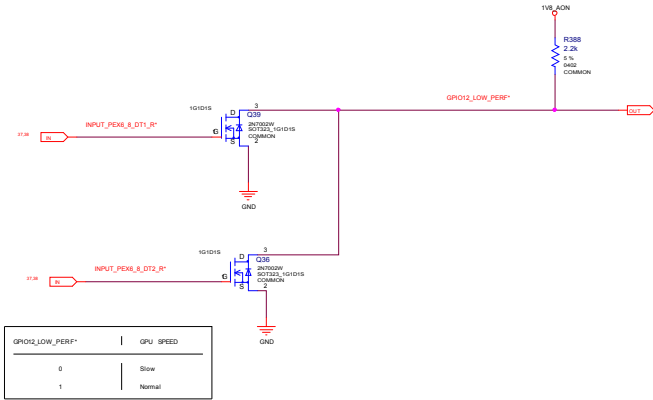
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

copied 12V CURRENT STEERING from V373-2.0 and BOM stuff ed



PEX Input - Power Level/PSI* Control



delete regulator for USBC_VBUS ◦

Unused USB_I2C* leaving Pull high resistor to 1.8V ◦

delete PPC ◦

Unused USB_I2C* leaving Pull high resistor to 1.8V ◦

Unused IFPB_I2C* leaving Pull high resistor to 1.8V ◦

delete GPC04_IFPB_HFD ◦

delete PEX_EST_BUF* ◦

delete GPC01_GCS_FB_EN* ◦

	MICRO-STAR INT'L CO.,LTD		
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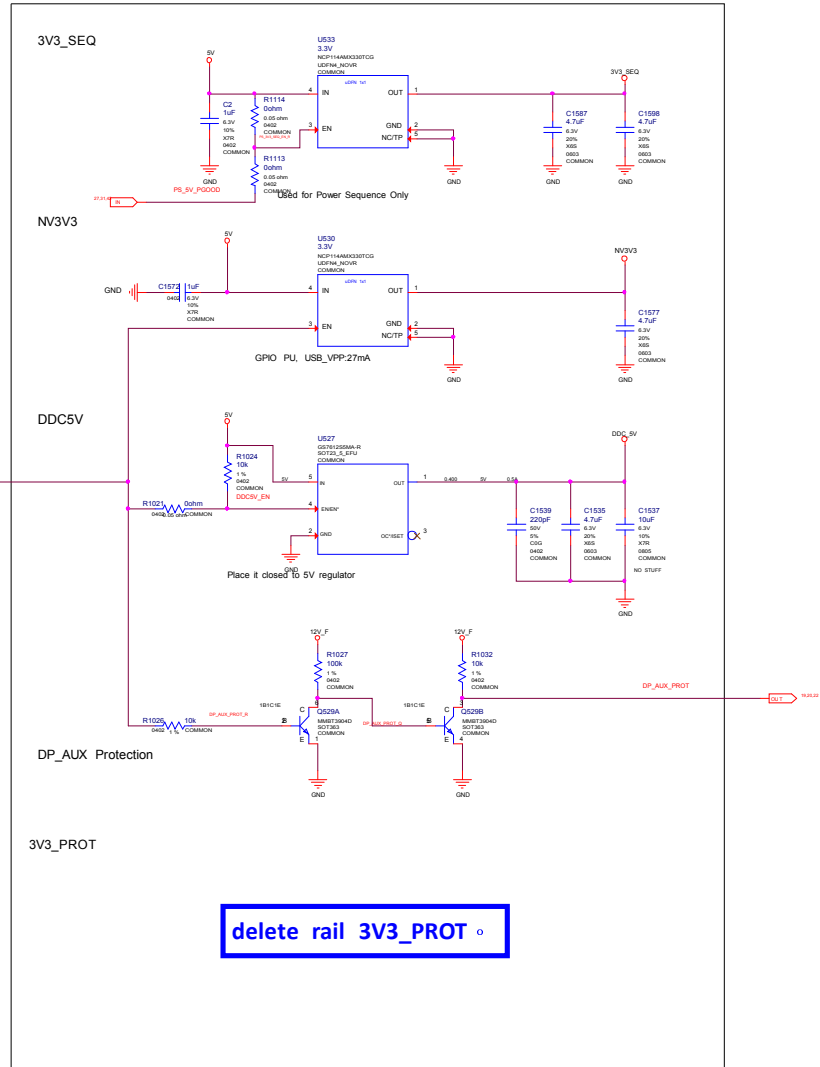
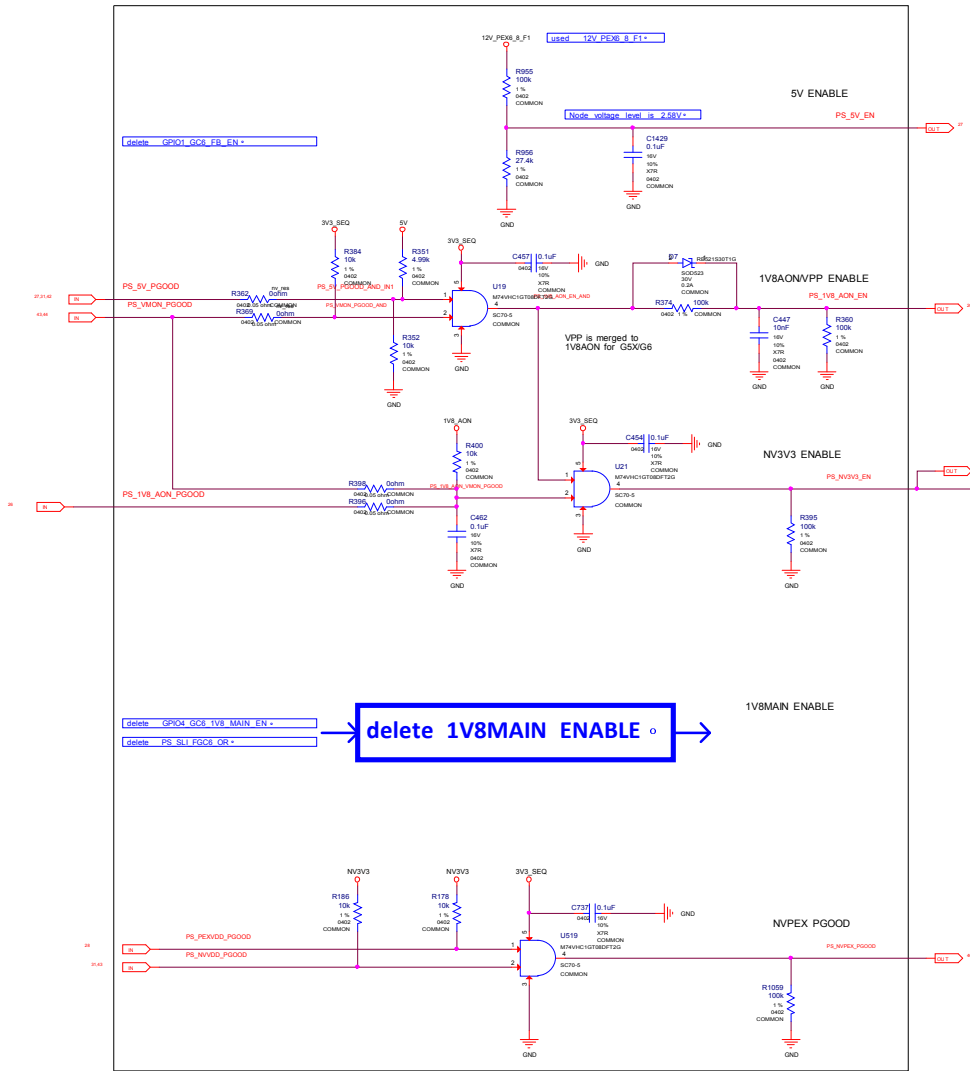
unused and delete all °

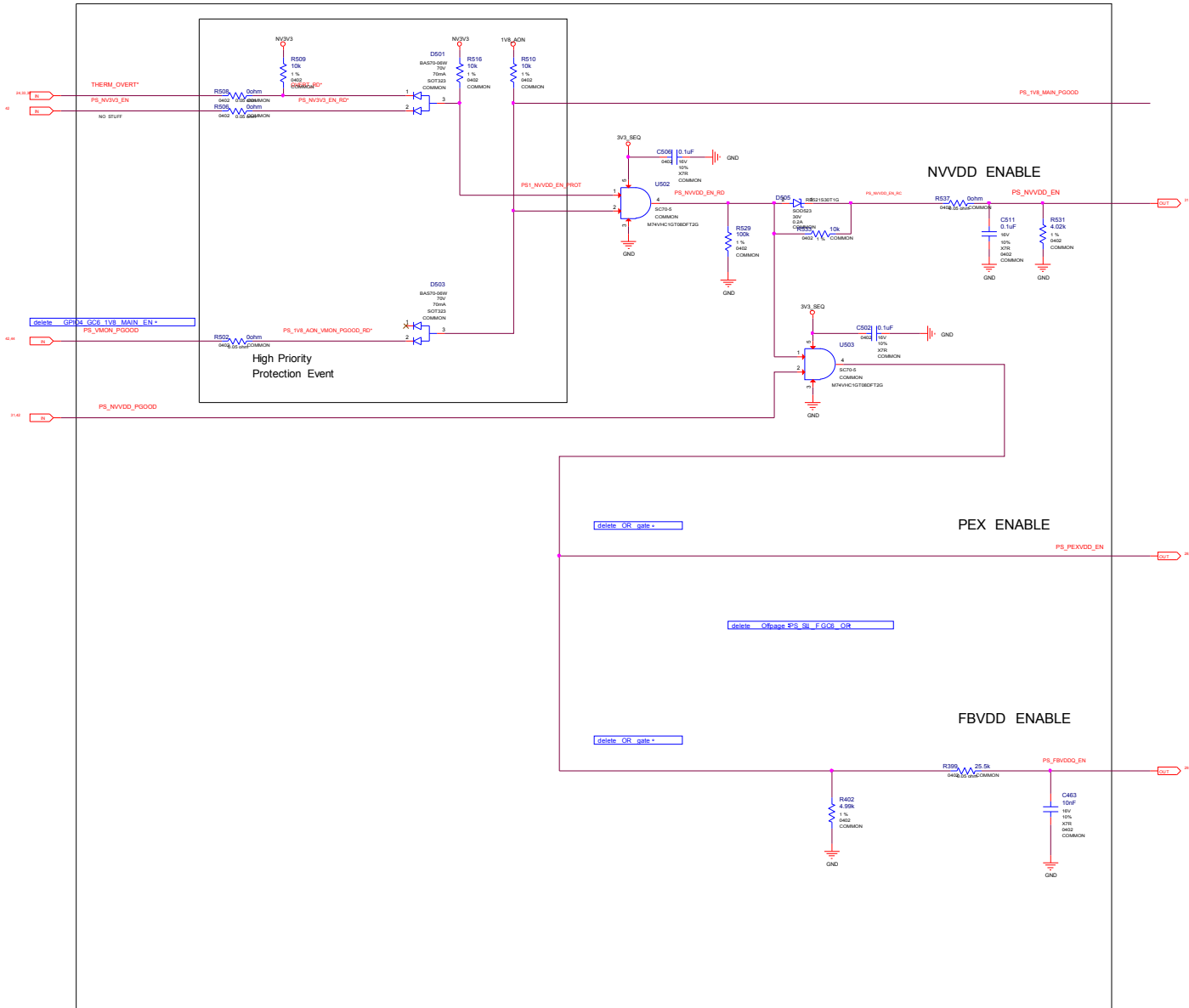
delete GP01_GCK_FB_EN+
delete GP02_DLE_IN_SW1

delete offpage RFD SWITCH

unused and delete C004

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	MS-V375		
	Size Custom	Document Description 12V & 3V3_A SWITCHER	Rev 4.0
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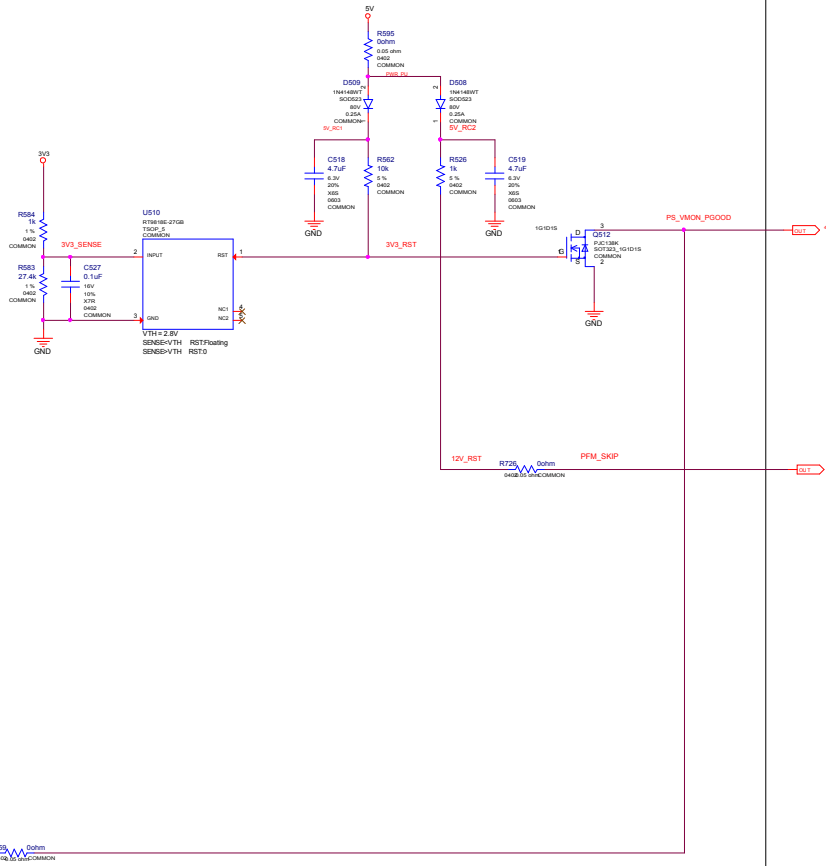




delete unused parts ◦

Voltage Monitor

Route the trace to PCIe Golden Finger



delete GPC1_G0C6_FB_EN+

delete PS_3TD_SWITCH+

PFM_PF_BSK

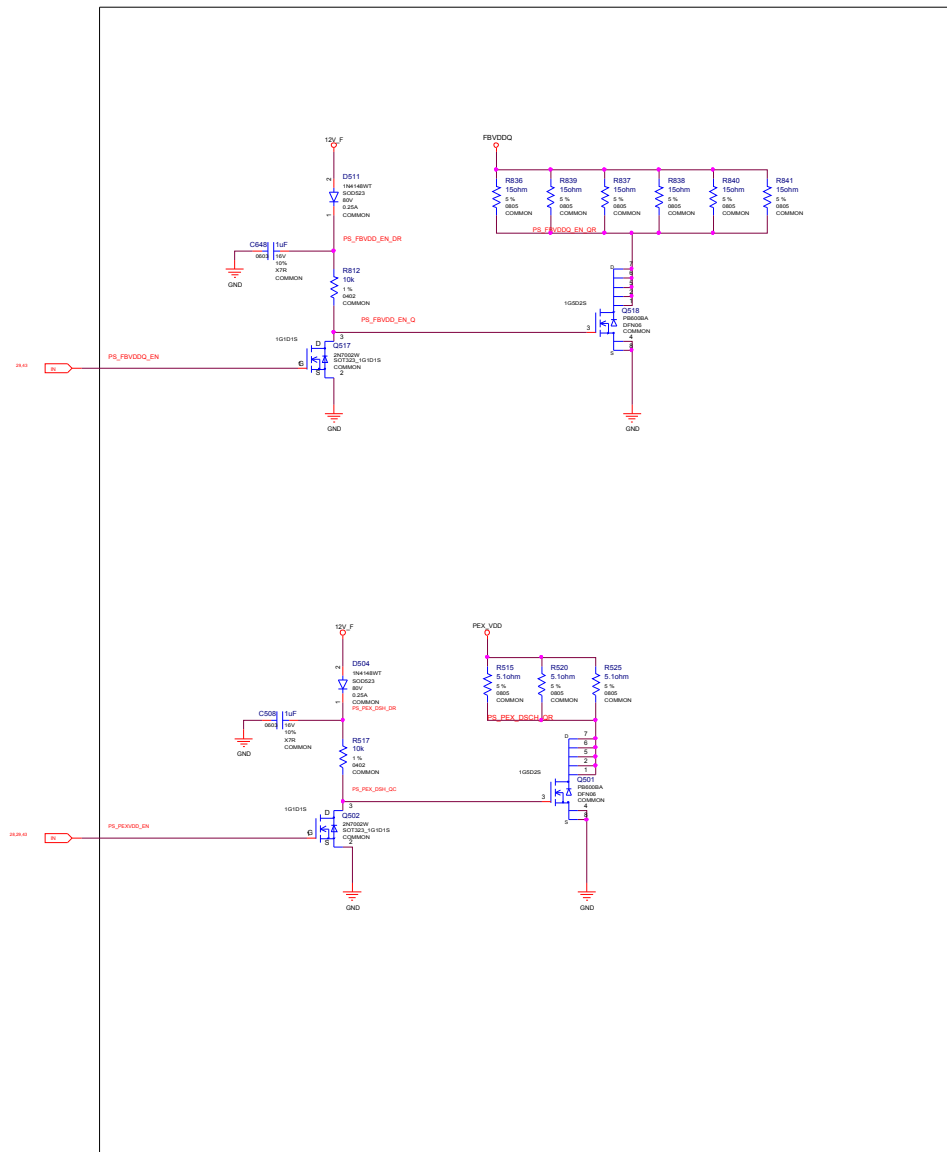
BOM Configuration

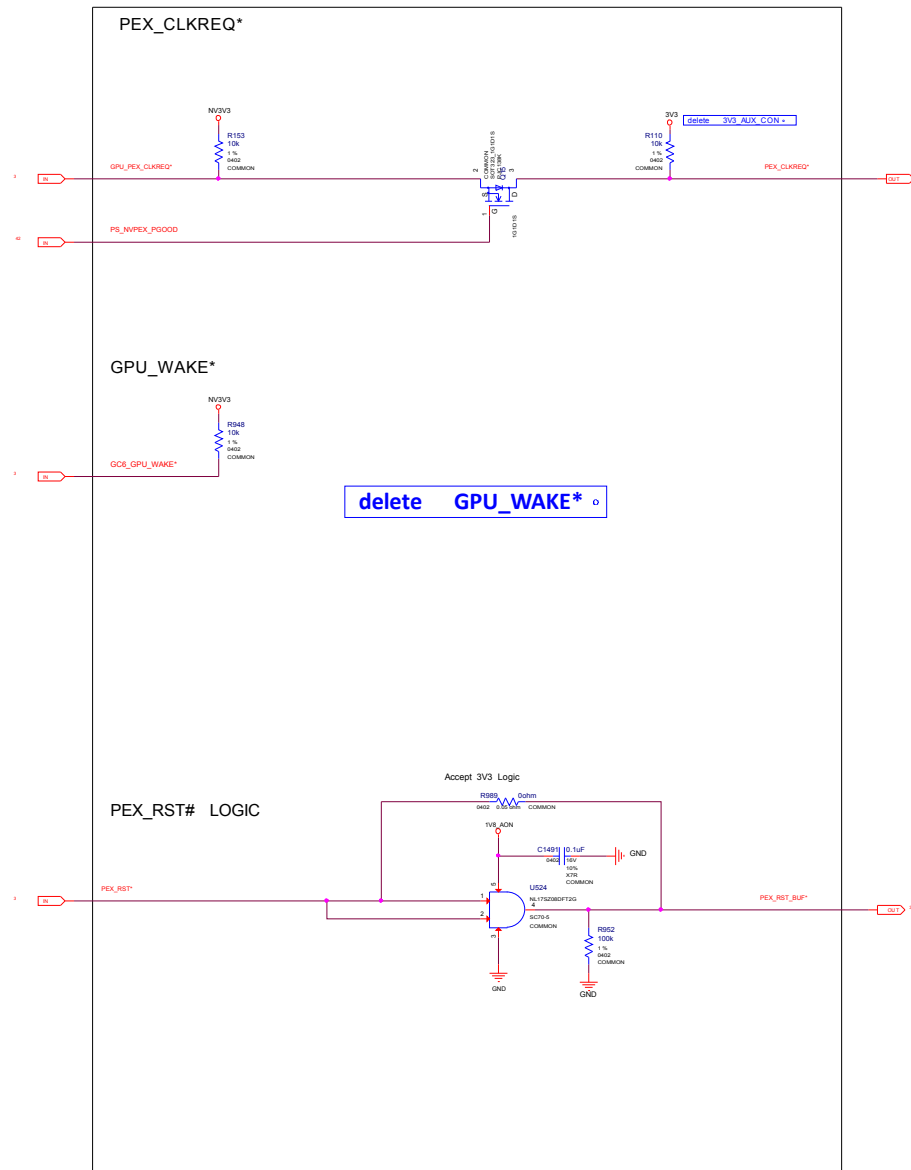
OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221	Voltage_Monitor	Voltage_Monitor	N/A
NO Pre-Filter			

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence.Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

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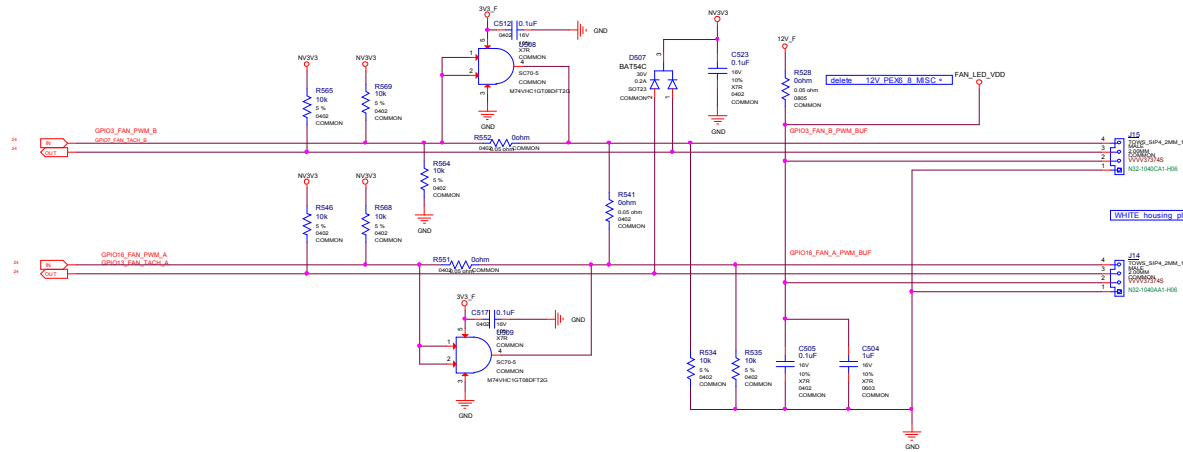


delete all unused

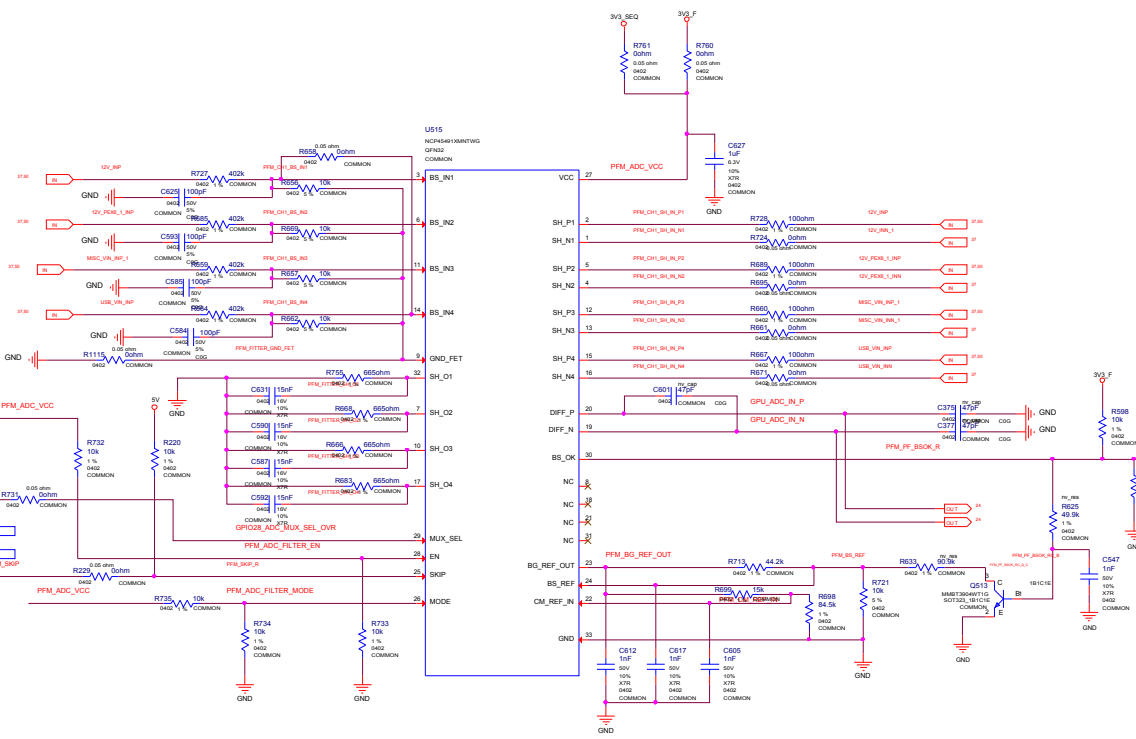
	MICRO-STAR INT'L CO.,LTD		
	MS-V375		
	Size Custom	Document Description LOGO LED	Rev 4.0
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delete all unused

copied V373-2.0 housing PN and footprint ◦

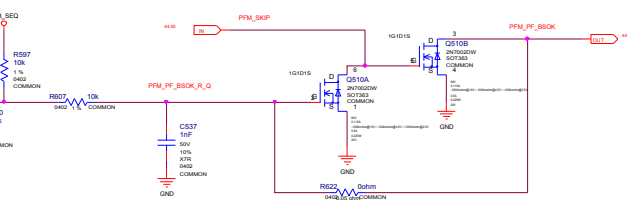


		MICRO-STAR INT'L CO.,LTD	
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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

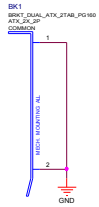


MICRO-STAR INT'L CO.,LTD

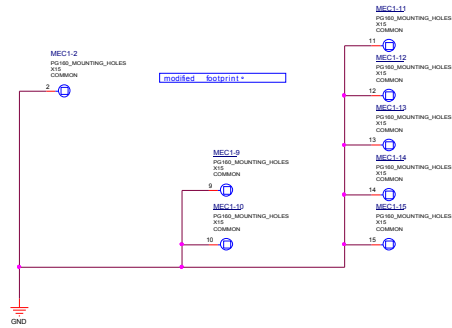
MS-V375

Size: Custom Document Description: PWR SENSE Rev: 4.0
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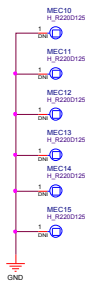
Brackets:



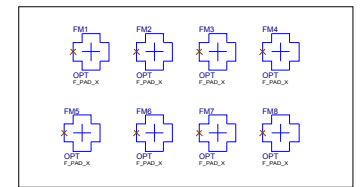
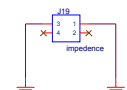
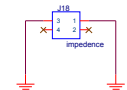
MOUNTING HOLES FOR HS:



Mechanical Holes Symbol

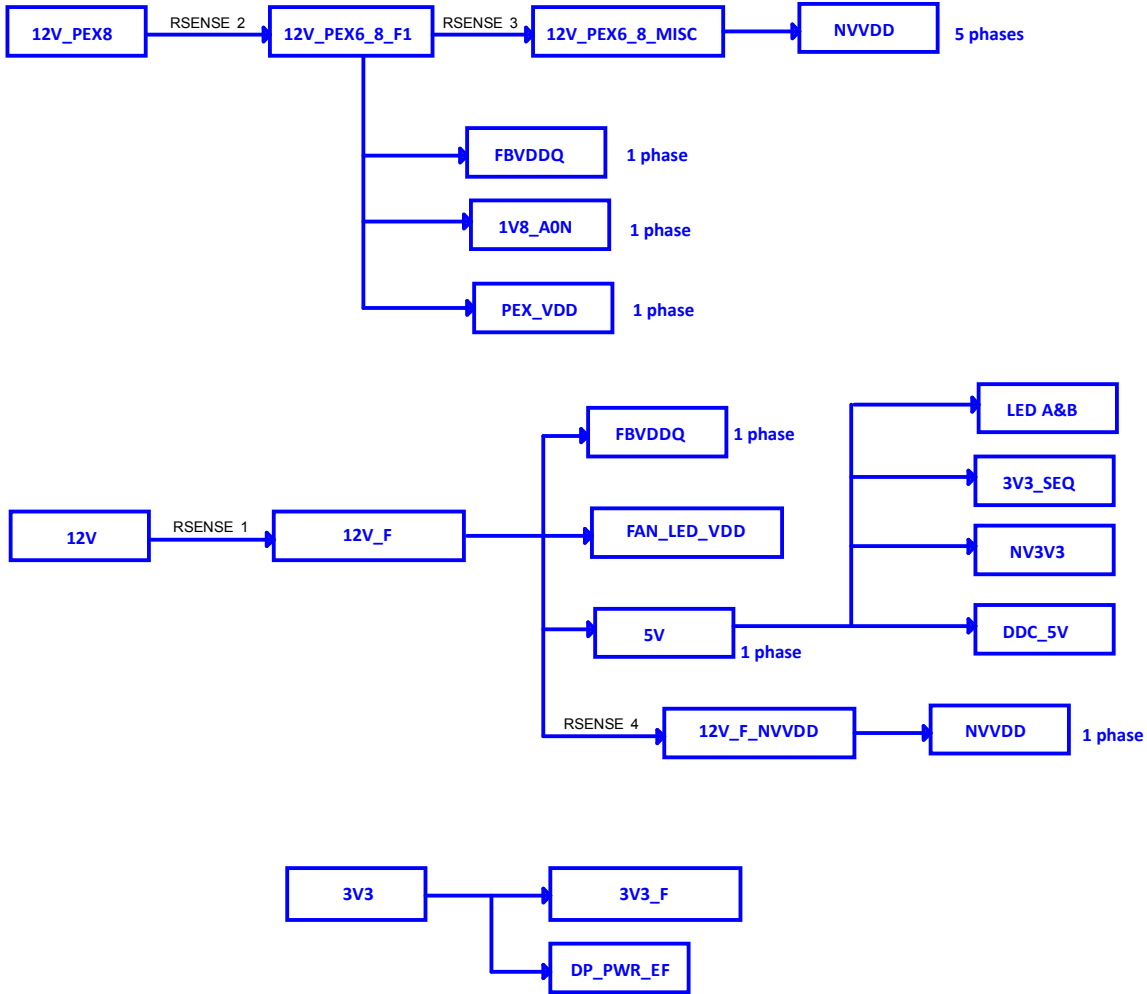


Bracket Screw



improved FBVDDQ PSU parts don't require a PTC

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Power on Sequence

