

PG161-A00

TU106 6GB GDDR6, 192b, X16 DVI-D/DP + DP + HDMI

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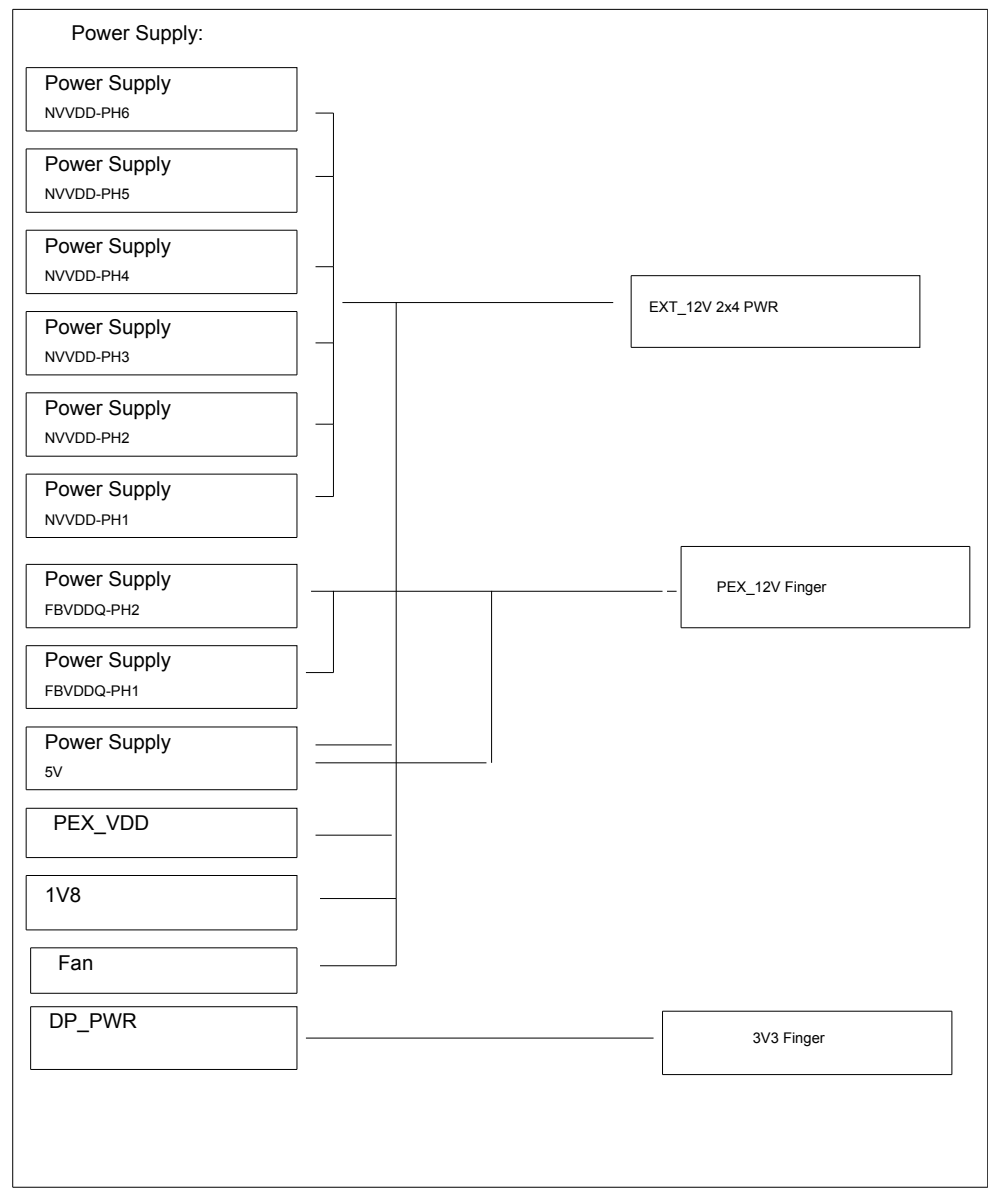
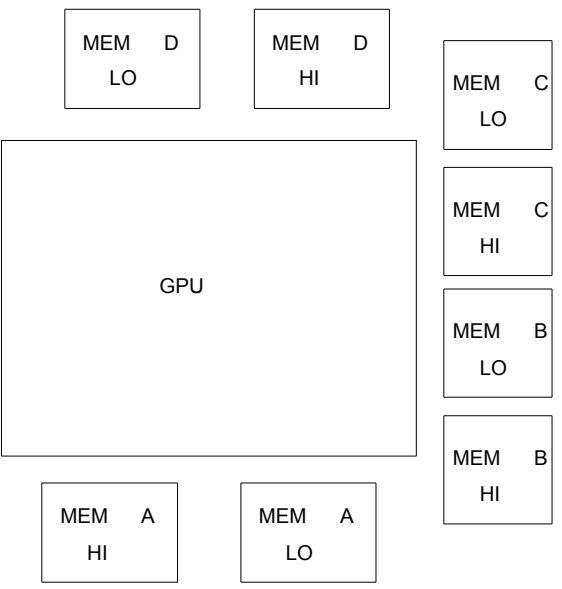
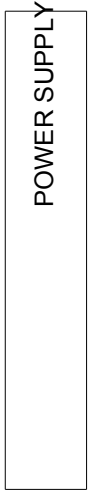
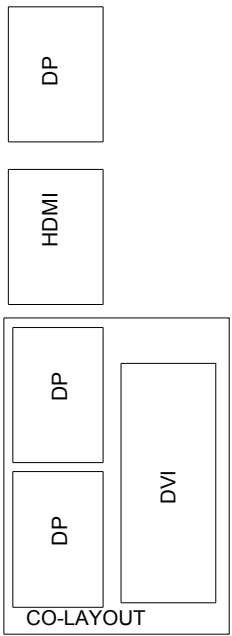
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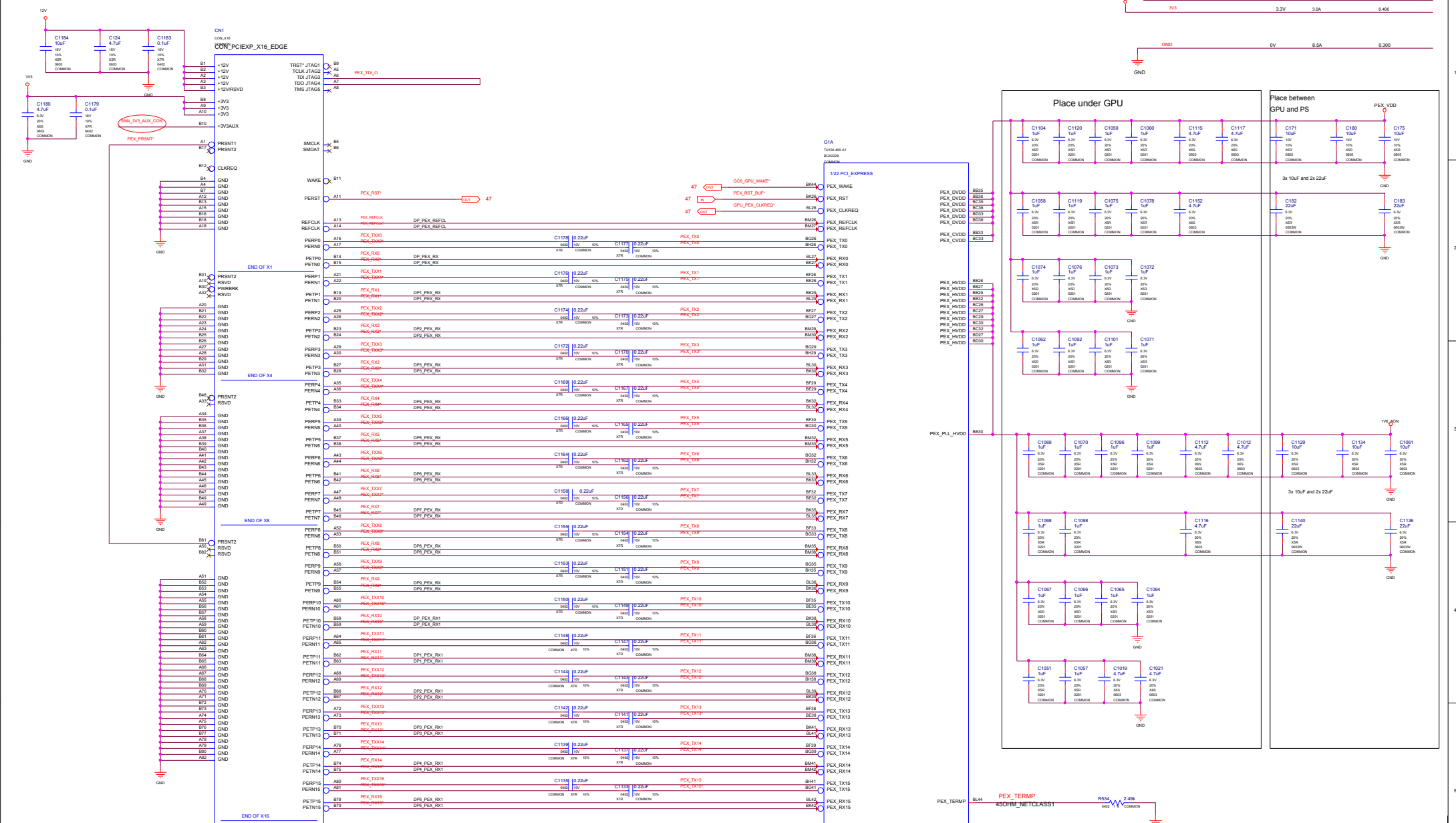
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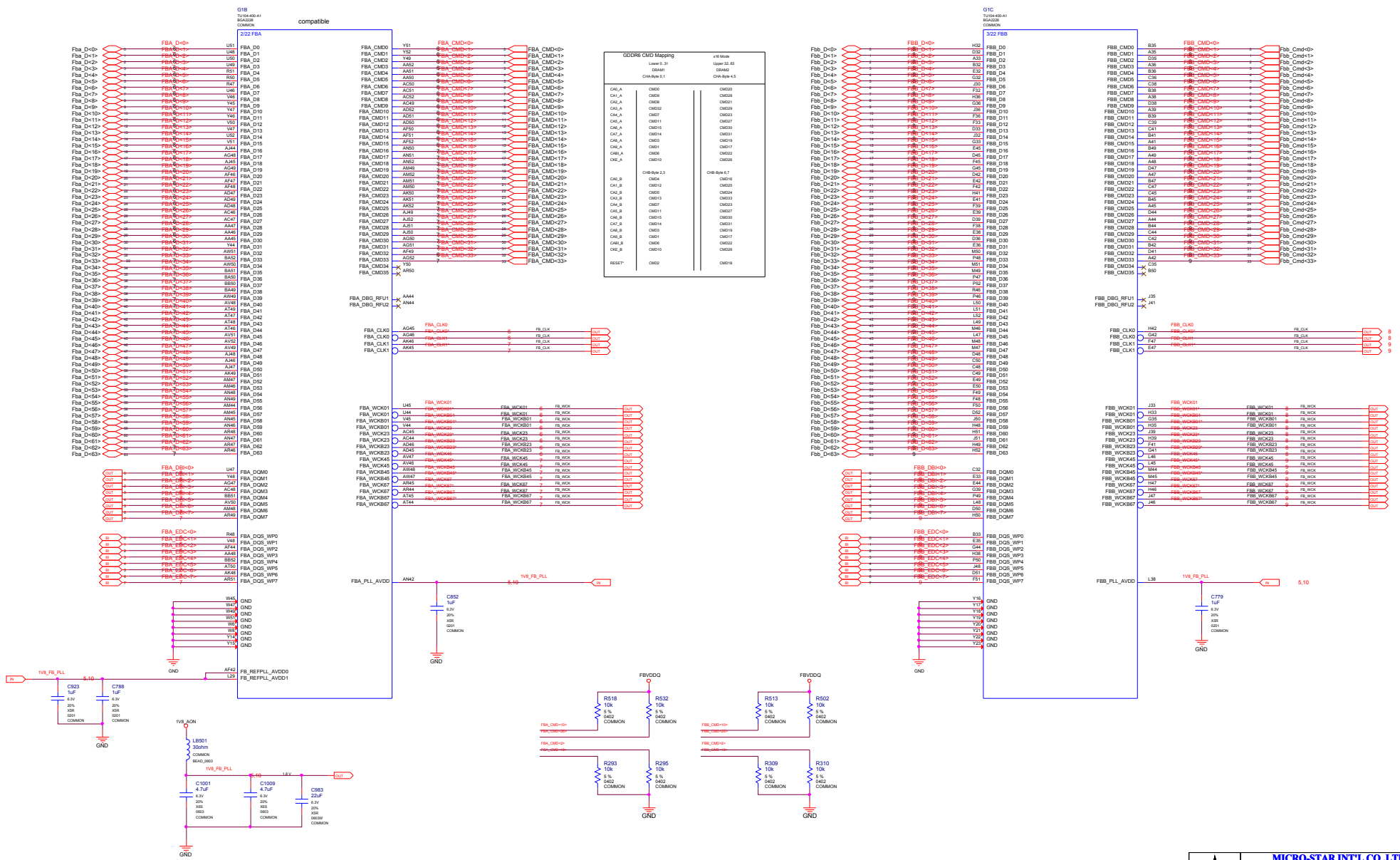




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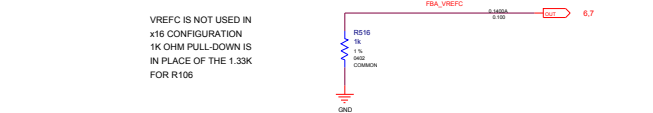
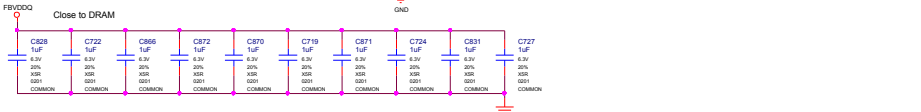
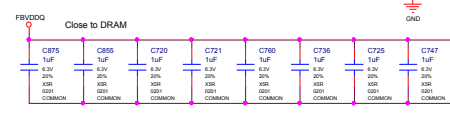
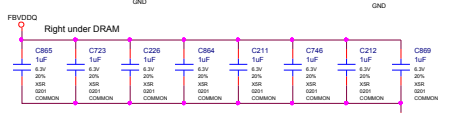
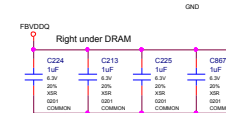
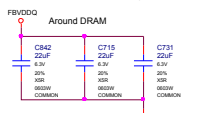
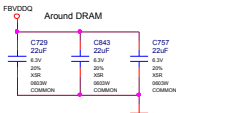
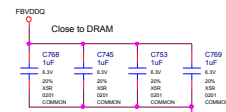
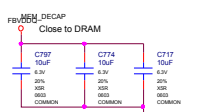
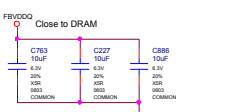
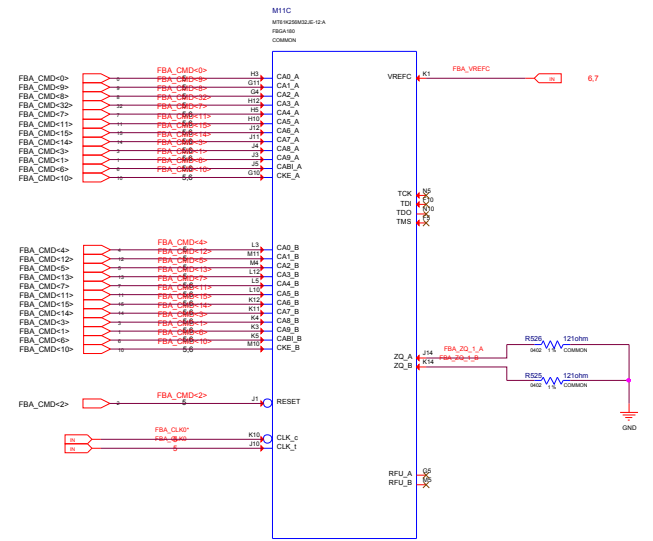
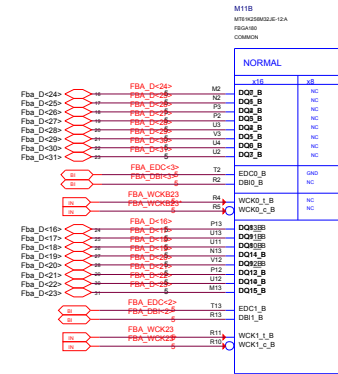
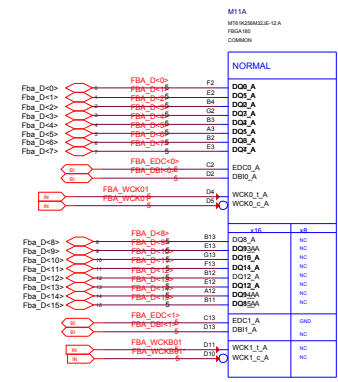
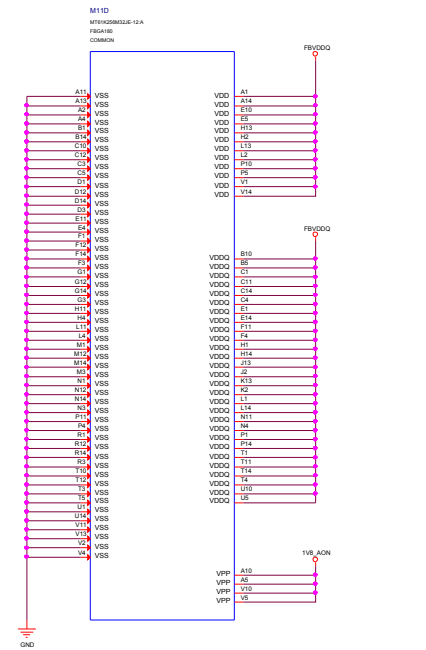
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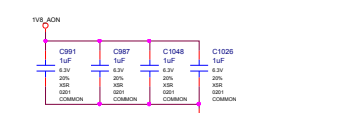
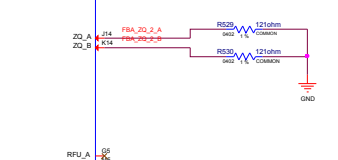
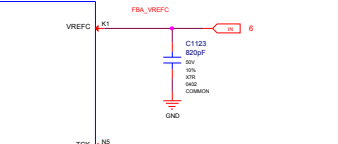
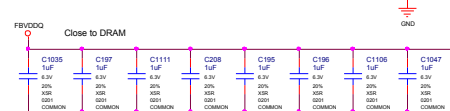
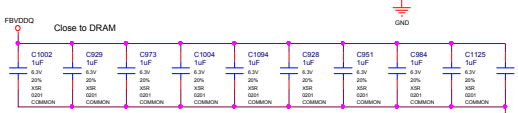
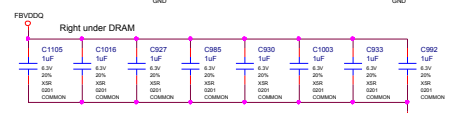
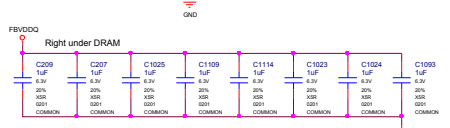
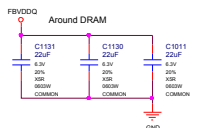
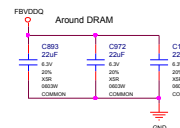
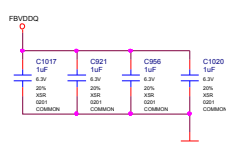
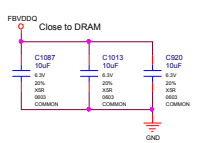
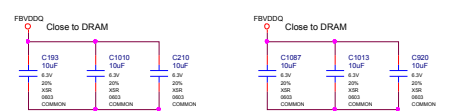
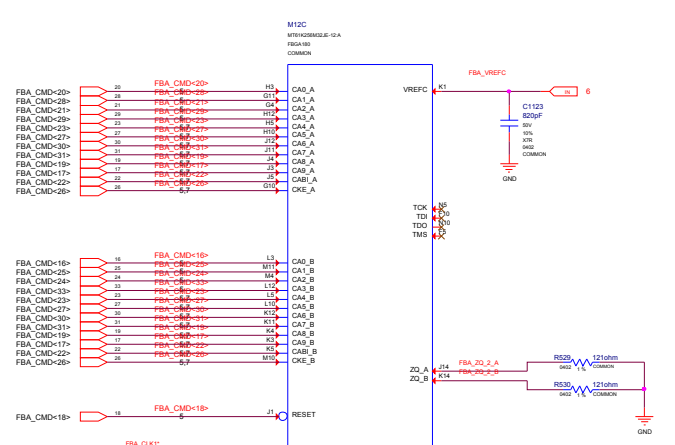
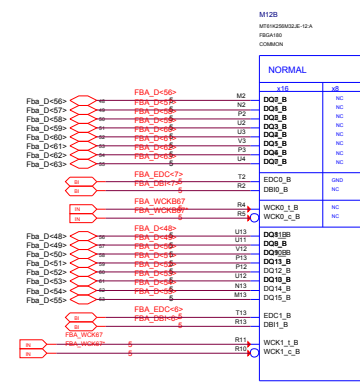
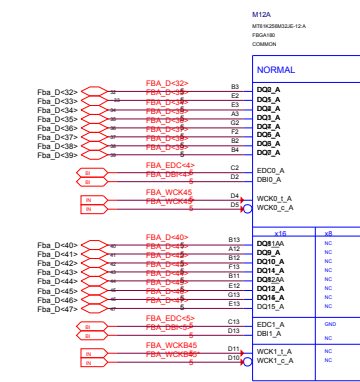
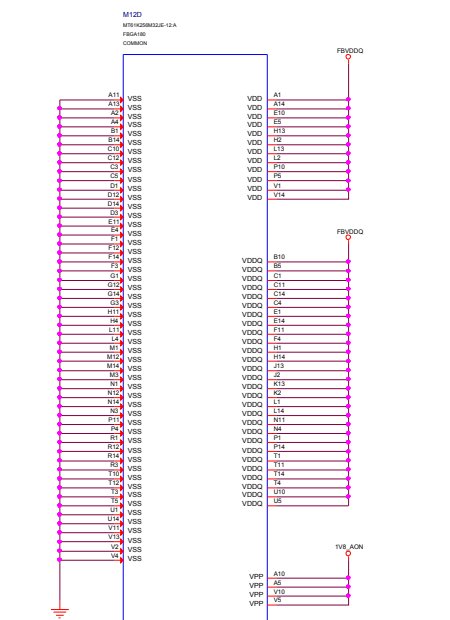
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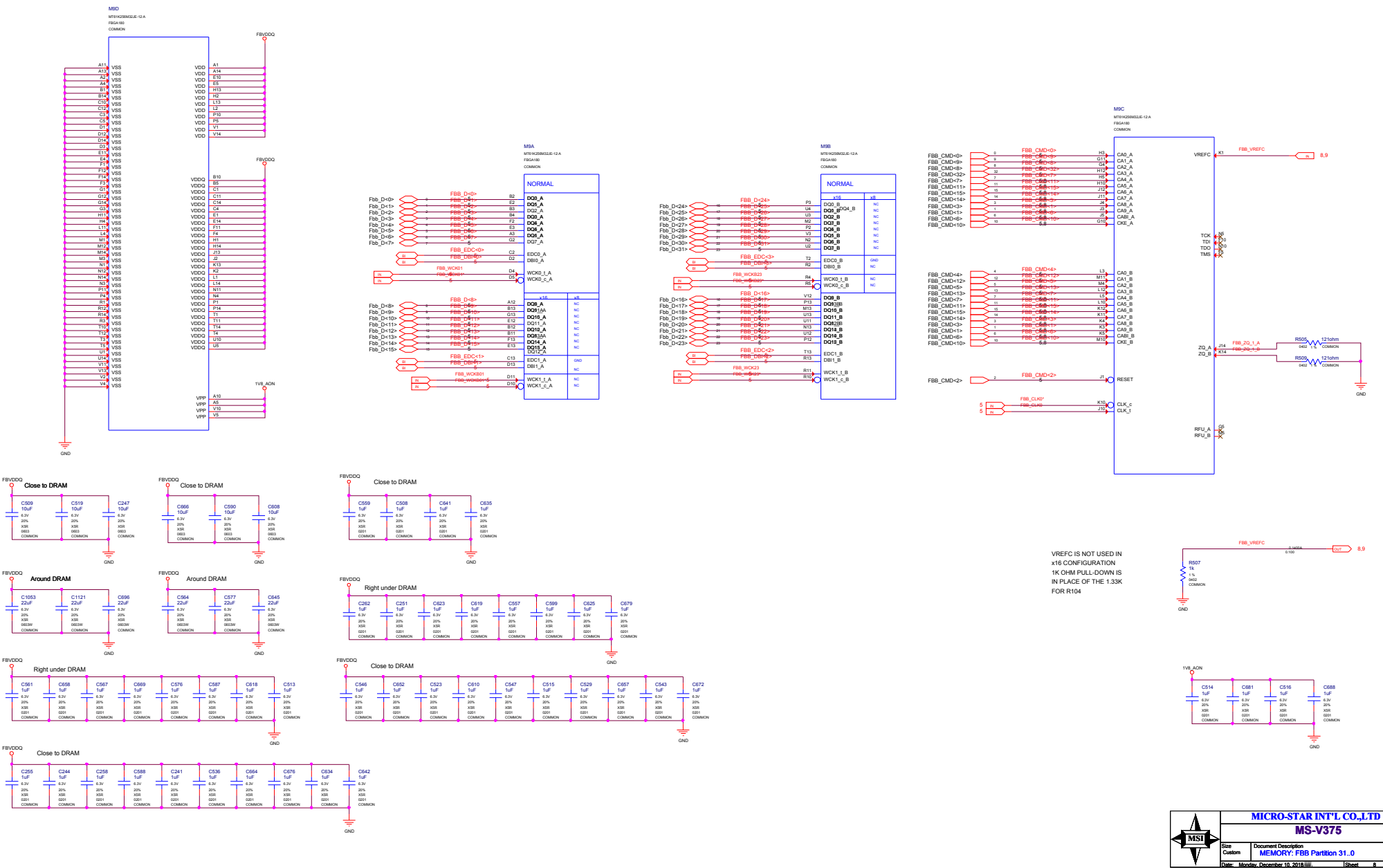
VREFC IS NOT USED IN x16 CONFIGURATION. 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R106.

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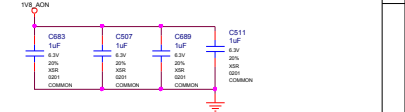
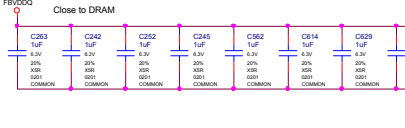
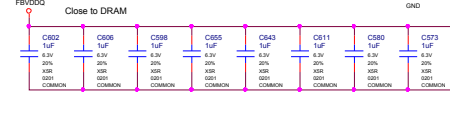
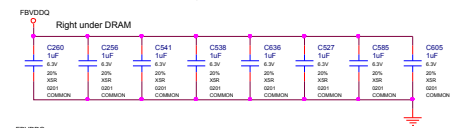
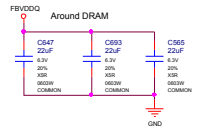
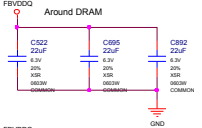
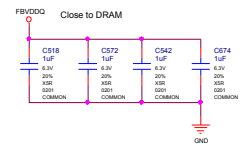
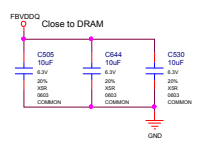
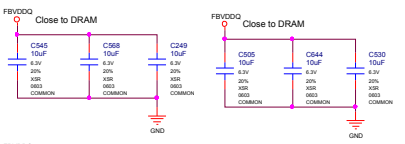
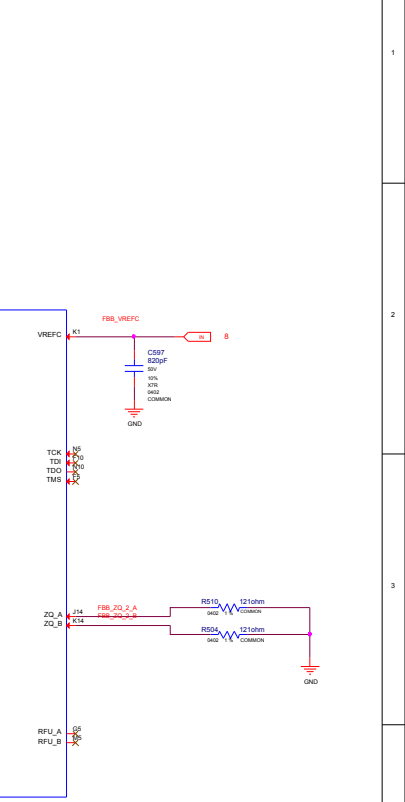
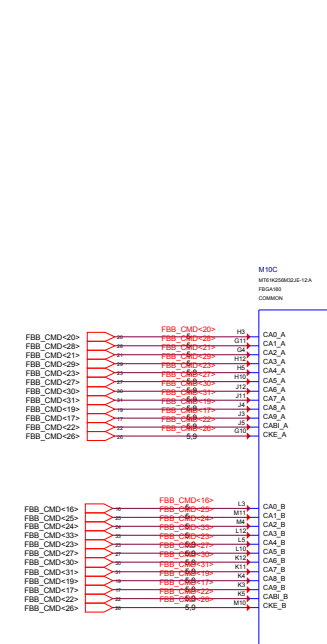
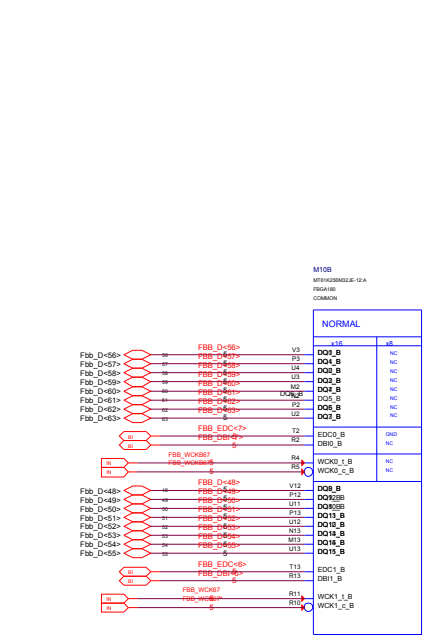
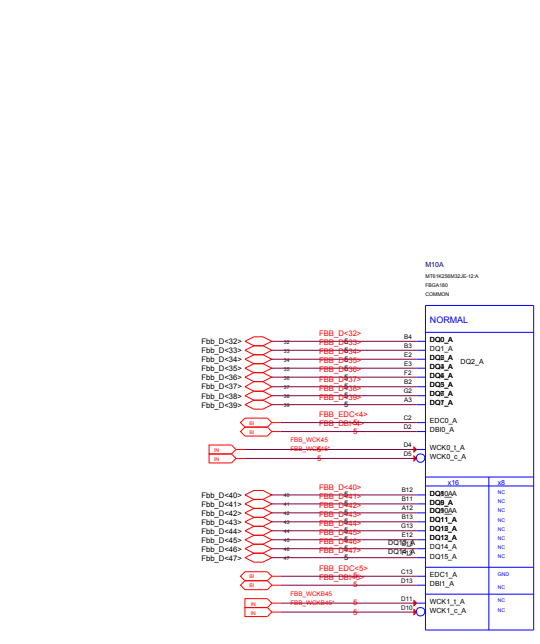
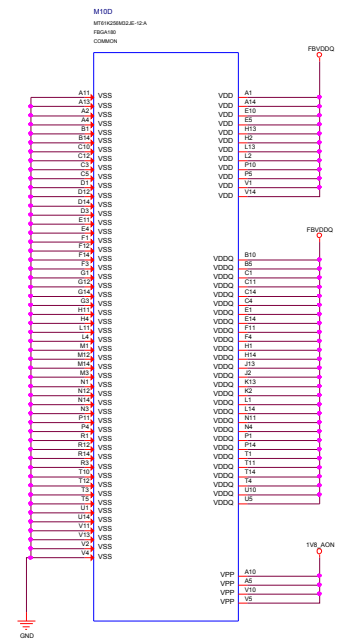
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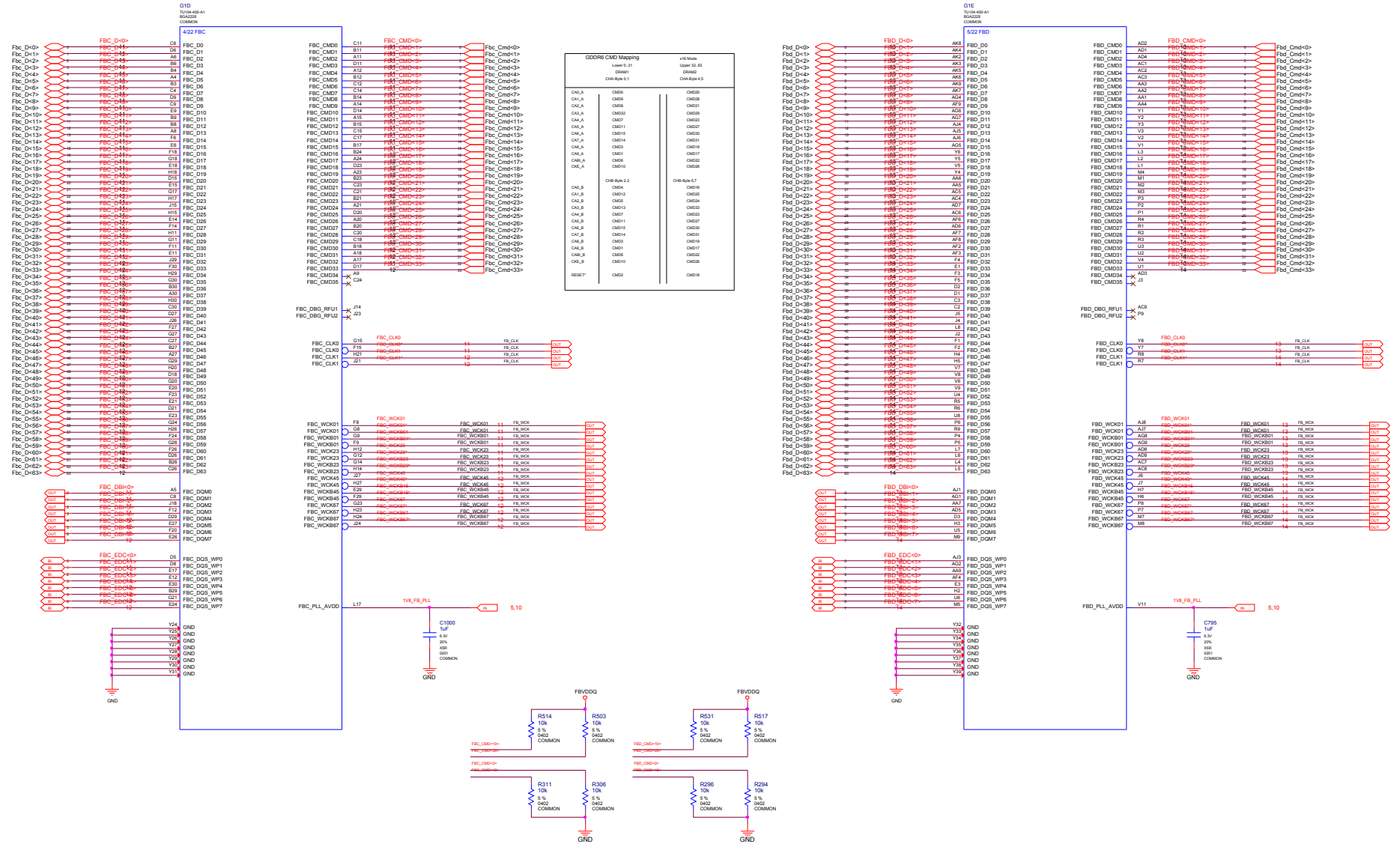


VREFC IS NOT USED IN x16 CONFIGURATION
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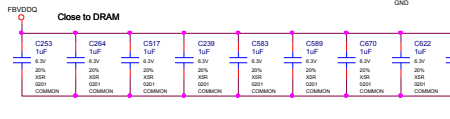
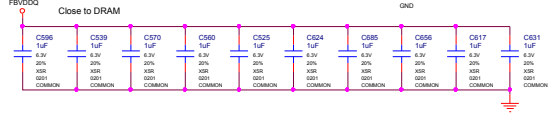
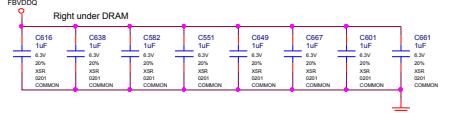
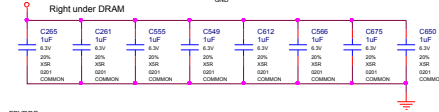
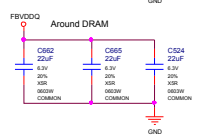
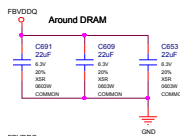
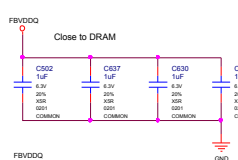
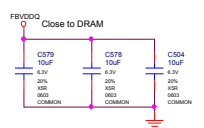
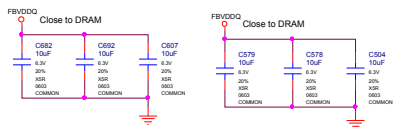
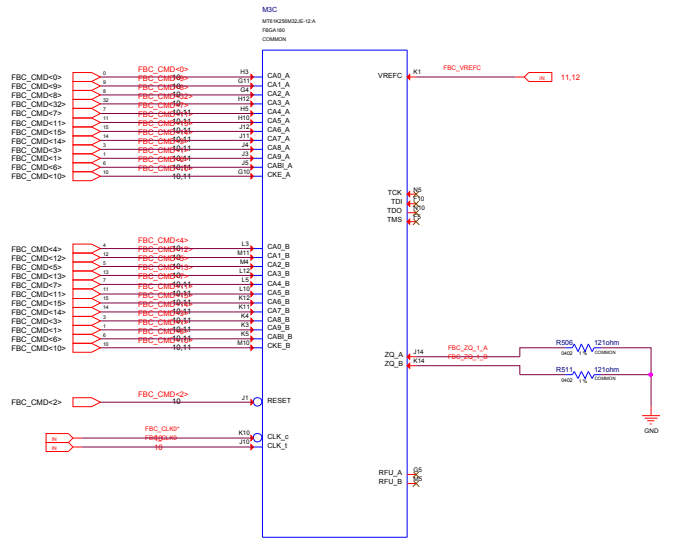
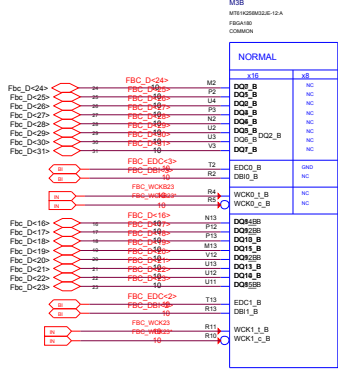
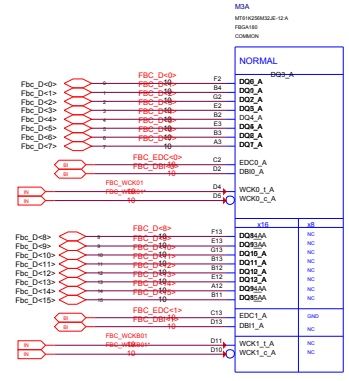
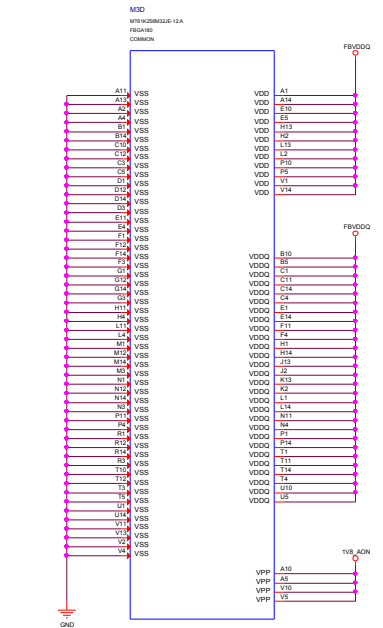


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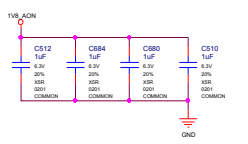
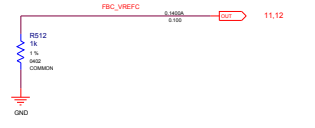


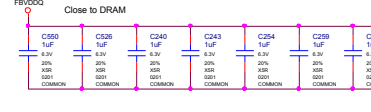
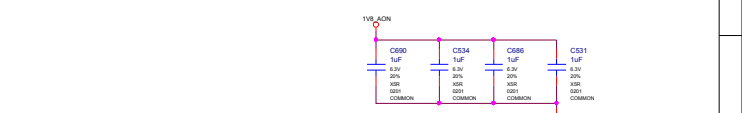
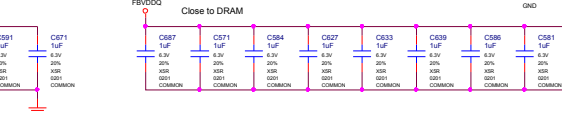
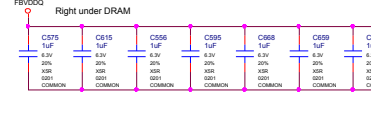
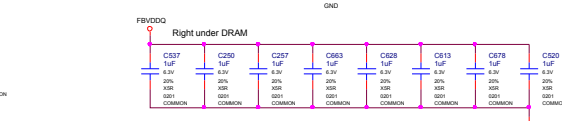
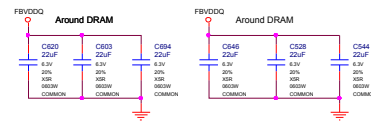
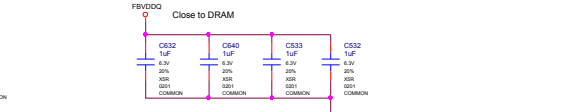
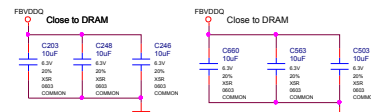
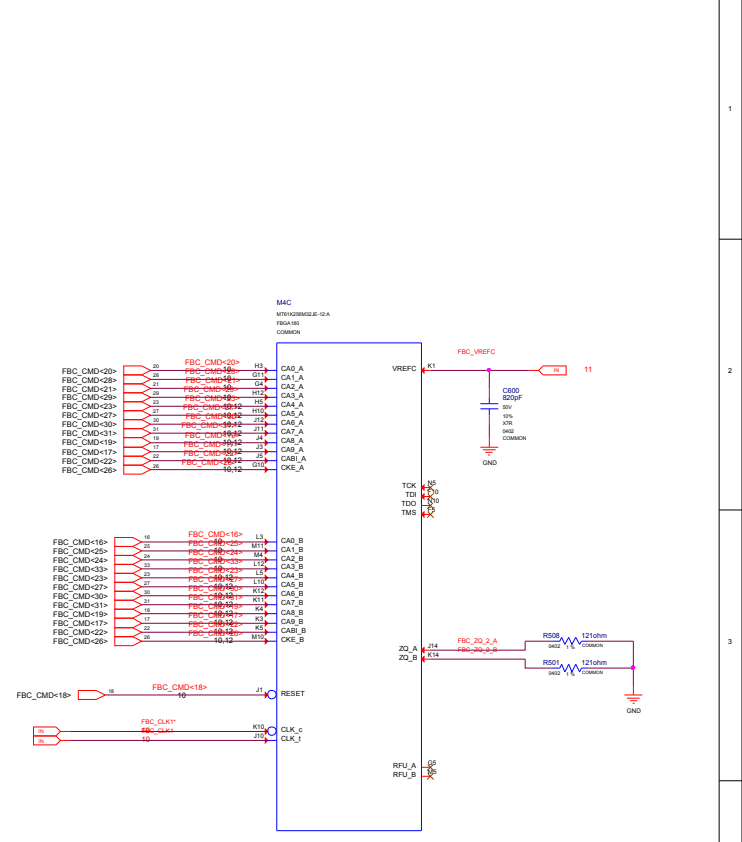
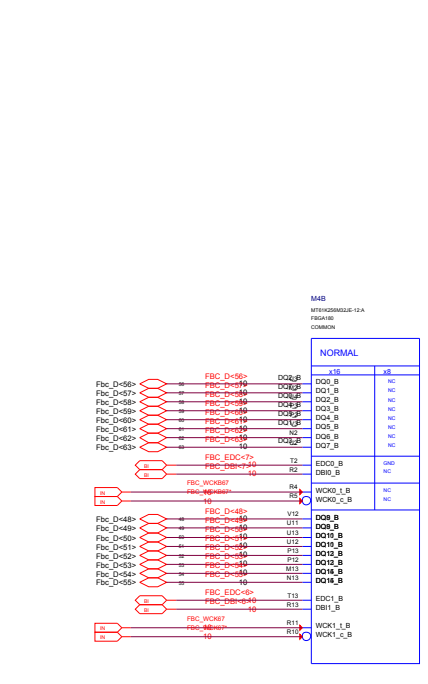
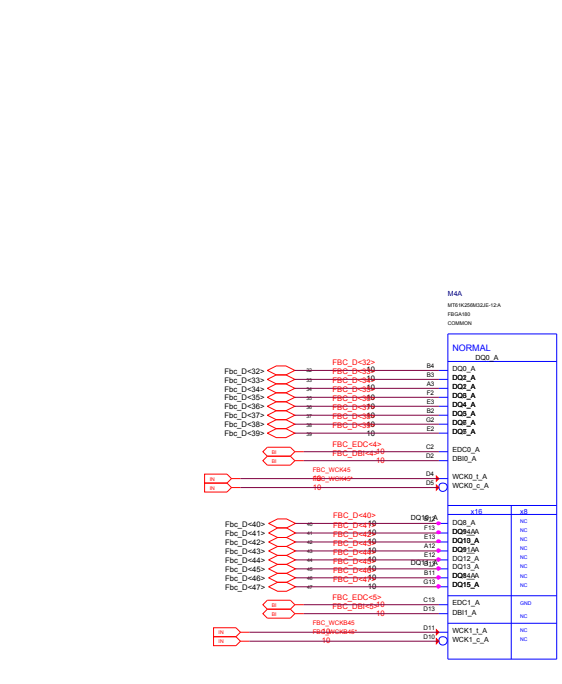
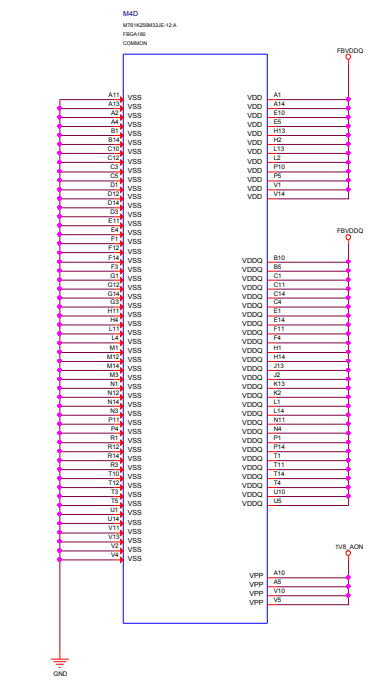
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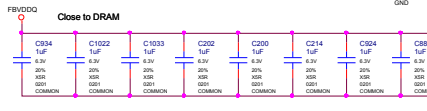
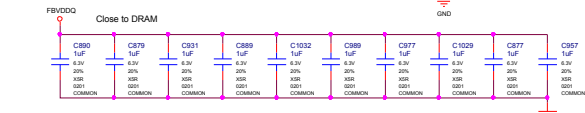
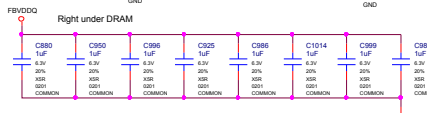
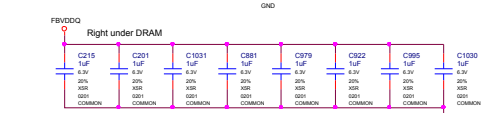
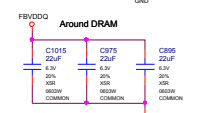
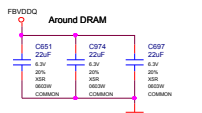
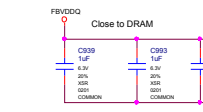
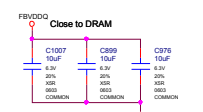
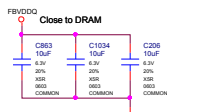
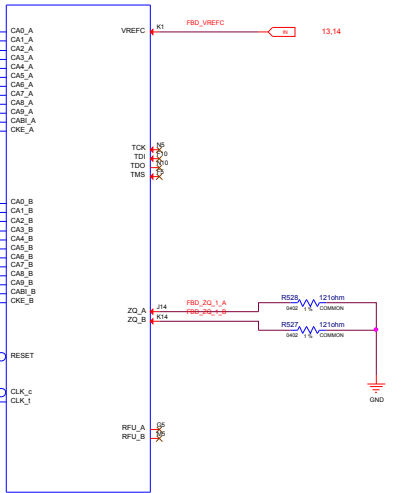
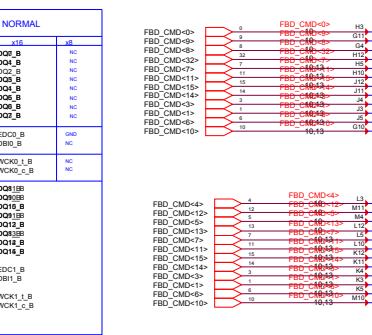
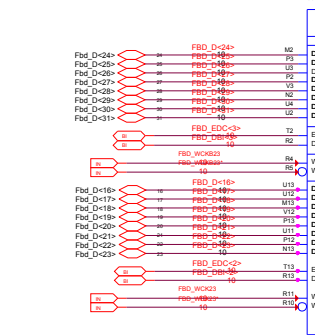
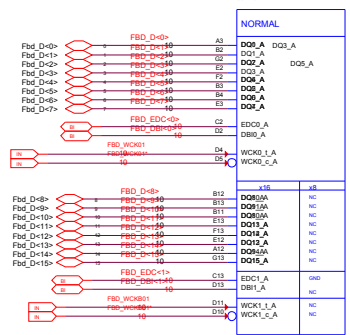
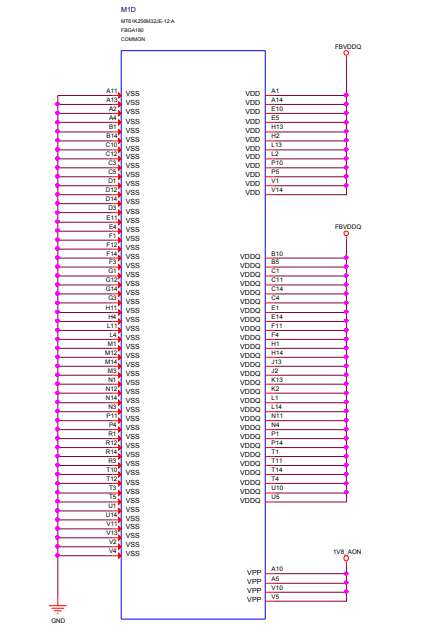


VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R75

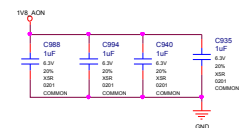
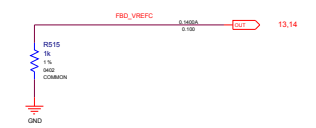


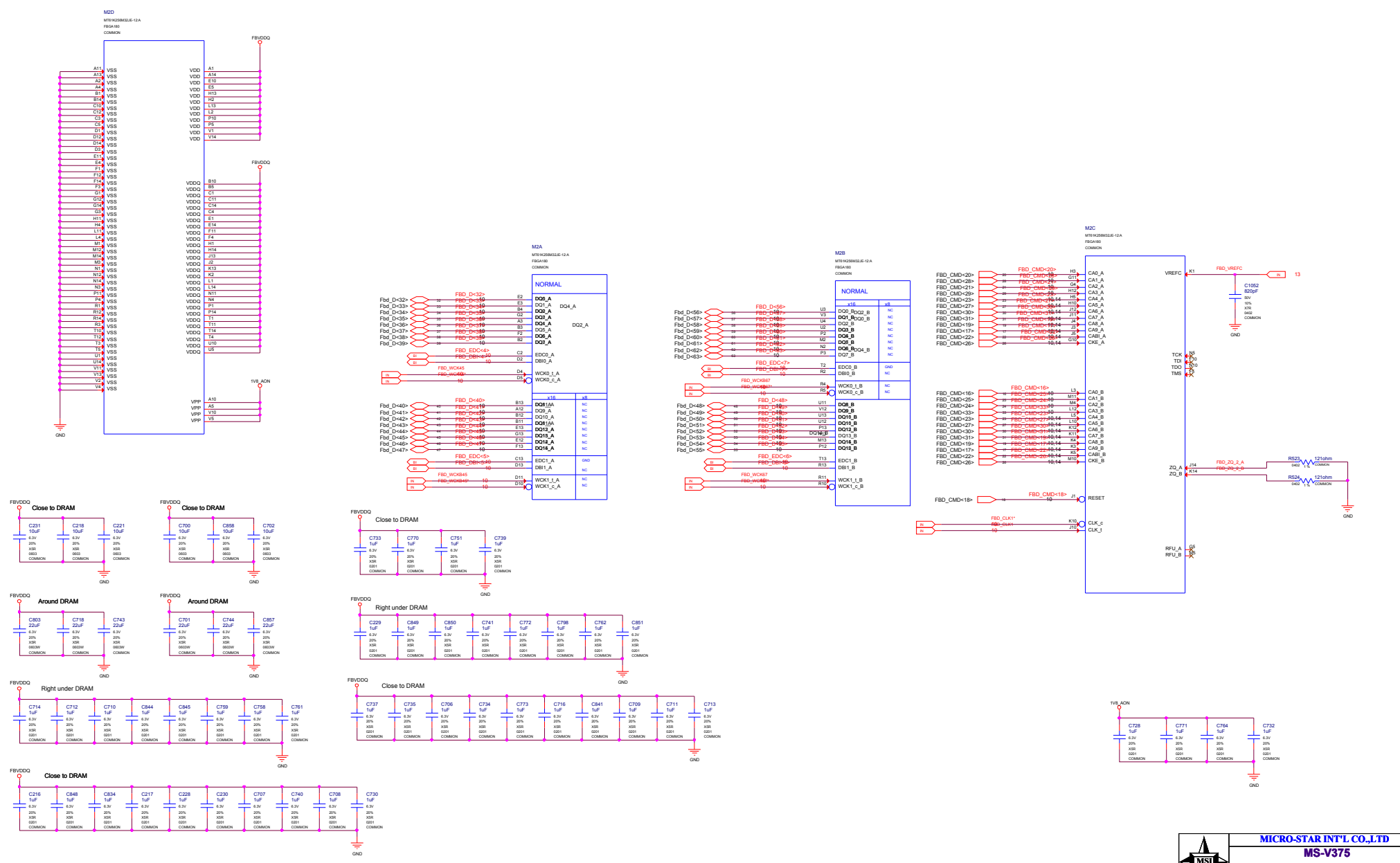


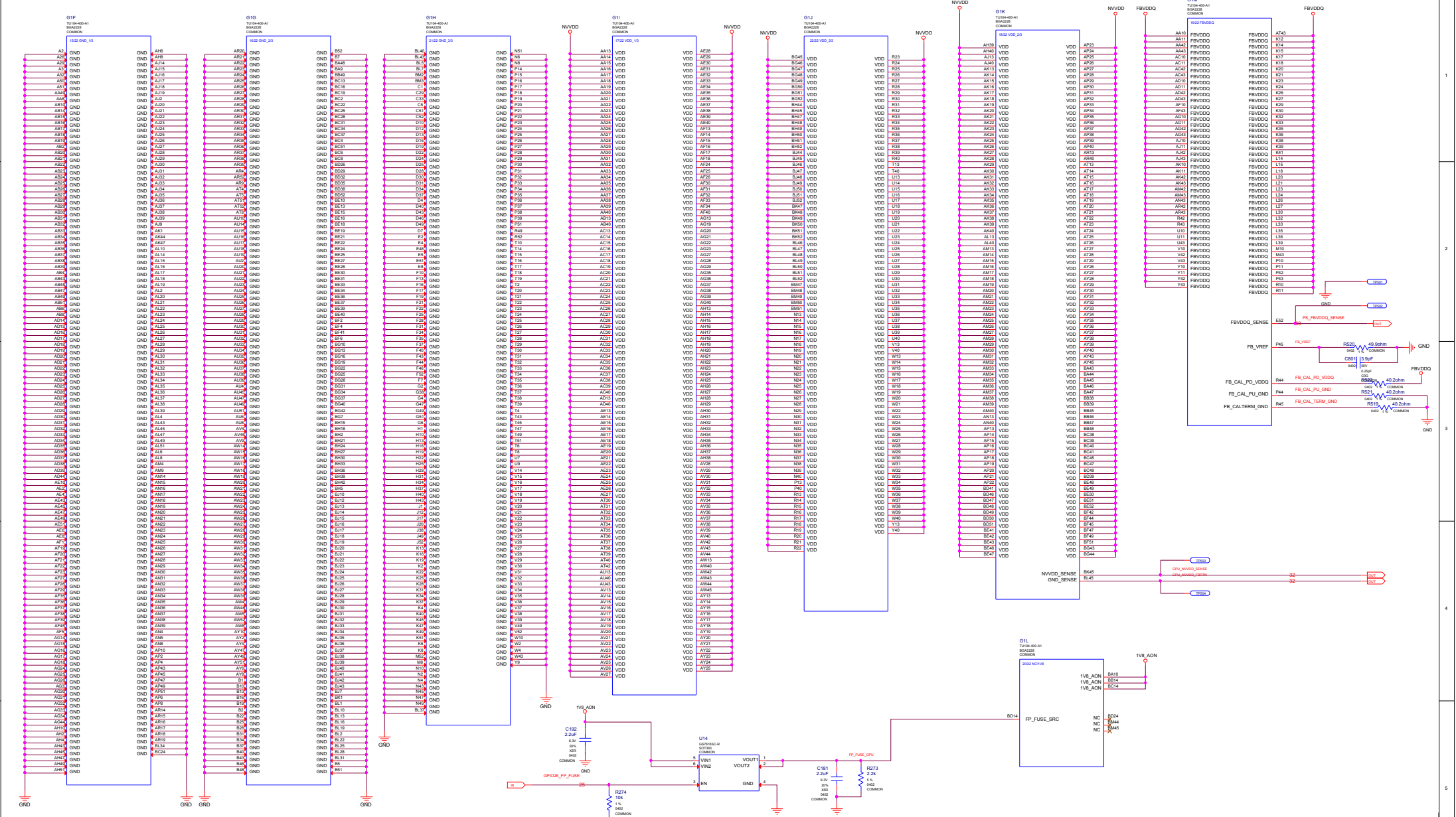
	MICRO-STAR INT'L CO.,LTD		Rev 2.0	
	MS-V375			
	Size Custom	Document Descriptor MEMORY: FBC Partition 63..32		
	Date: Monday, December 10, 2018	Sheet 12 of 53		



VREFC IS NOT USED IN X16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R62

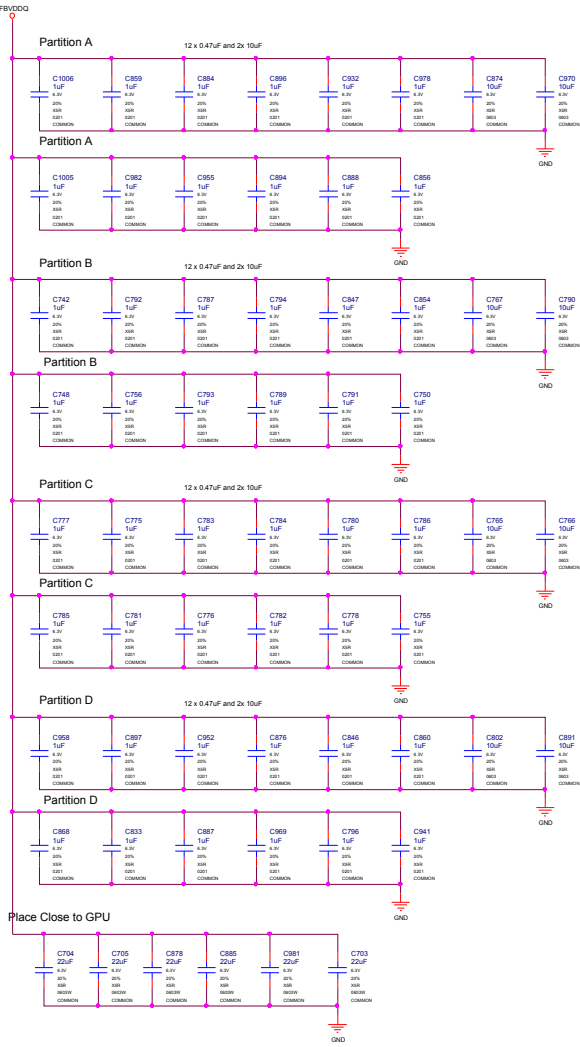




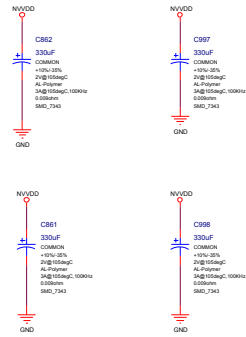


		MICRO-STAR INT'L CO., LTD MS-V375	
		Doc: Custom Date: Monday, December 10, 2018	Description: GPU PWR and GND Sheet: 15 of 63

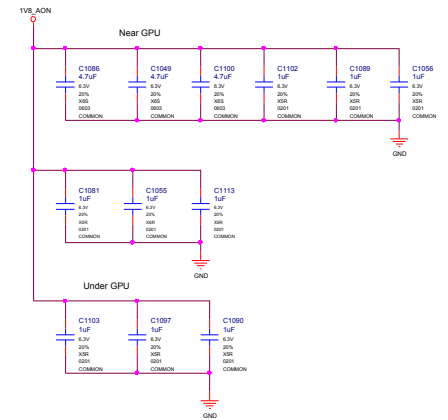
FBVDDQ



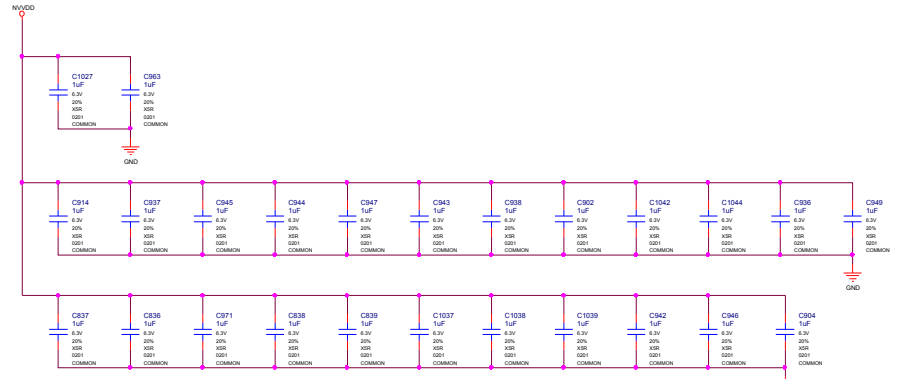
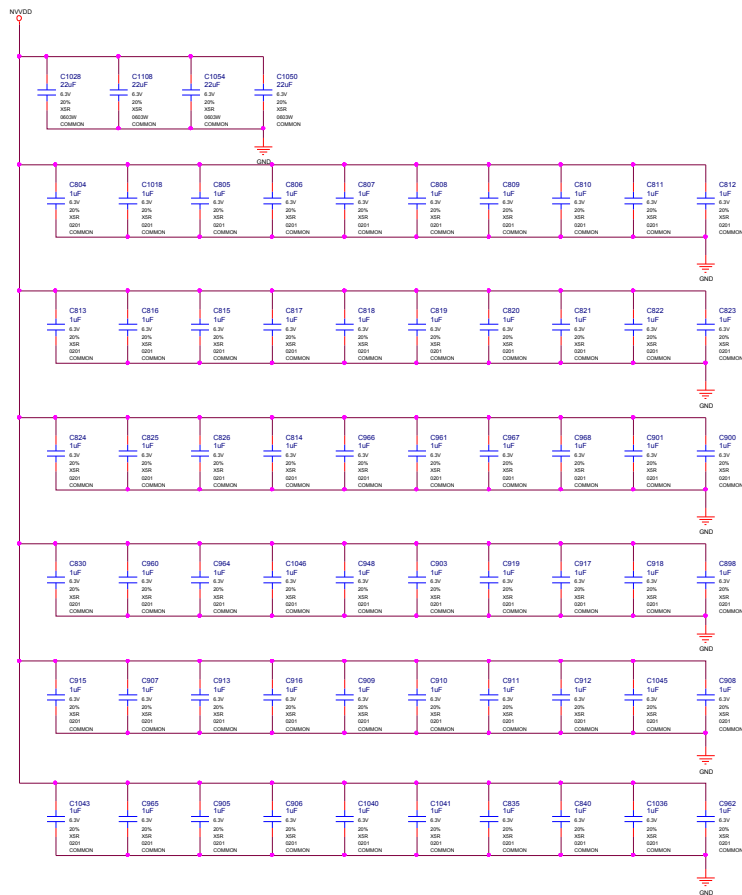
NVVDD



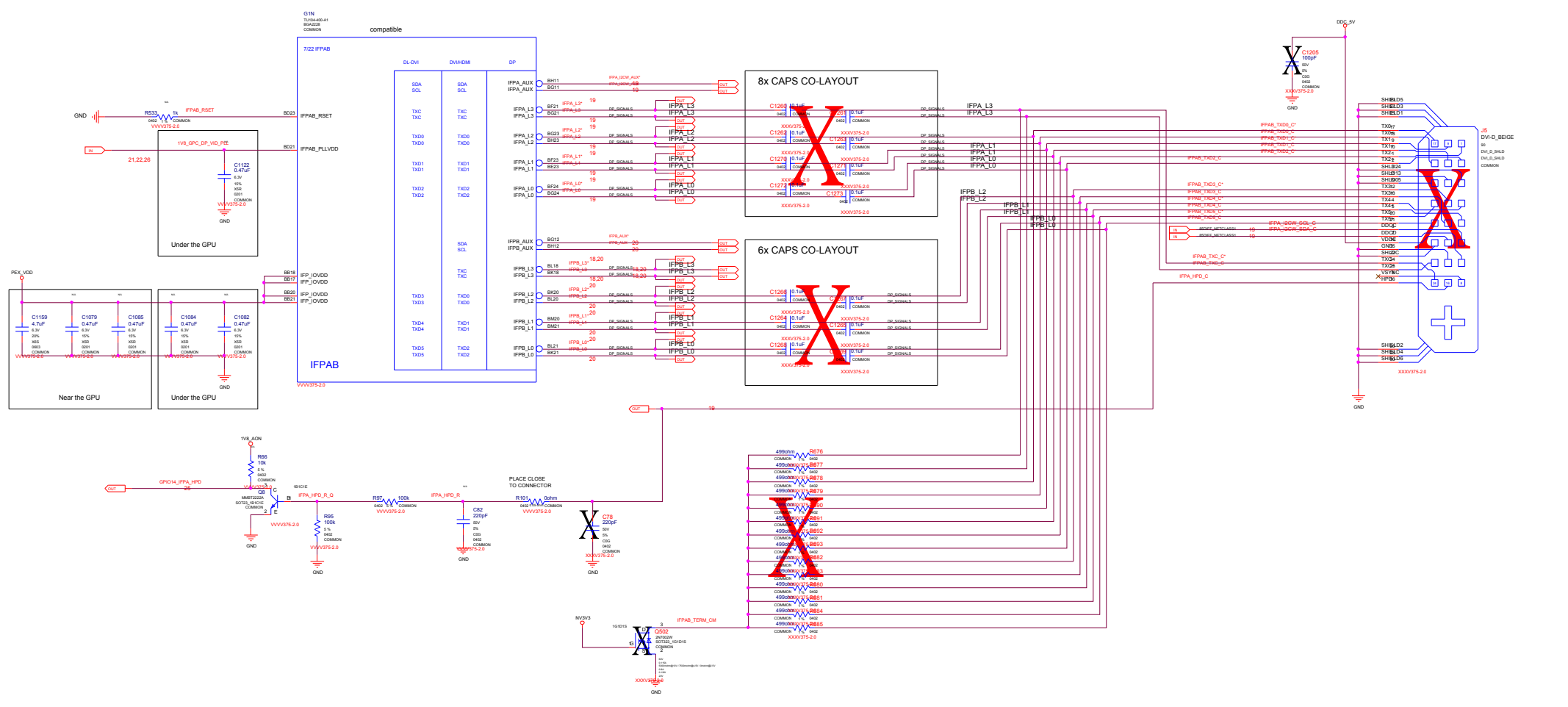
1V8_AON

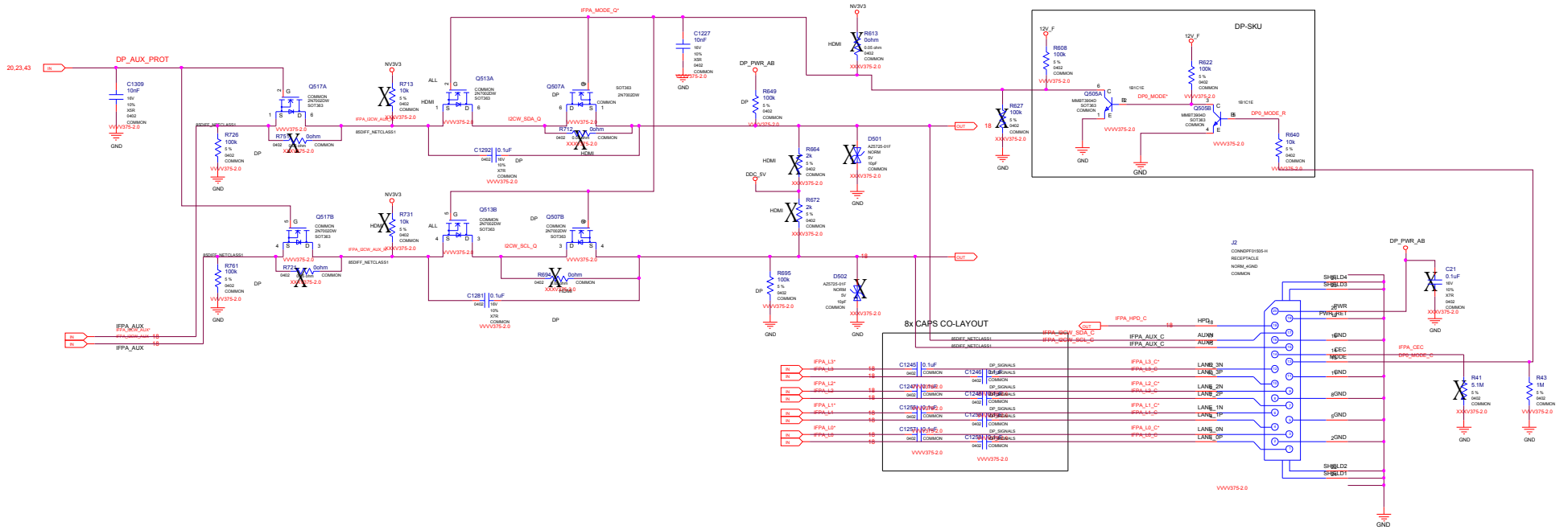


NVVD



IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



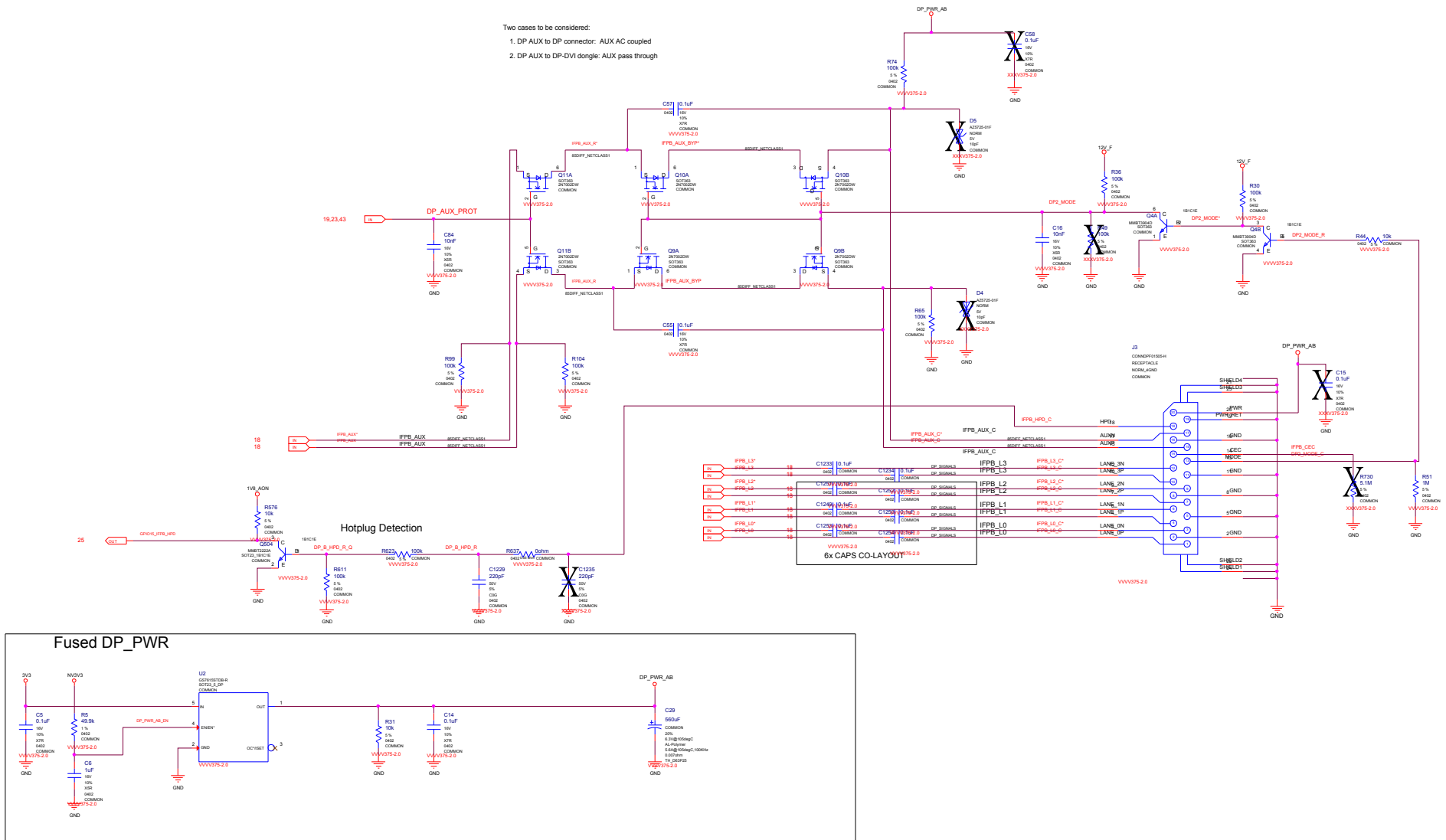


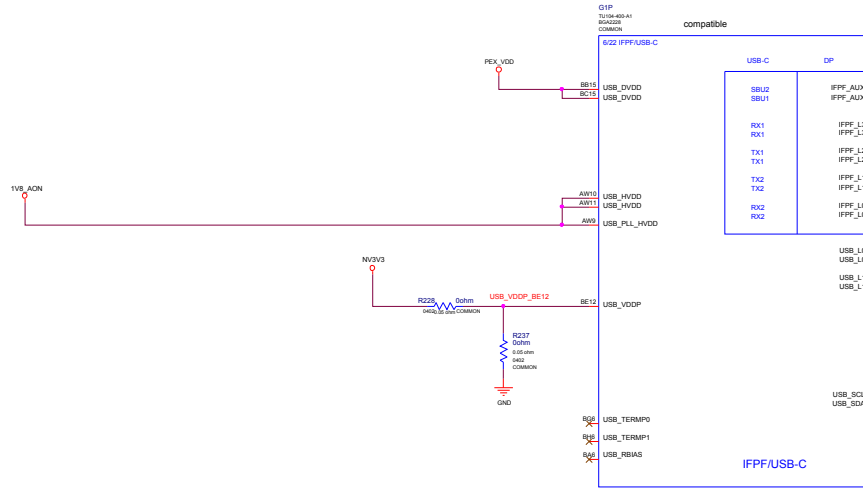
IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

		MICRO-STAR INT'L CO.,LTD MS-V375	
Size Custom	Document Description IFPA DP	Rev. 2.0	
Date: Monday, December 10, 2018		Sheet 19 of 33	

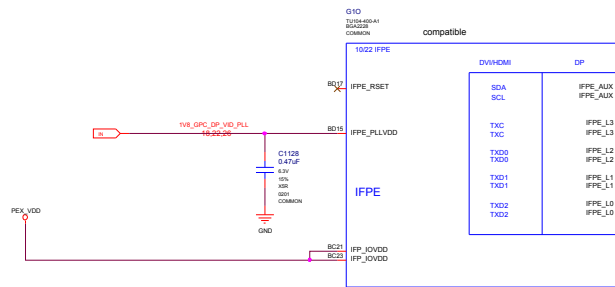
IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

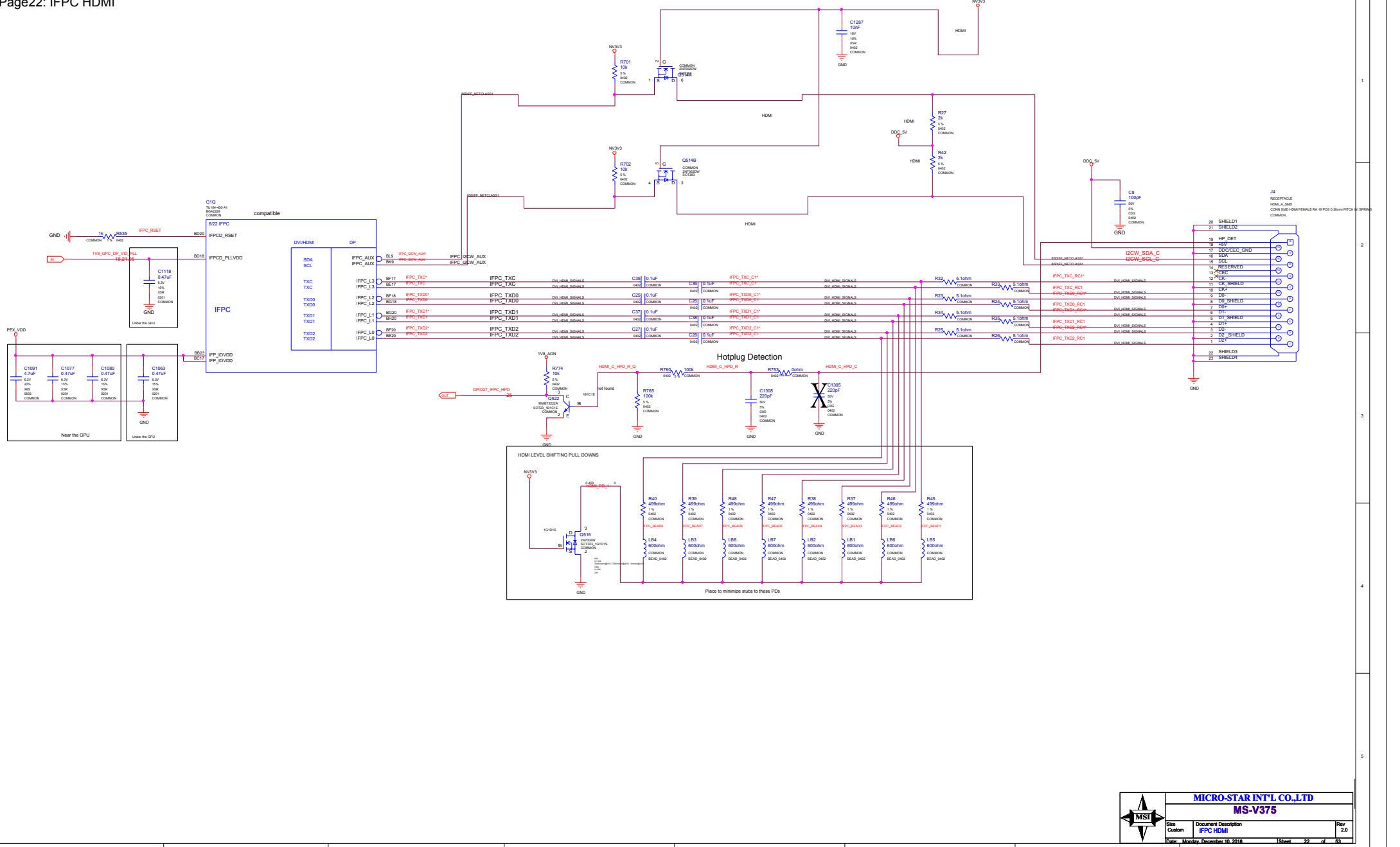




IFPF NC

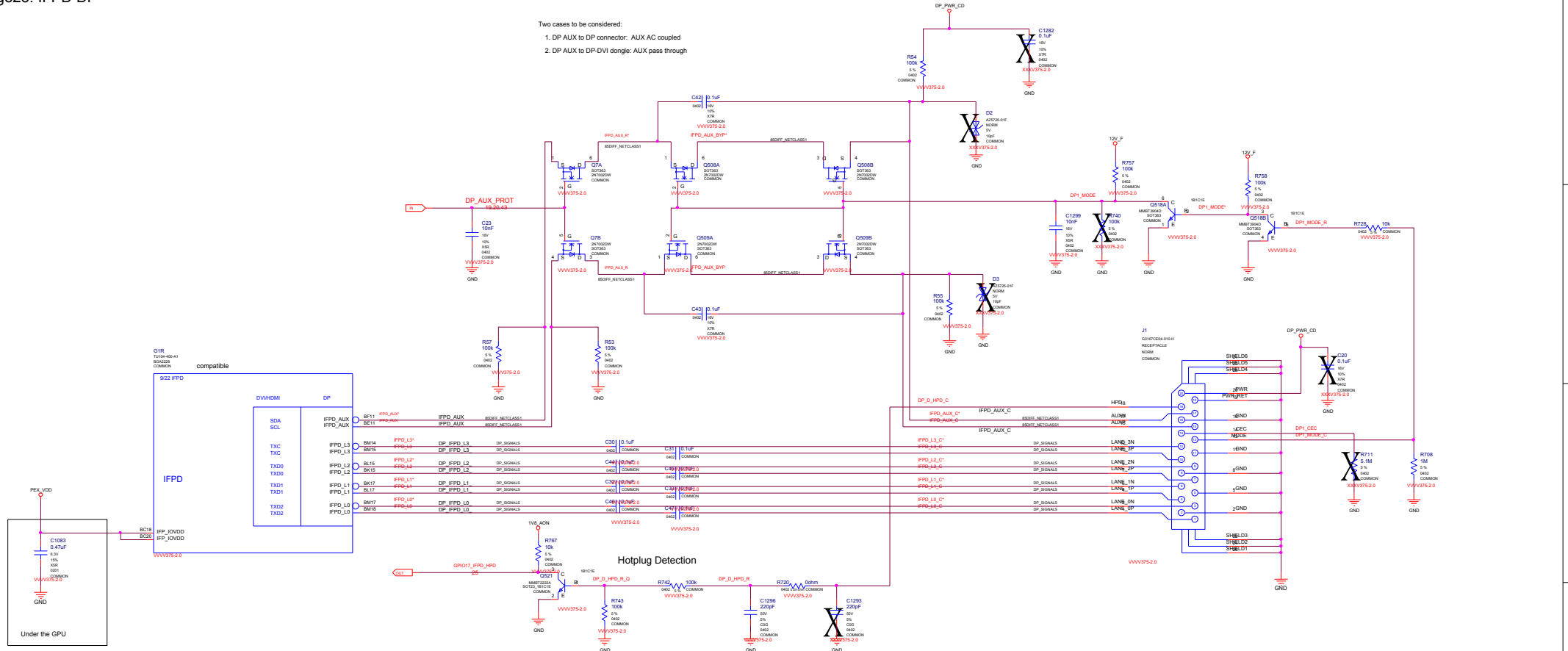


IFPE NC

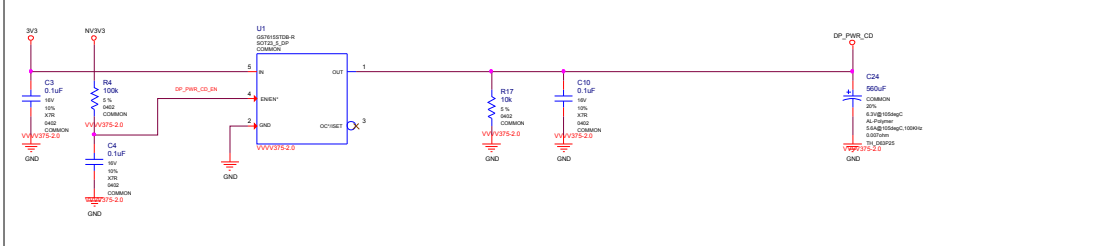


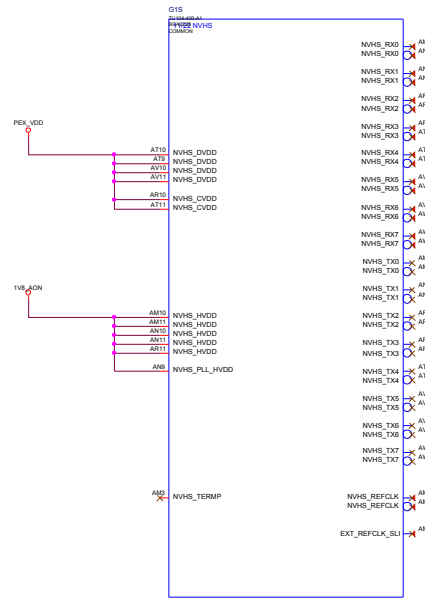
MICRO-STAR INT'L CO., LTD.			
MS-V375			
Size: Custom	Document Description: IFPC HDMI	Rev: 2.0	
Date: Monday, December 10, 2018	Sheet: 22 of 53		

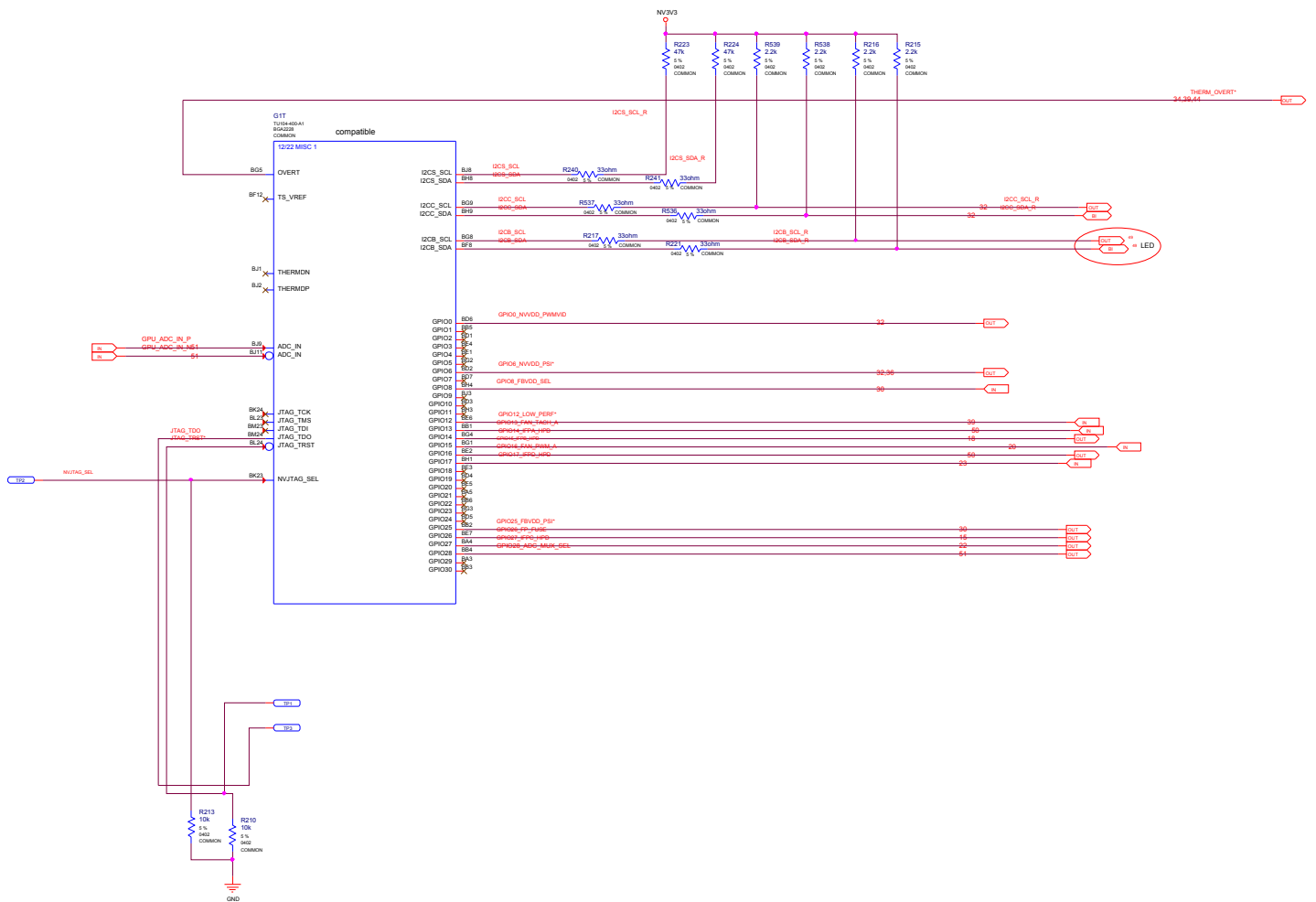
Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR







STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

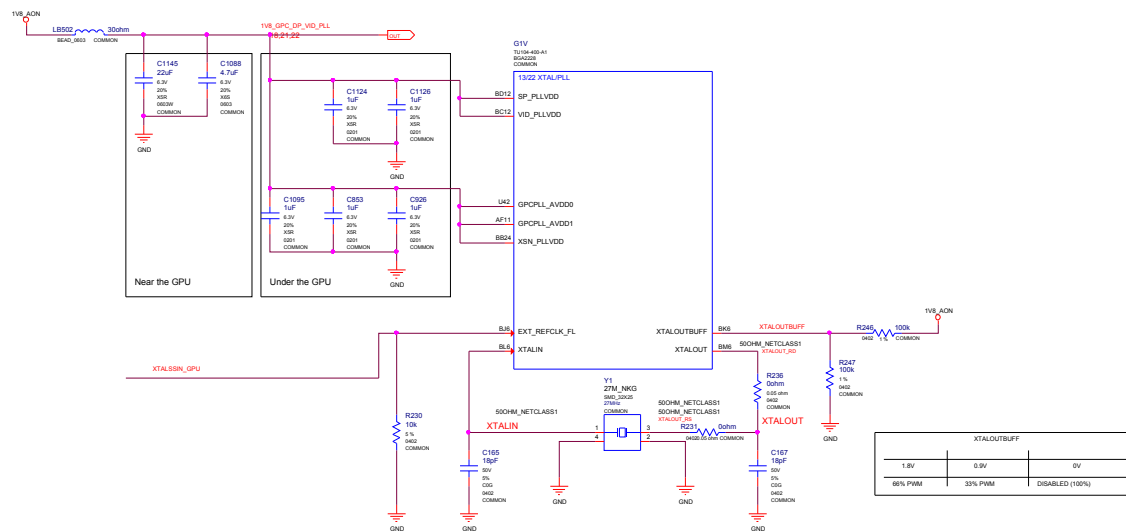
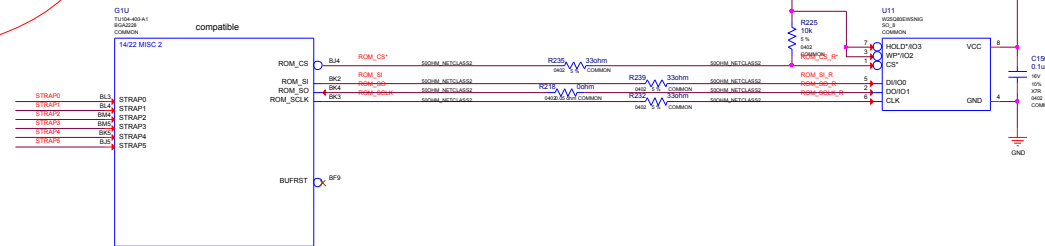
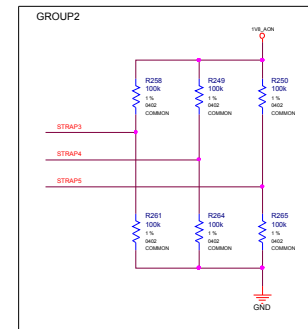
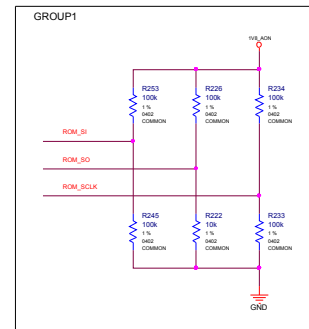
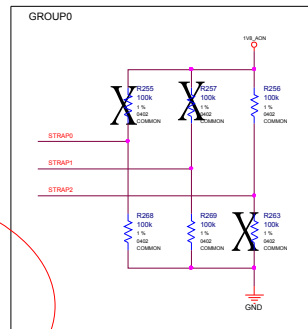
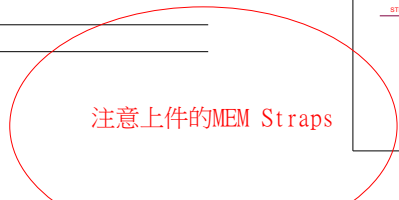
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1.ENABLE 0.DISABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCI_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

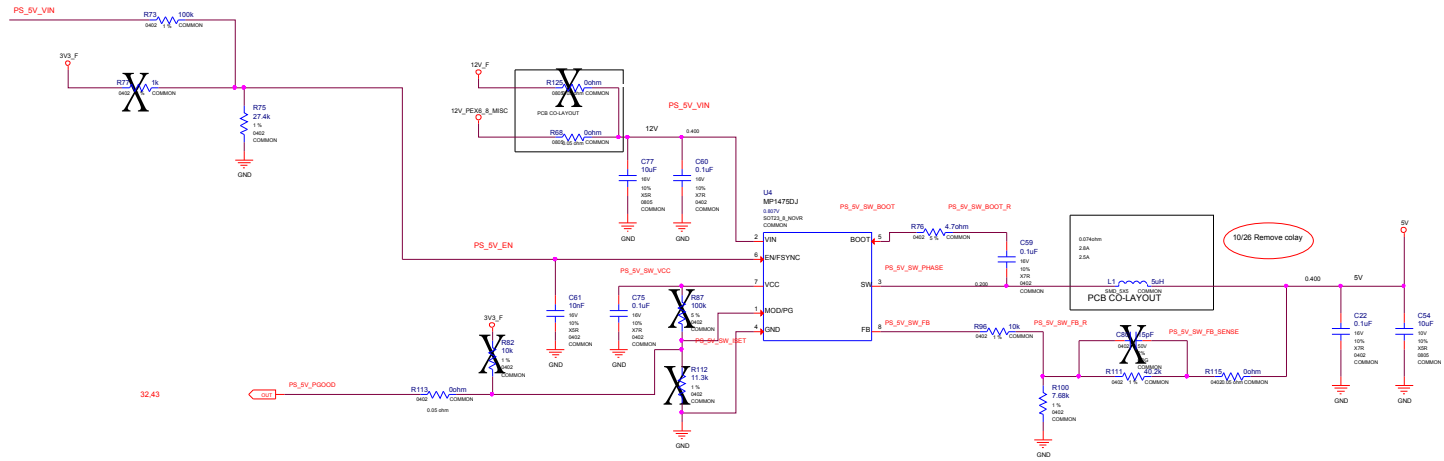
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCI_CFG LOW POWER
0:PCI_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



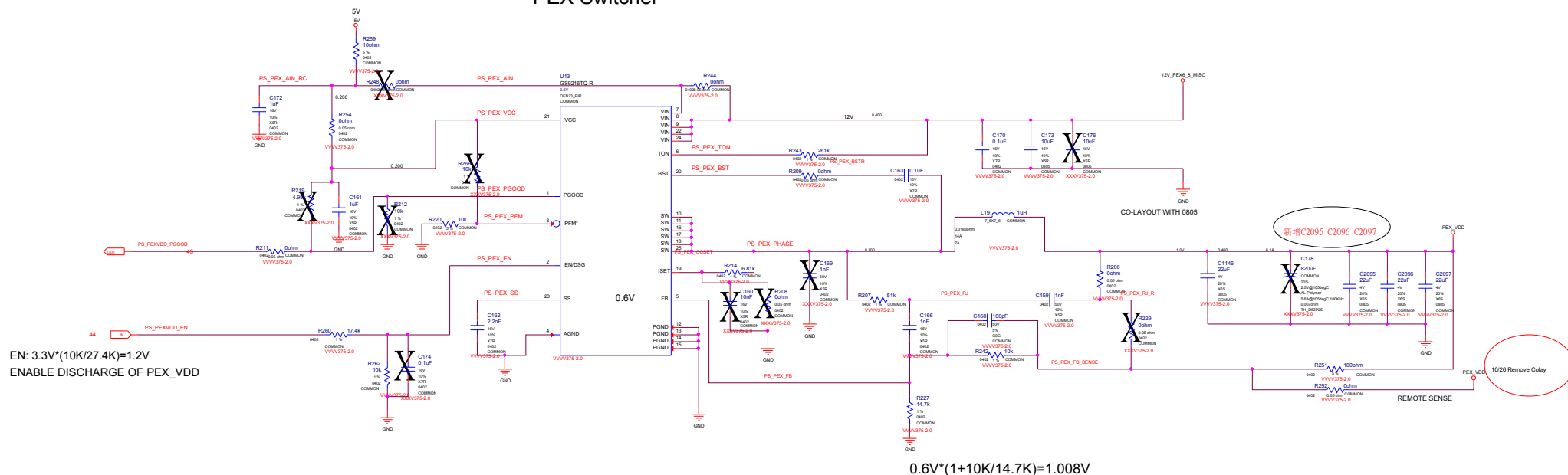
XTALOUT/BUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

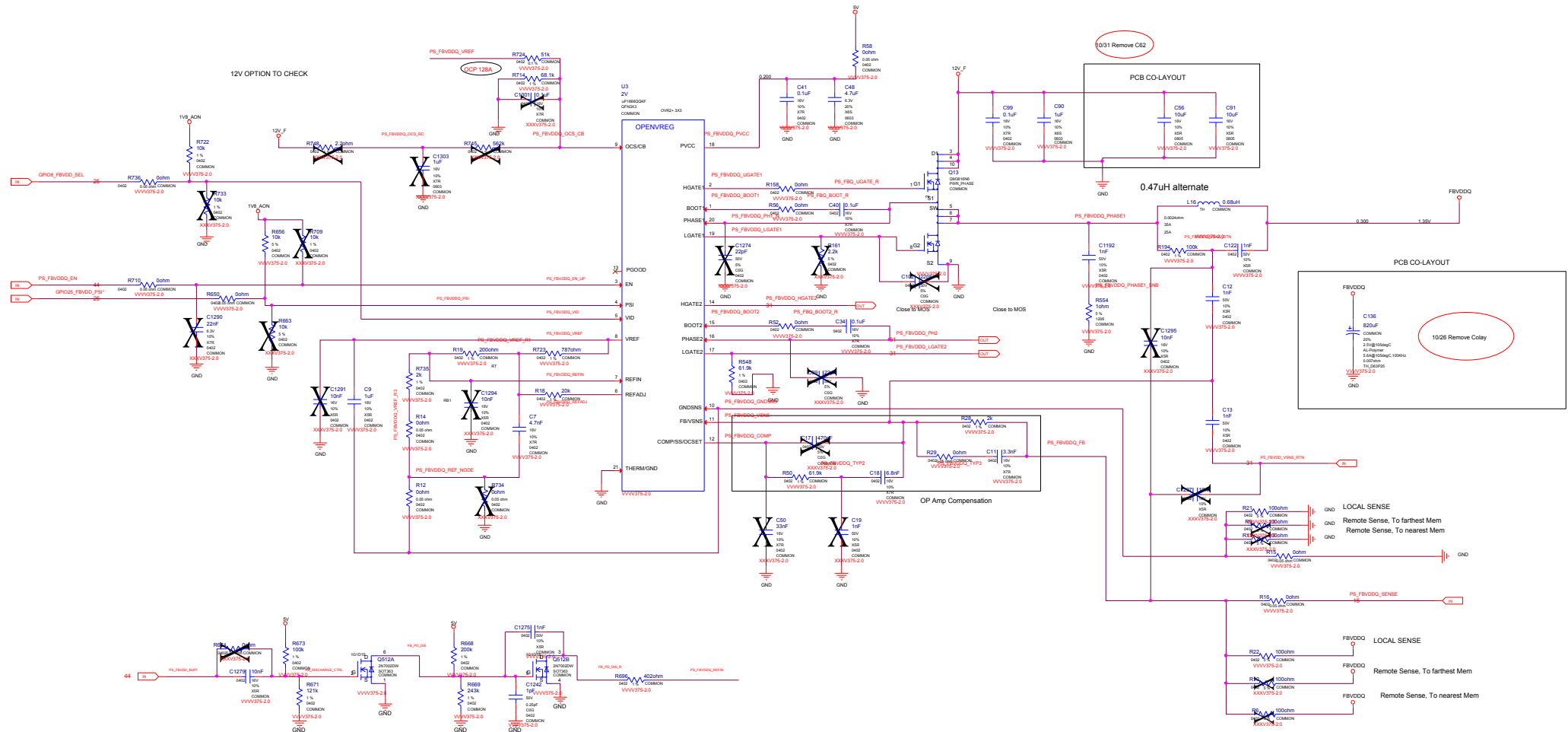
MSI MICRO-STAR INT'L CO.,LTD
MS-V375
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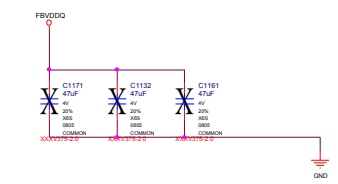
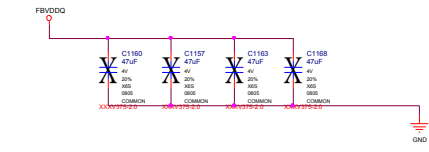
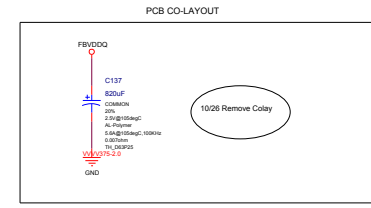
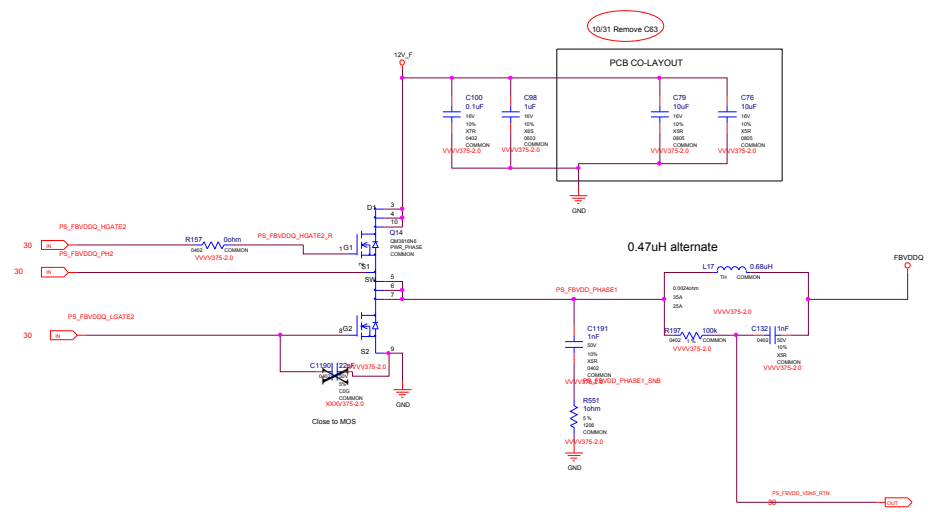


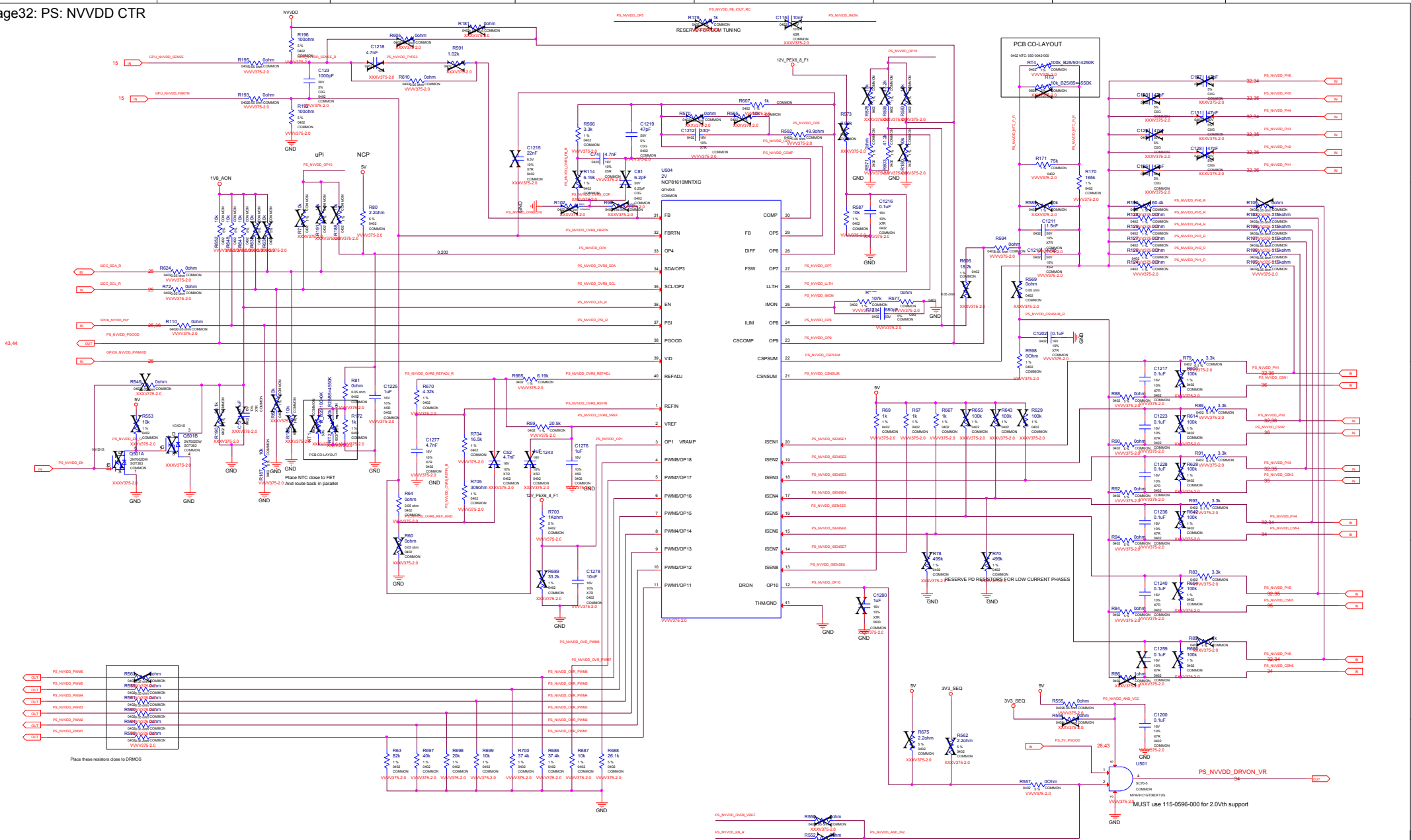
$$0.8V * (1 + 40.2K / 7.68K) = 4.9875V$$

PEX Switcher

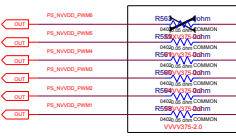




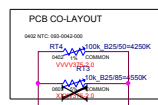




43.44



Place these resistors close to DRMONS



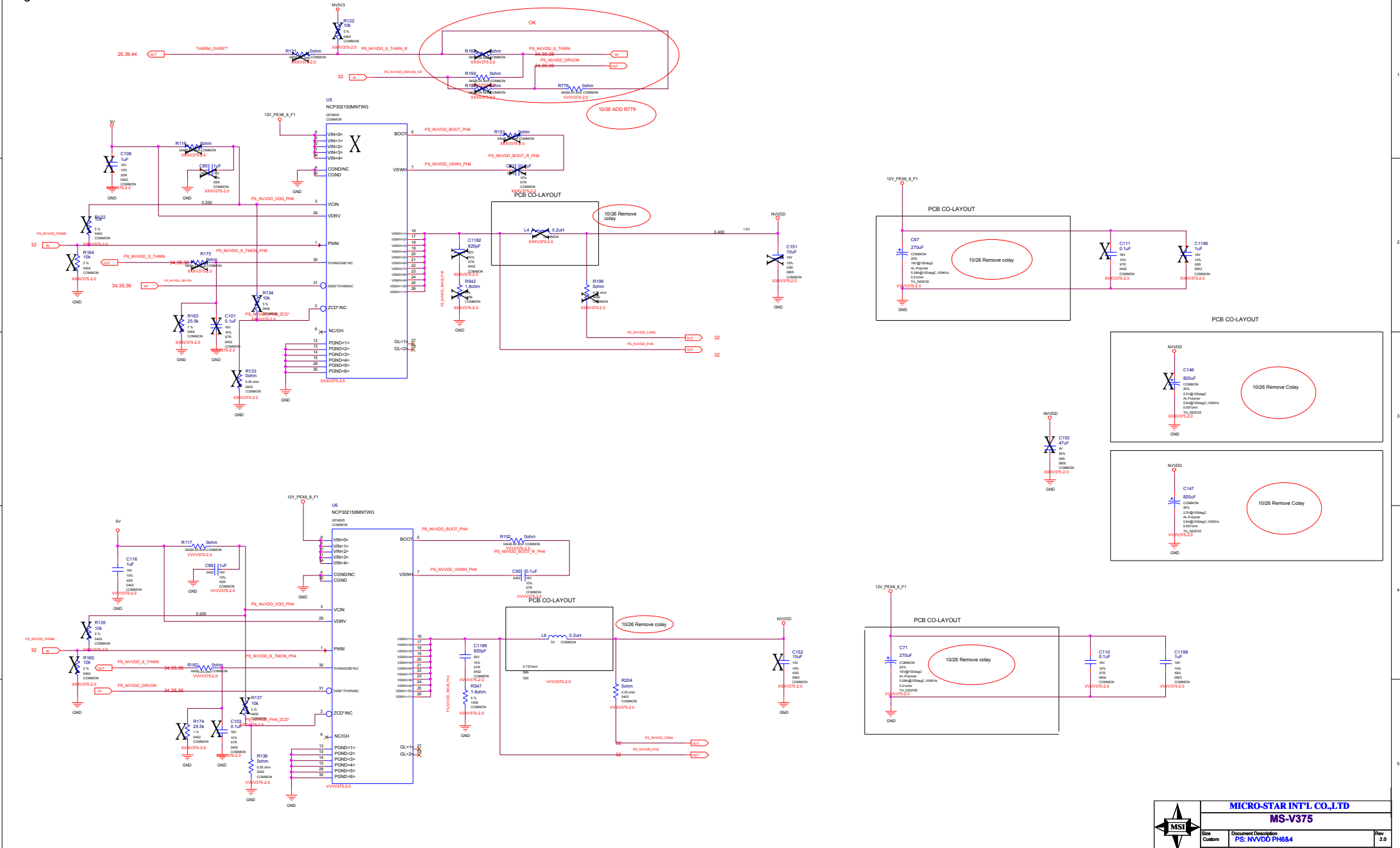
MUST use 115-0596-000 for 2.0Vth support

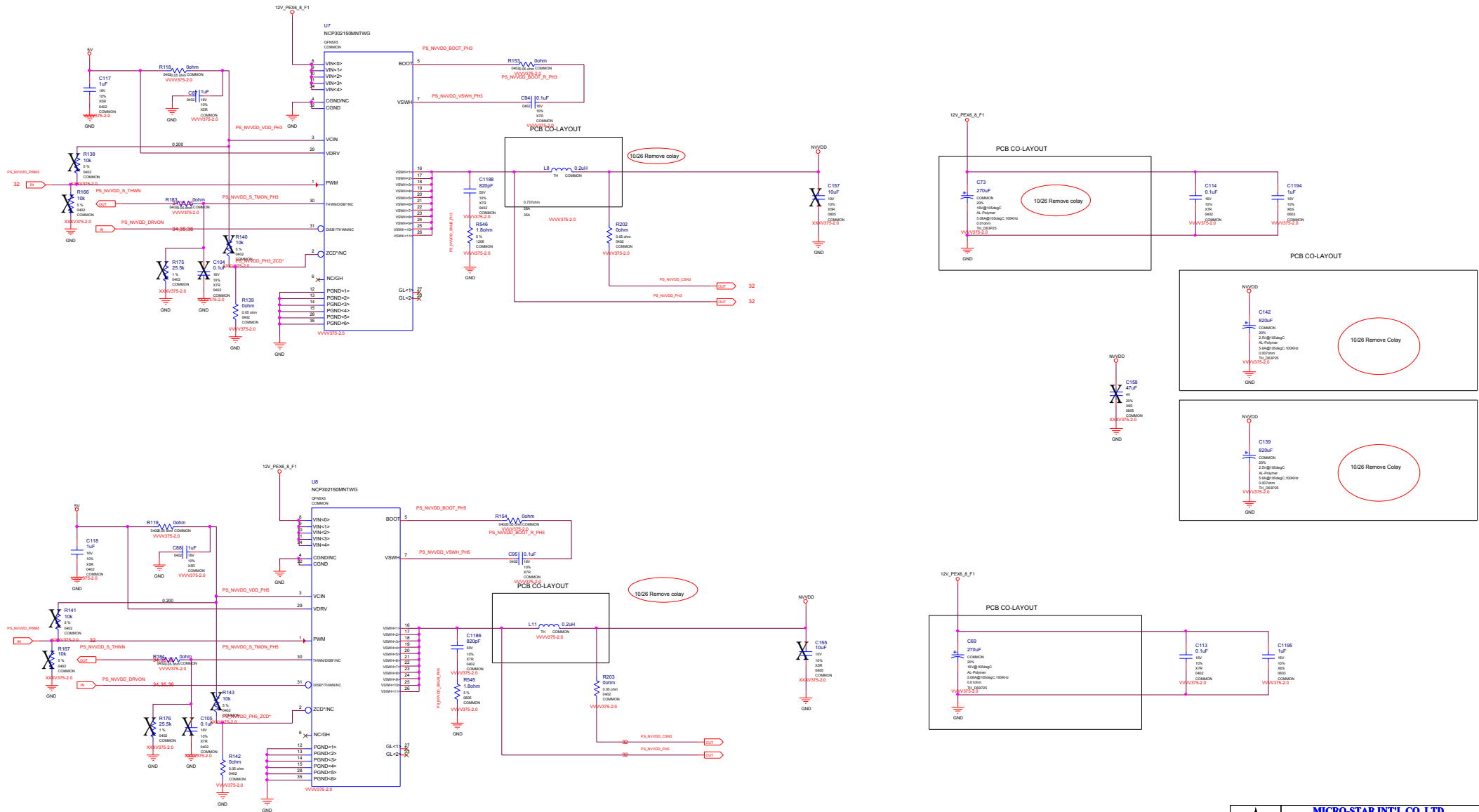
	MICRO-STAR INT'L CO.,LTD		MS-V375
	Size Custom	Document Description PS: NVVDD CTR	Rev 2.0
	Date: Monday, December 10, 2018		Sheet 32 of 53


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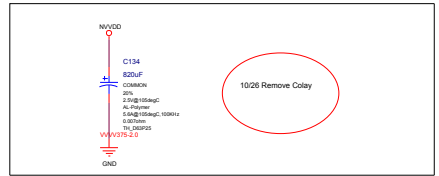
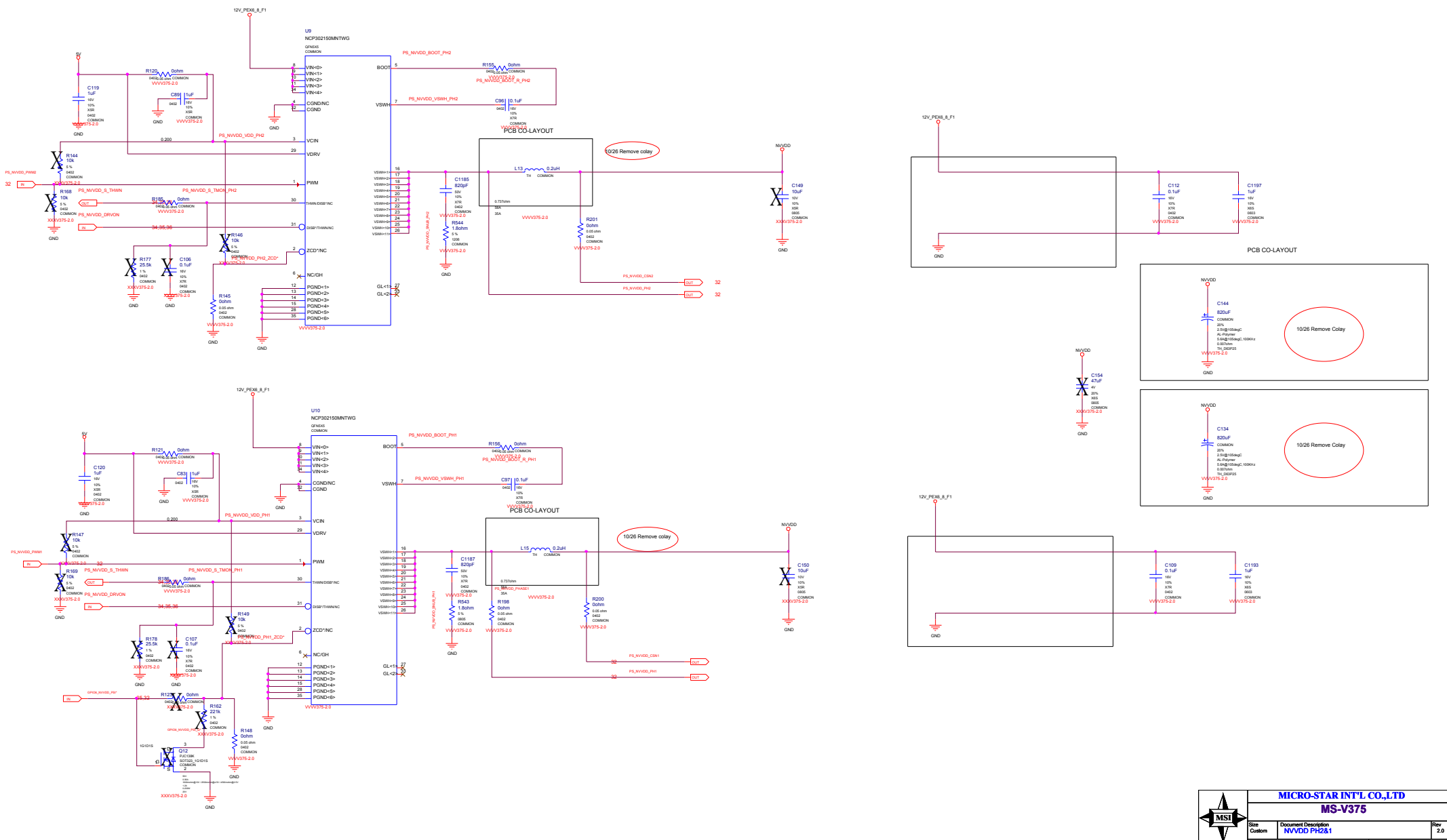
DROP OVR3i SOLUTION

	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
Size Custom	Document Description PS: NVVDD CTR OVR3i	Rev 2.0
Date: Monday, December 10, 2018		Sheet 33 of 53





	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
Size: Custom	Document Description: PS: NVVDD PH3&5	Rev: 2.0
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MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Documen Description: NVVDD PH2&1	Rev: 2.0
Date: Monday, December 10, 2018	Sheet: 36	of: 63

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DELETE RAIL BALANCE CIRCUIT

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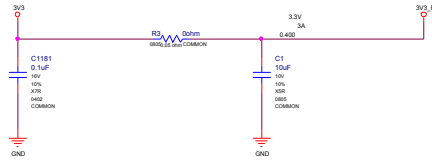
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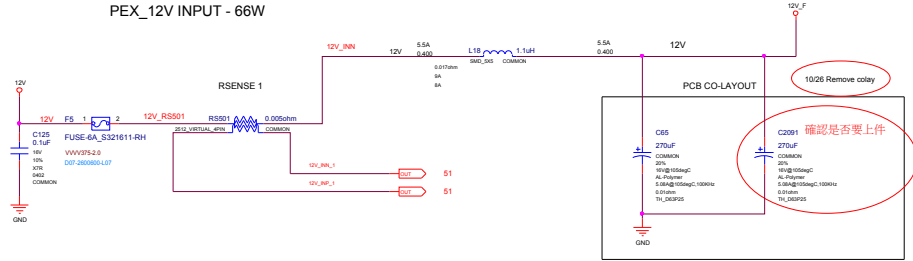
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	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description Input Power Balancing Switcher
Date: Monday, December 10, 2018		Sheet 37 of 53

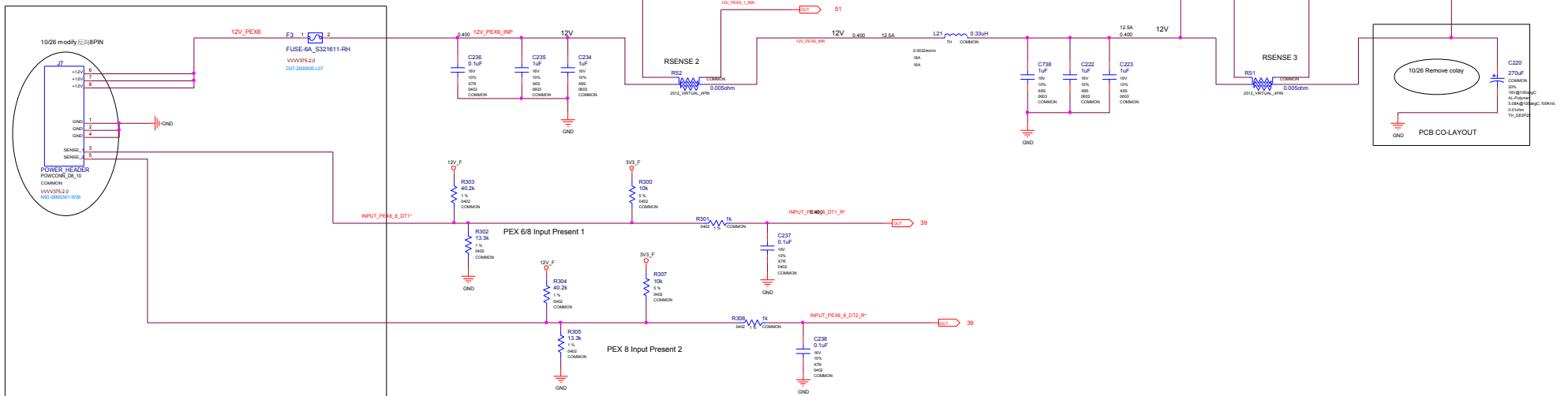
PEX 3V3 INPUT - 10W



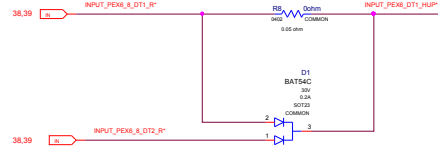
PEX_12V INPUT - 66W



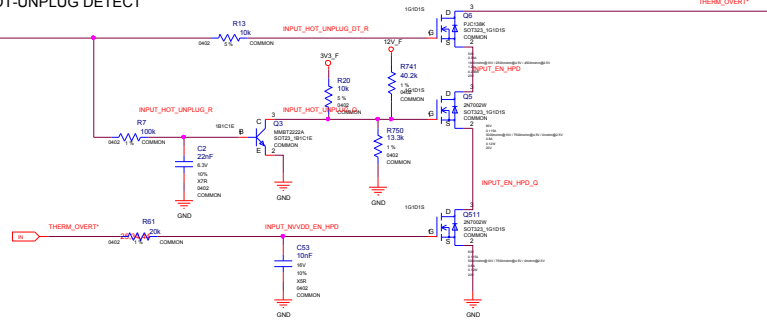
PEX8 INPUT 1 - 2x4 PCIE CON 150W



PEX Input Present 1

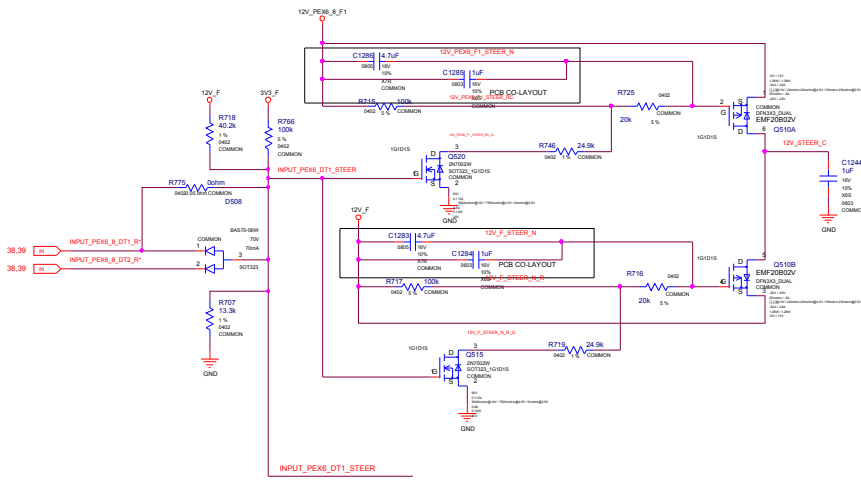


POWER CONNECTOR HOT-UNPLUG DETECT

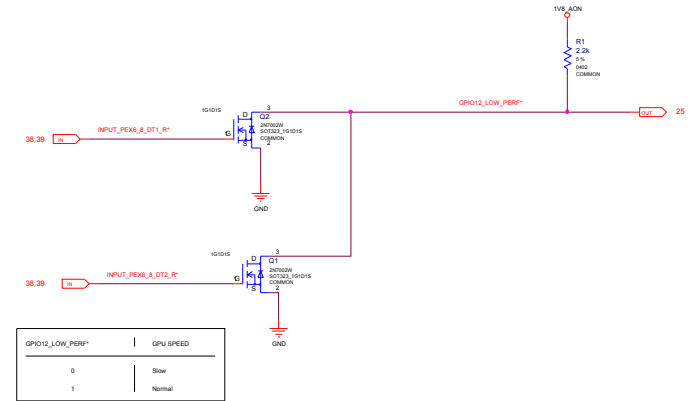


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPU12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description BUCKBOOST
Date: <u>Monday, December 10, 2018</u>		Sheet <u>40</u> of <u>53</u>

A B C D E F G H

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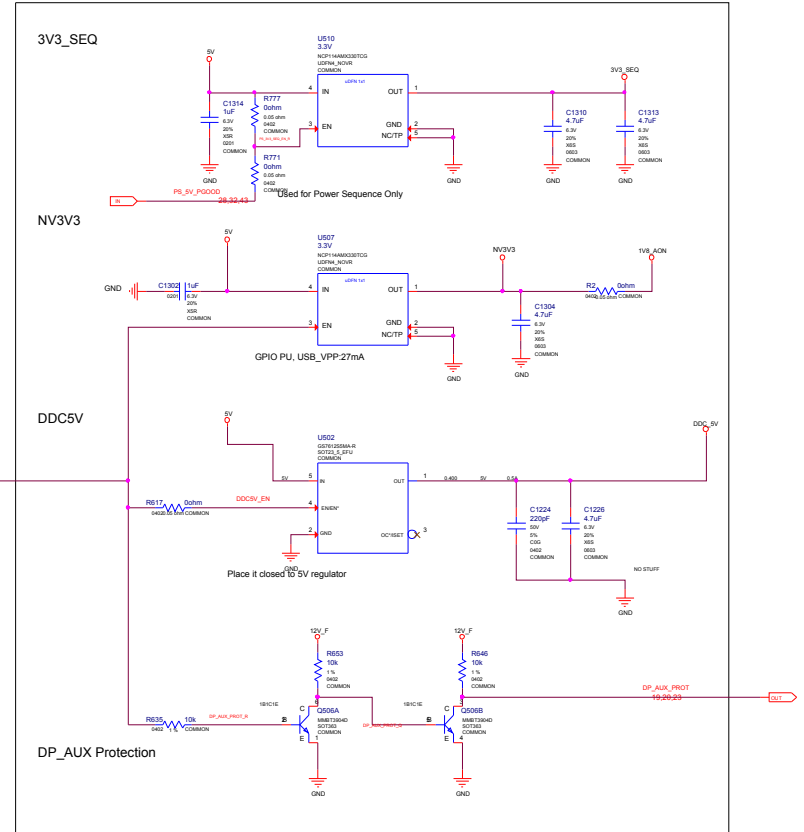
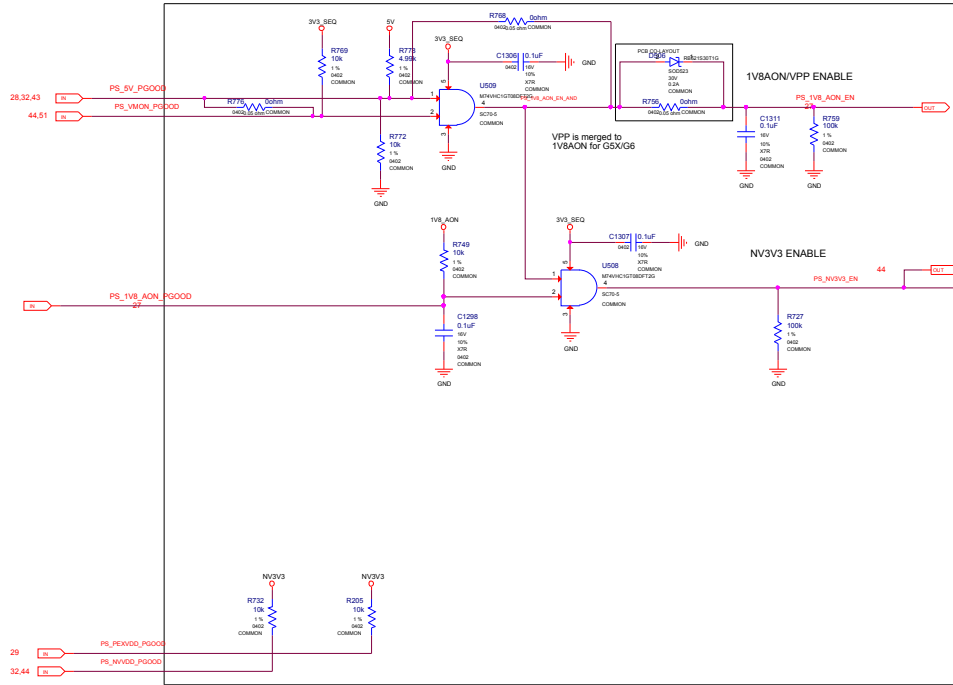
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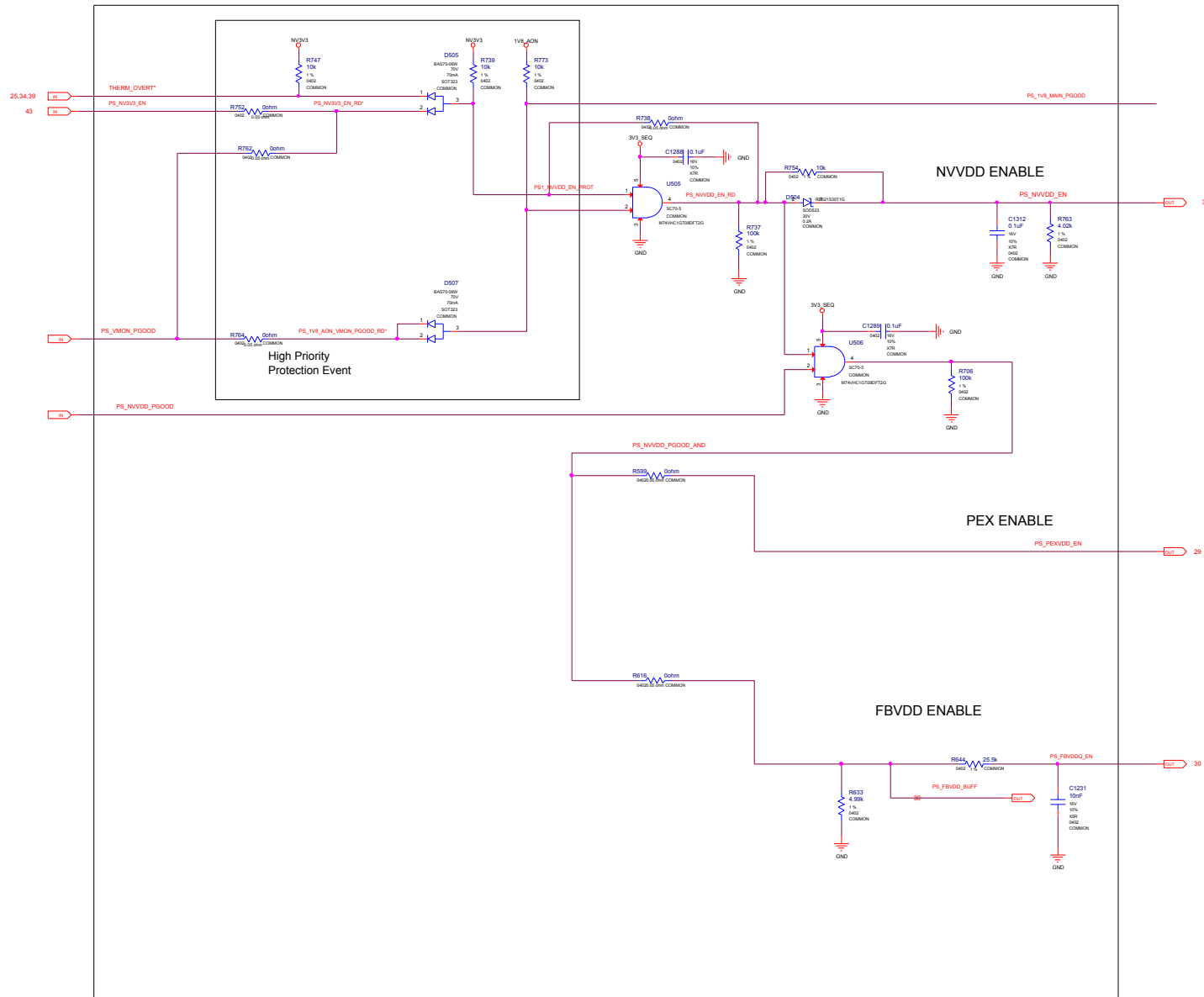
	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description PPC
Date: Monday, December 10, 2018		Sheet 41 of 53

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	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description 12V & 3V3_A SWITCHER
Date: Monday, December 10, 2018		Sheet 42 of 53





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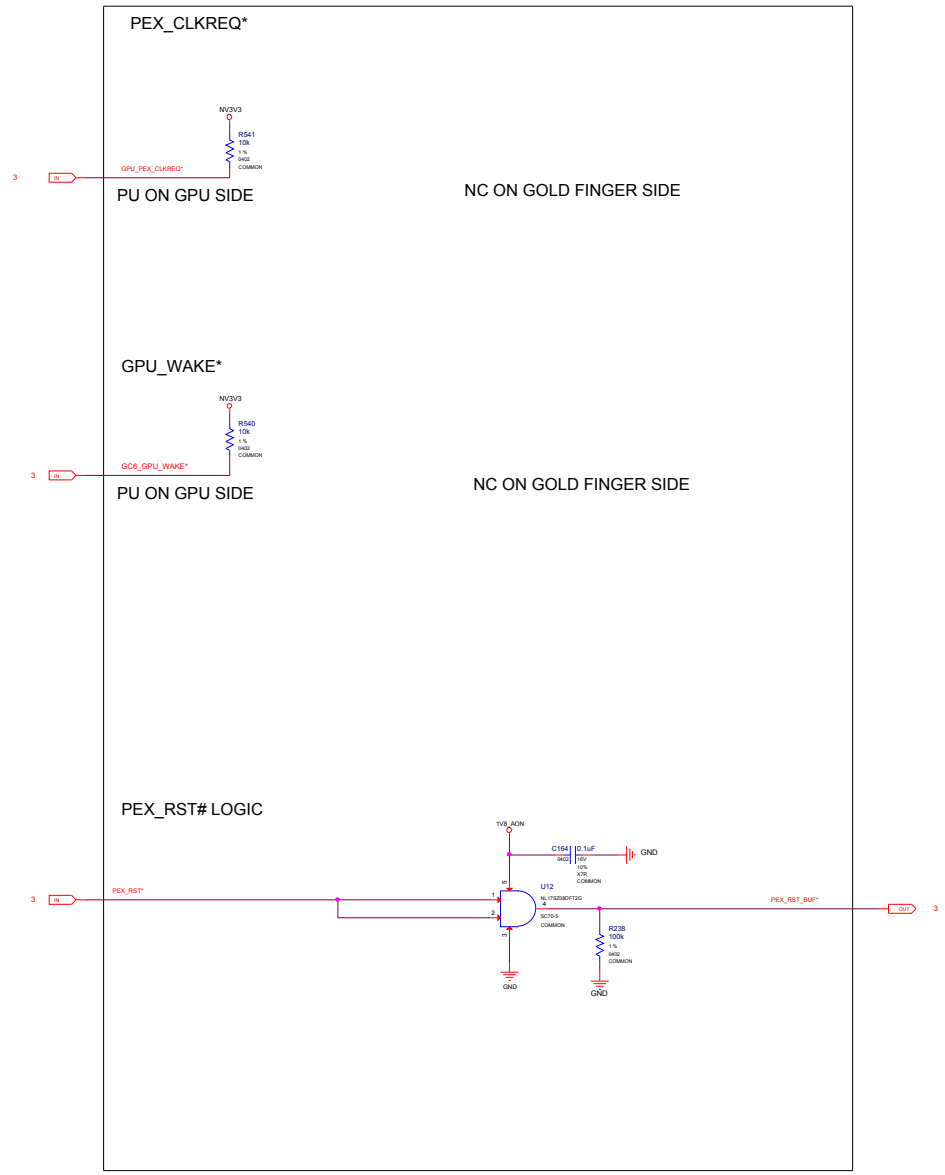
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	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description SEQUENCE:Voltage Monitor
Date: <u>Monday, December 10, 2018</u>		Sheet <u>45</u> of <u>53</u>

	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description SEQUENCE:Discharge
Date: Monday, December 10, 2018		Sheet 46 of 53



A B C D E F G H

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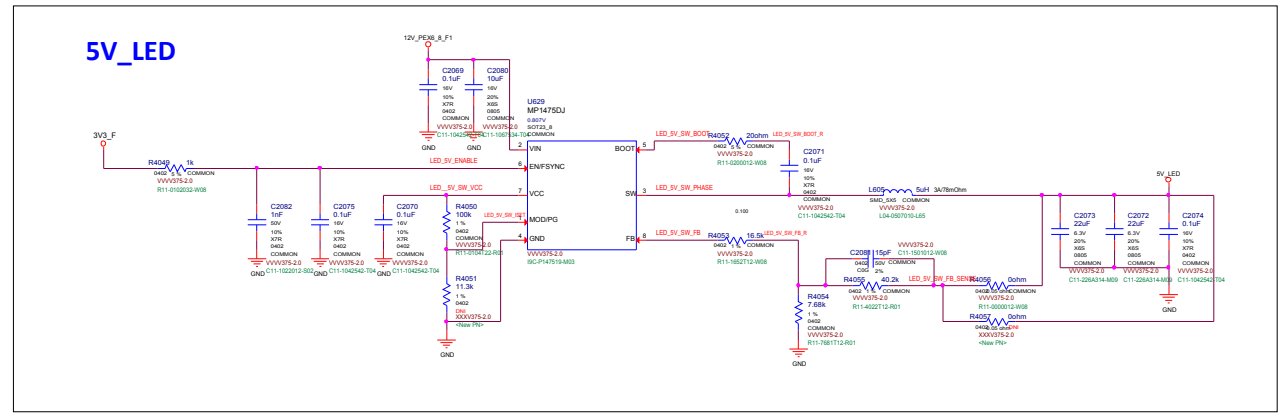
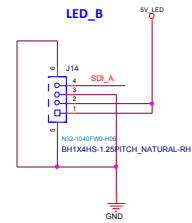
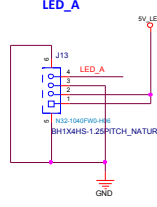
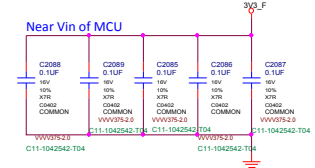
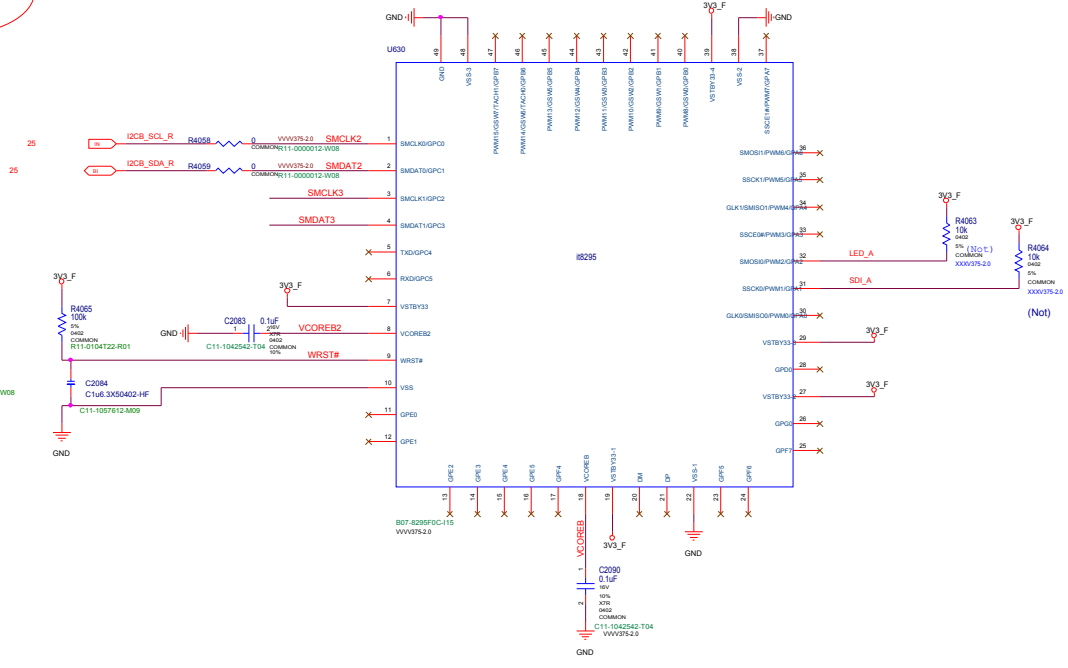
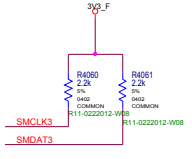
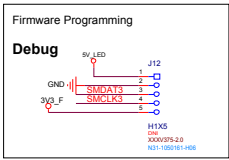
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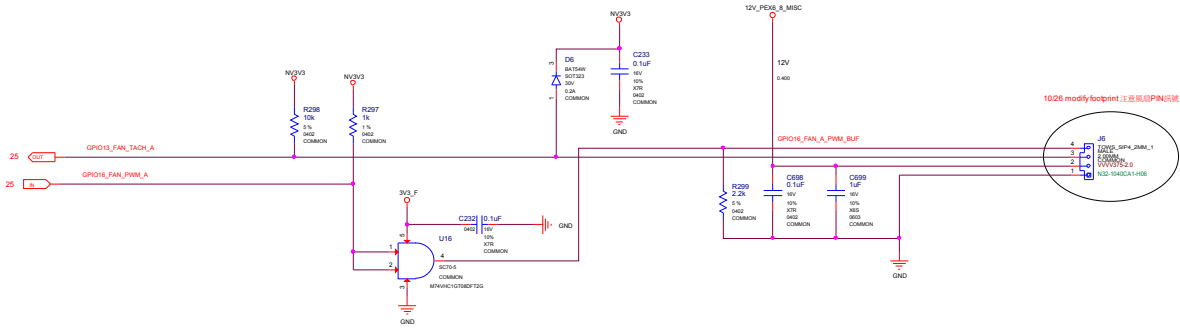
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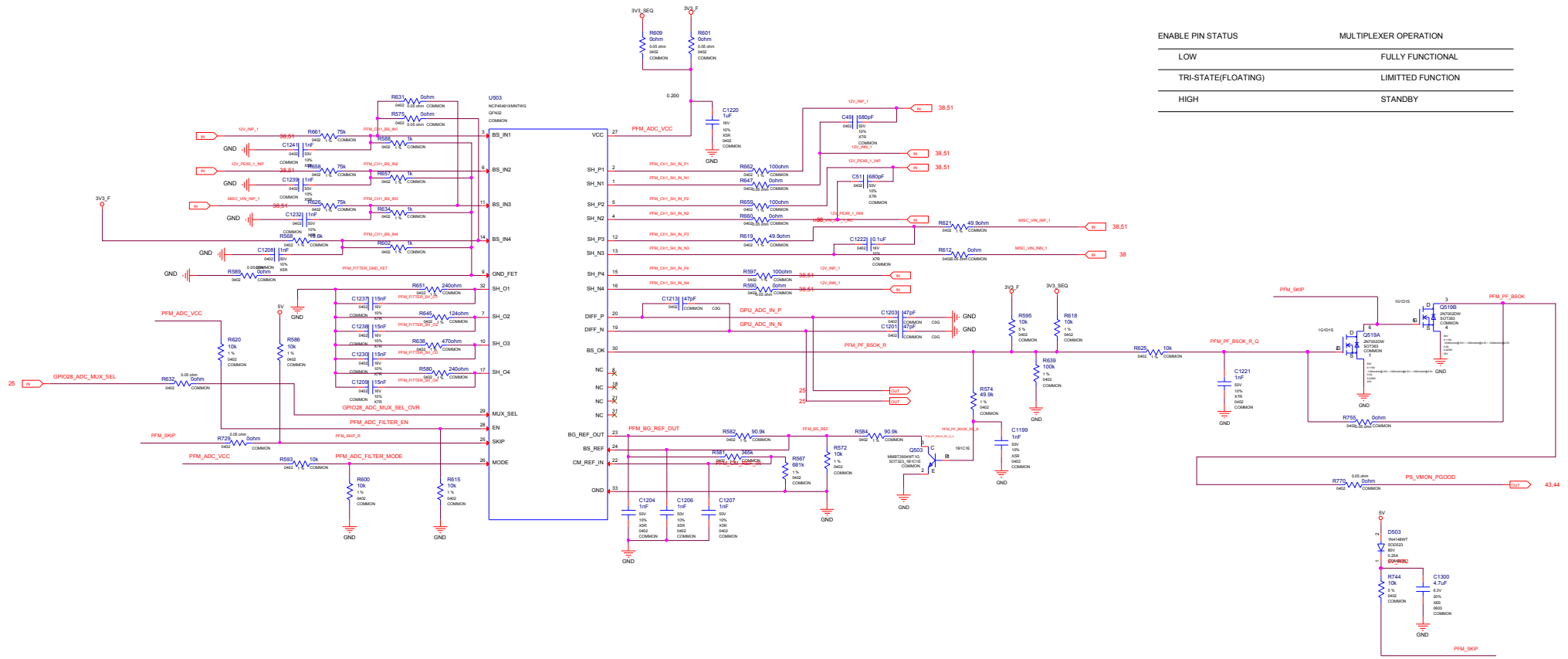
A B C D E F G H

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	MS-V375	
	Size Custom	Document Description LOGO LED
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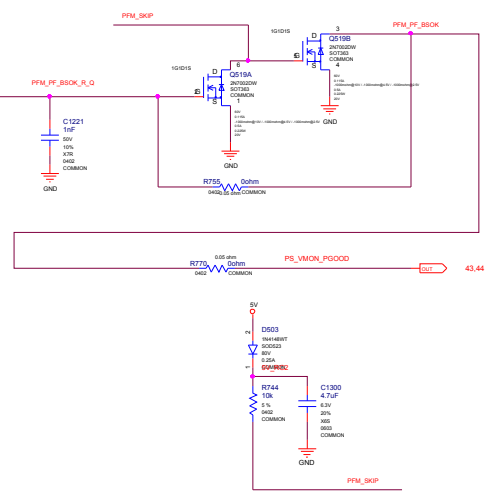


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		MS-V375	
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Custom	FAN	2.0	
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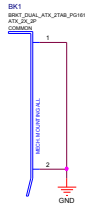


MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

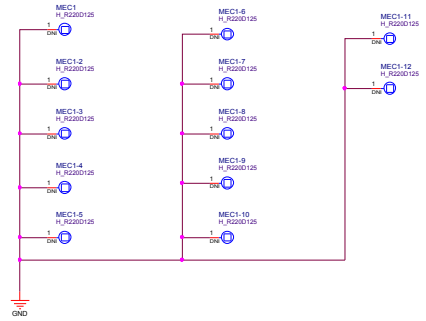
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



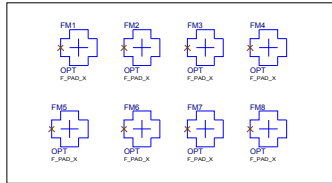
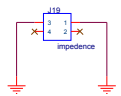
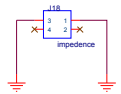
Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:



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	Custom	PTC
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