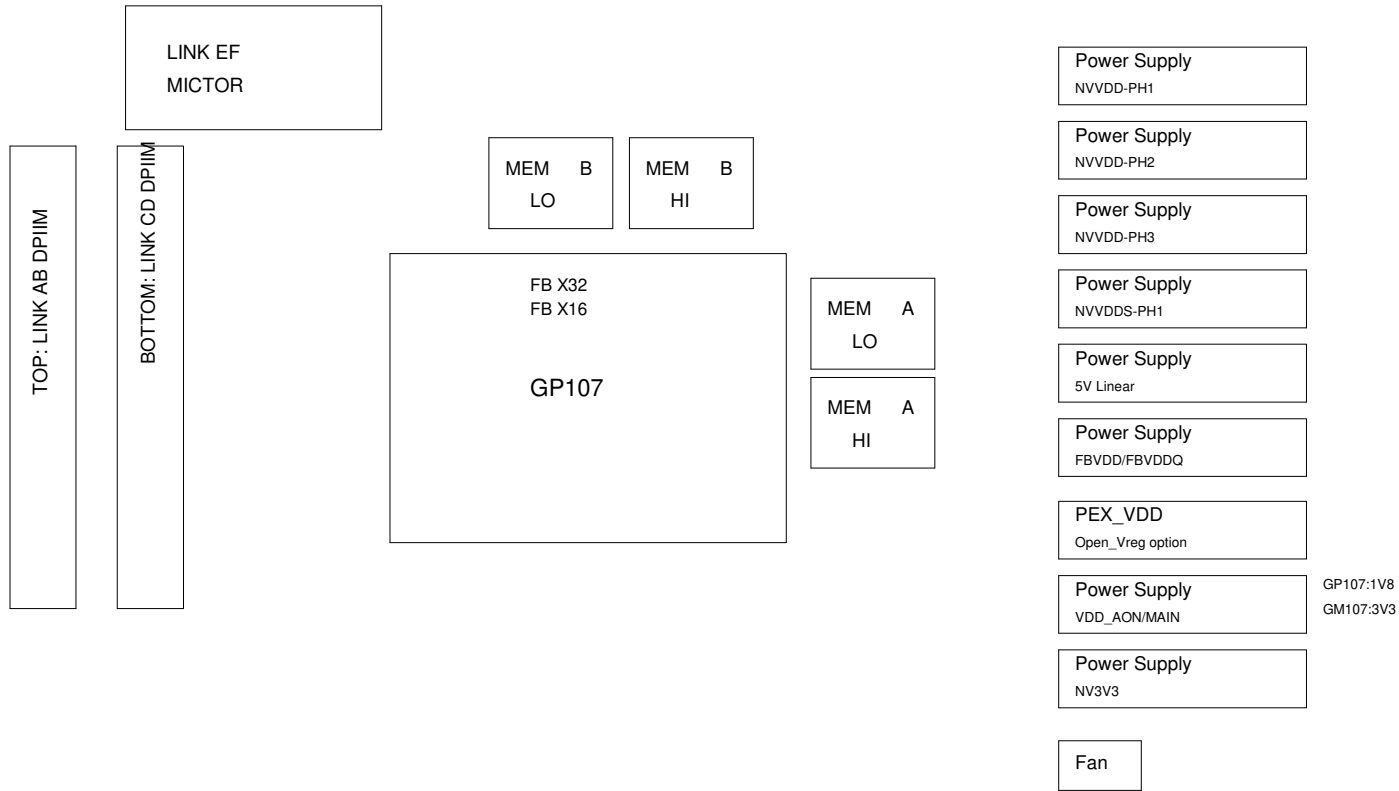


MS-V378-21
E2904
4GB GDDR5, 128b, 256Mx32
modular displays

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Page Description

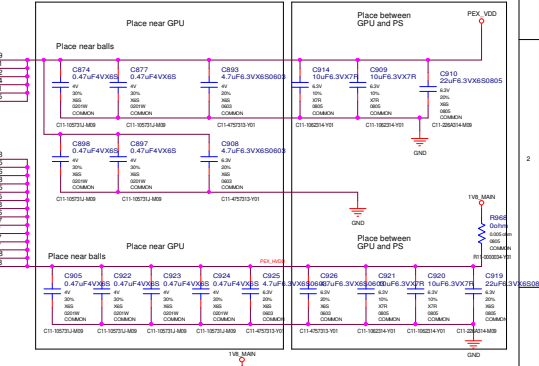
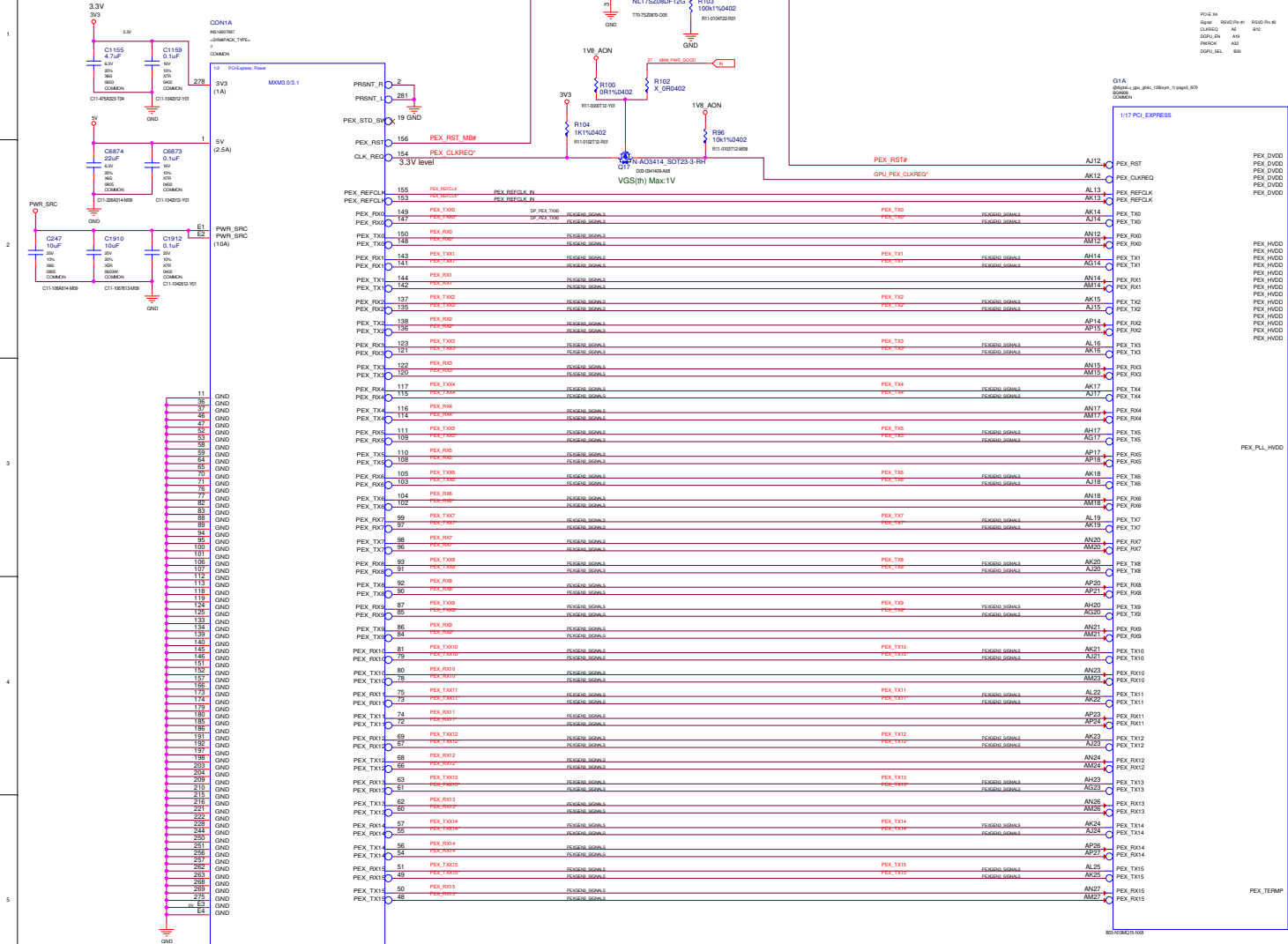
1	Table of Contents
2	BLOCK DIAGRAM
3	PCI Express
4	GPU FB_AB
5	MEM: FBA[31:0]
6	MEM: FBA[63:32]
7	MEM: FBB[31:0]
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9	GPU PWR
10	GPU GND FBVDDQ
11	IFPAB
12	IFPEF
13	IFPCD
14	GPIO, THERMAL, MISC
15	Straps,ROM, XTAL,
16	Power Sequence Control
17	1V8_AON
18	PEXVDD
19	FBVDD CONTROLLER
20	NVVDD CONTROLLER
21	MXM Connector
22	GPIO Pin Define



ROE M1
 ROW R00 P+H1 R50 P+H
 COLR2 AL R51
 COLR3 AH R44
 PER2K R10 A2
 COLR1LH AH R44
 COLR1LH AH R44
 COLR1LH AH R44

ROE M4
 ROW R00 P+H1 R50 P+H
 COLR2 AL R51
 COLR3 AH R44
 PER2K R10 A2
 COLR1LH AH R44
 COLR1LH AH R44

PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N19M-Q3	4	2	2	1



PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N19M-Q3	4	2	2	1

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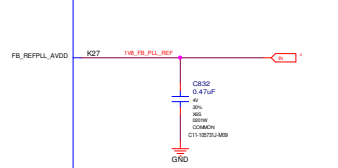
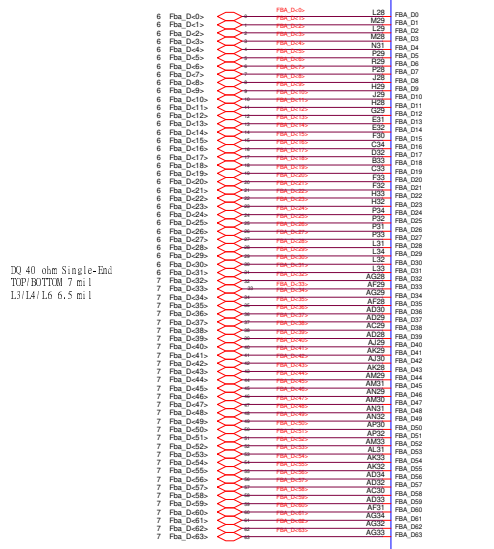
Doc: Document Description
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 Date: Monday, October 14, 2019
 Sheet: 3 of 22

G18
@Silicon Labs, 2018
COMMON

G17C
@Silicon Labs, 2018
COMMON

S17 FBA

S17 FBB



DO 40 ohm Single-End
TOP/BOTTOM 7 m l
1.3/1.4/1.6 6.5 m l

DO 40 ohm Single-End
TOP/BOTTOM 7 m l
1.3/1.4/1.6 6.5 m l

DO 45 ohm Single-End
TOP/BOTTOM 5.5 m l
1.3/1.4/1.6 5.5 m l

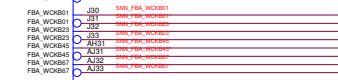
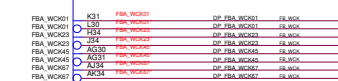
DO 45 ohm Single-End
TOP/BOTTOM 5.5 m l
1.3/1.4/1.6 5.5 m l

DBI / EDC 40 ohm Single-End
TOP/BOTTOM 7 m l
1.3/1.4/1.6 6.5 m l

DBI / EDC 40 ohm Single-End
TOP/BOTTOM 7 m l
1.3/1.4/1.6 6.5 m l

CLK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 m l
1.3/1.4/1.6 4.5 / 4 m l

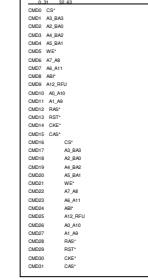
WCK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 m l
1.3/1.4/1.6 4.5 / 4 m l



Place near GPU



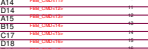
GDQR, BDAT0, MIRR COMMAND MAP



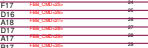
CKE



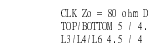
RESET



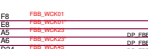
FB_VDD0



FB_VDD0



FB_VDD0



FB_VDD0



FB_VDD0



FB_VDD0



FB_VDD0



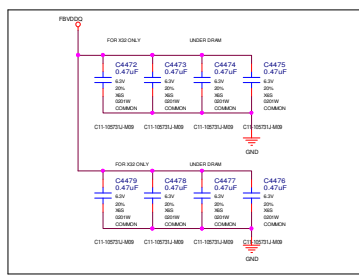
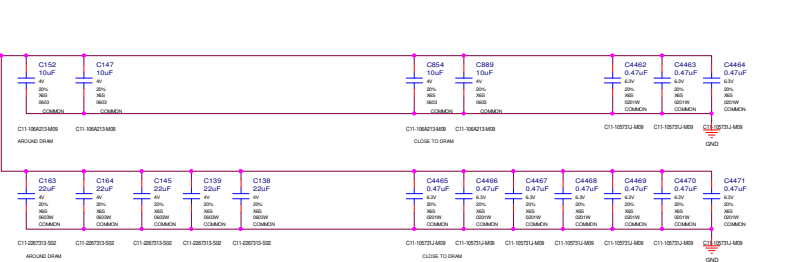
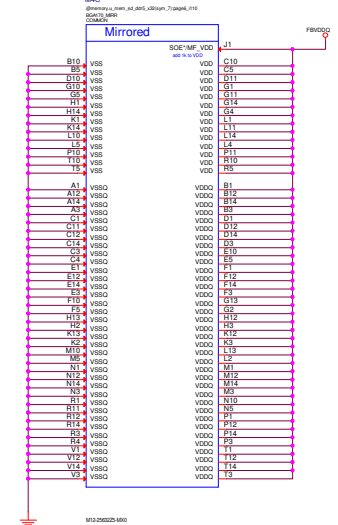
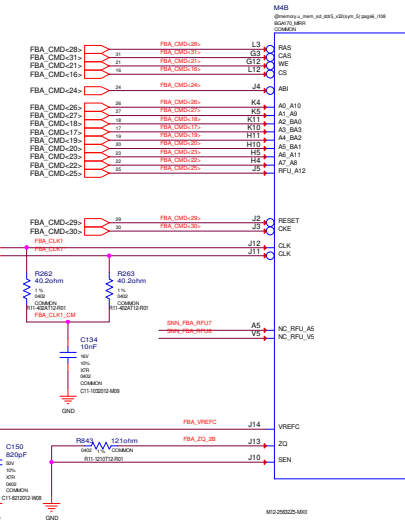
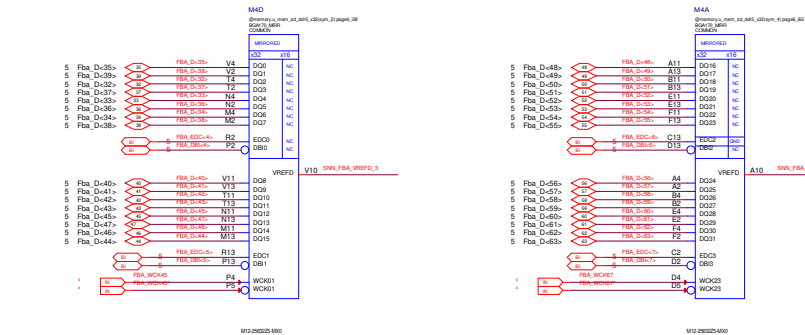
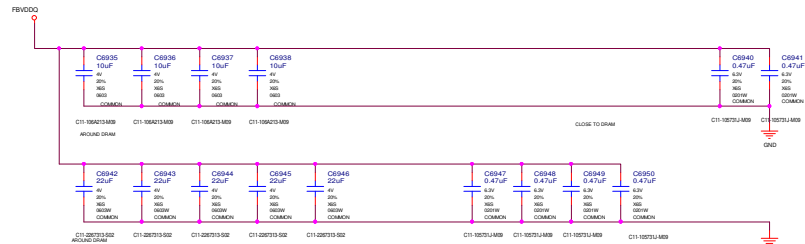
FB_VDD0

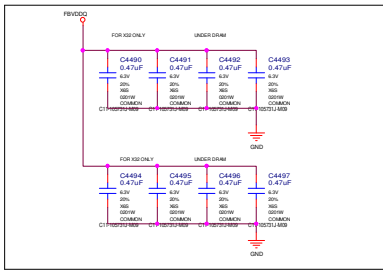
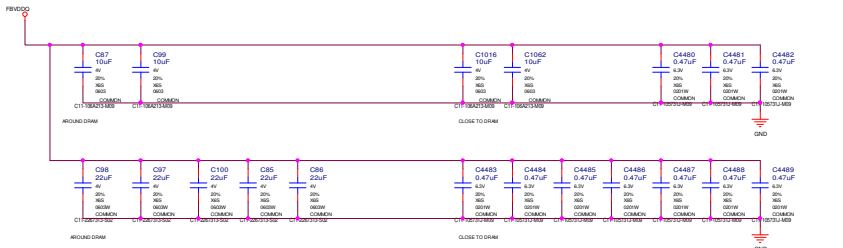
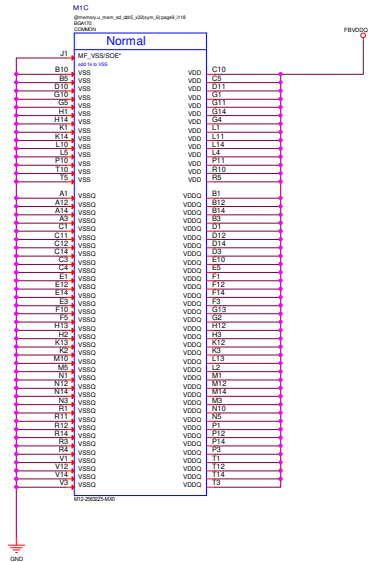
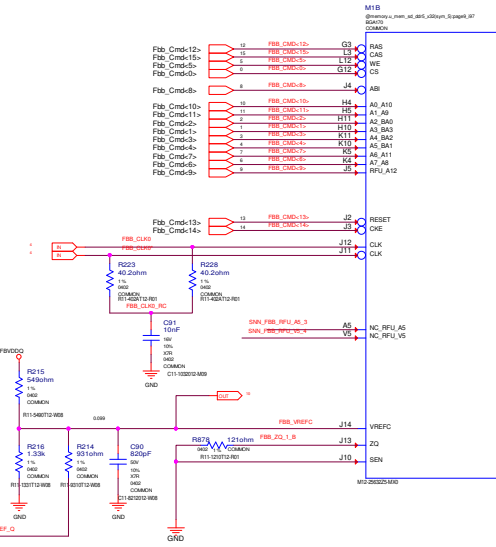
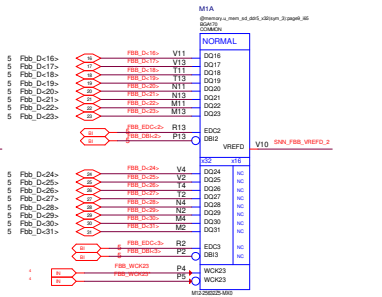
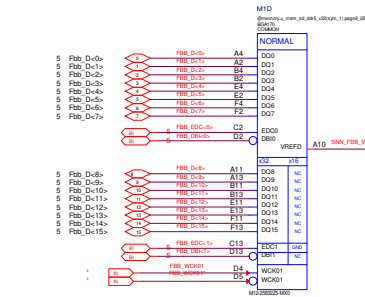
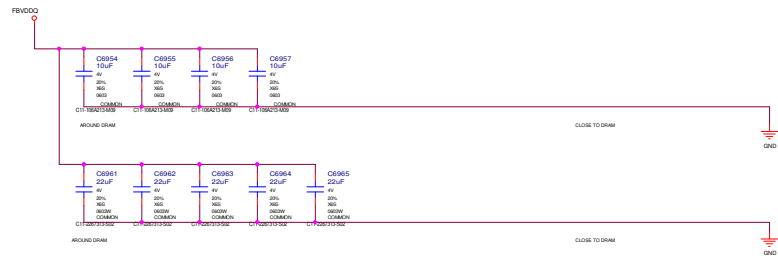


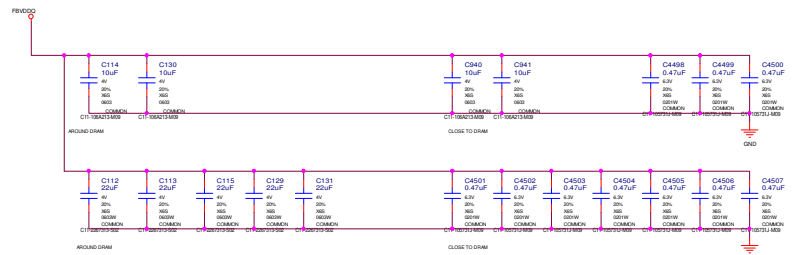
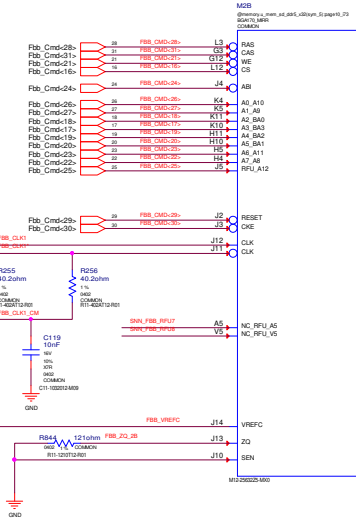
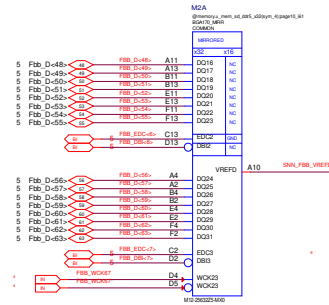
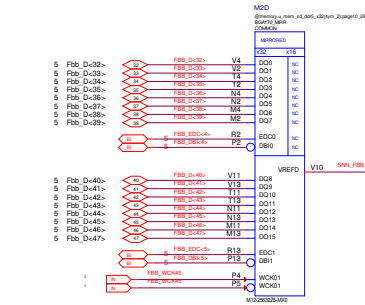
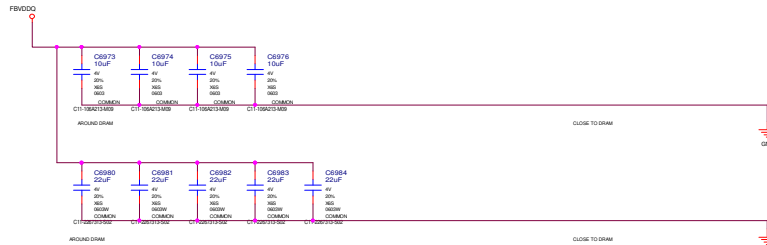
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1.0	GPU FB_AB	2.1

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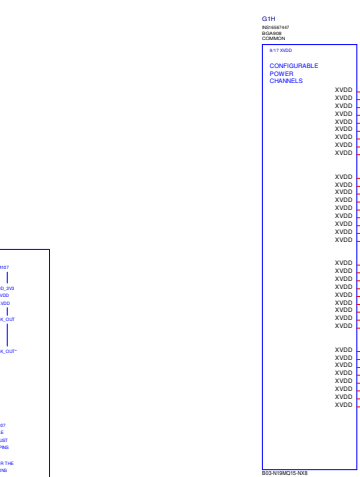
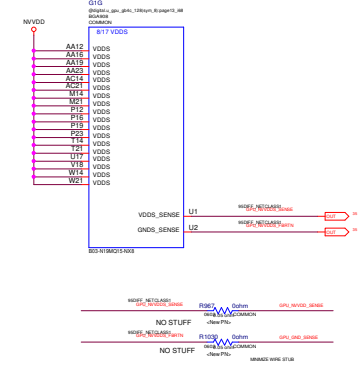
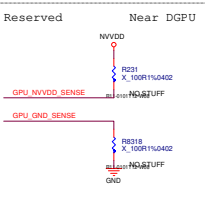
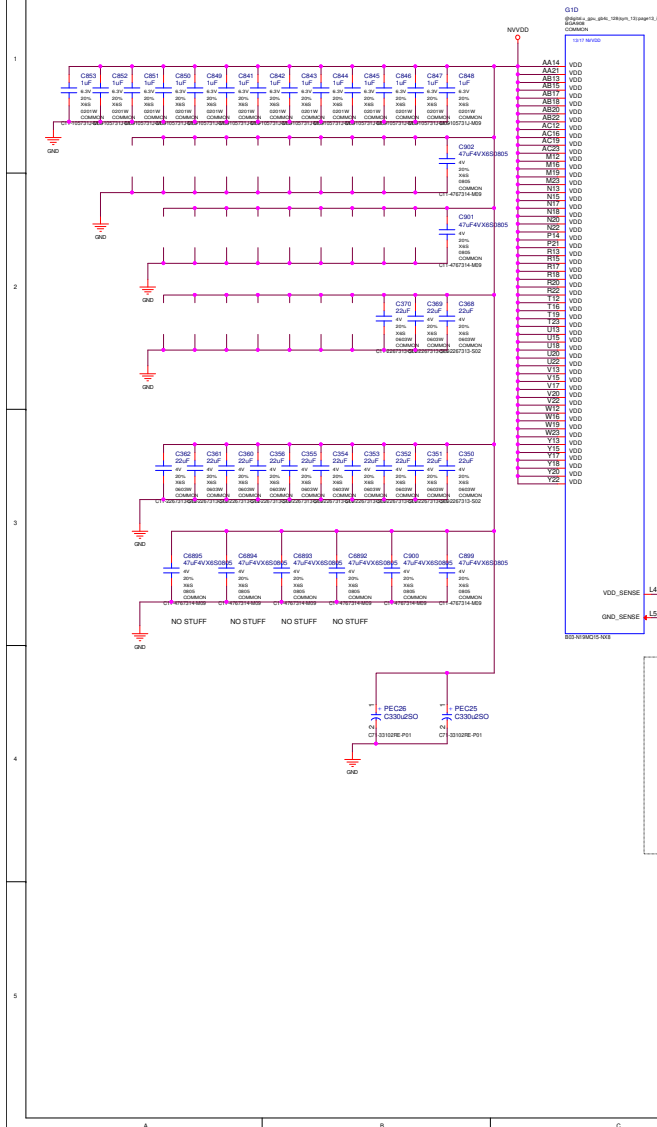




NVDD+NVDD5

13 x 1uF(Under GPU)
 2 x 47uF(Under GPU)
 3 x 22uF(Near GPU)
 2 x 47uF(Near GPU)
 10 x 22uF(Near GPU)

NVDD	1uF X7R	47uF X6S	10uF X6S	22uF X6S
N19M-Q3	13	4	0	13



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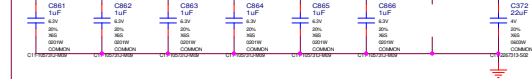
Doc: MS-V378-01 Rev: 1.0
 Date: 2018/10/14

FBVDDQ

Partition A
1X 22uF, 6 X 1uF



Partition B
1 X 22uF, 6 X 1uF



Place close to GPU



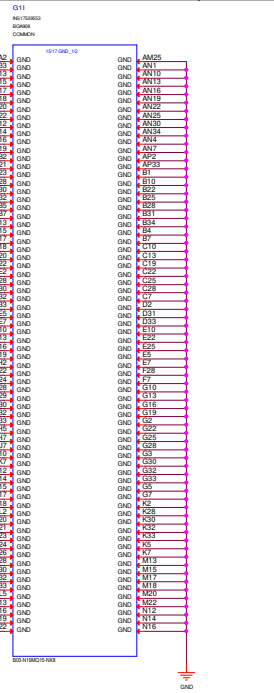
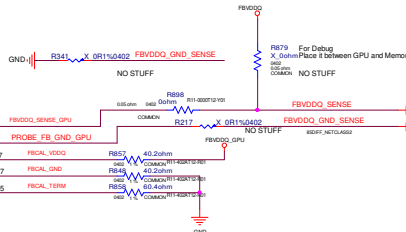
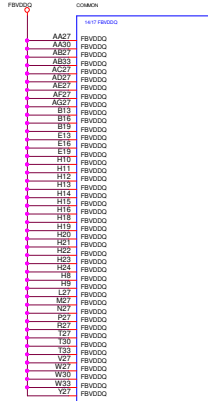
FBVDDQ
12 x 1uF(Under GPU)
2 x 22uF(Under GPU)
6 x 22uF(Near GPU)

Place close to GPU



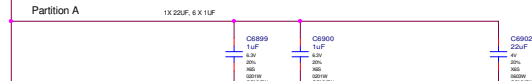
FBVDDQ	1uF X7R	10uF X6S	22uF X6S
N19M-Q3	12	0	8

FBVDDQ



1V8_AON	0.1uF X7R	1uF X6S	4.7uF X6S
N19M-Q3	2	1	1

Partition A
1X 22uF, 6 X 1uF



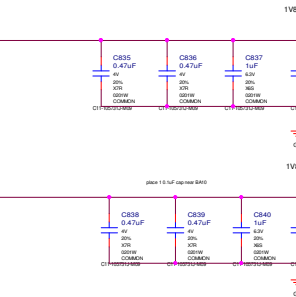
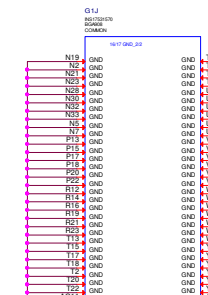
Partition B
1 X 22uF, 6 X 1uF



Place close to GPU

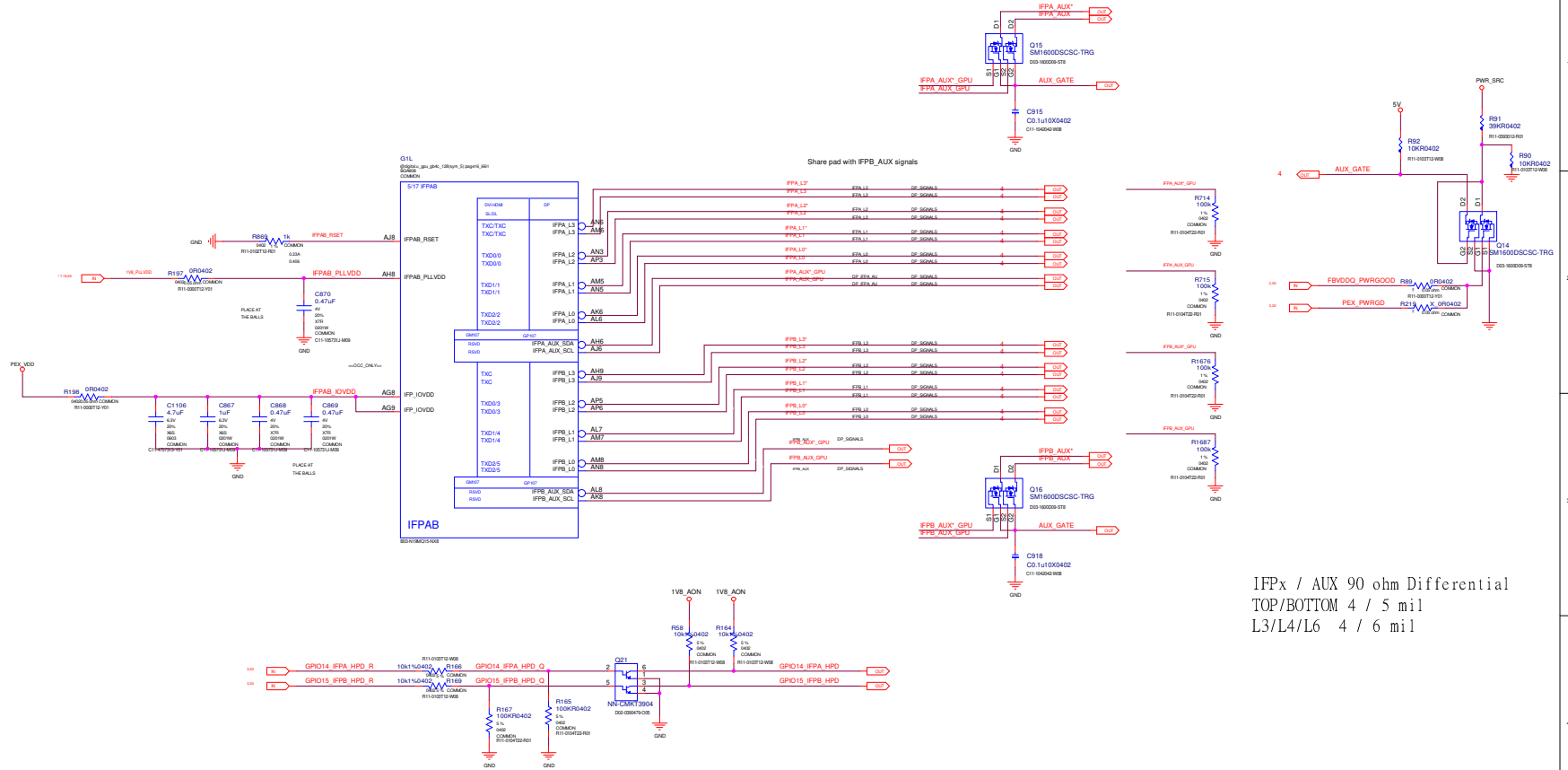


FBVDDQ
12 x 1uF(Under GPU)
2 x 22uF(Under GPU)
6 x 22uF(Near GPU)

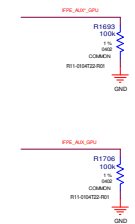
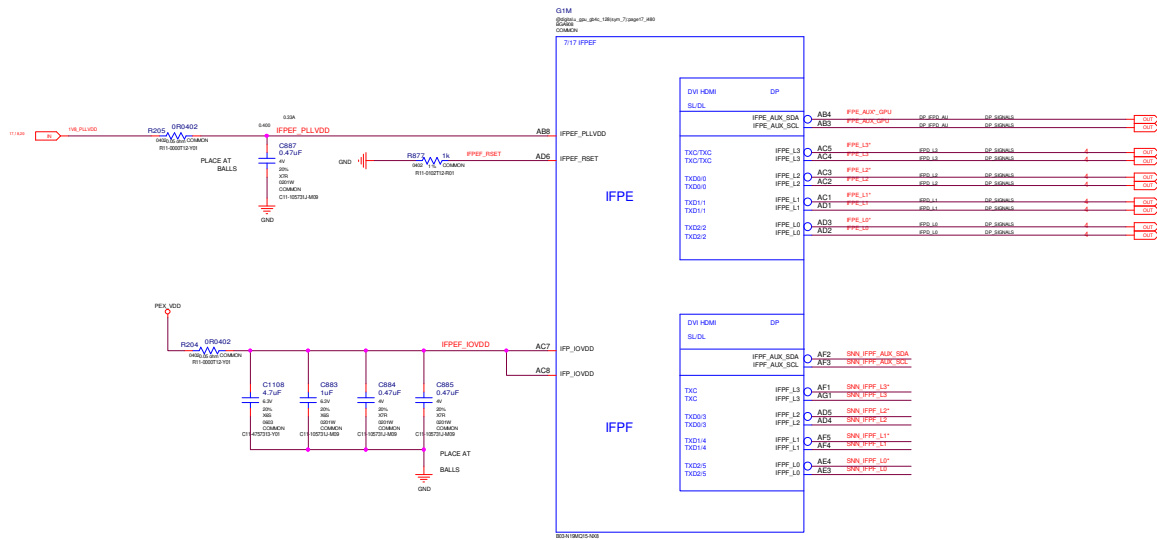


1V8_AON	0.1uF X7R	1uF X6S	4.7uF X6S
N19M-Q3	2	1	1

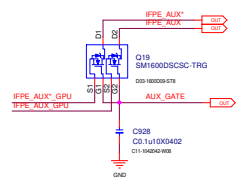


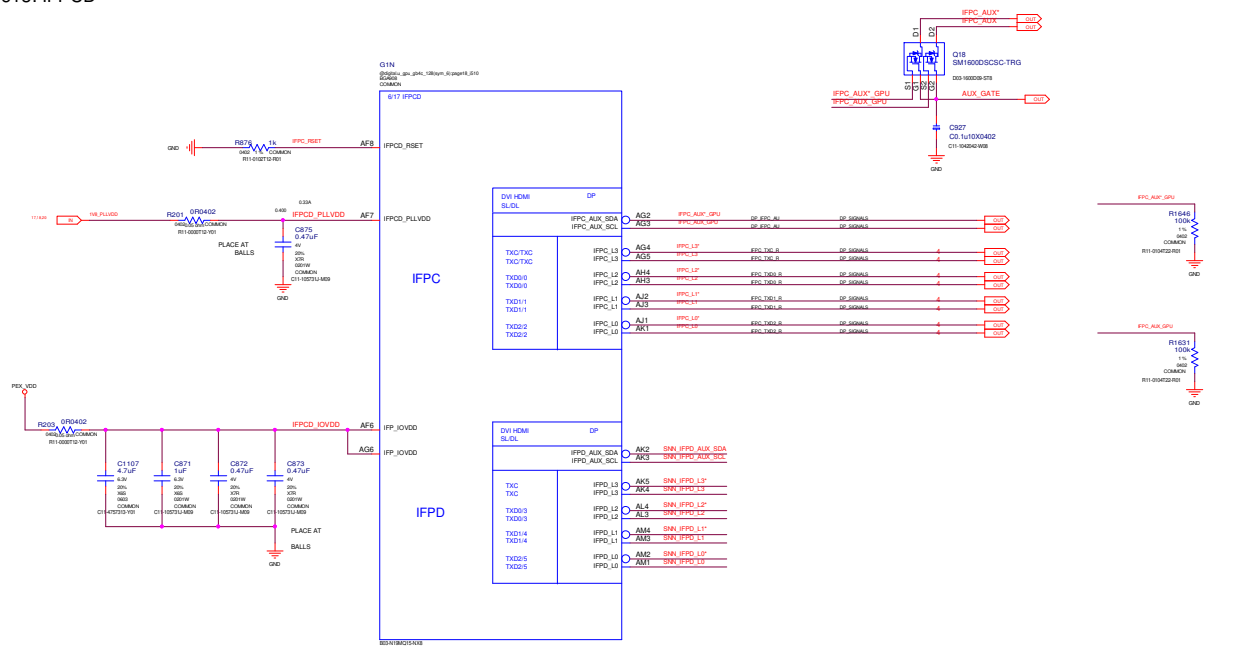


IFPx / AUX 90 ohm Differential
 TOP/BOTTOM 4 / 5 mil
 L3/L4/L6 4 / 6 mil

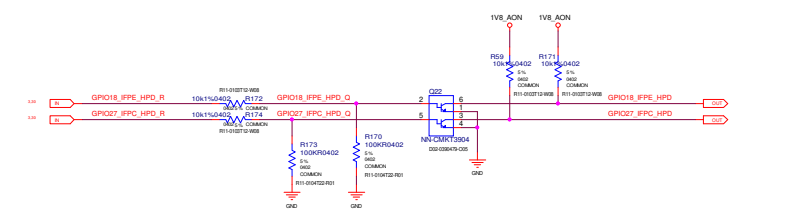


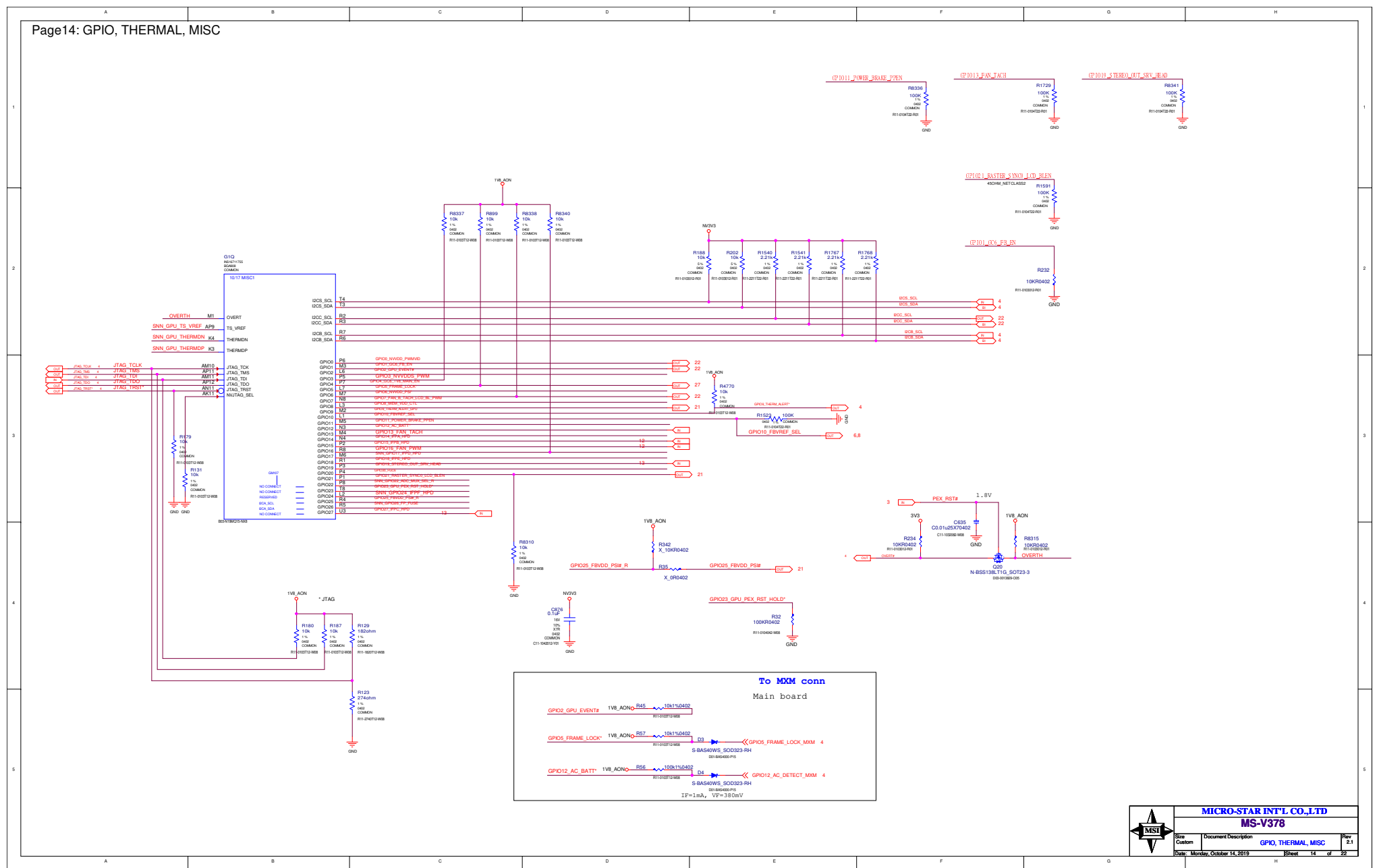
IFPx / AUX 90 ohm Differential
 TOP/BOTTOM 4 / 5 mil
 L3/L4/L6 4 / 6 mil





IFPx / AUX 90 ohm Differential
 TOP/BOTTOM 4 / 5 mil
 L3/L4/L6 4 / 6 mil

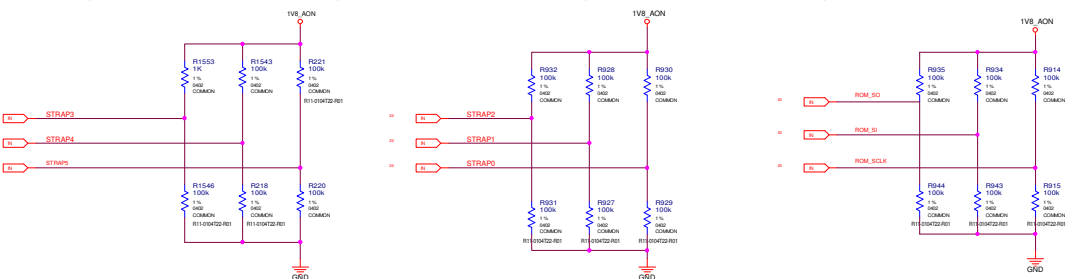




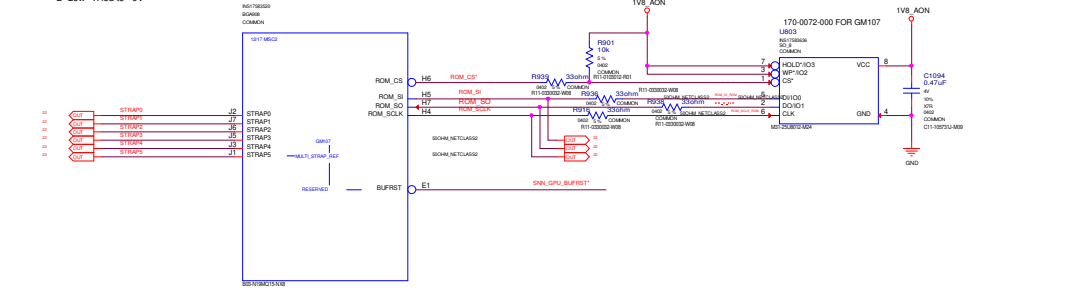
Page15: Straps,ROM, XTAL

STRAP2	STRAP1	STRAP0	RAMCF[4:0]	
L	L	L	0000	SAMSUNG 256x32
L	L	H	0001	MICRON-F 256x32 8G
L	H	L	0010	HYNX-M 256x32 8G
L	H	H	0011	
H	H	L	0110	HYNX-A 128Mx32 4G
H	H	H	0111	SAMSUNG-E 128Mx32 4G
L	L	M	1000	HYNX-B 128x32 4G
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	0	1
L	L	M	1	0	0	0
L	L	L	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	1
L	L	L	0	0	0	0

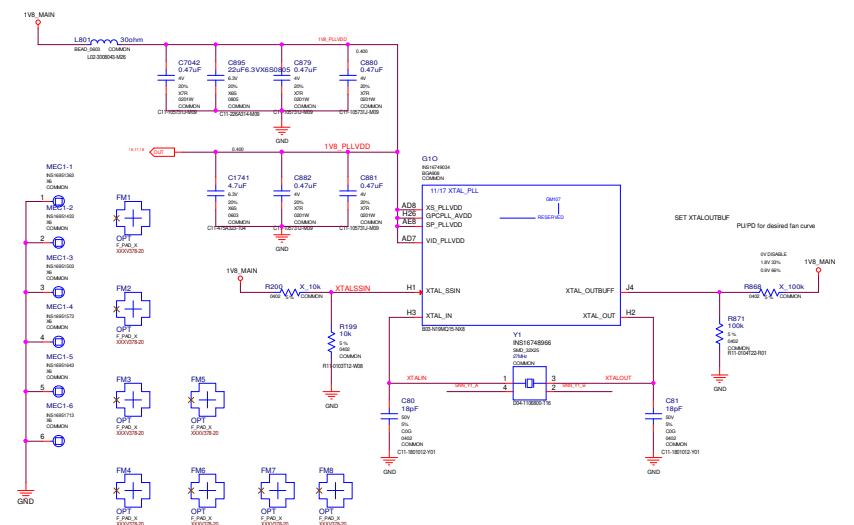



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE

0000	5.0k Ω GND	1000	5.0k Ω VCC
0001	10k Ω GND	1001	10k Ω VCC
0010	15k Ω GND	1010	15k Ω VCC
0011	20k Ω GND	1011	20k Ω VCC
0100	30k Ω GND	1100	30k Ω VCC
0101	35k Ω GND	1101	35k Ω VCC
0110	40k Ω GND	1110	40k Ω VCC
0111	45k Ω GND	1111	45k Ω VCC



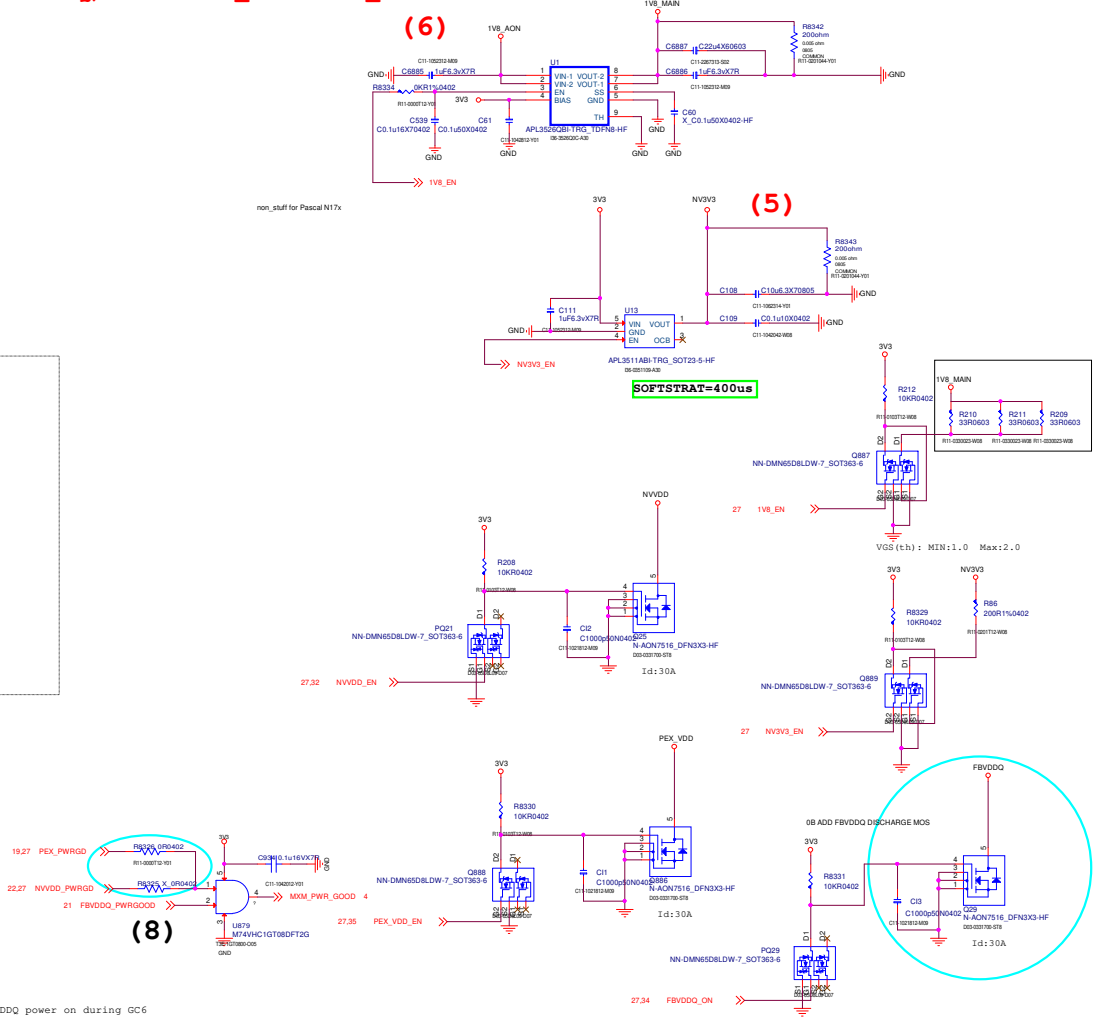
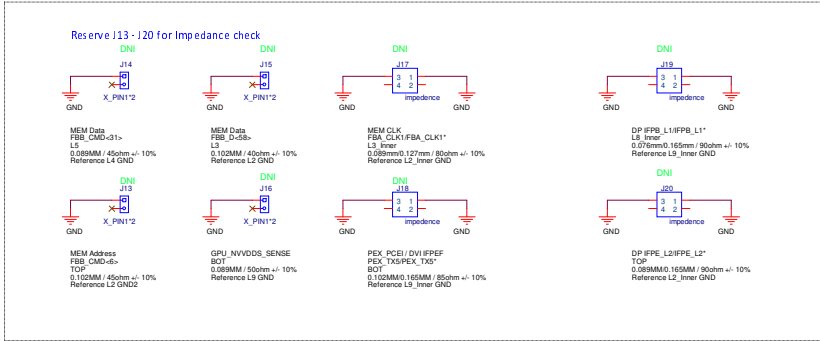


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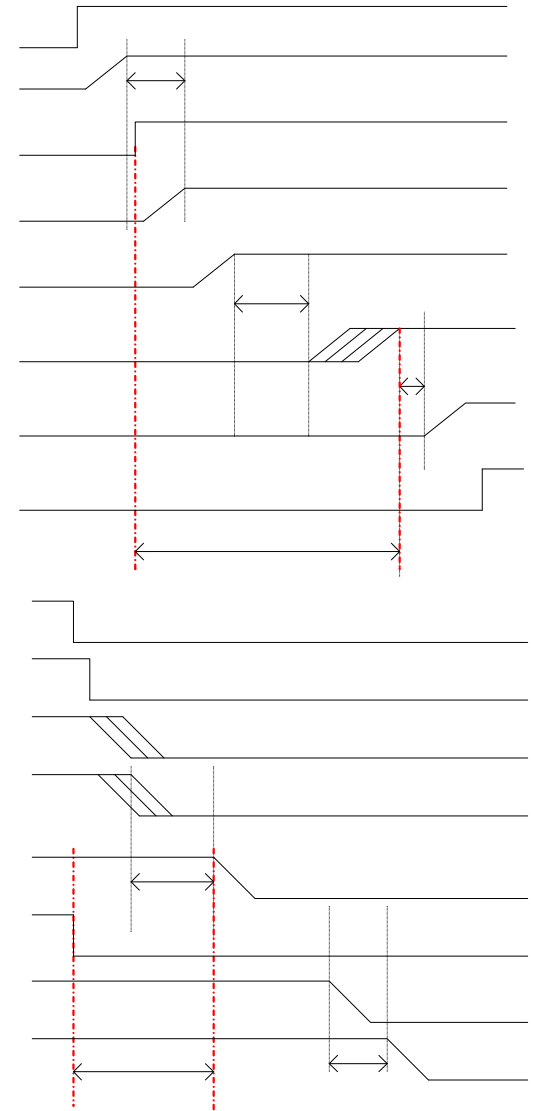
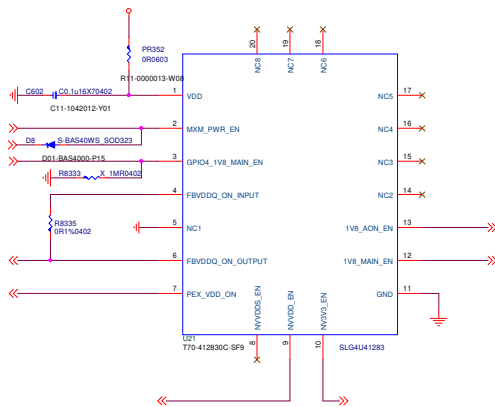
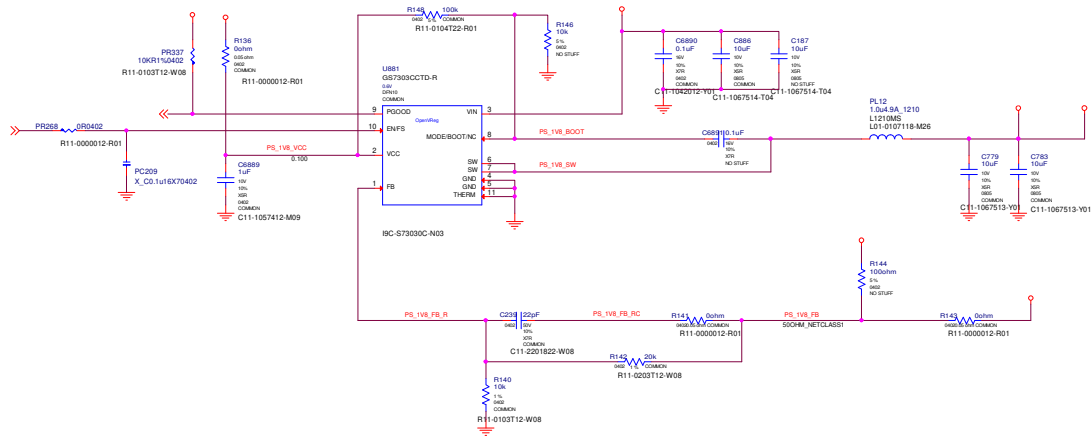
N17x POWER ON= 1V8_AON->1V8_MAIN->NVVDD->PEX_VDD->FBVDDQ->DGPU_PWRGD

N17x POWER OFF= PEX_VDD->FBVDDQ/NVVDD->1V8_MAIN->1V8_AON

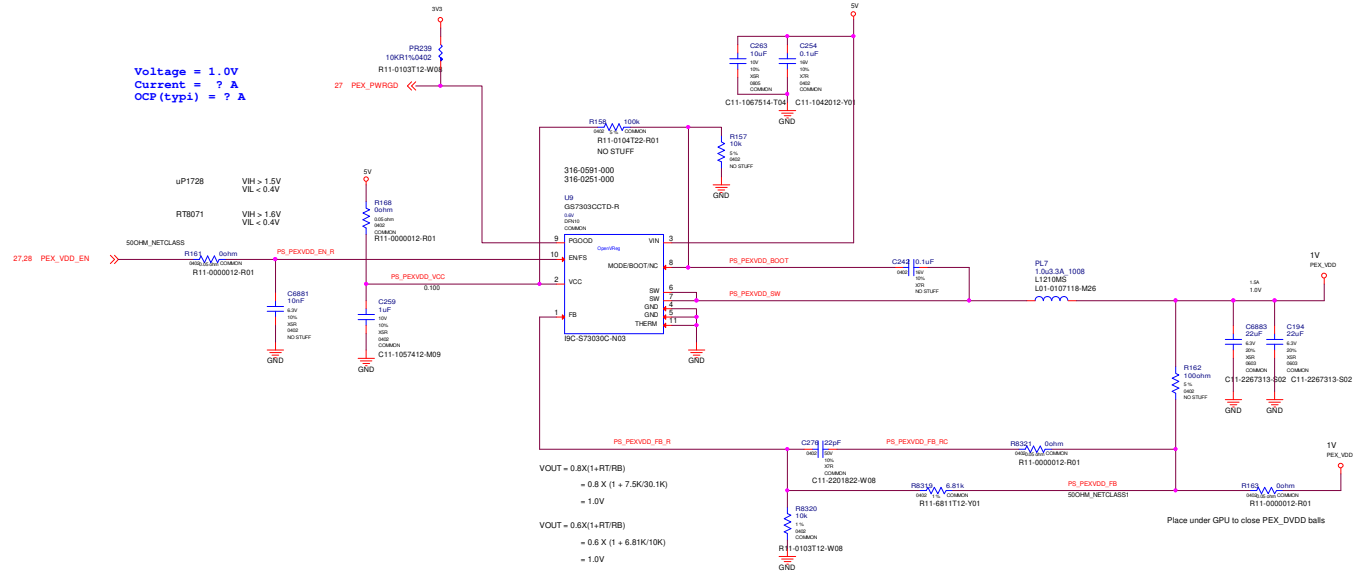


GPI01_GC6FBEN: it is high for keeping FBVDDQ power on during GC6

OR GATE	M74VHC1G132DF2G	VCC=3V (V _{IH} Min=1.4 V; LH Max=0.53V)
AND GATE	M74VHC1G108DF2G	VCC=3V (V _{IH} Min=1.4 V; LH Max=0.53V)

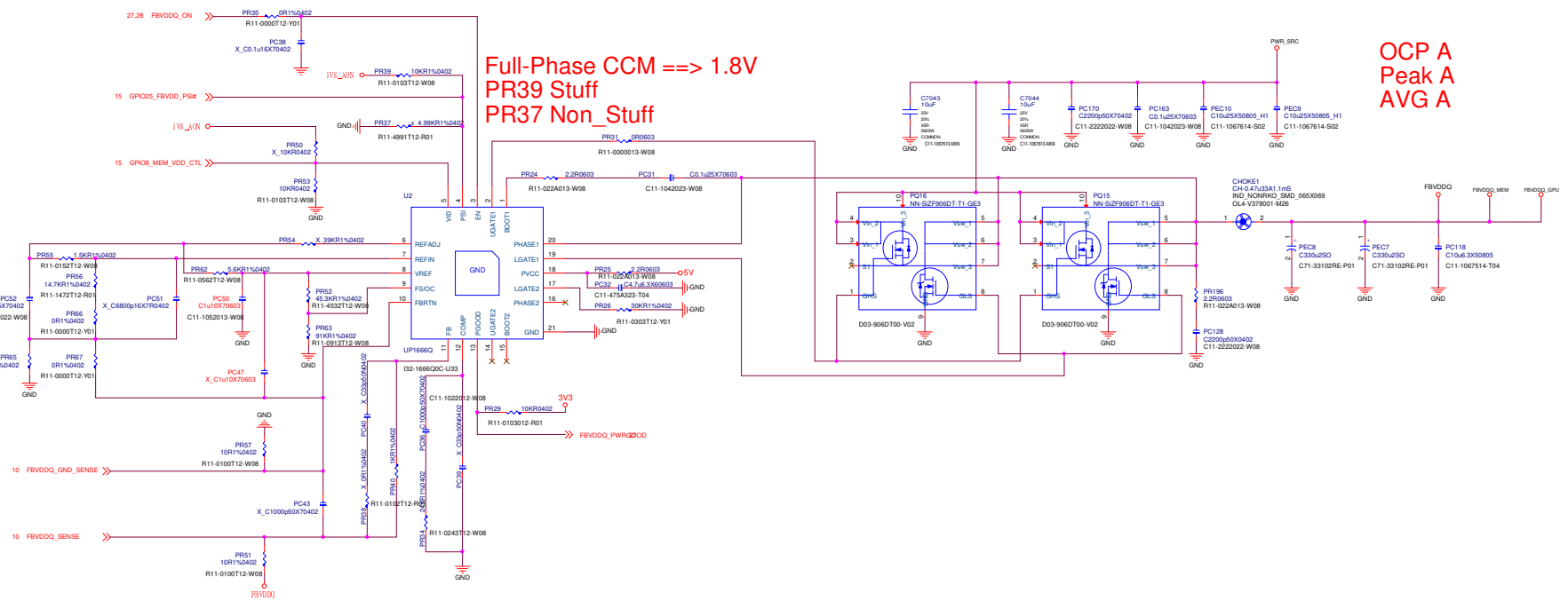


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Page 19: FBVDD CONTROLLER

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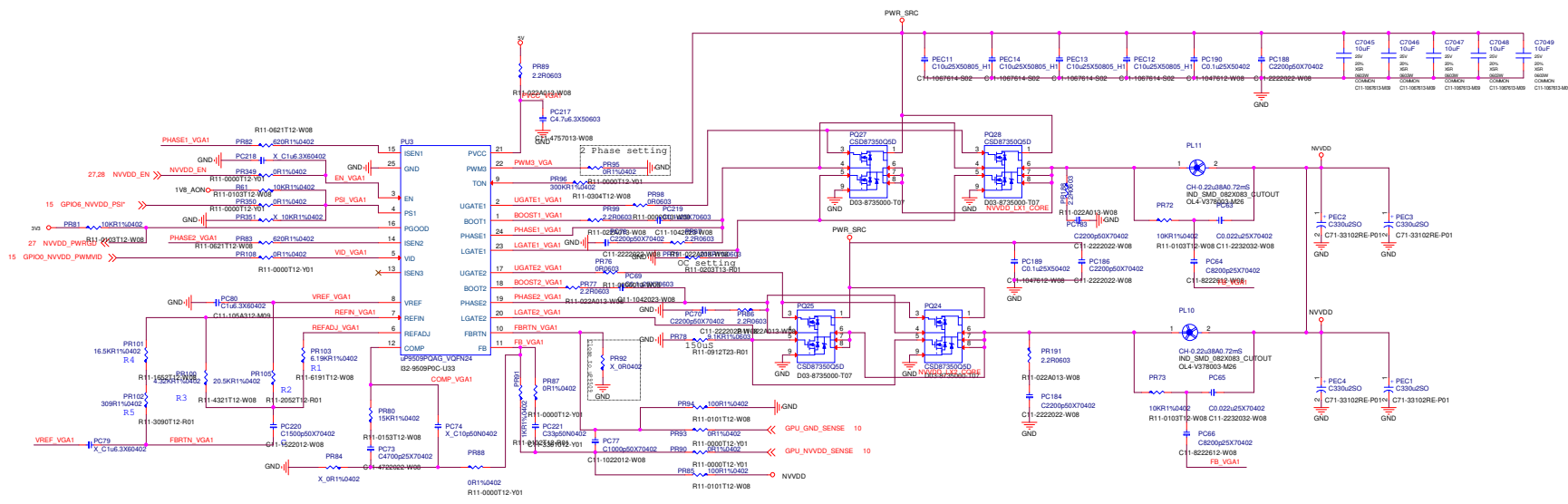


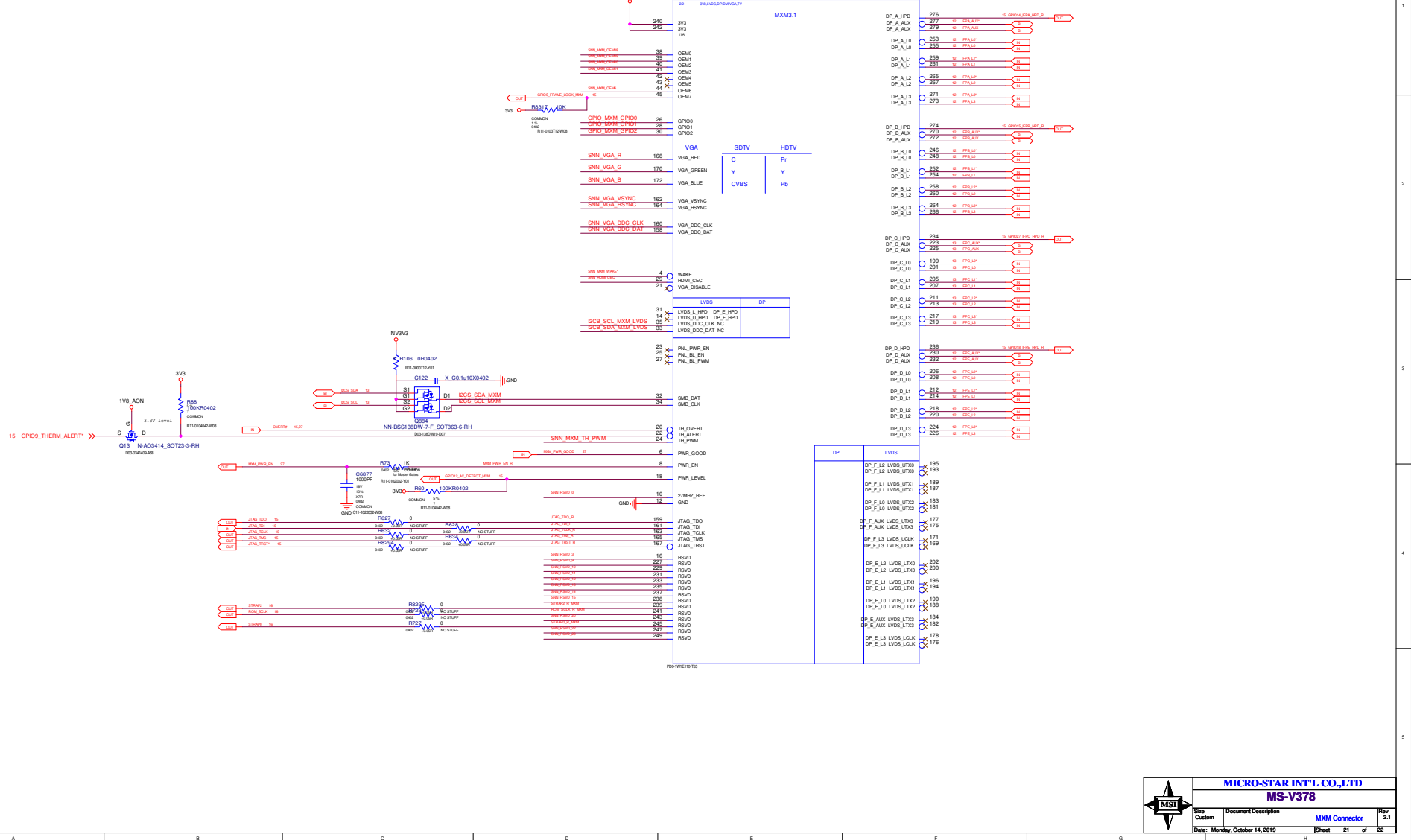
Copy from
MS-16R1-1.0

UP9509P

EDP-Peak 90A
EDP-Con 47A

VBoot:0.8V
Vmin:0.5V / Vmax:1.25V





Page23: GPIO Pin Define

Pin Name	N17P	N18P	N17P Functional Description	N17P Recommended Default Pull-up or Pull-down	N18P Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	NVVDD_PWM_VID	PWM Output to control NVVDD	0 to 1V8 PWM output	
GPIO1	GC6_FB_EN	GC6_FB_EN	FB Enable for GC6 2.1	0Ω, 10K pull-down	0Ω, 10K pull-down
GPIO2	GPU_EVENT#	GPU_EVENT#	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AGN	10K pull-up to 1V8_AGN
GPIO3	NVVDD_PWM	UNUSED	PWM output to control the NVVDD power supply	0 to 1V8 output	
GPIO4	1V8_MAIN_EN	1V8_MAIN_EN	GPU POWER Sequencing for GC6 2.1	0Ω, 10K pull-up to 1V8_AGN	0Ω, 10K pull-up to 1V8_AGN
GPIO5	FRM_LCK#	FRM_LCK#	Active low Frame Lock	0Ω, 10K pull-up to 1V8_AGN	0Ω, 10K pull-up to 1V8_AGN
GPIO6	NVVDD_PSI	NVVDD_PSI	Phase shedding	10K pull-up to 1V8_AGN	10K pull-up to 1V8_AGN
GPIO7	LCD_BL_PWM	LCD_BL_PWM	Panel Backlight PWM Brightness Control	100K pull-down	100K pull-down
GPIO8	MEM_VDD_CTL	MEM_VDD_CTL	Memory Voltage Control	pull-up/pull-down to set the FBVDD/G power-on voltage	pull-up/pull-down to set the FBVDD/G power-on voltage
GPIO9	THERM_ALERT	THERM_ALERT	Active Low Thermal Alert	0Ω, 10K pull-up to 1V8_AGN	0Ω, 10K pull-up to 1V8_AGN
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL	Memory VREF Control	100K pull-down	100K pull-down
GPIO11	LCD_VCC	LCD_VCC	Panel Power Enable	100K pull-down	100K pull-down
GPIO12	PWR_LEVEL	PWR_LEVEL	AC power detect or power supply overdraw input	100K pull-up to 1V8_AGN	10K pull-up to 1V8_AGN
GPIO13	LCD_BLEN	UNUSED	Panel Backlight Enable	100K pull-down	
GPIO14	HPD_A	HPD_A	Hot Plug Detect for IFPA		10K pull-up to 1V8_AGN
GPIO15	HPD_B	HPD_B	Hot Plug Detect for IFPB		10K pull-up to 1V8_AGN
GPIO16	SYS_FEX_RST_MON#	UNUSED	System side PCIe reset monitor	10K pull-up to 1V8_AGN	1V8_AGN
GPIO17	HPD_D	HPD_D	Hot Plug Detect for IFPD		10K pull-up to 1V8_AGN
GPIO18	HPD_E	HPD_E	Hot Plug Detect for IFPE		10K pull-up to 1V8_AGN
GPIO19	3Dvision	UNUSED	3D Vision L/R signal	100K pull-down	1V8_AGN
GPIO20	GC5_MODE	NB_GC6			10K pull-down
GPIO21	UNUSED	LCD_BLEN			100K pull-down
GPIO22	UNUSED	ADC_MUX_SEL			2.2K pull-up See Circuit
GPIO23	GPU_PEX_RST_HOLD#	RESERVED	GPU PCIe self-reset control	0Ω, 10K pull-up to a gated 3V3	100K pull-down
GPIO24	HPD_F	UNUSED	Hot Plug Detect for IFPF		
GPIO25	UNUSED	FBVDD_PSI#			
GPIO26	UNUSED	FP_FUSE			10K pull-down
GPIO27	HPD_C	HPD_C	Hot Plug Detect for IFPC		10K pull-up to 1V8_AGN

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Size	Document Description	Rev	
Custom	GPIO Pin Define	2.1	
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