

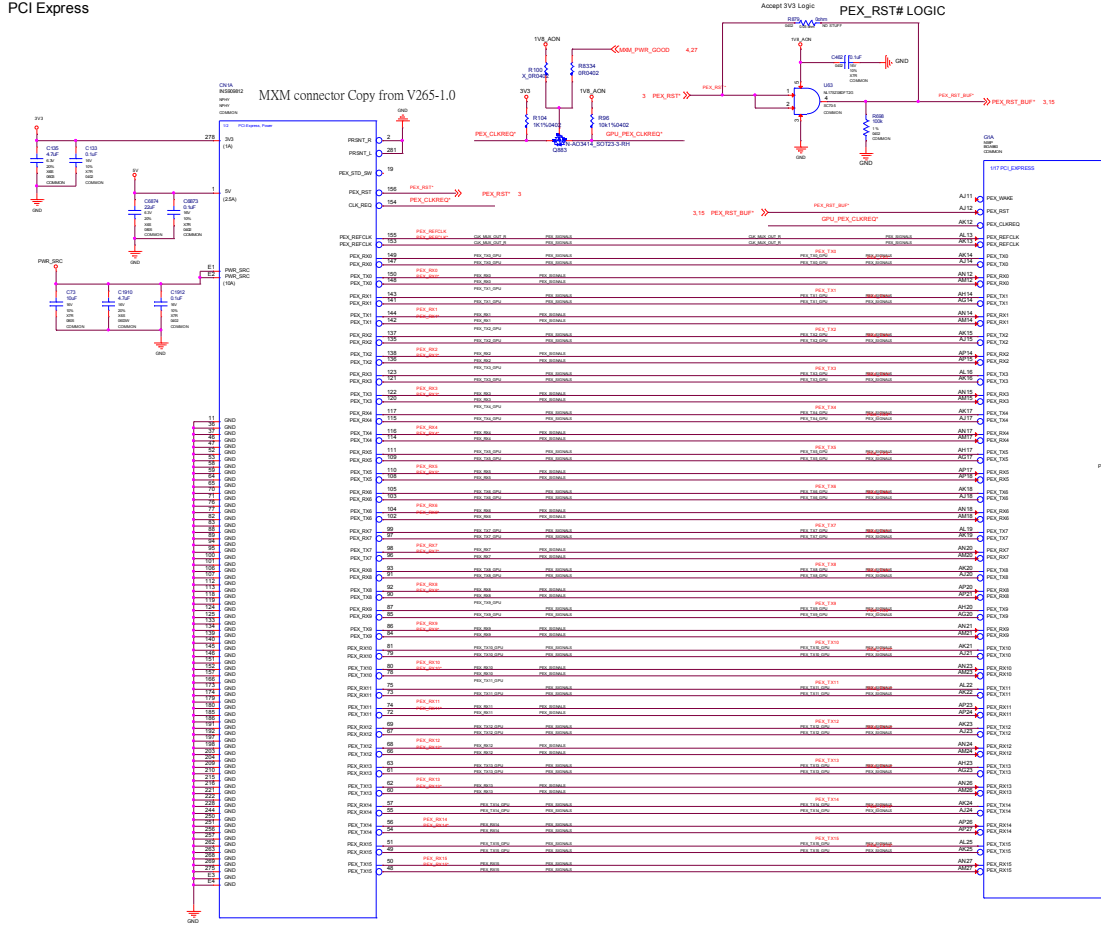
N18P GDDR5 X32 128BITS  
PCIE AND MODULAR DISPLAY

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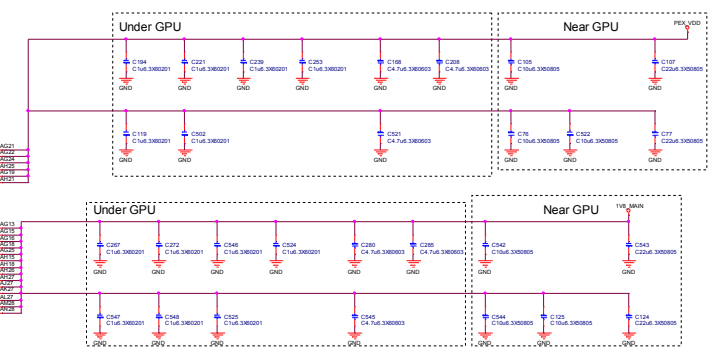
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	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>N19P</b>	
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PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X6R
N18P	6	3	3	2

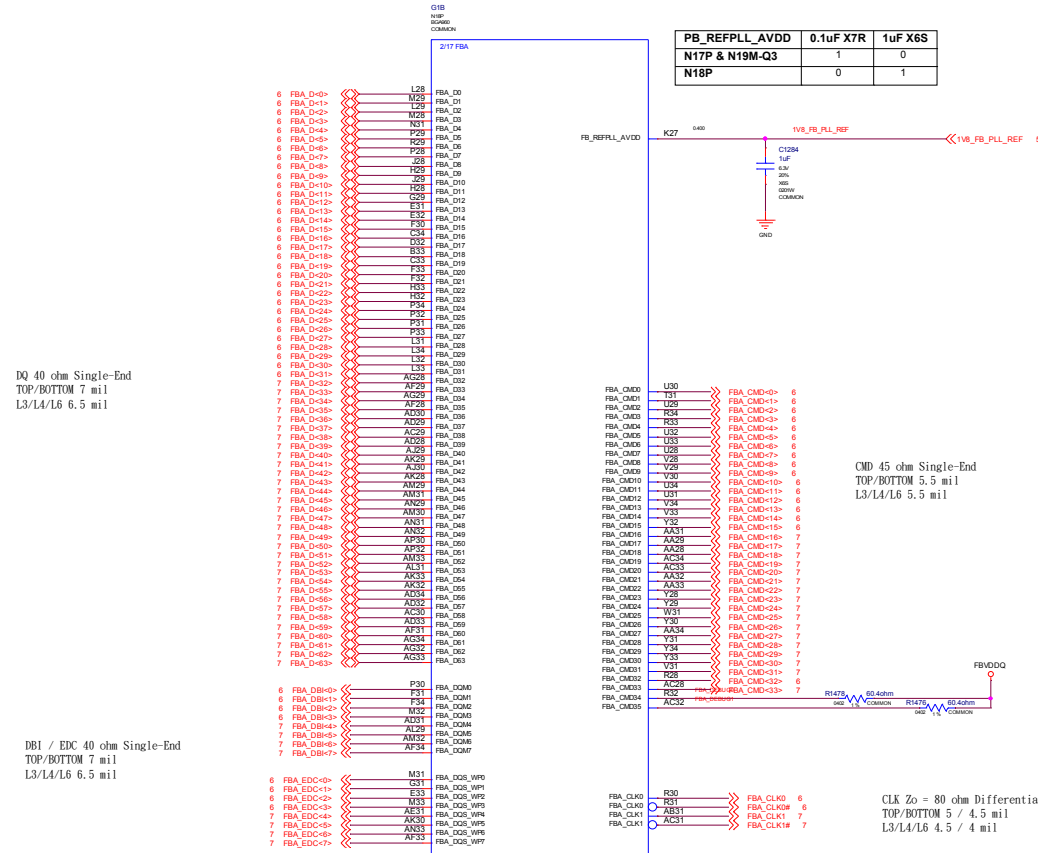


PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X6R
N18P	7	3	3	2

PEX_PLL_HVDD	0.1uF X7R	1uF X6S
N17P & N18M-Q3	1	0
N18P	0	1



MEMORY: GPU PARTITION A/B



DQ 40 ohm Single-End  
TOP/BOTTOM 7 mil  
L3/L4/L6 6.5 mil

DBI / EDC 40 ohm Single-End  
TOP/BOTTOM 7 mil  
L3/L4/L6 6.5 mil

PB_REFPLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

DQ 40 ohm Single-End  
TOP/BOTTOM 7 mil  
L3/L4/L6 6.5 mil

CMD 45 ohm Single-End  
TOP/BOTTOM 5.5 mil  
L3/L4/L6 5.5 mil

CLK Zo = 80 ohm Differential  
TOP/BOTTOM 5 / 4.5 mil  
L3/L4/L6 4.5 / 4 mil

WCK Zo = 80 ohm Differential  
TOP/BOTTOM 5 / 4.5 mil  
L3/L4/L6 4.5 / 4 mil

Under GPU  
C1991 1uF  
5.0V  
20%  
SLOW COMMON

PBA_PLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

PBx_PLL_AVDD	4.7uF X6S	22uF X6S
N17P & N19M-Q3	1	1
N18P	2	1

Under GPU  
C1991 1uF  
5.0V  
20%  
SLOW COMMON

Under GPU  
C1991 1uF  
5.0V  
20%  
SLOW COMMON

Under GPU  
C1991 1uF  
5.0V  
20%  
SLOW COMMON

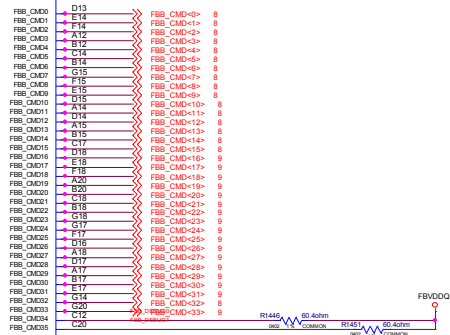
DBI / EDC 40 ohm Single-End  
TOP/BOTTOM 7 mil  
L3/L4/L6 6.5 mil

DBI / EDC 40 ohm Single-End  
TOP/BOTTOM 7 mil  
L3/L4/L6 6.5 mil

GD00E\_BGA170\_MFR COMMAND MAP

GD00	GD0
GD01	GD1
GD02	GD2
GD03	GD3
GD04	GD4
GD05	GD5
GD06	GD6
GD07	GD7
GD08	GD8
GD09	GD9
GD10	GD10
GD11	GD11
GD12	GD12
GD13	GD13
GD14	GD14
GD15	GD15
GD16	GD16
GD17	GD17
GD18	GD18
GD19	GD19
GD20	GD20
GD21	GD21
GD22	GD22
GD23	GD23
GD24	GD24
GD25	GD25
GD26	GD26
GD27	GD27
GD28	GD28
GD29	GD29

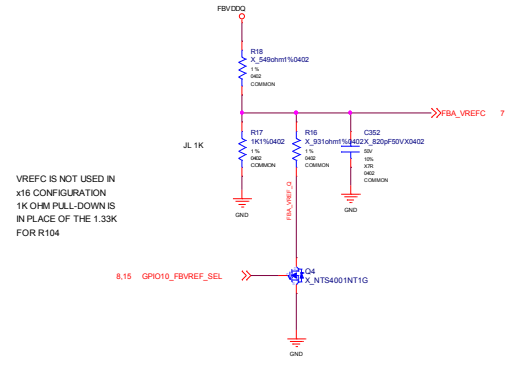
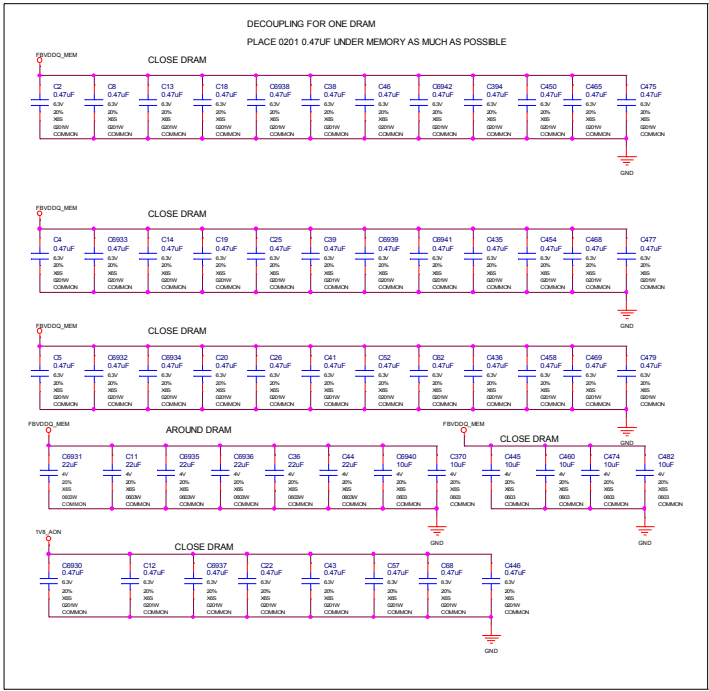
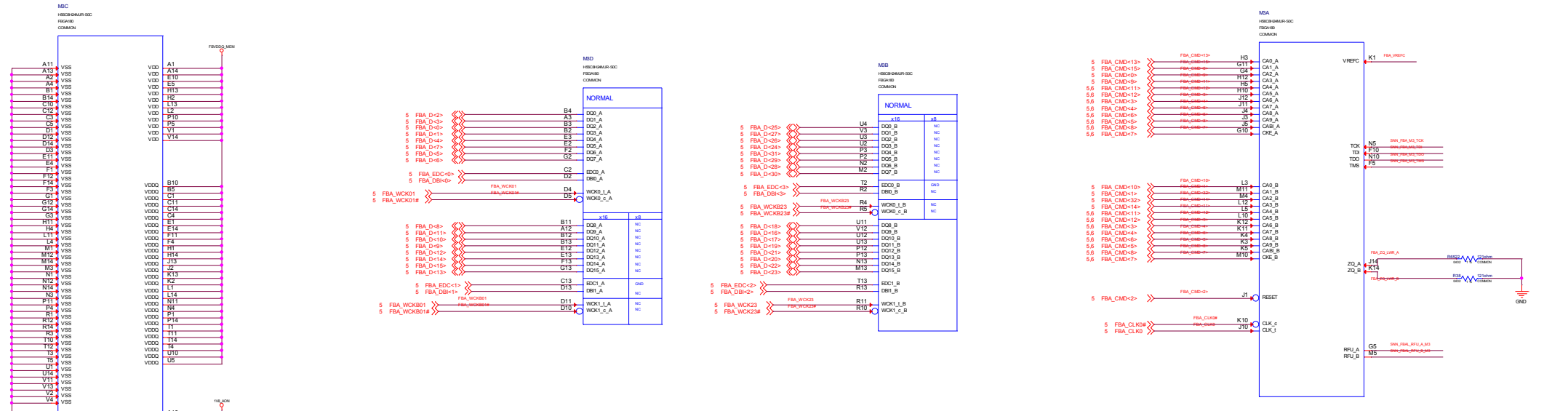
CMD 45 ohm Single-End  
TOP/BOTTOM 5.5 mil  
L3/L4/L6 5.5 mil

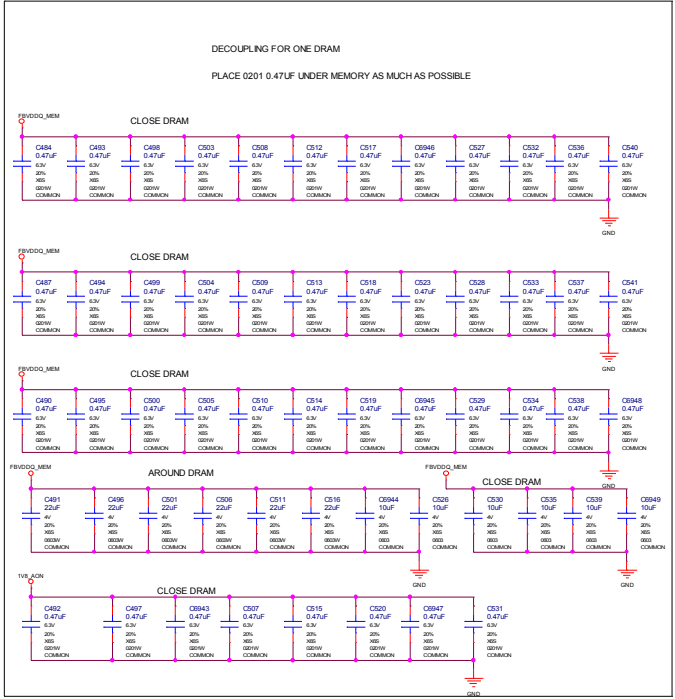
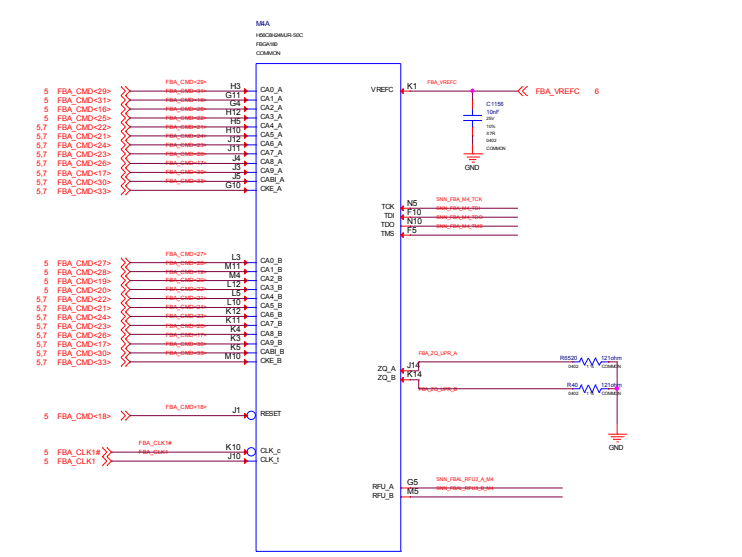
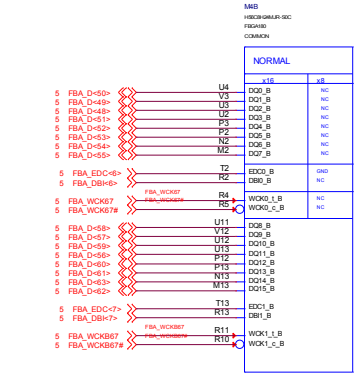
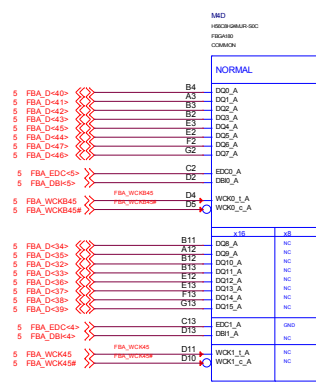
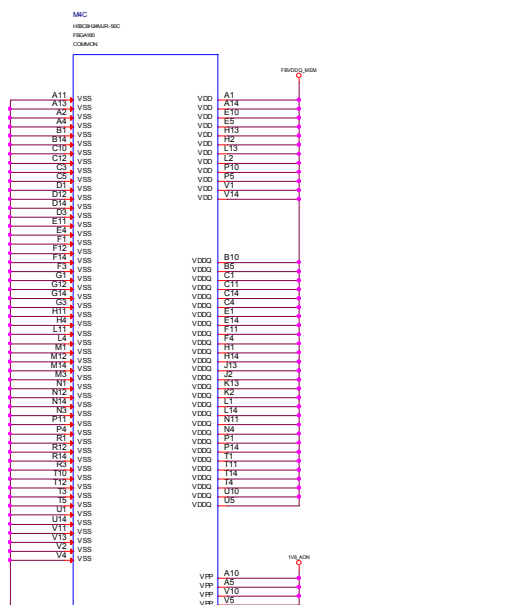


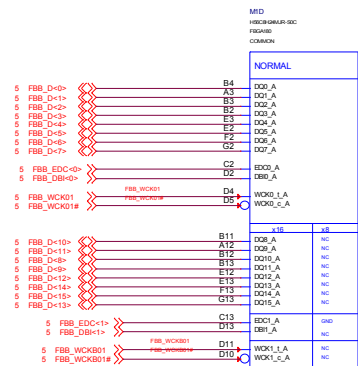
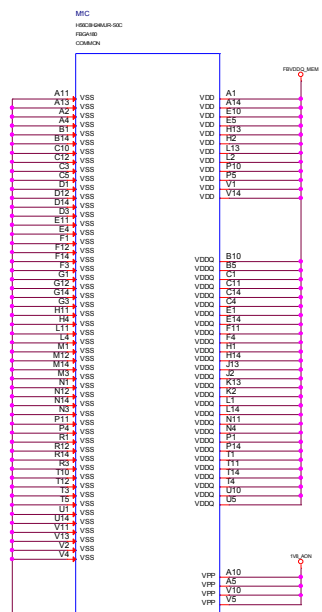
CLK Zo = 80 ohm Differential  
TOP/BOTTOM 5 / 4.5 mil  
L3/L4/L6 4.5 / 4 mil

WCK Zo = 80 ohm Differential  
TOP/BOTTOM 5 / 4.5 mil  
L3/L4/L6 4.5 / 4 mil

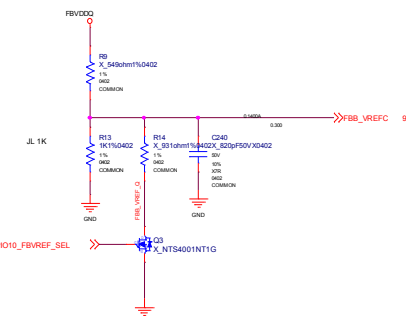
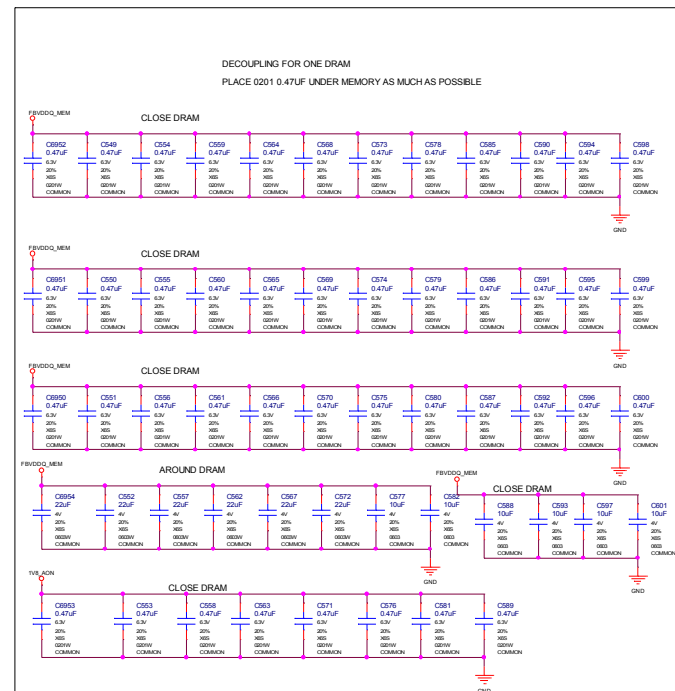
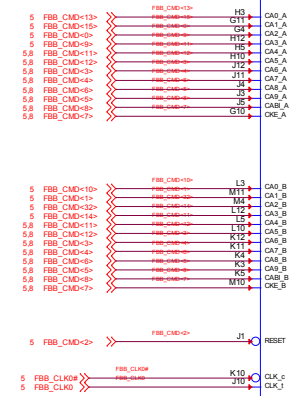
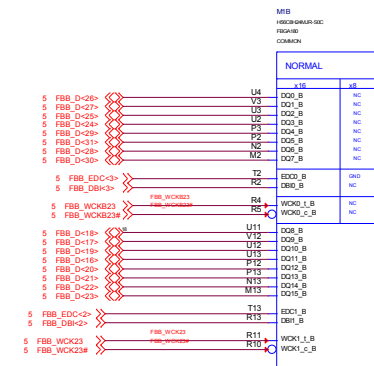






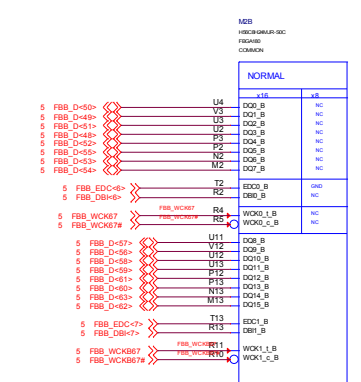
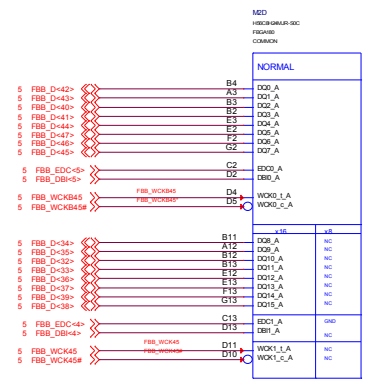
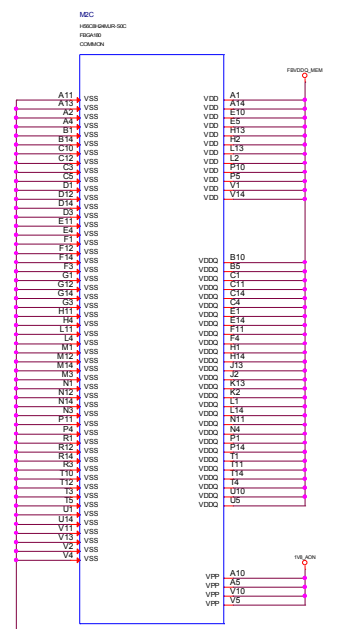


Place DRAM on TOP w/ R1 RFA1 A1y away from GPU

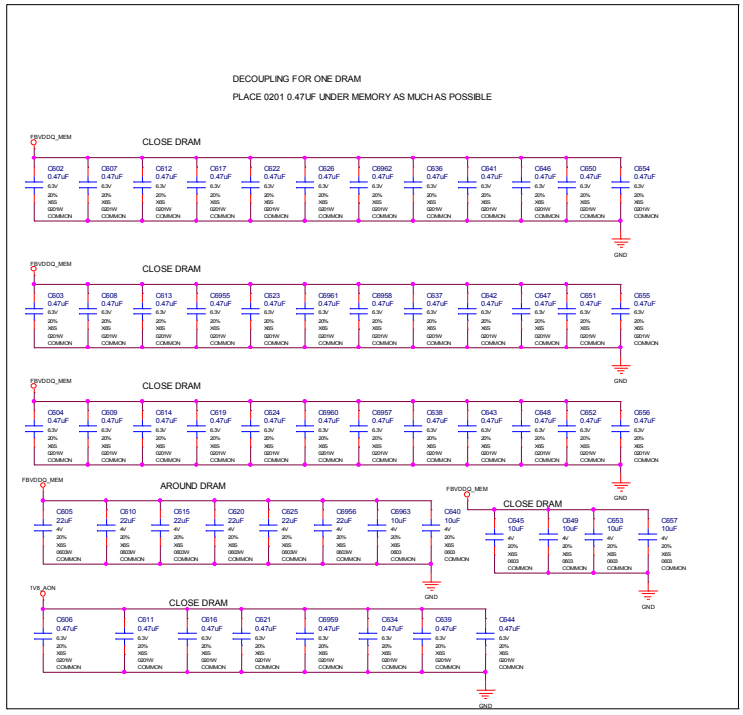
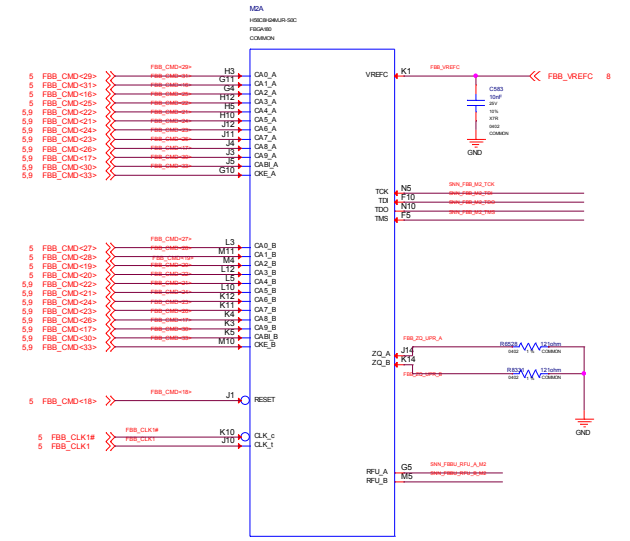


VREFC IS NOT USED IN X16 CONFIGURATION. 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R104.

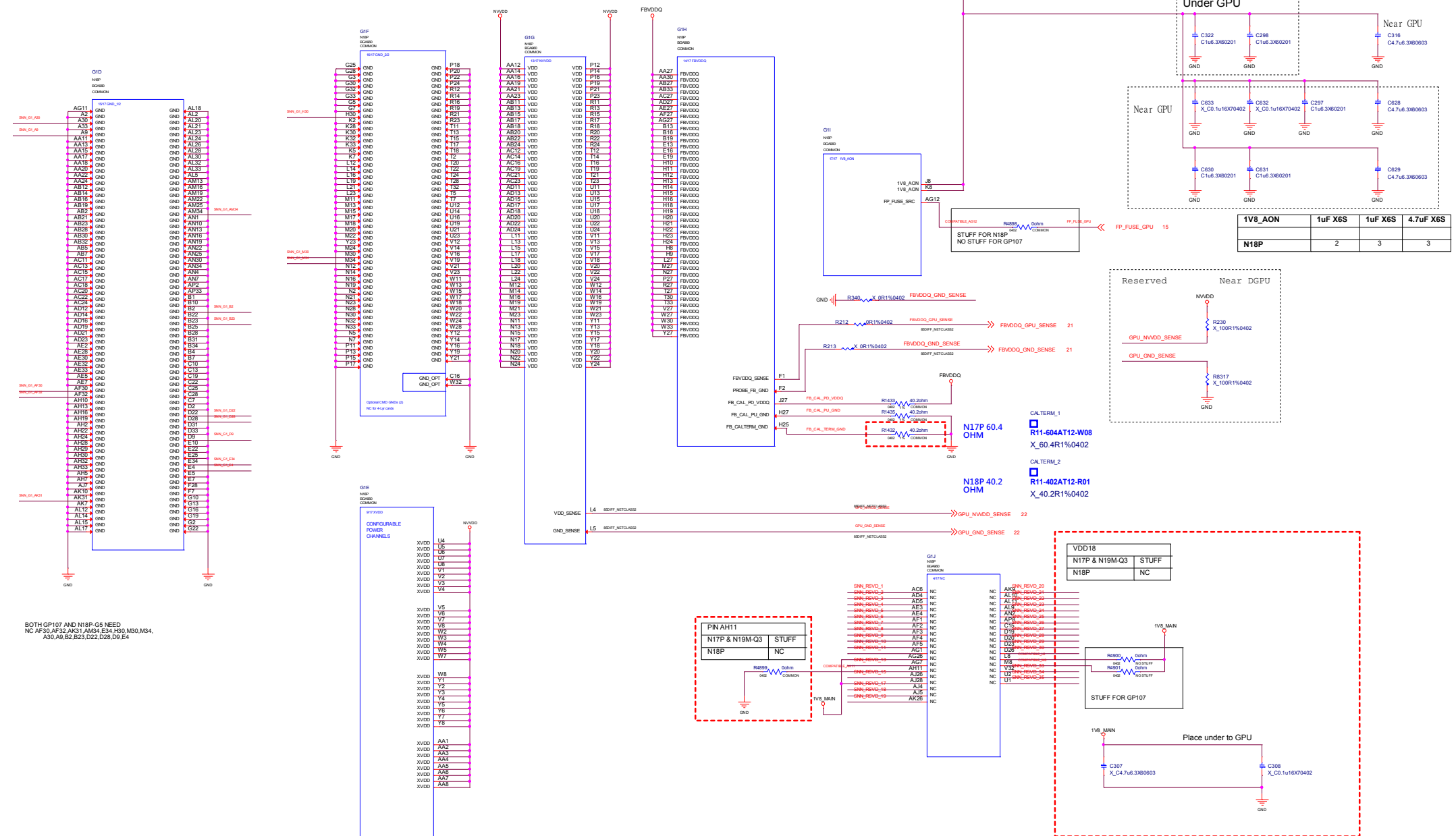




Place DRAM on TOP with FN A1 Toward GPU



GPU PWR. GND and NCs



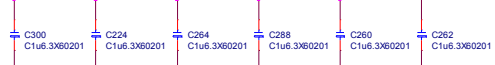
BOTH GP107 AND N18P-G5 NEED  
NC: AF30, AF32, AK31, AM34, EM30, M00, M34,  
A30, A9, B2, B23, D22, D28, D9, E4

# GPU DECOUPLING

NVDD

NVDD

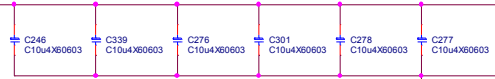
Place under to GPU



Place under to GPU



Place under to GPU



Place under to GPU



Place under to GPU



Place under to GPU



Place near to GPU



Place near to GPU



Place near to GPU

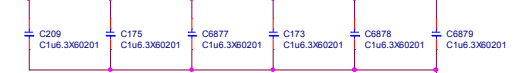


NVDD	1uF X6S	10uF X6S	22uF X6S
	0201	0603	0805
N19P-Q3/Q1	13	34	15

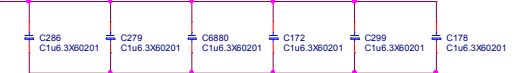
FBVDDQ

FBVDDQ

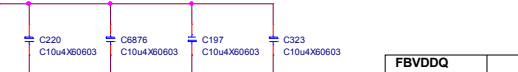
Place under to GPU



Place under to GPU



Place under to GPU



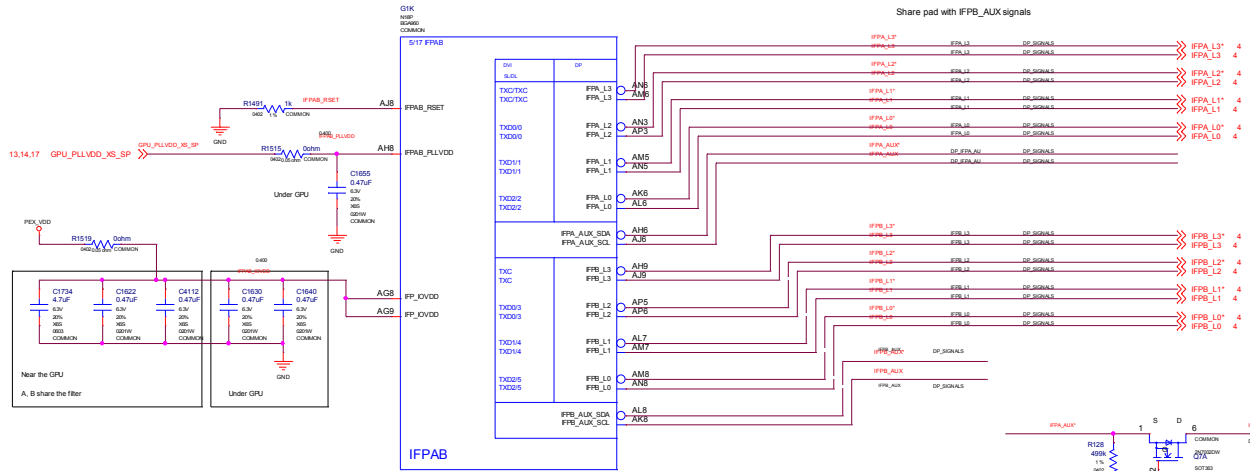
FBVDDQ	1uF X6S	10uF X6S	22uF X6S	10uF X6S
	0201	0603	0603	0603
N19P-Q3/Q1	12	4	5	2

Place near to GPU

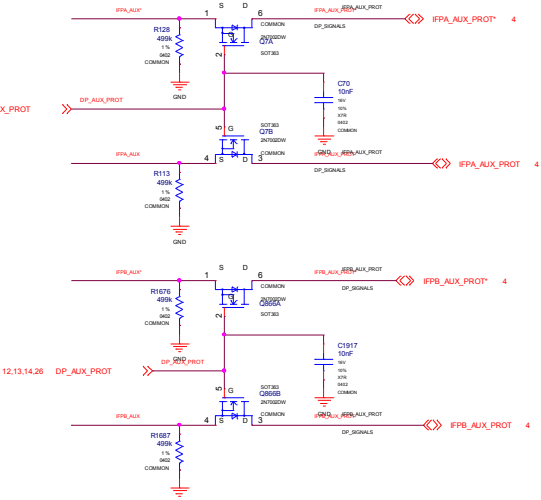
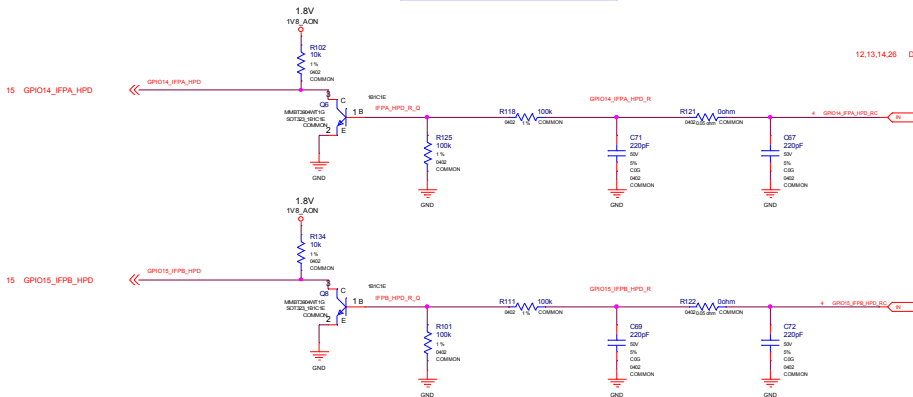


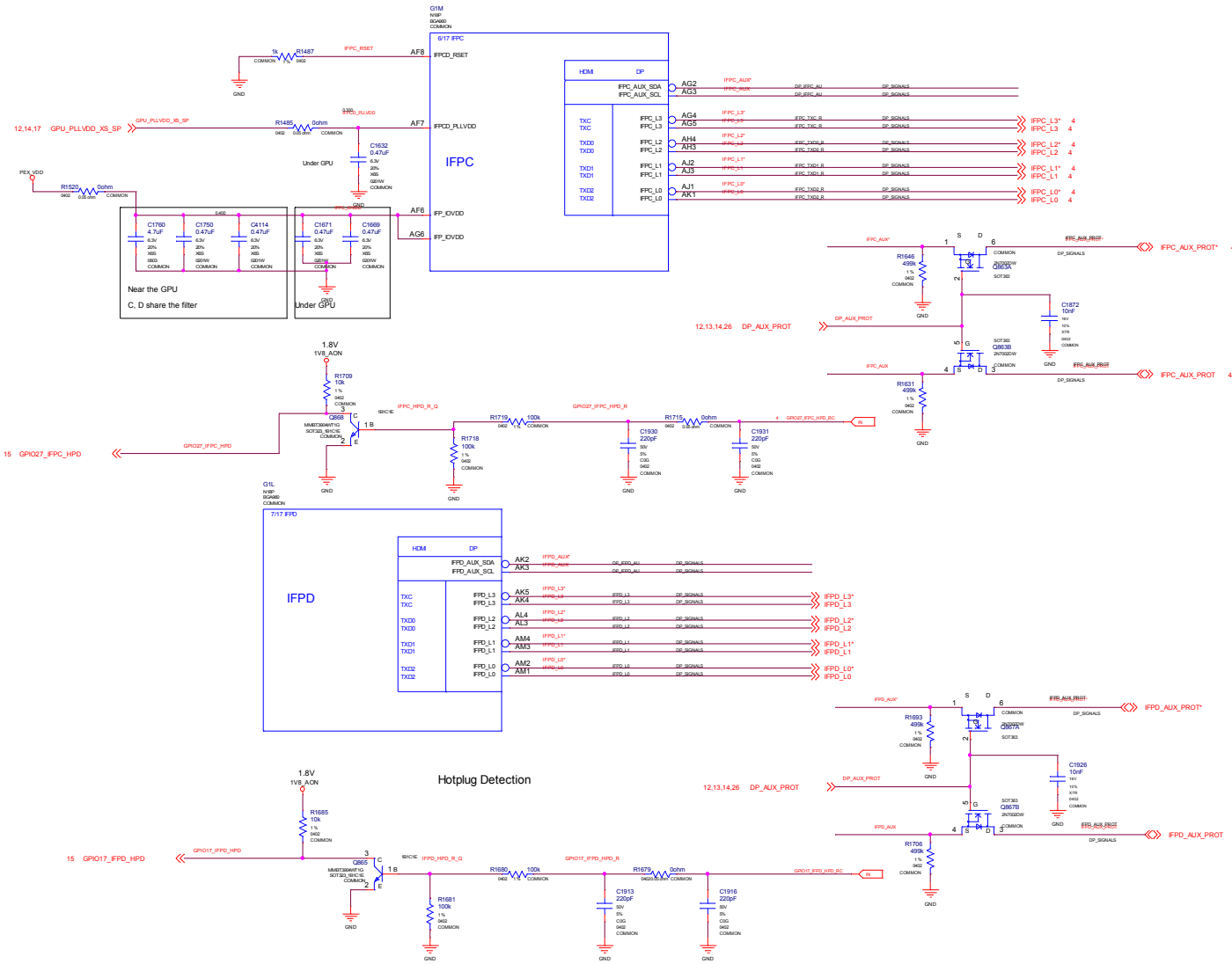
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N19P

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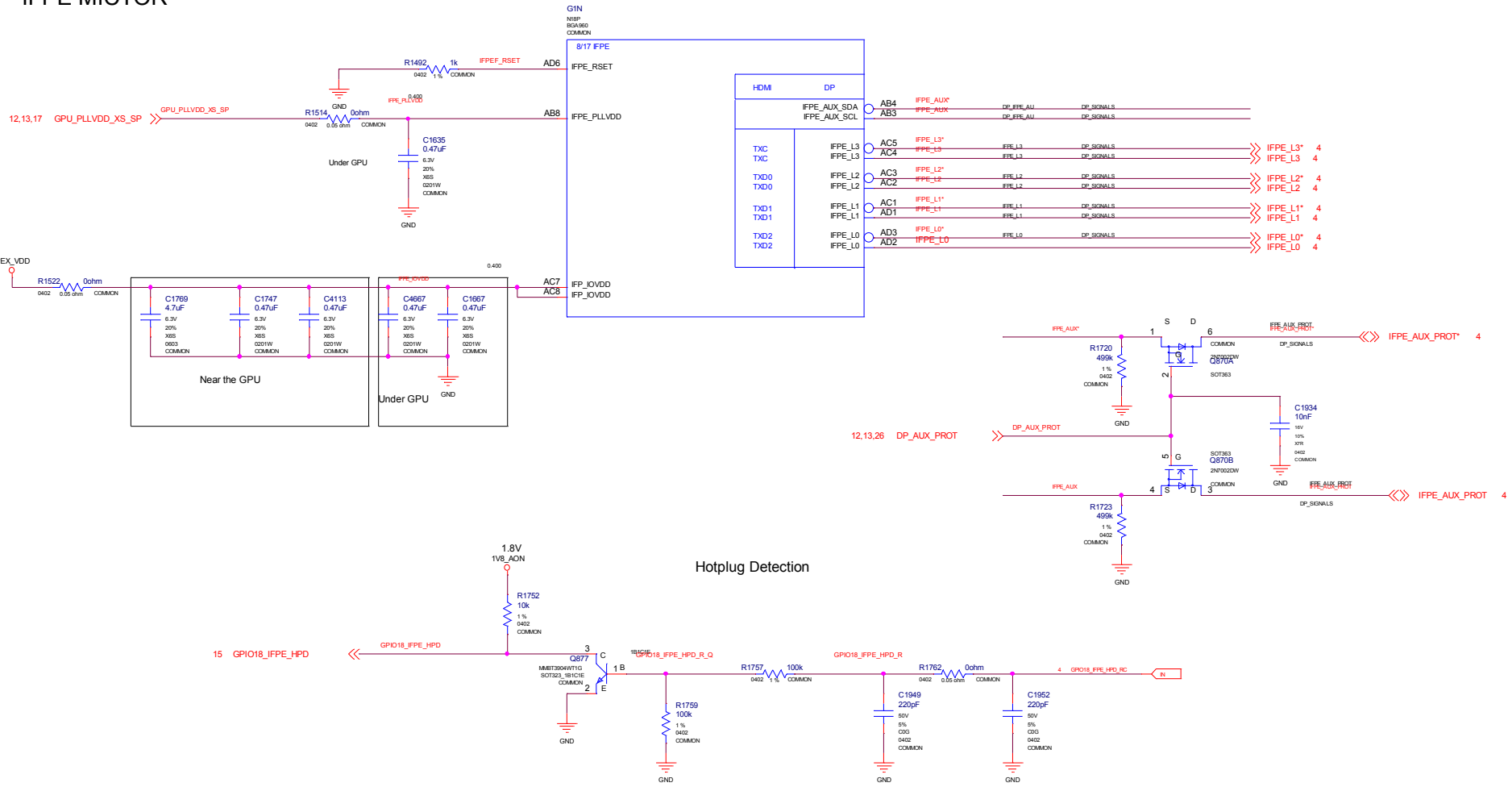


IFPx / AUX 90 ohm Differential  
 TOP/BOTTOM 4 / 5 mil  
 L3/L4/L6 4 / 6 mil

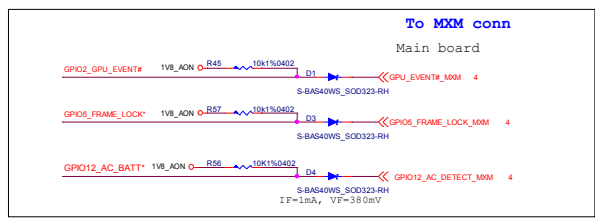
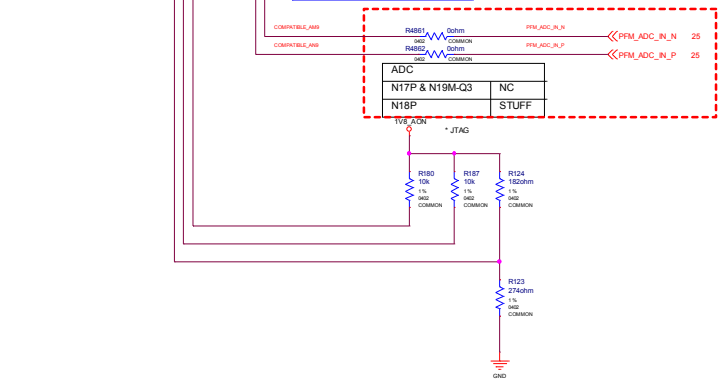
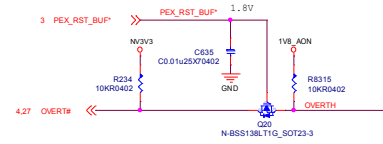
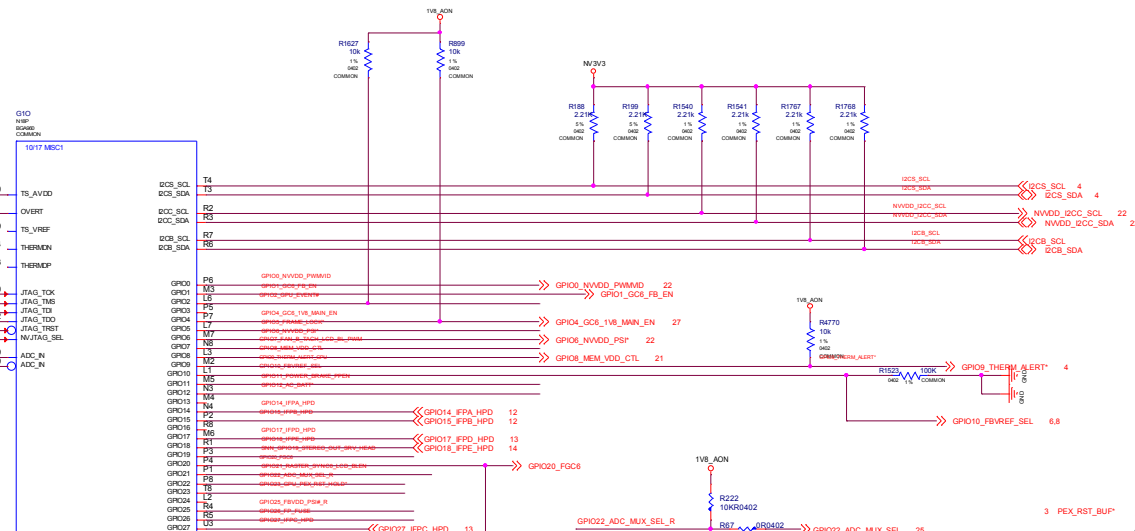
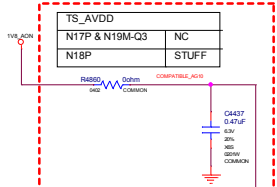
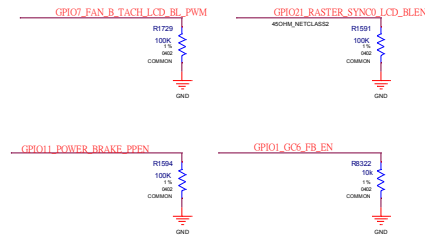
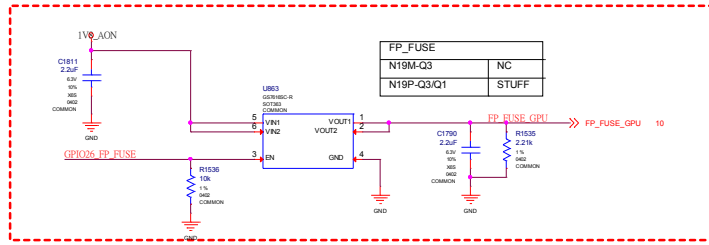




# IFPE MICTOR



<b>MICRO-STAR INT'L CO.,LTD</b>			
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# MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

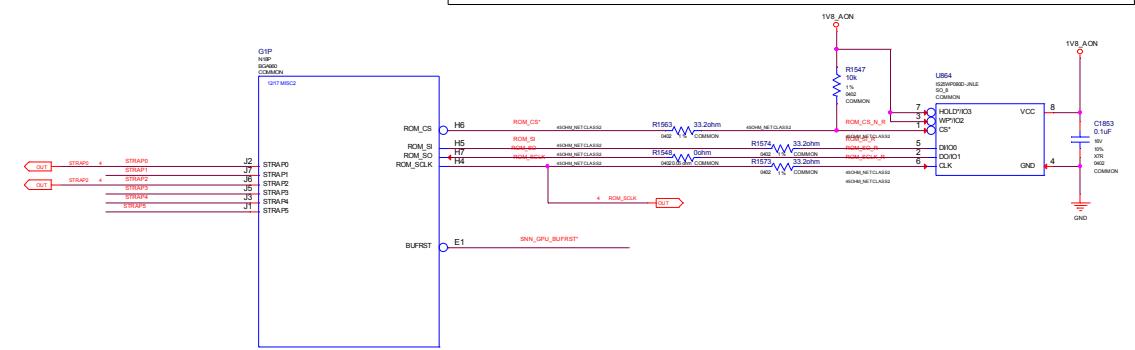
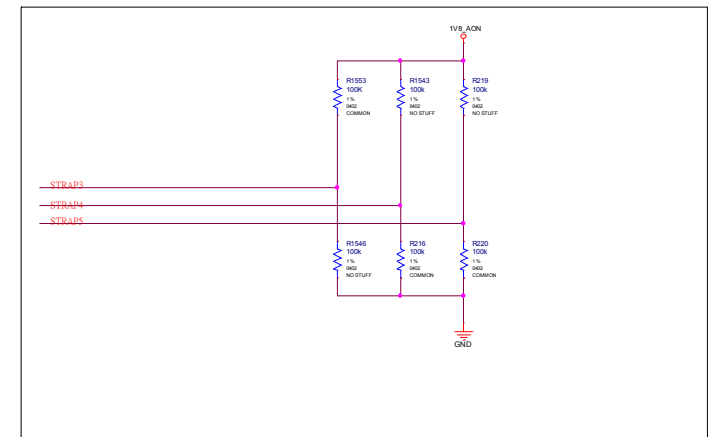
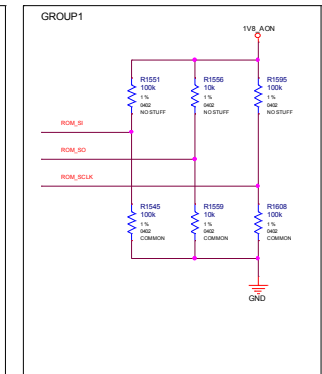
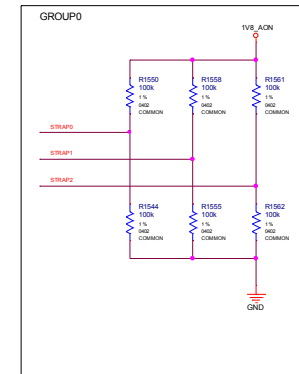
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1.ENABLE 0.DISABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	L	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

DEFAULT

- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE ENABLE
- 0:VGA\_DEVICE DISABLE

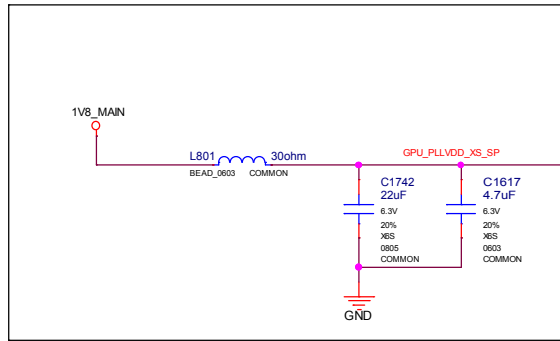
Default



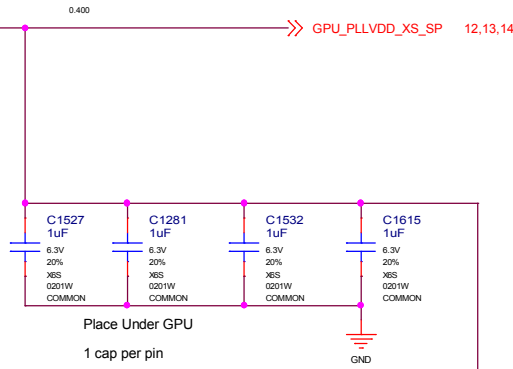


# MISC2: XTAL. PLL

XSN_PLLVDD	0.1uF X7R	1uF X6S	4.7uF X6S	22uF X6S
GPCPLL_AVDD				
SP_PLLVDD				
VID_PLLVDD				
N17P & N19M-Q3	4	0	1	1
N18P	0	4	1	1



Place near GPU



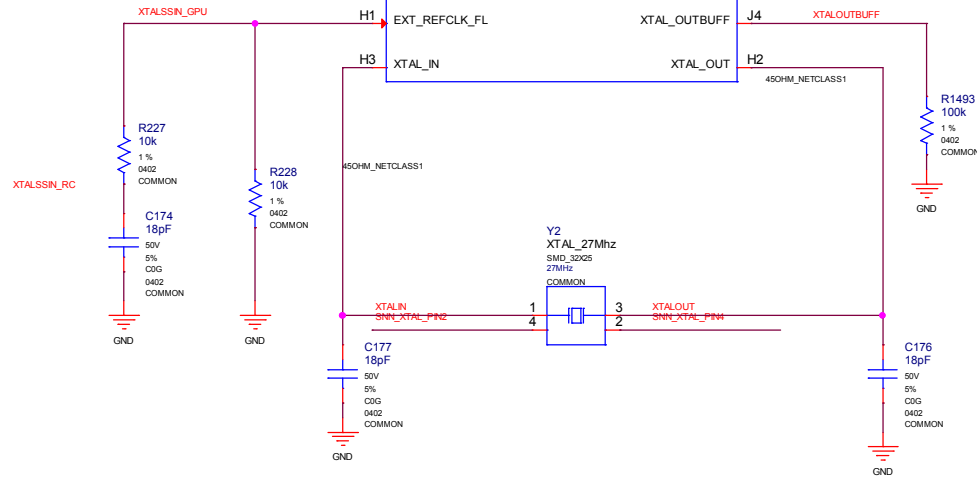
Place Under GPU  
1 cap per pin

SmartFan Strap Table

Voltage	Inverted SmartFan PWM %
0V	GPIO DISABLED
0.9V	33% PWM
1.8V	66% PWM

## 12.2.2.5 XTALOUTBUFF Circuit Node

For mobile graphics circuit designs (or other designs wherein the graphics circuit does not directly and fully control its own cooling fan), the XTALOUTBUFF circuit node must be tied to GND through 100KΩ resistors.

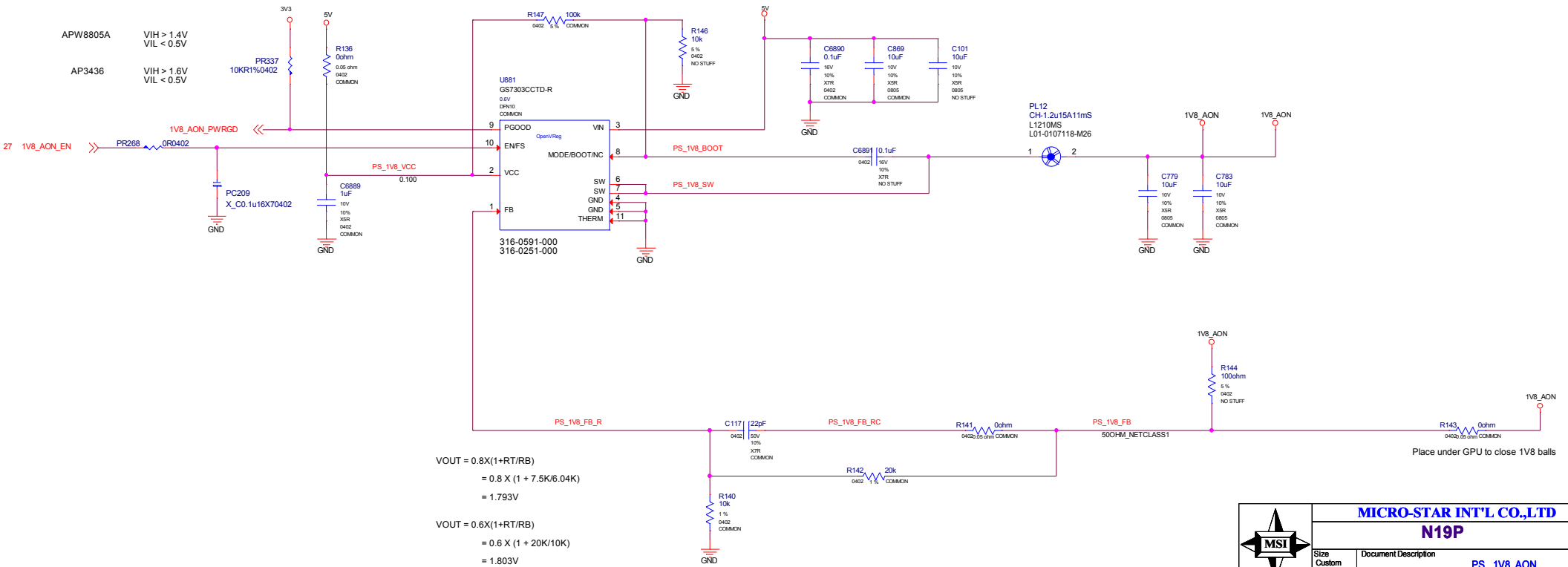


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PS: 1V8\_AON

Voltage = 1.8V  
 Current = ? A  
 OCP(typi) = ? A

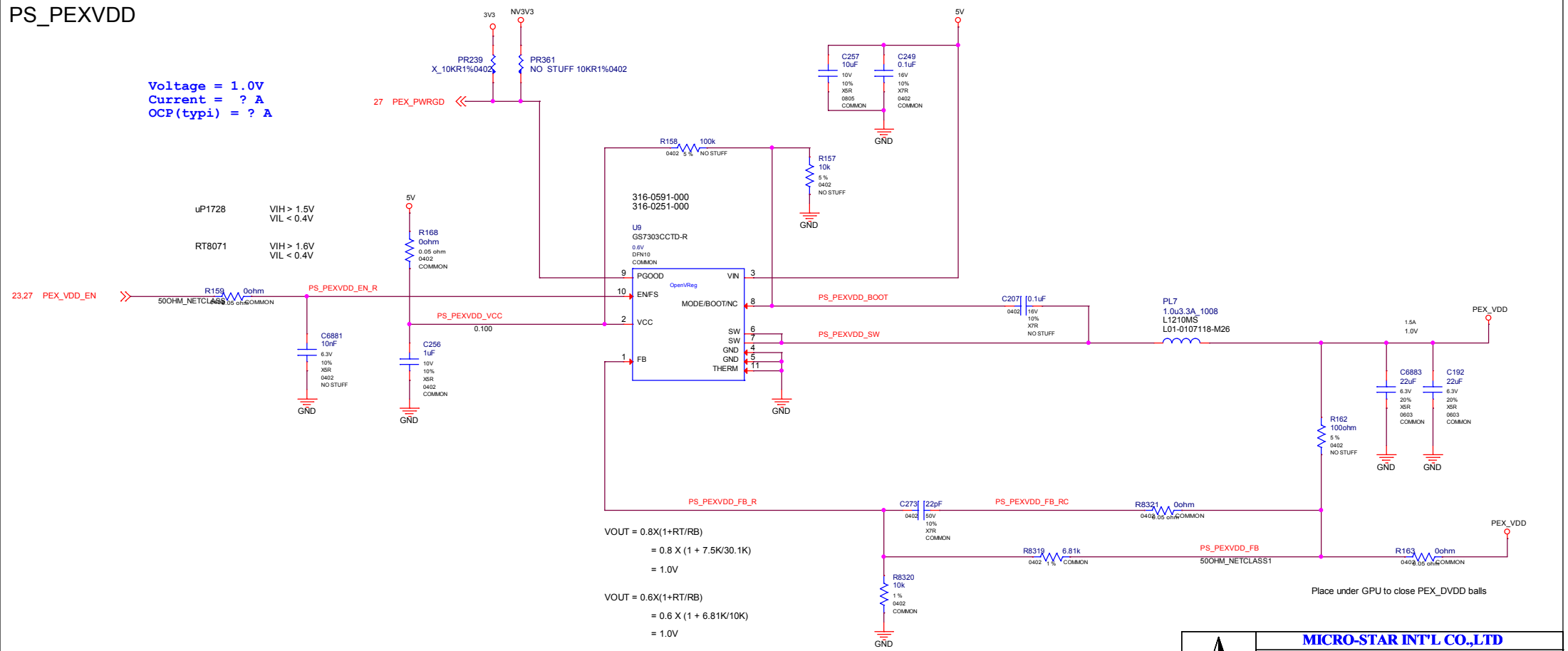
# 1V8\_AON



<b>MICRO-STAR INT'L CO.,LTD</b>		
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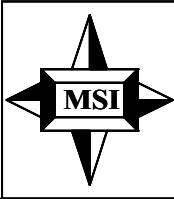
# PS\_PEXVDD

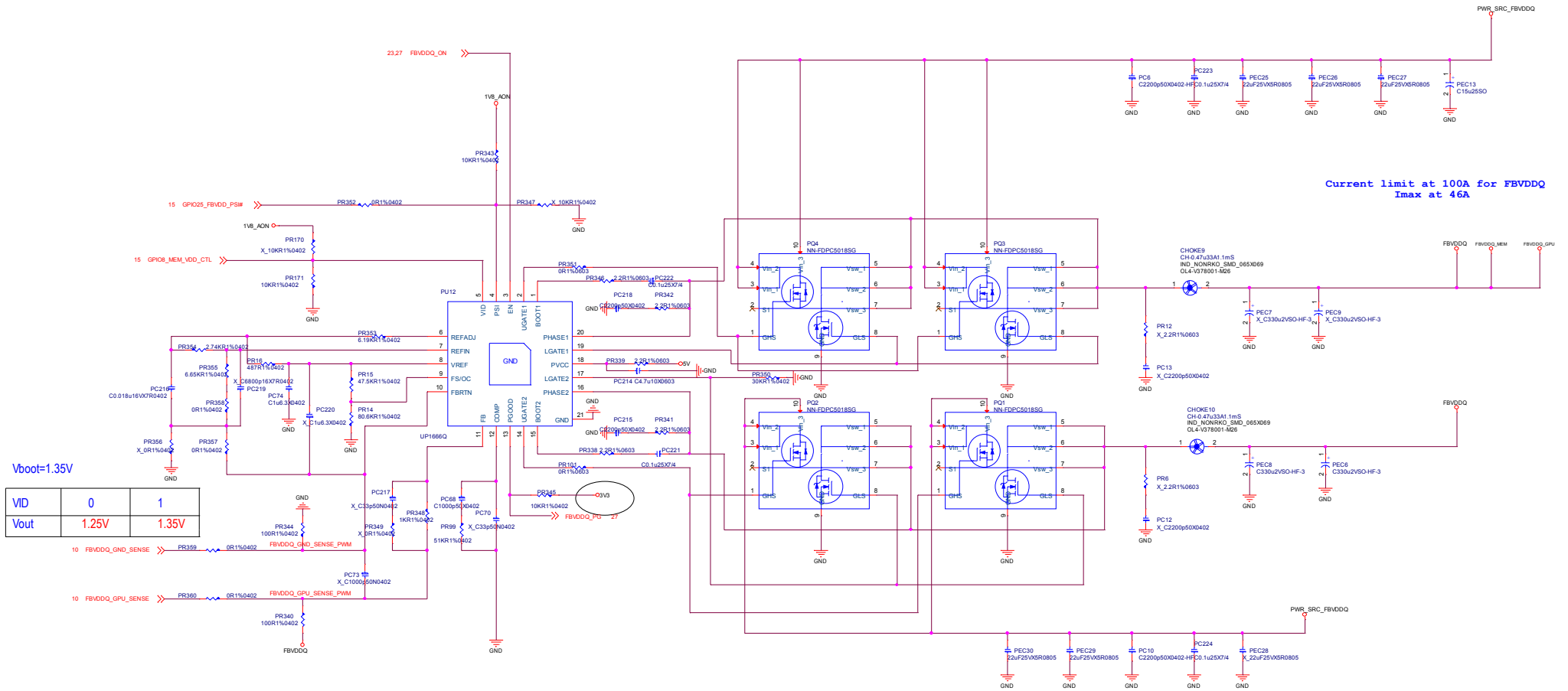
Voltage = 1.0V  
 Current = ? A  
 OCP(typi) = ? A



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>N19P</b>		
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	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>N19P</b>		
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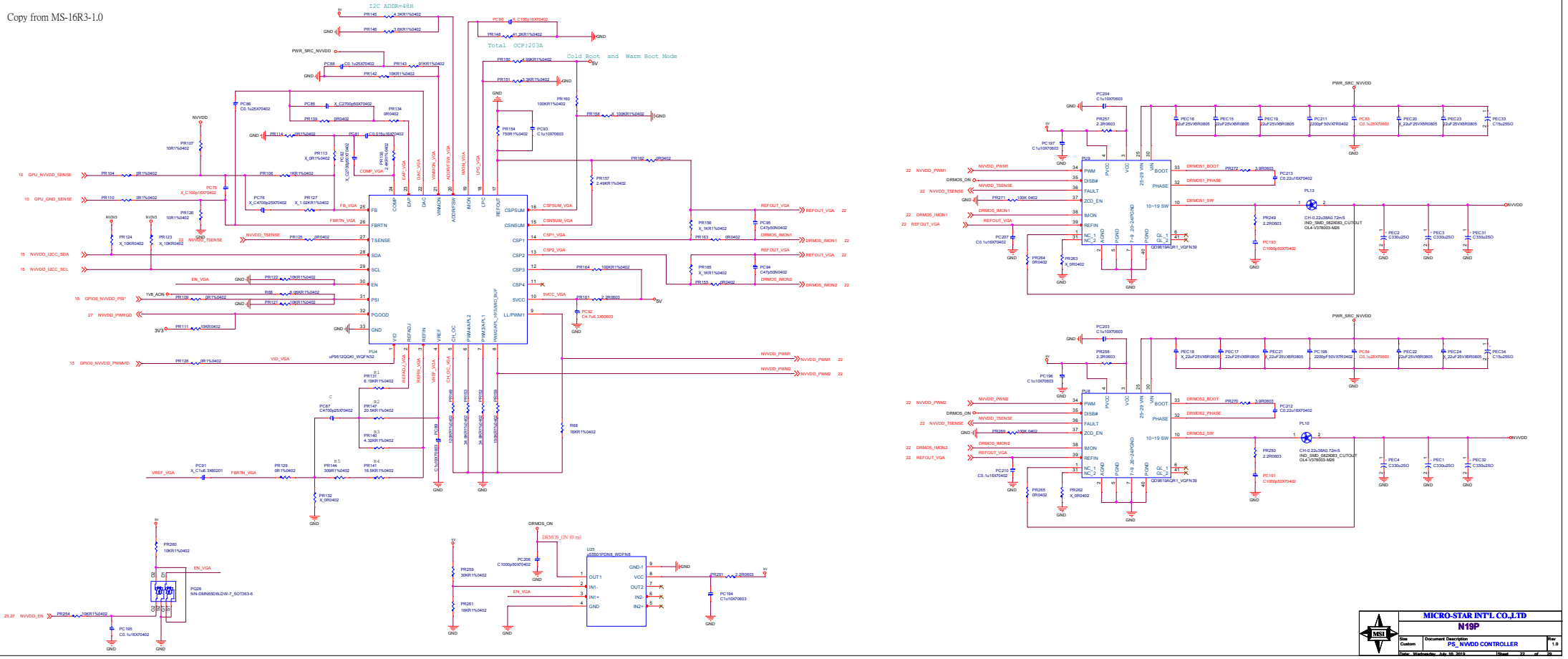


V<sub>boot</sub>=1.35V

VID	0	1
V <sub>out</sub>	1.25V	1.35V

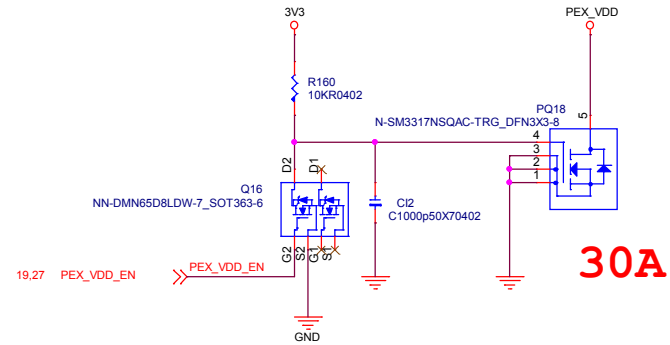
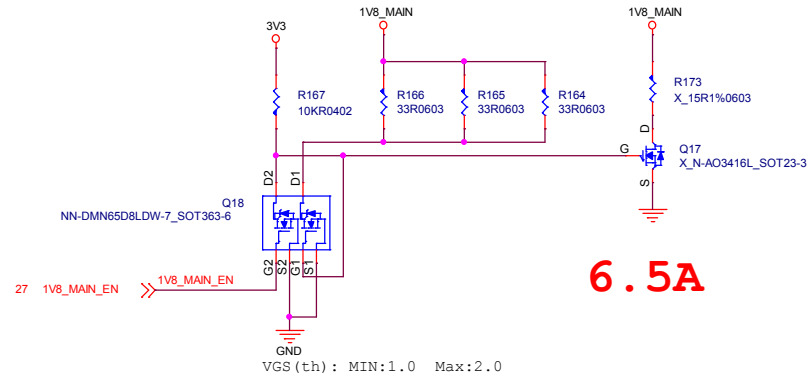
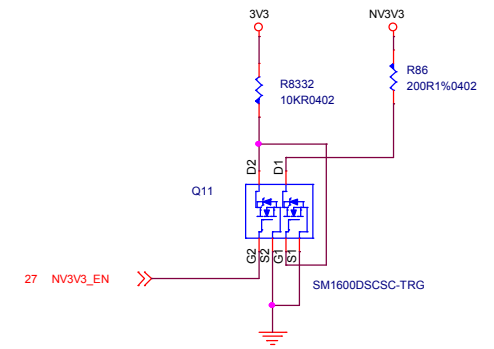
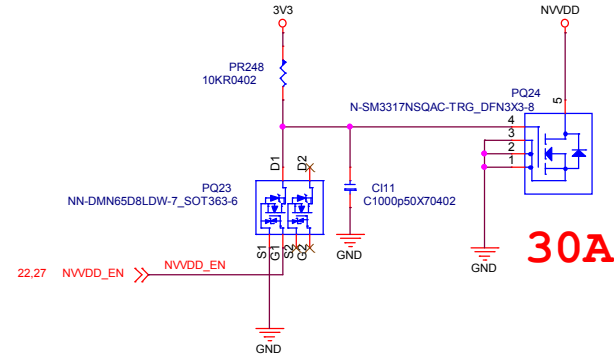
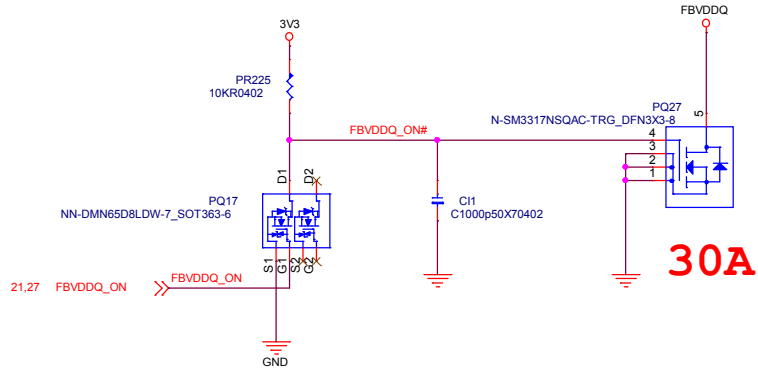
PS: NVDD CONTROLLER


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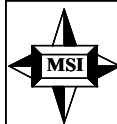
		<b>MICRO-STAR INT'L CO., LTD</b>	
		<b>N19P</b>	
Doc Control	Document Description	<b>PS: NVDD CONTROLLER</b>	
	Rev Control	1.0	

# Discharge



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Pin Name	N17P	N18P	N17P Functional Description	N17P Recommended Default Pull-up or Pull-down	N18P Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	NVVDD_PWM_VID	PWM Output to control NVVDD	0 to 1V8 PWM output	
GPIO1	GC6_FB_EN	GC6_FB_EN	FB Enable for GC6 2.1	OD, 10K pull-down	OD, 10K pull-down
GPIO2	GPU_EVENT#	GPU_EVENT#	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO3	NVVDDS_PWM	UNUSED	PWM output to control the NVVDDS power supply	0 to 1V8 output	
GPIO4	1V8_MAIN_EN	1V8_MAIN_EN	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	FRM_LCK#	Active low Frame Lock	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO6	NVVDD_PSI	NVVDD_PSI	Phase shedding	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	LCD_BL_PWM	Panel Backlight PWM Brightness Control	100K pull-down	100K pull-down
GPIO8	MEM_VDD_CTL	MEM_VDD_CTL	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	THERM_ALERT	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL	Memory VREF Control	100K pull-down	100K pull-down
GPIO11	LCD_VCC	LCD_VCC	Panel Power Enable	100K pull-down	100K pull-down
GPIO12	PWR_LEVEL	PWR_LEVEL	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON	10K pull-up to 1V8_AON
GPIO13	LCD_BLEN	UNUSED	Panel Backlight Enable	100K pull-down	
GPIO14	HPD_A	HPD_A	Hot Plug Detect for IFPA		10K pull-up to 1V8_AON
GPIO15	HPD_B	HPD_B	Hot Plug Detect for IFPB		10K pull-up to 1V8_AON
GPIO16	SYS_PEX_RST_MON#	UNUSED	System side PCIe reset monitor	10K pull-up to 1V8 _AON	
GPIO17	HPD_D	HPD_D	Hot Plug Detect for IFPD		10K pull-up to 1V8_AON
GPIO18	HPD_E	HPD_E	Hot Plug Detect for IFPE		10K pull-up to 1V8_AON
GPIO19	3DVision	UNUSED	3D Vision L/R signal	100K pull-down	
GPIO20	GC5_MODE	NB_GC6			10K pull-down
GPIO21	UNUSED	LCD_BLEN			100K pull-down
GPIO22	UNUSED	ADC_MUX_SEL			2.2K pull-up See Circuit
GPIO23	GPU_PEX_RST_HOLD#	RESERVED	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3	100K pull-down
GPIO24	HPD_F	UNUSED	Hot Plug Detect for IFFF		
GPIO25	UNUSED	FBVDD_PSI#			
GPIO26	UNUSED	FP_FUSE			10K pull-down
GPIO27	HPD_C	HPD_C	Hot Plug Detect for IFPC		10K pull-up to 1V8_AON



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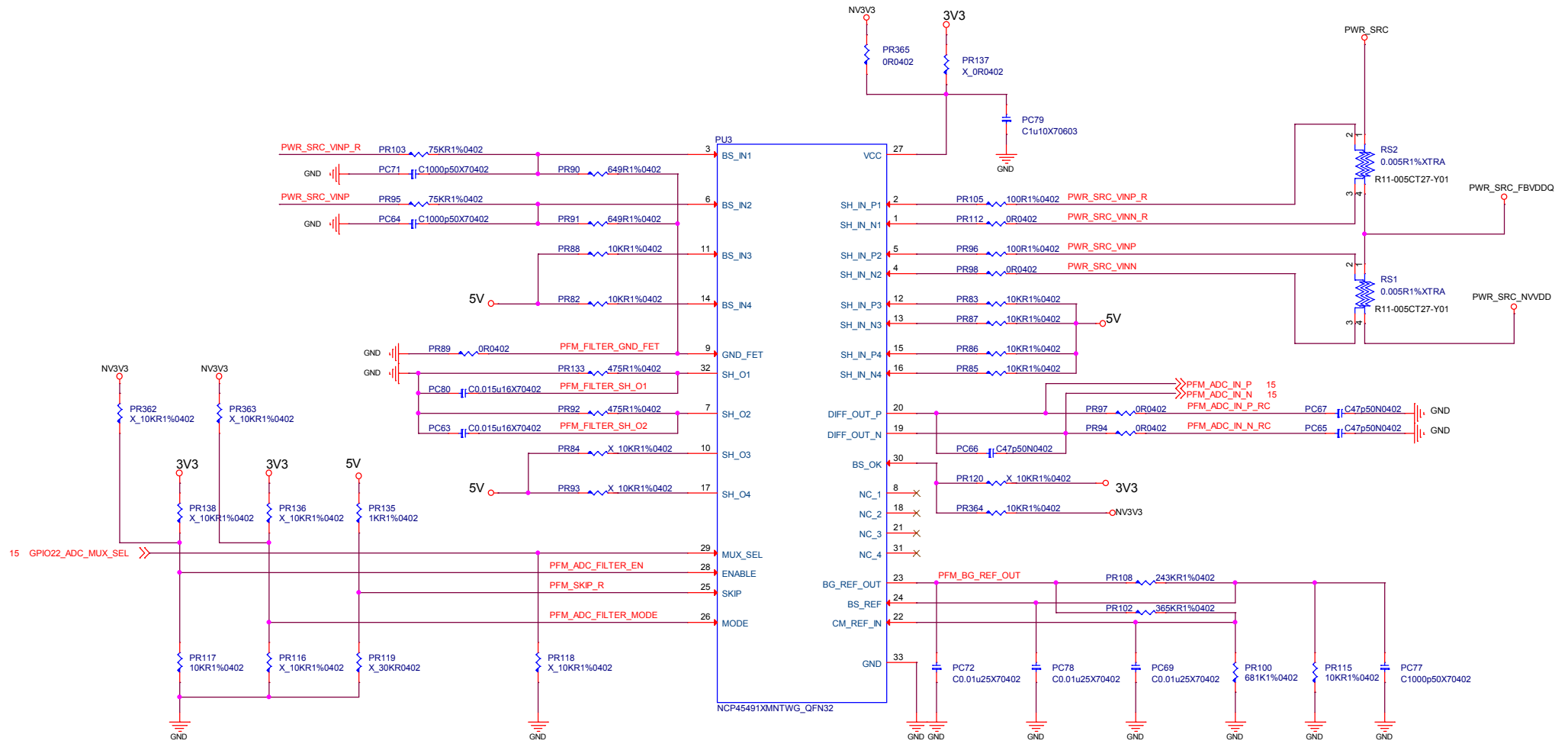
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# INPUT PREFILTER

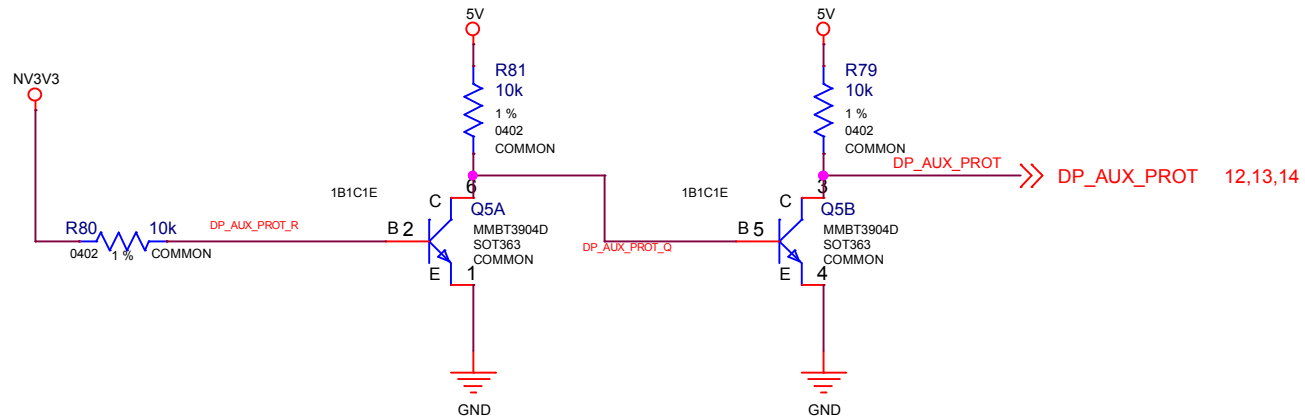
On Semi	PR90, PR91	PR92, PR133	PR108	PR95, PR103	PC64, PC71
CONFIG	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	649R	475R	243K	75K	1.0nF




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# SEQUENCE:5V,1V8,NV3V3 ENABLE

DP\_AUX Protection

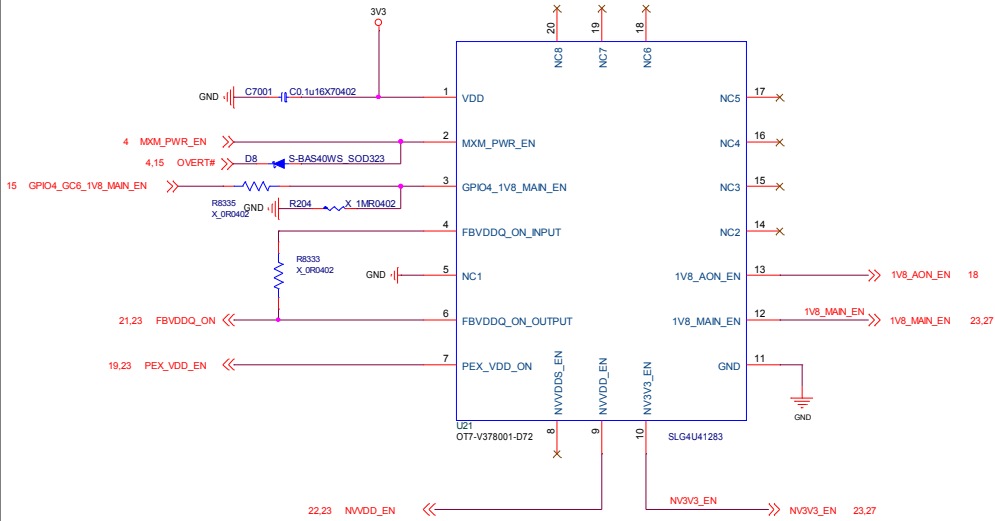


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	Size A	Document Description <b>DP_AUX Protection</b>	Rev 1.0
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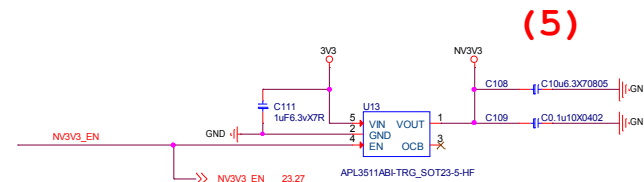
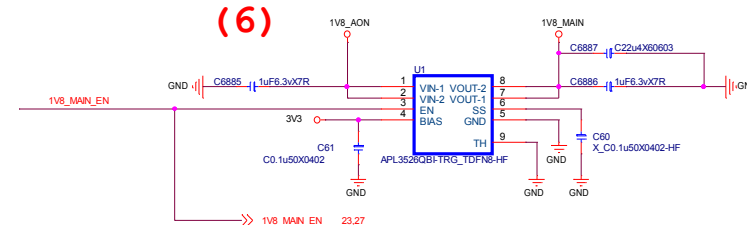
# Power Sequence Control

POWER ON= 1V8\_AON->1V8\_MAIN->NV3V3->NVVDD->PEX\_VDD->FBVDDQ->>DGPU\_PWRGD

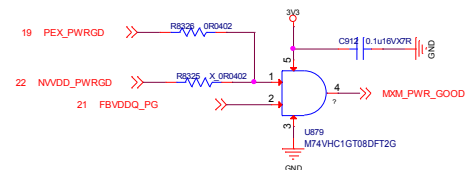
POWER OFF= PEX\_VDD/FBVDDQ->NVVDD->NV3V3->1V8\_MAIN->1V8\_AON



PIN2	MXM_PWR_EN	is	3.3V	INPUT
PIN3	GPIO4_GC6_PWR_EN	is	1.8V	INPUT
PIN4	FBVDDQ_ON_INPUT		3.3V	INPUT
PIN6	FBVDDQ_ON_OUTPUT		3.3V	OUTPUT
PIN7	PEX_VDD_EN_IC		3.3V	OUTPUT
PIN9	NVVDD_EN_IC		3.3V	OUTPUT
PIN12	1V8_MAIN_EN_IC		3.3V	OUTPUT
PIN13	1V8_AON_EN_IC		3.3V	OUTPUT




**SOFTSTRAT=400us**



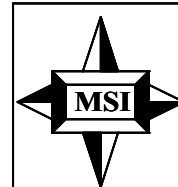
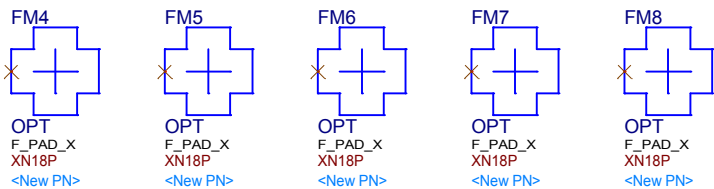
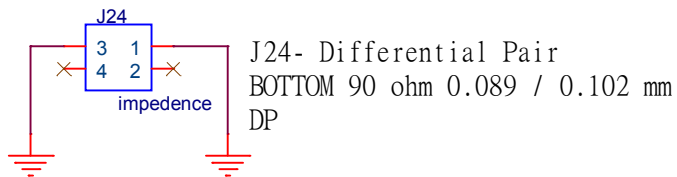
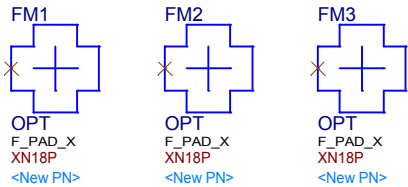
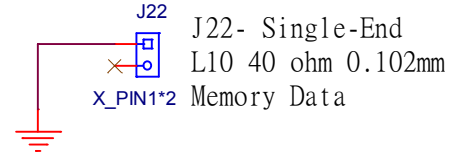
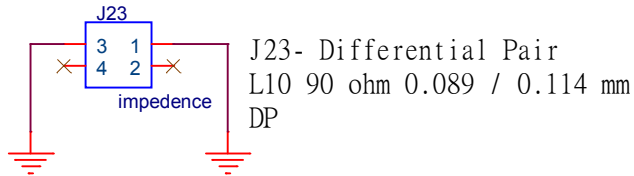
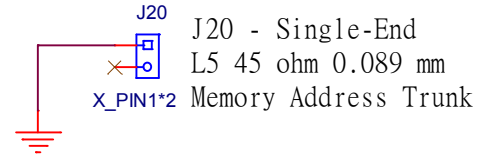
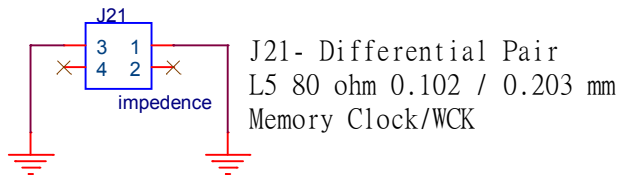
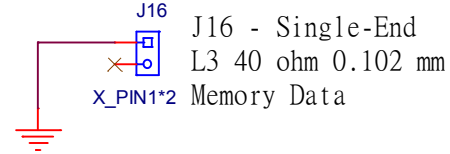
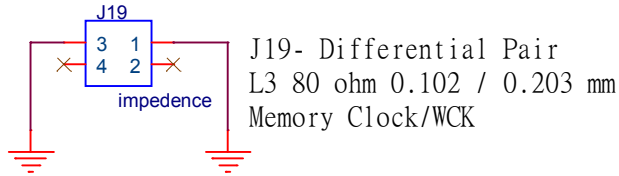
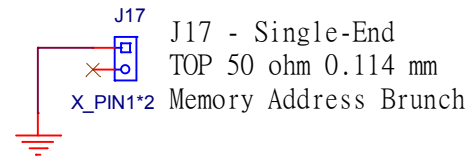
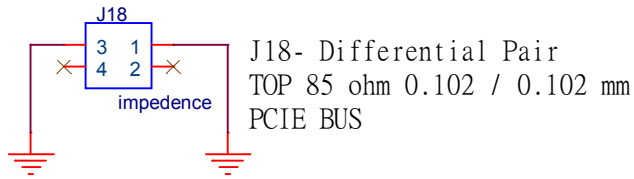
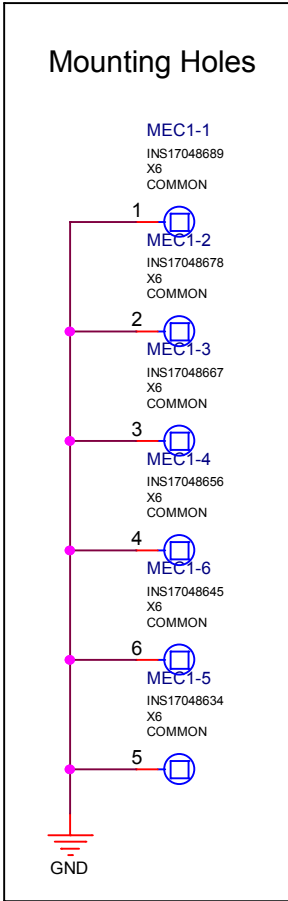
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SEQUENCE:DISCHARGE

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# MECH

## Mounting Holes



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