

PG174-A01

TU117, 128b GDDR5 x32, 75W DVI-D DL/DUAL DP + HDMI

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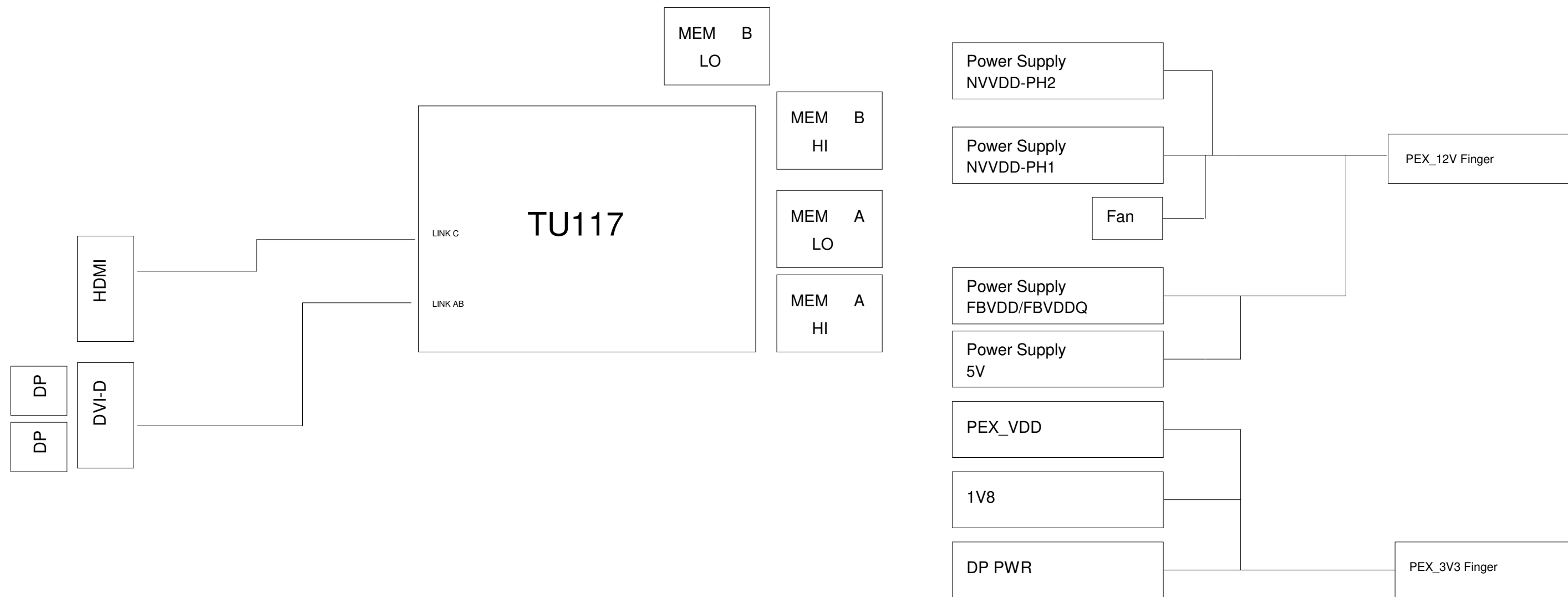
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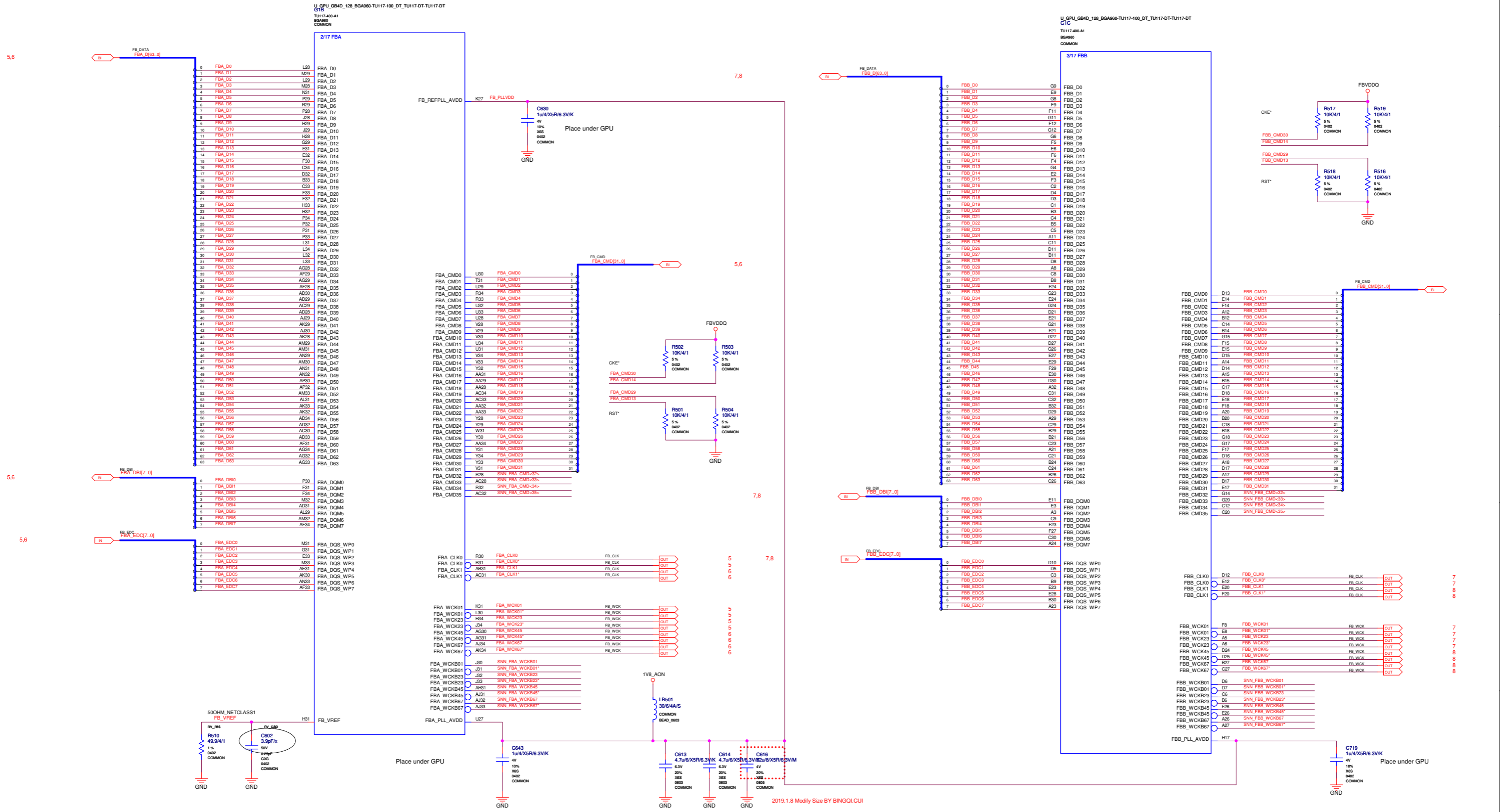
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Block Diagram



MEMORY: GPU Partition A/B



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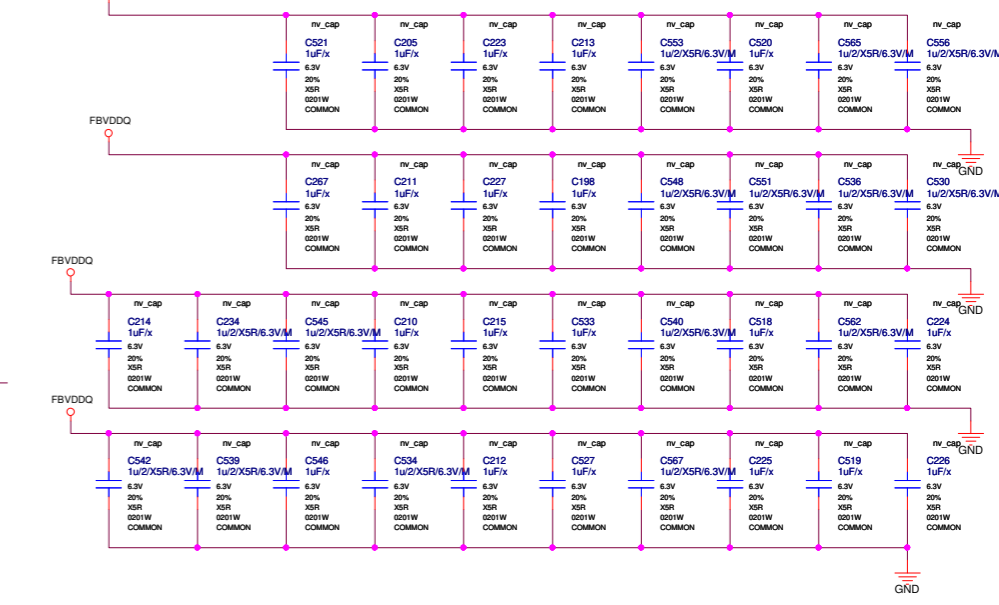
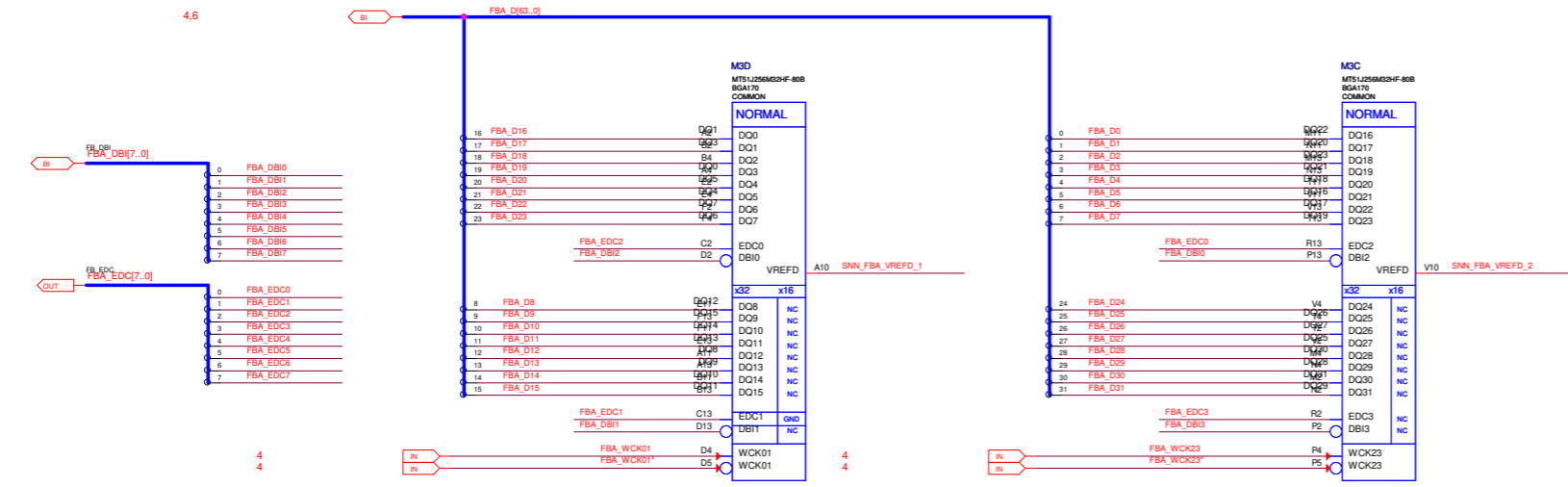
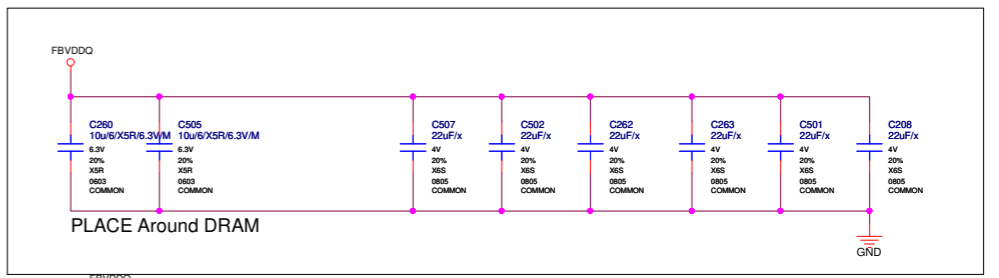
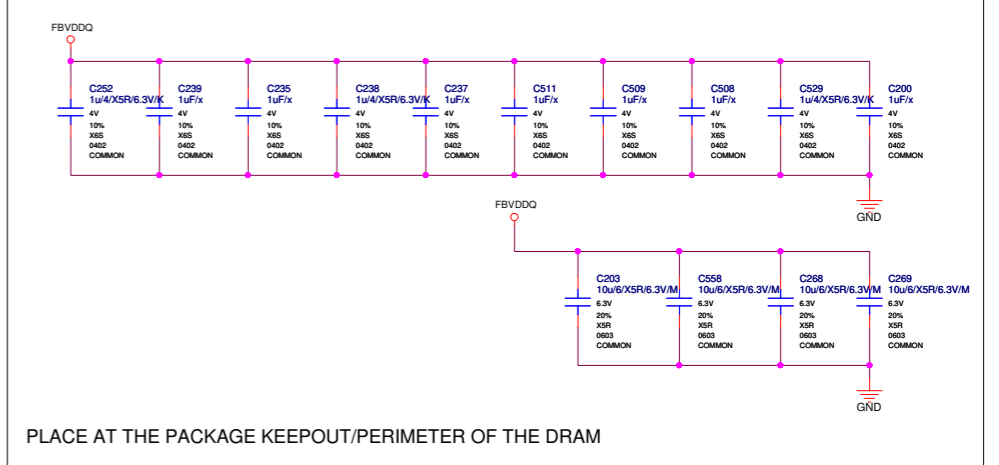
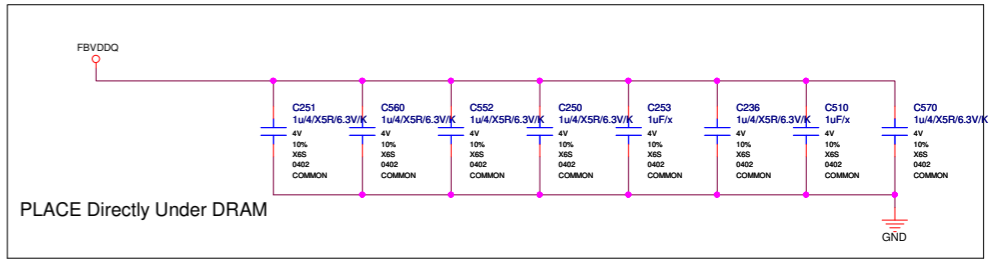
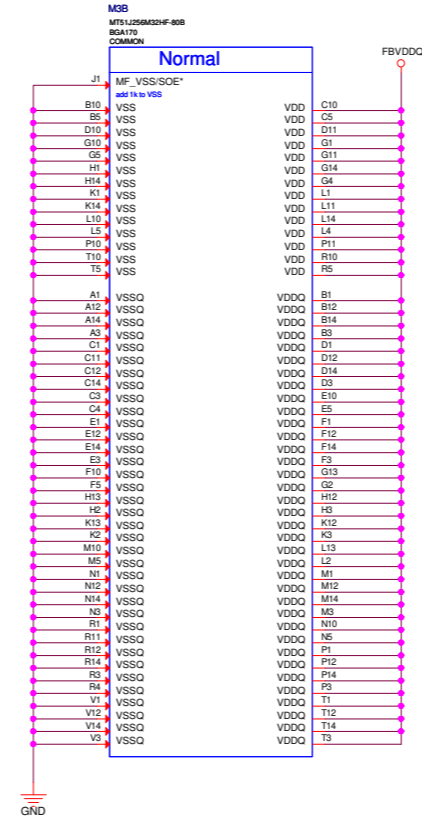
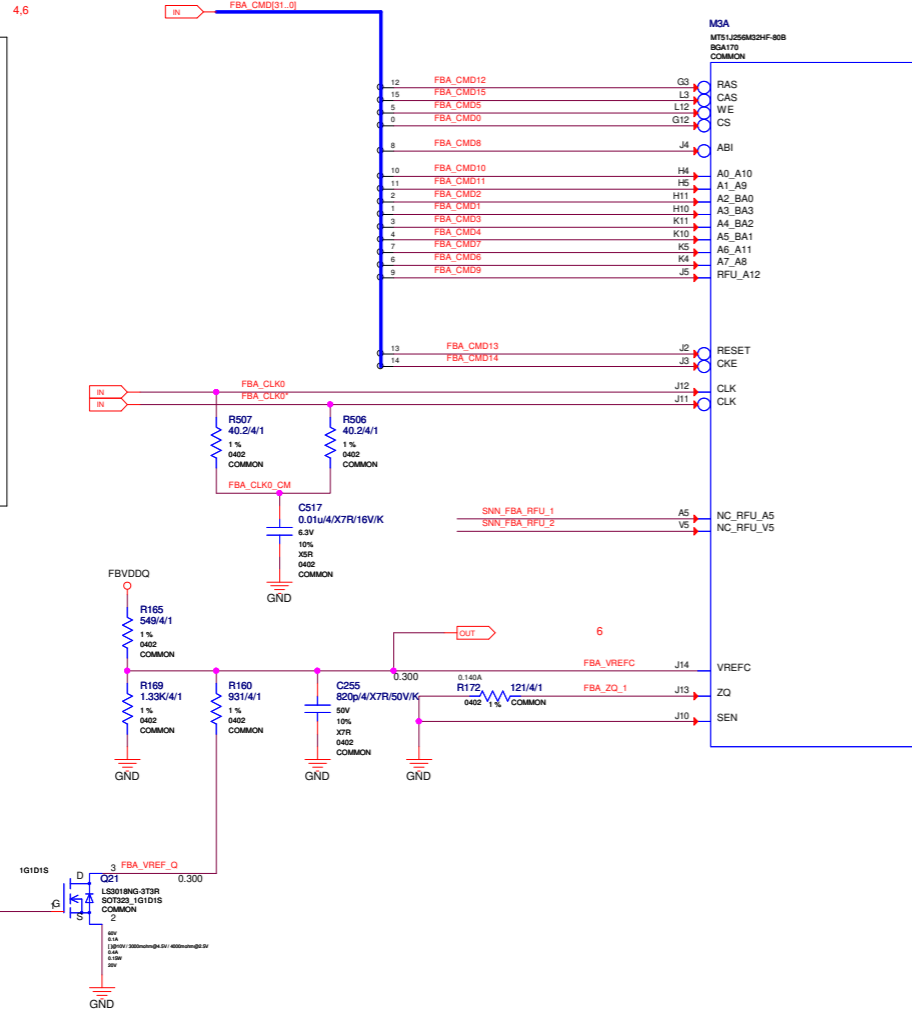
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MEMORY: FBA Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15		CS*
CMD16		A3_BA3
CMD17		A2_BA0
CMD18		A4_BA2
CMD19		A5_BA1
CMD20		WE*
CMD21		A7_A8
CMD22		A6_A11
CMD23		ABI*
CMD24		A12_RFU
CMD25		A0_A10
CMD26		A1_A9
CMD27		RAS*
CMD28		RST*
CMD29		CKE*
CMD30		CAS*
CMD31		



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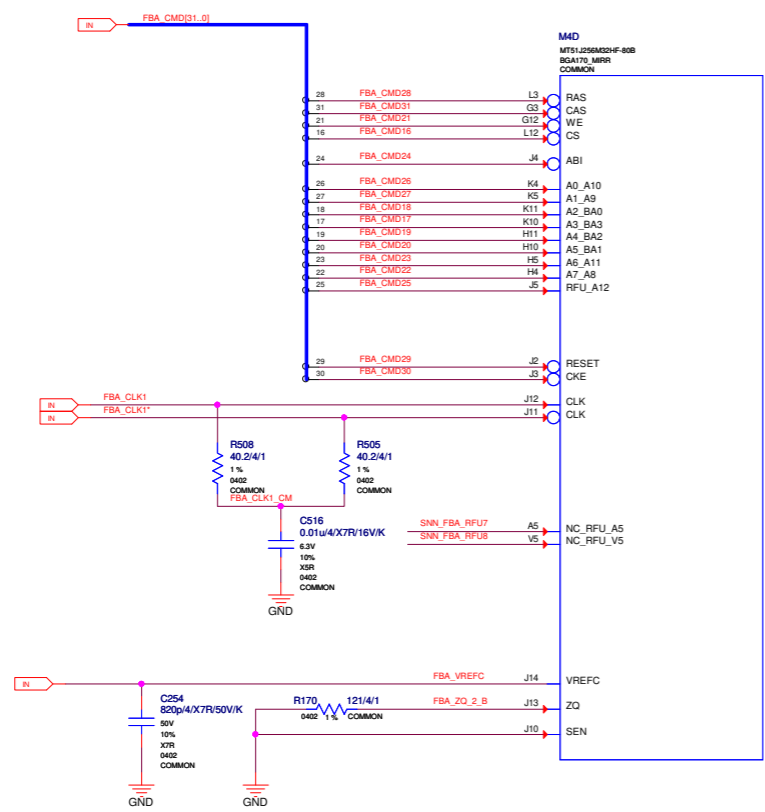
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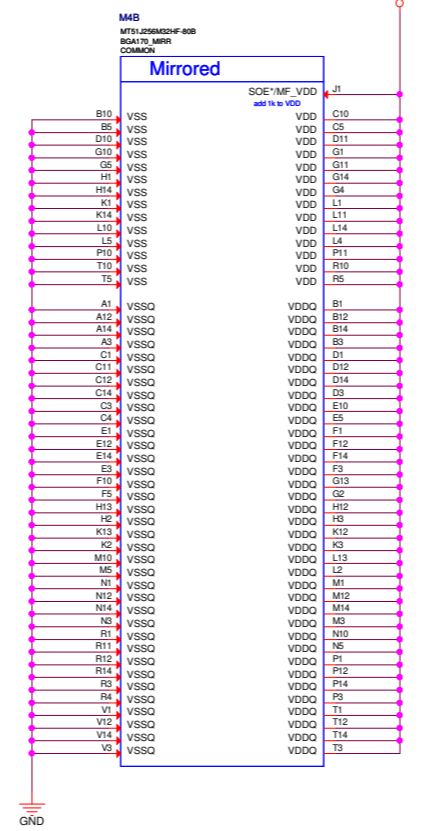
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CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

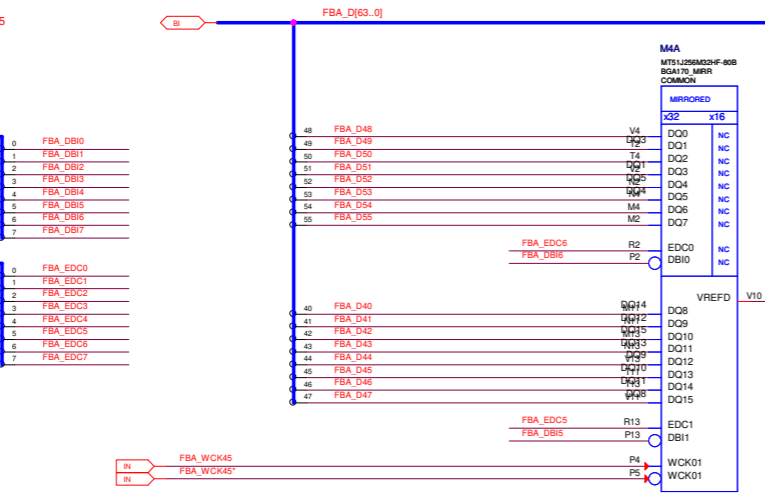
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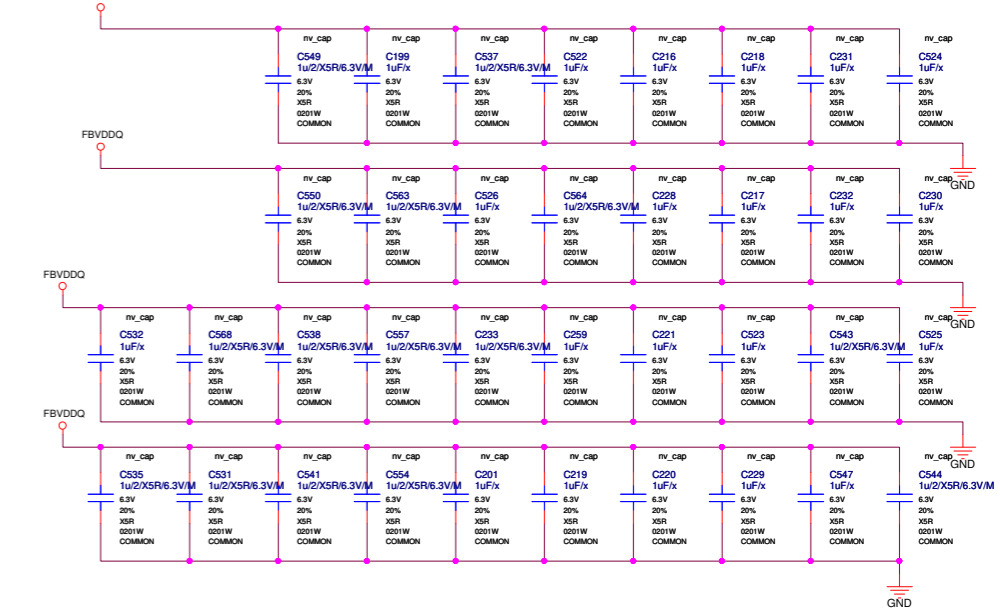
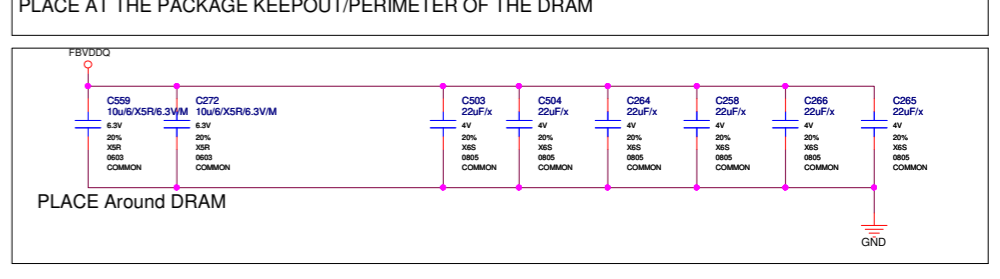
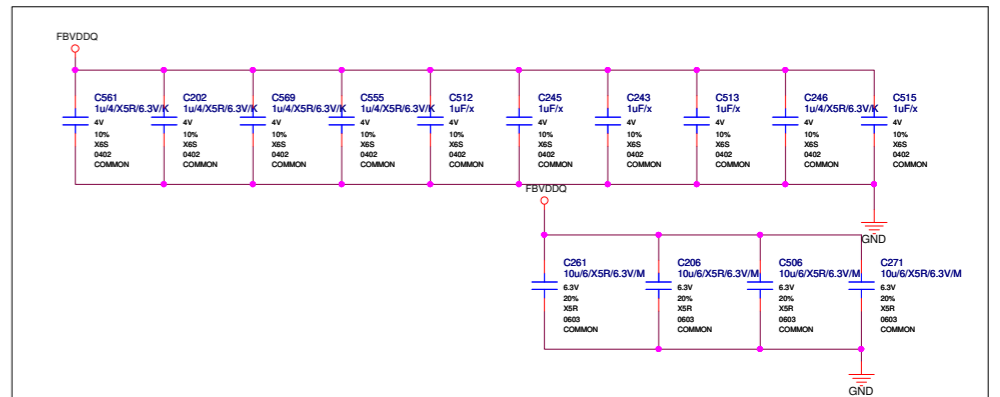
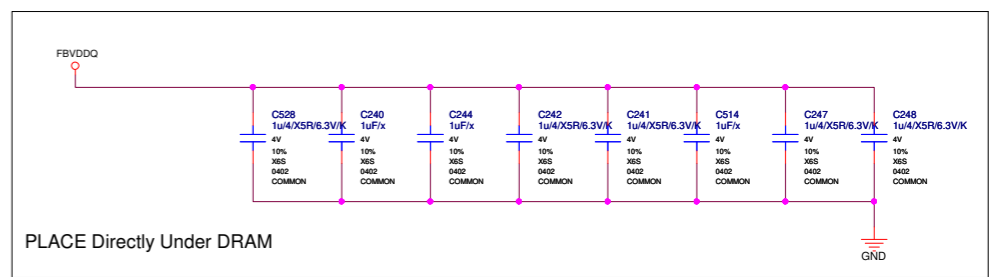
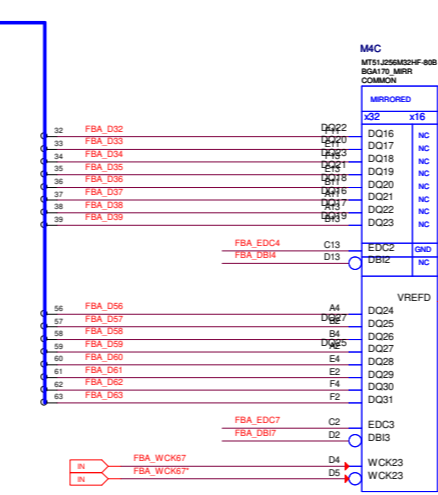
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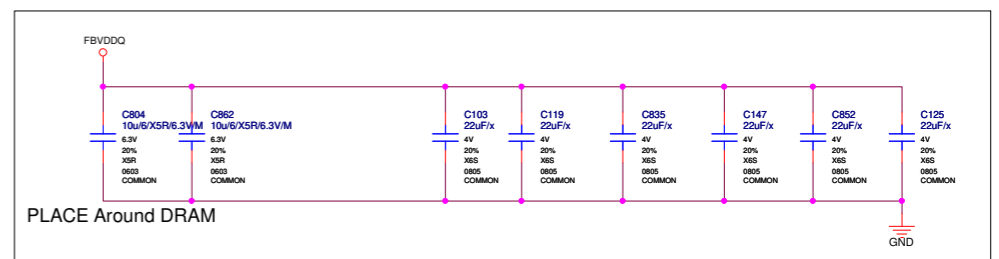
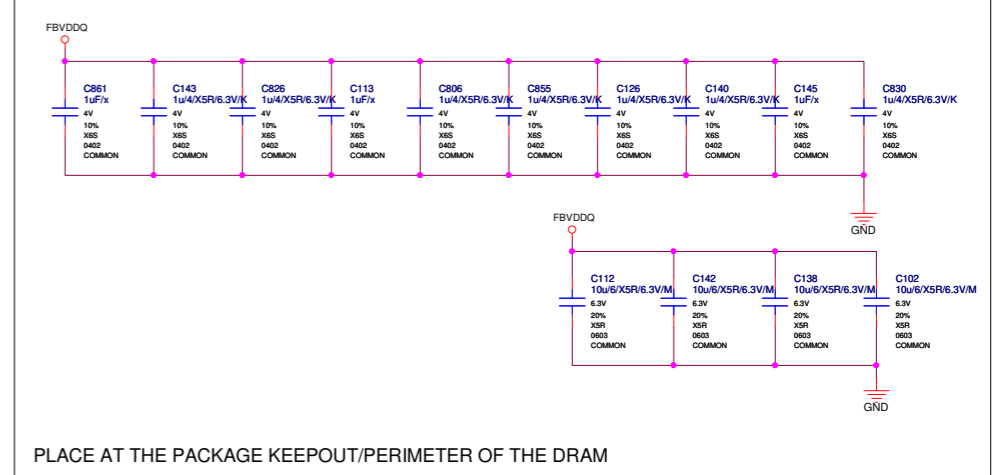
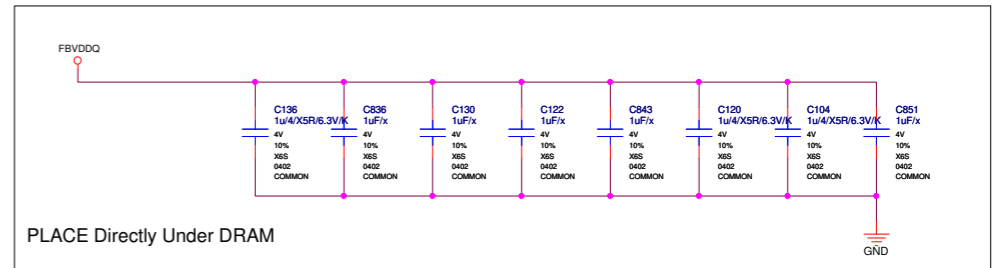
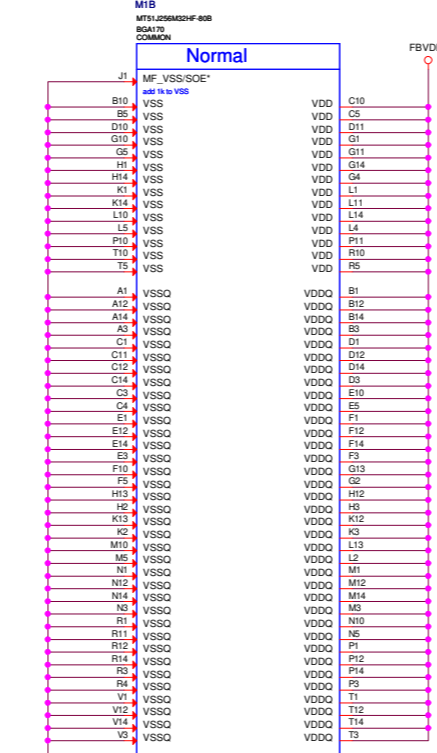
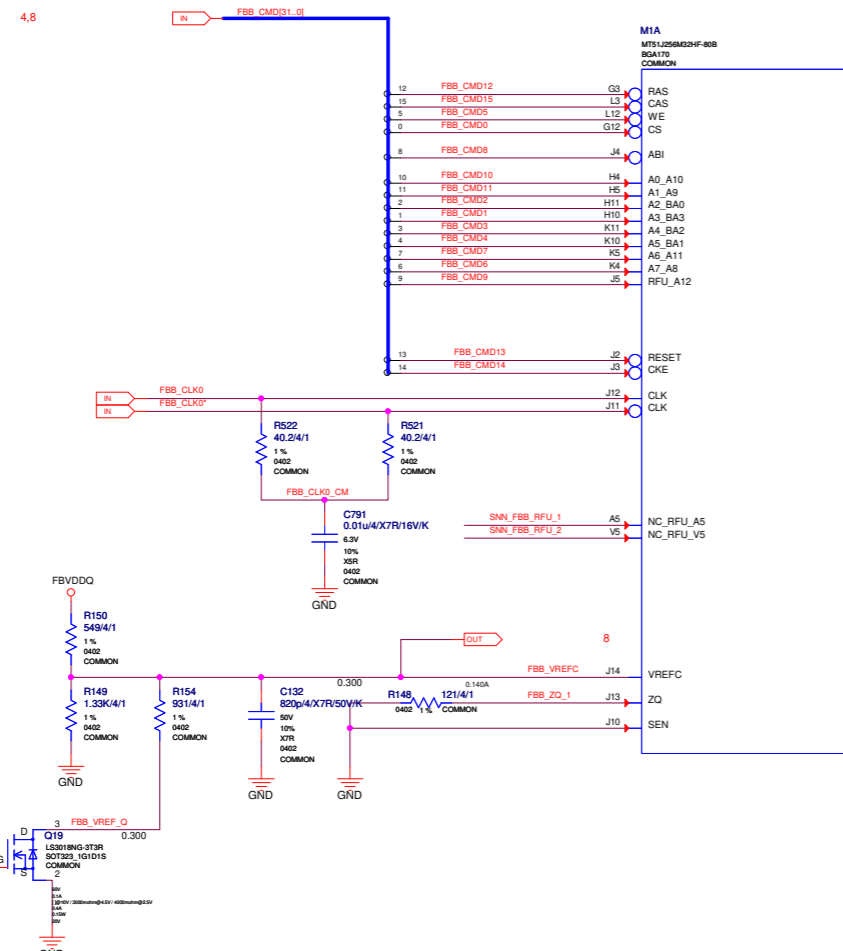
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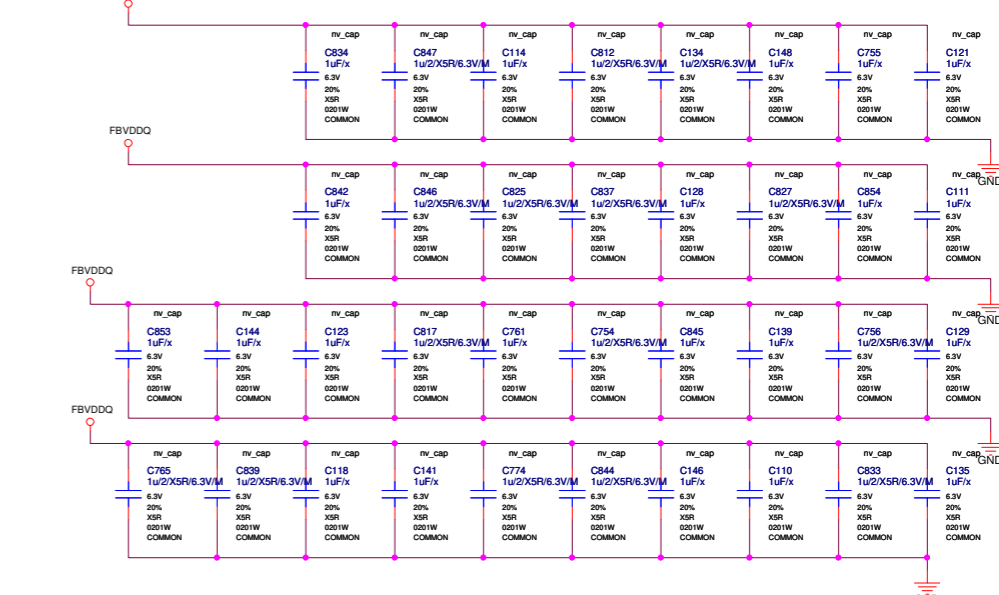
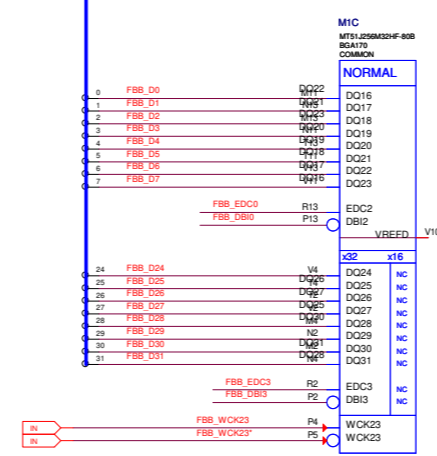
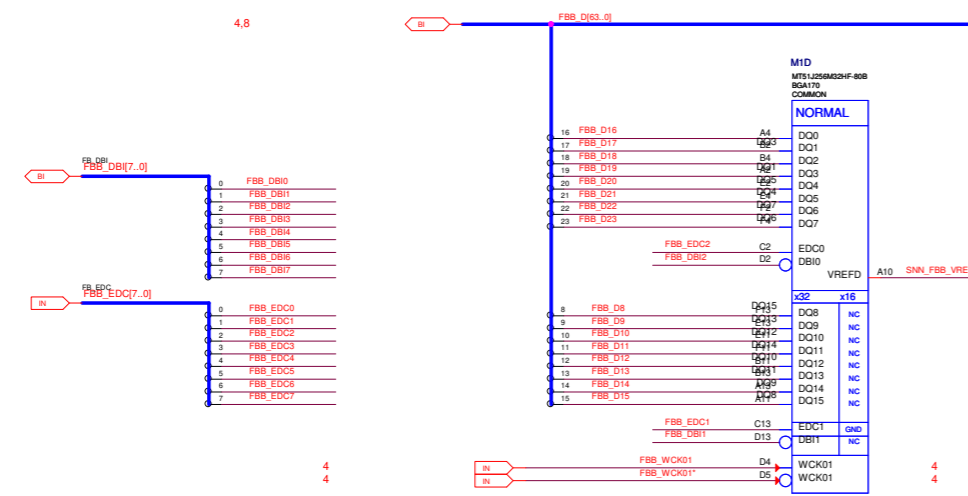
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MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16	CS*	
CMD17	A3_BA3	
CMD18	A2_BA0	
CMD19	A4_BA2	
CMD20	A5_BA1	4
CMD21	WE*	4
CMD22	A7_A8	
CMD23	A6_A11	
CMD24	AB1*	
CMD25	A12_RFU	
CMD26	A0_A10	
CMD27	A1_A9	
CMD28	RAS*	
CMD29	RST*	
CMD30	CKE*	
CMD31	CAS*	



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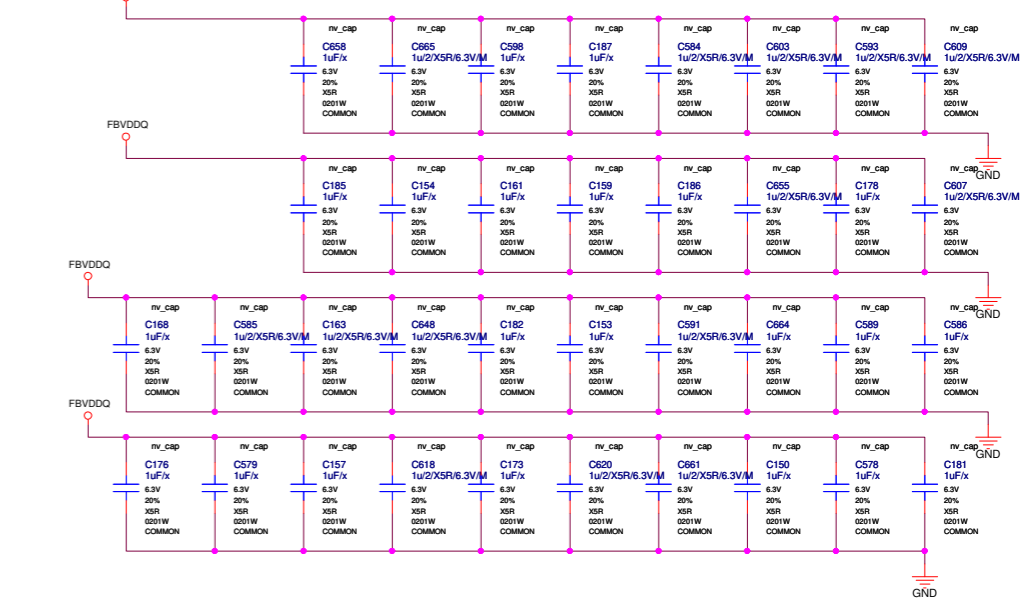
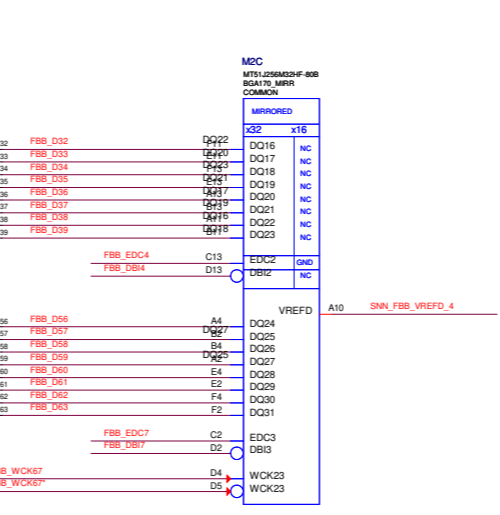
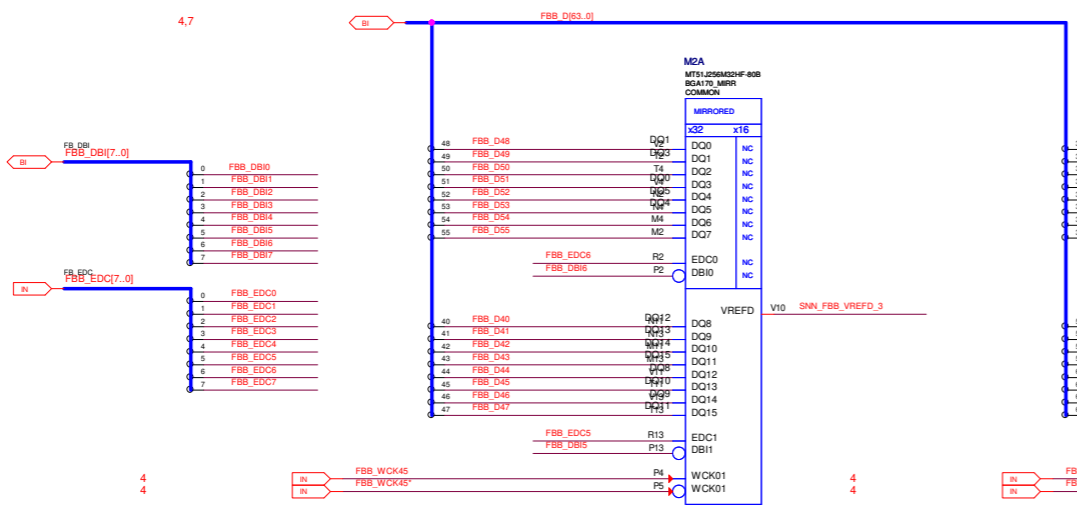
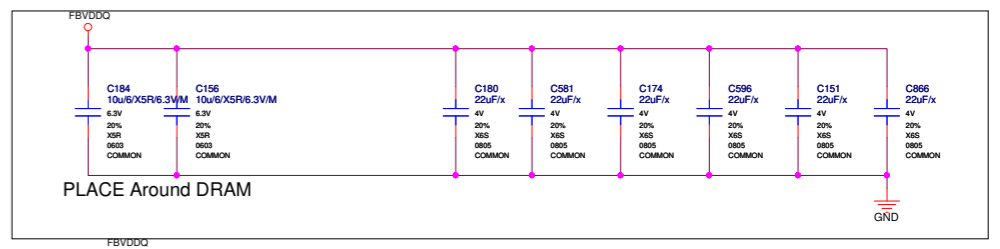
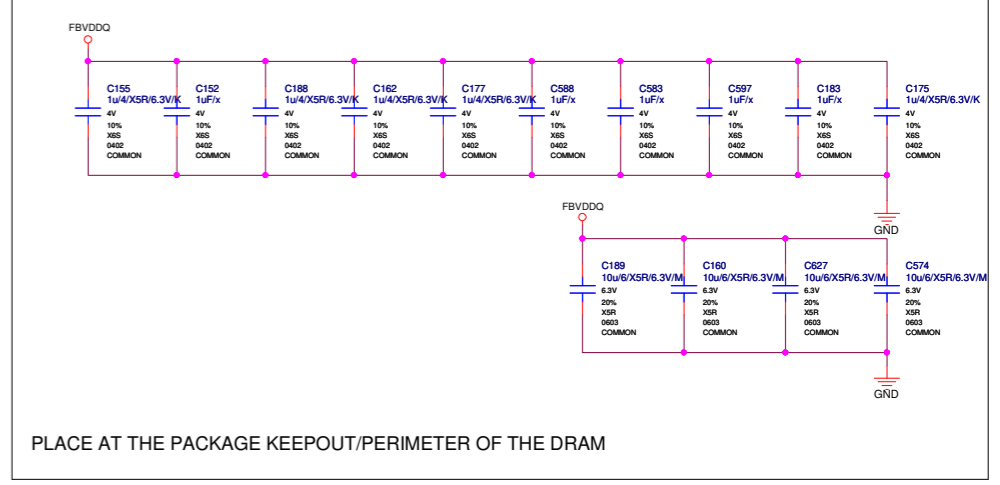
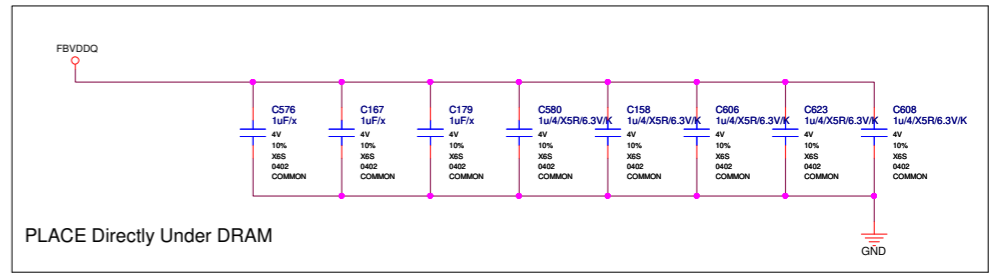
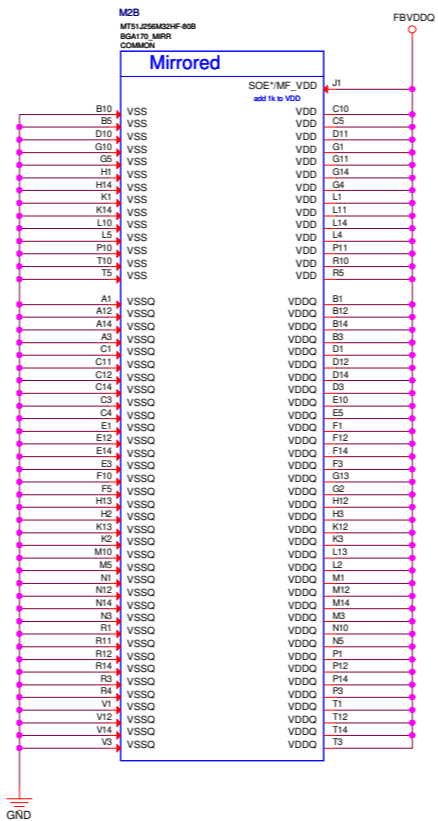
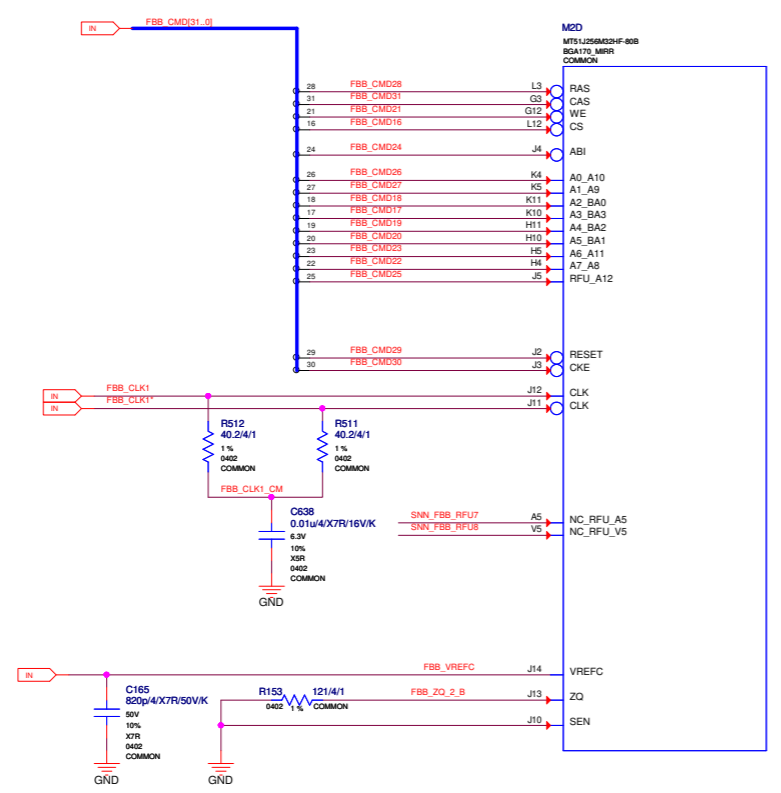
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CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	CS*
CMD13	RST*	A3_BA3
CMD14	CKE*	A2_BA0
CMD15	CAS*	A4_BA2
CMD16		A5_BA1
CMD17		WE*
CMD18		A7_A8
CMD19		A6_A11
CMD20		AB1*
CMD21		A12_RFU
CMD22		A0_A10
CMD23		A1_A9
CMD24		RAS*
CMD25		RST*
CMD26		CKE*
CMD27		CAS*
CMD28		
CMD29		
CMD30		
CMD31		



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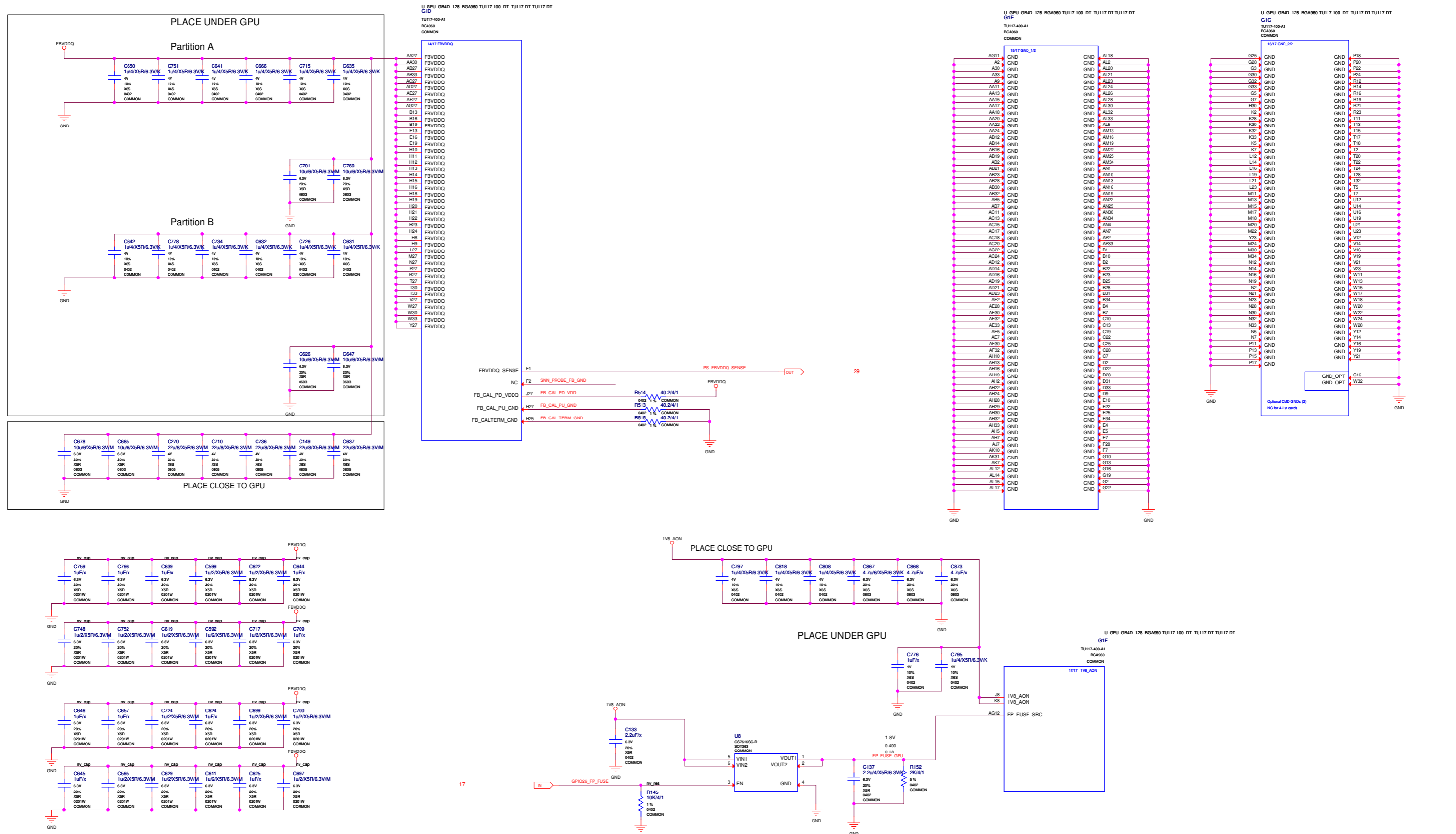
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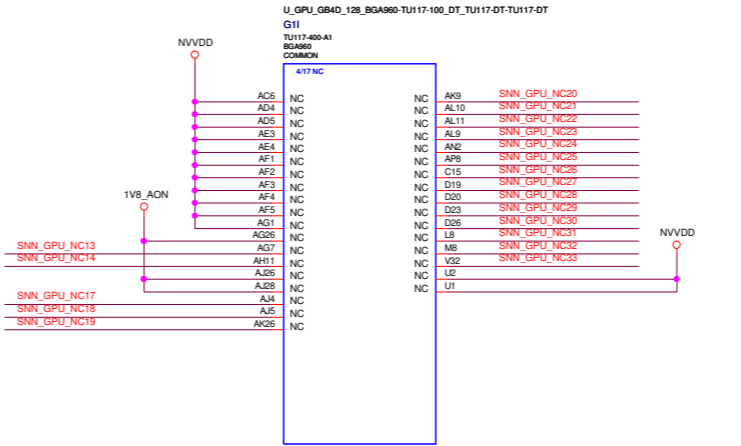
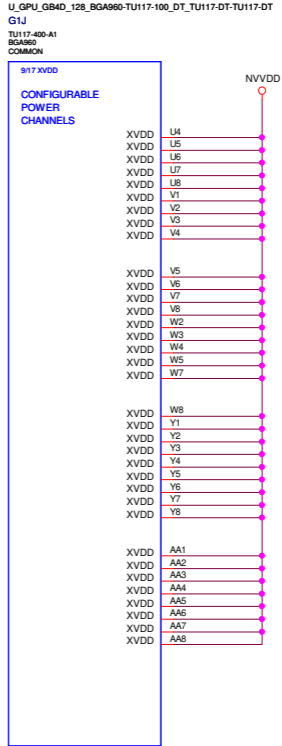
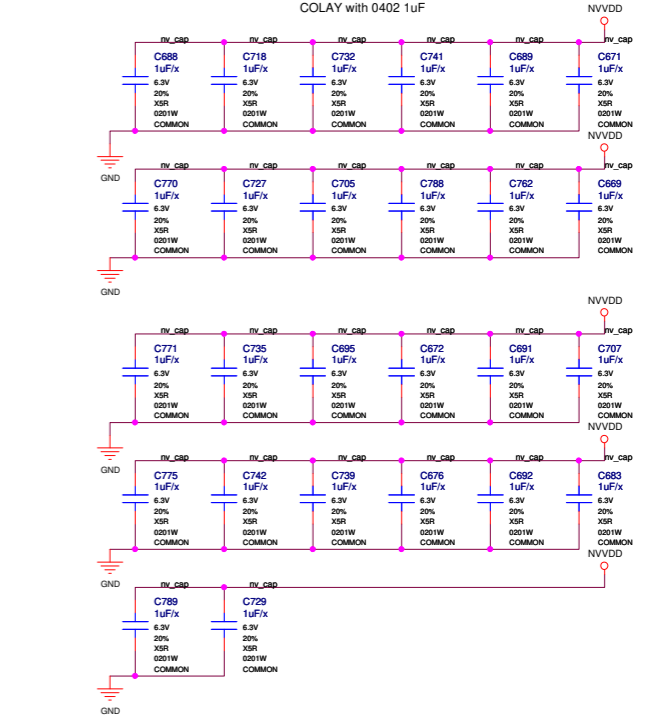
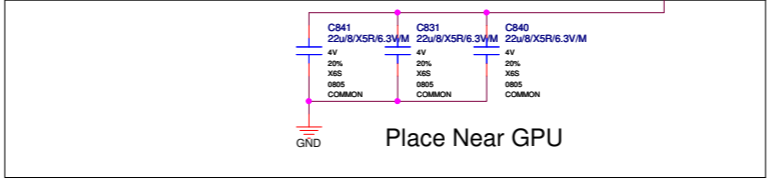
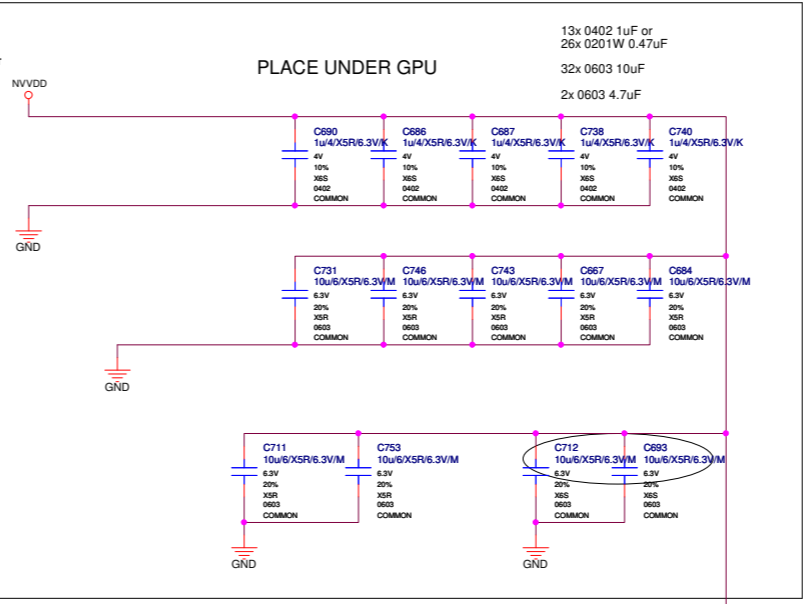
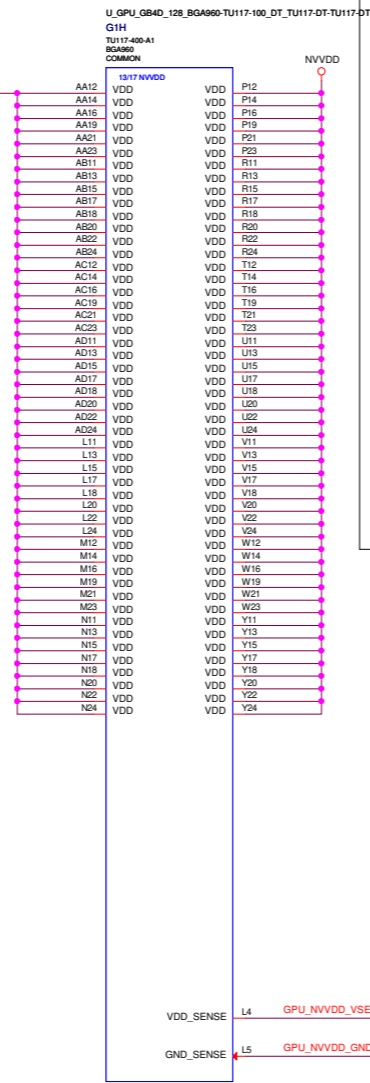
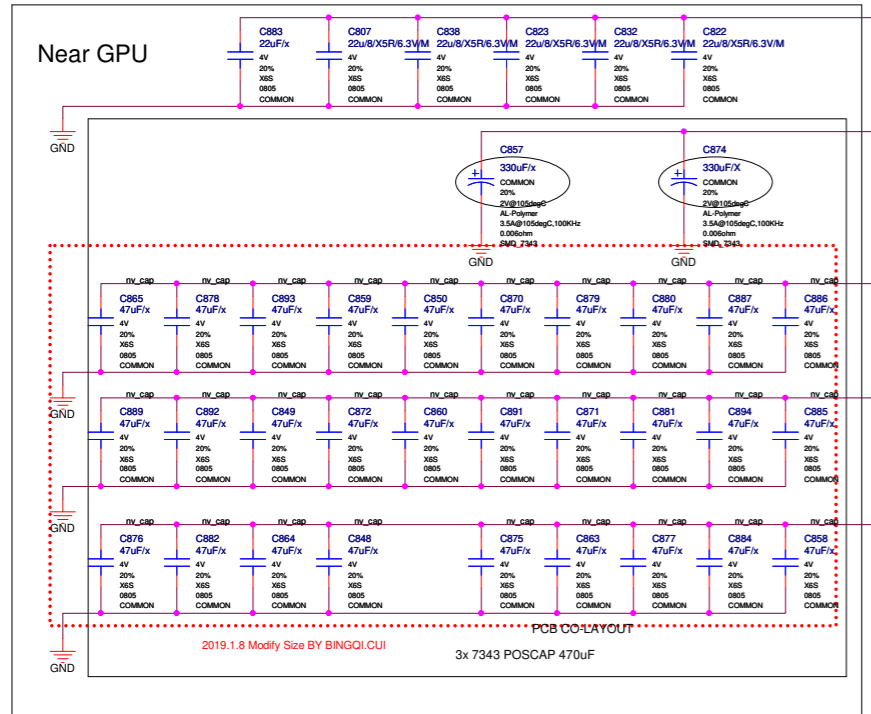
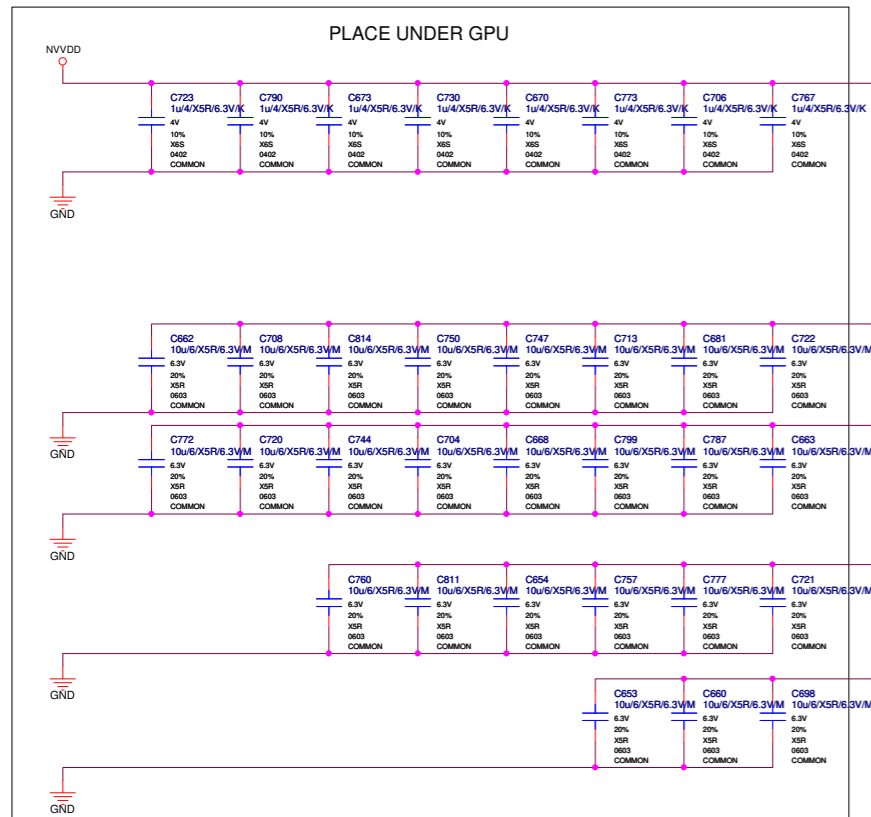
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GPU FBVDDQ & 1V8 Decoupling



GPU NVVDD Decoupling



ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- GPU NVVDD DECOUPLING
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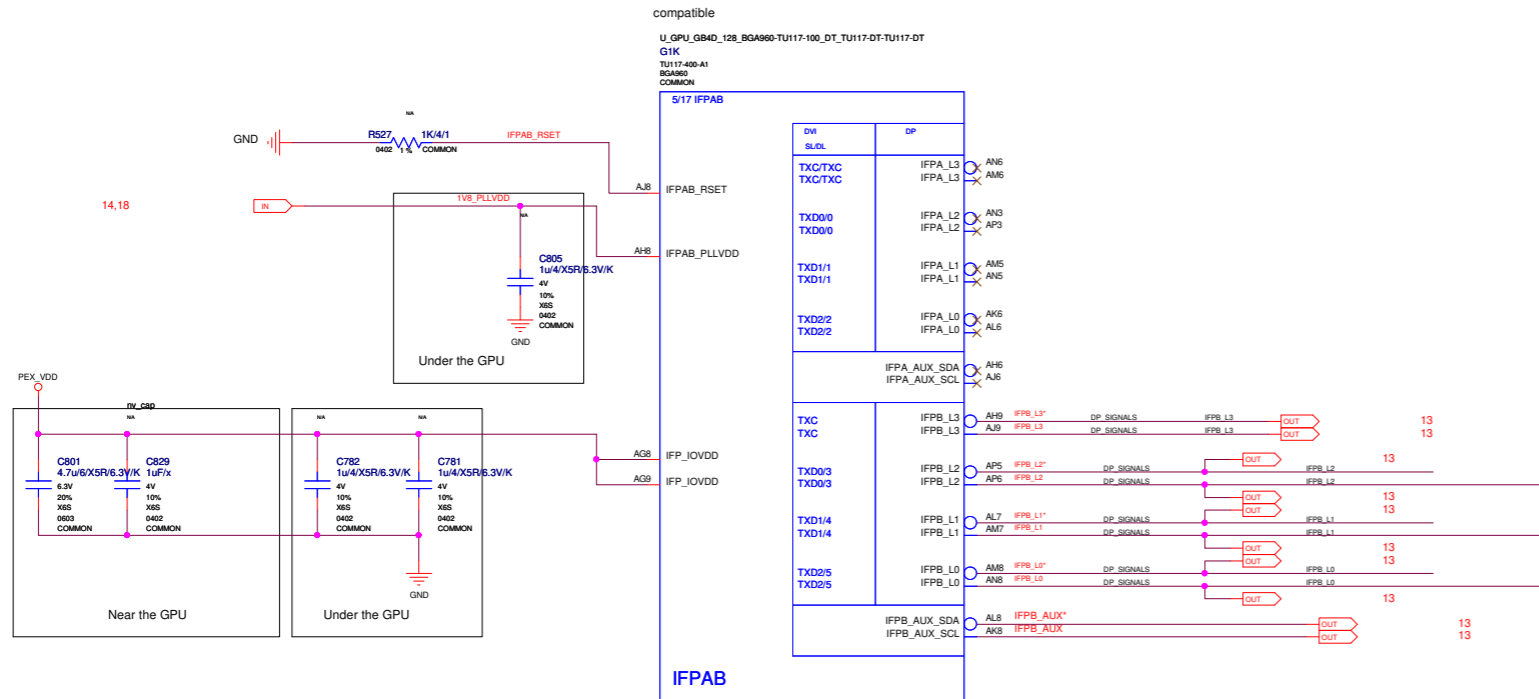
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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

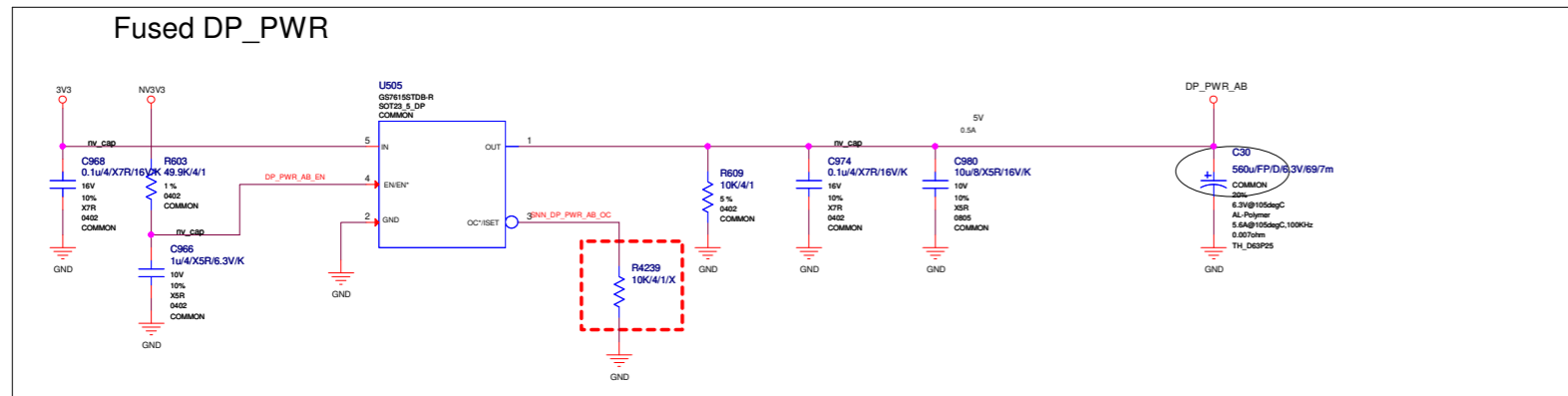
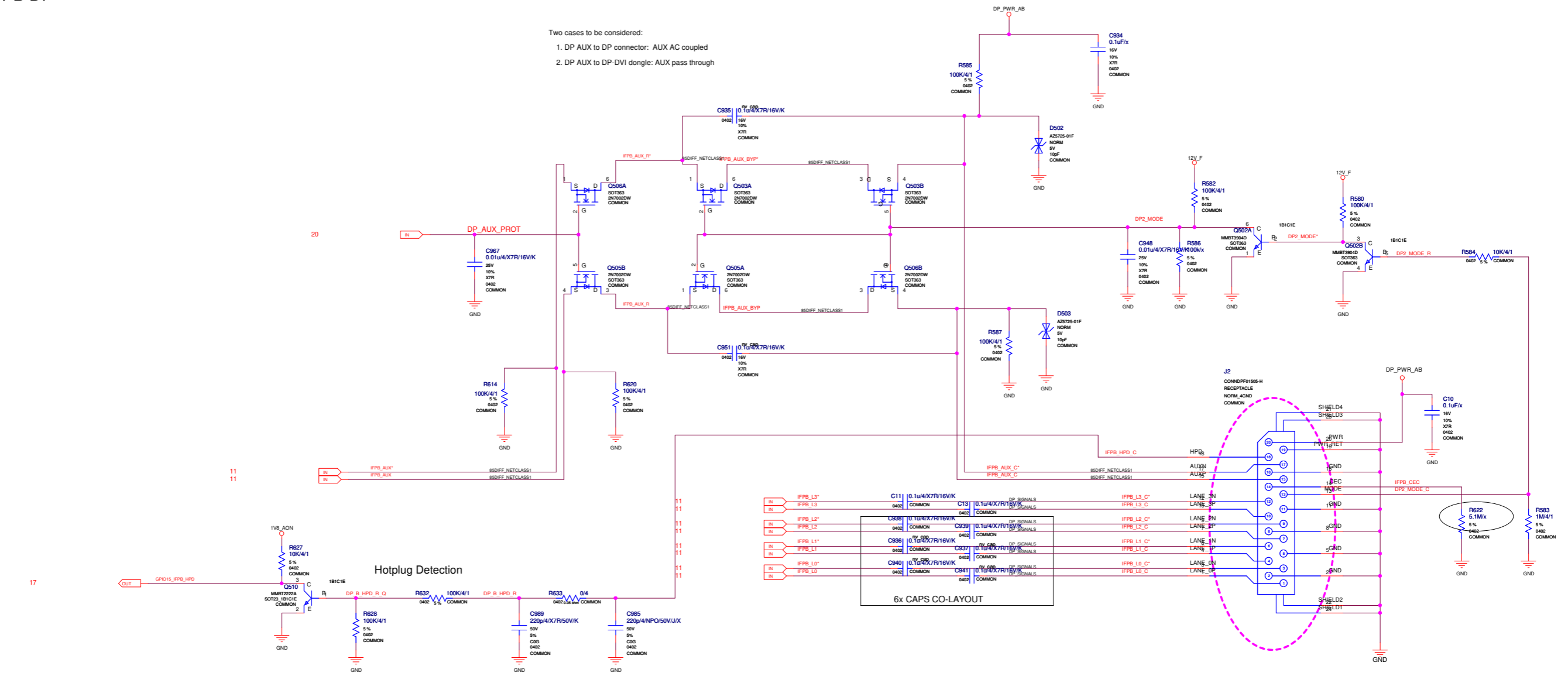
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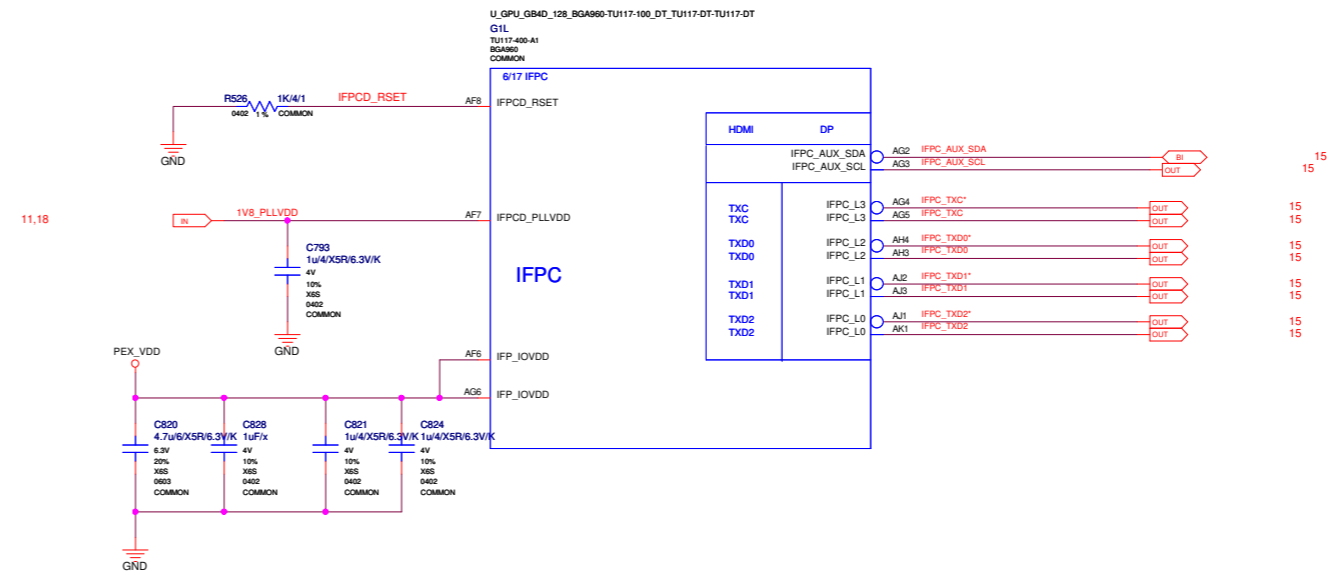
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IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



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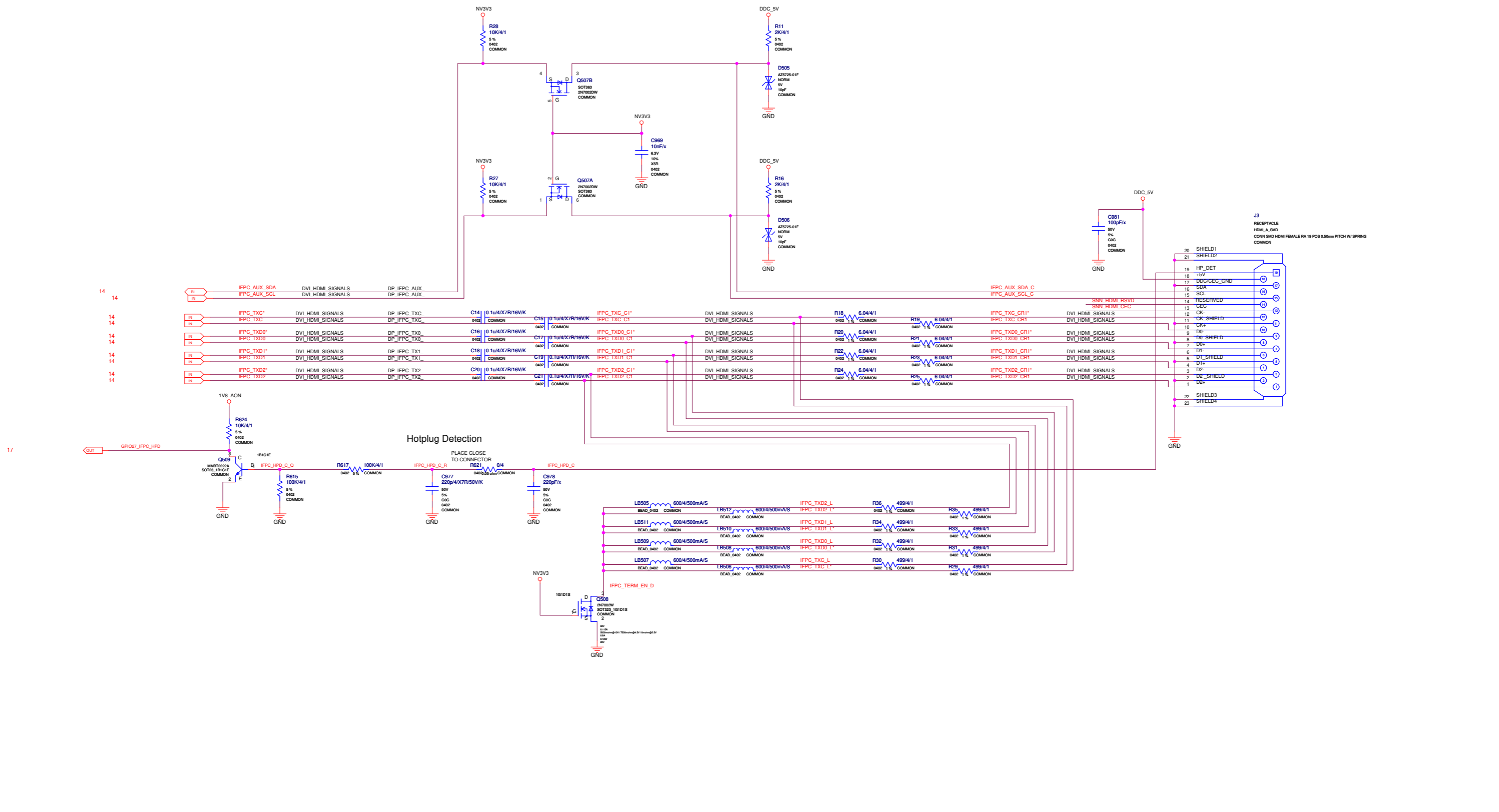


ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> IFPC
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IFPC HDMI



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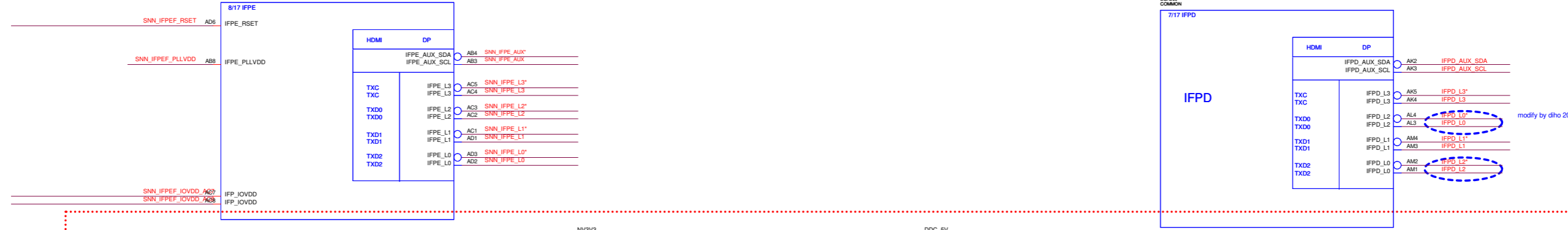
ASSEMBLY PAGE DETAIL -ASSEMBLY_DESCRIPTION- IFPC HDMI

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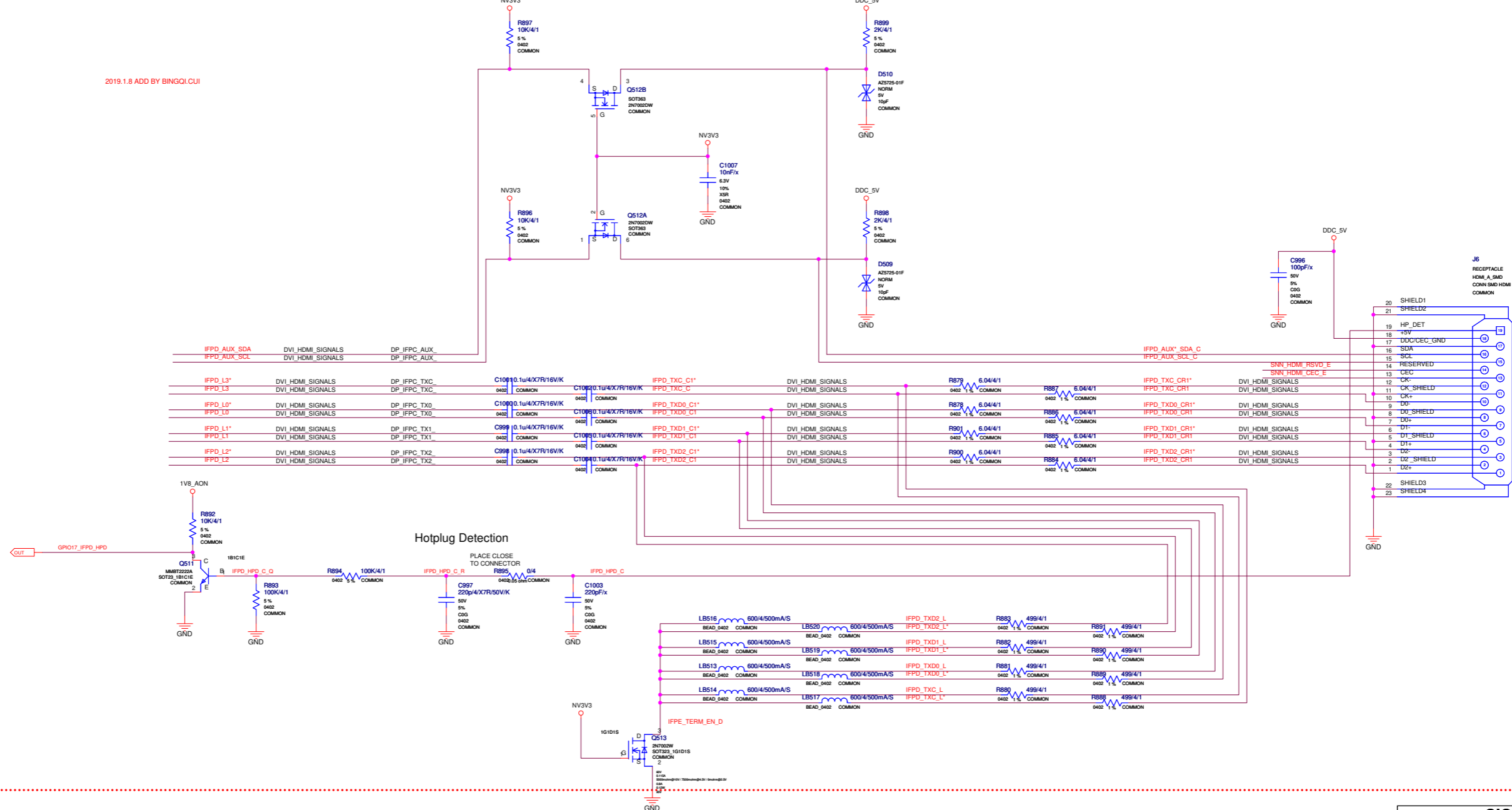
IFPDEF UNUSED

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 G1M
 TU117-400-A1
 BGA960
 COMMON

U_GPU_GB4D_128_BGA960-TU117-100_DT_TU117-DT-TU117-DT
 G1N
 TU117-400-A1
 BGA960
 COMMON

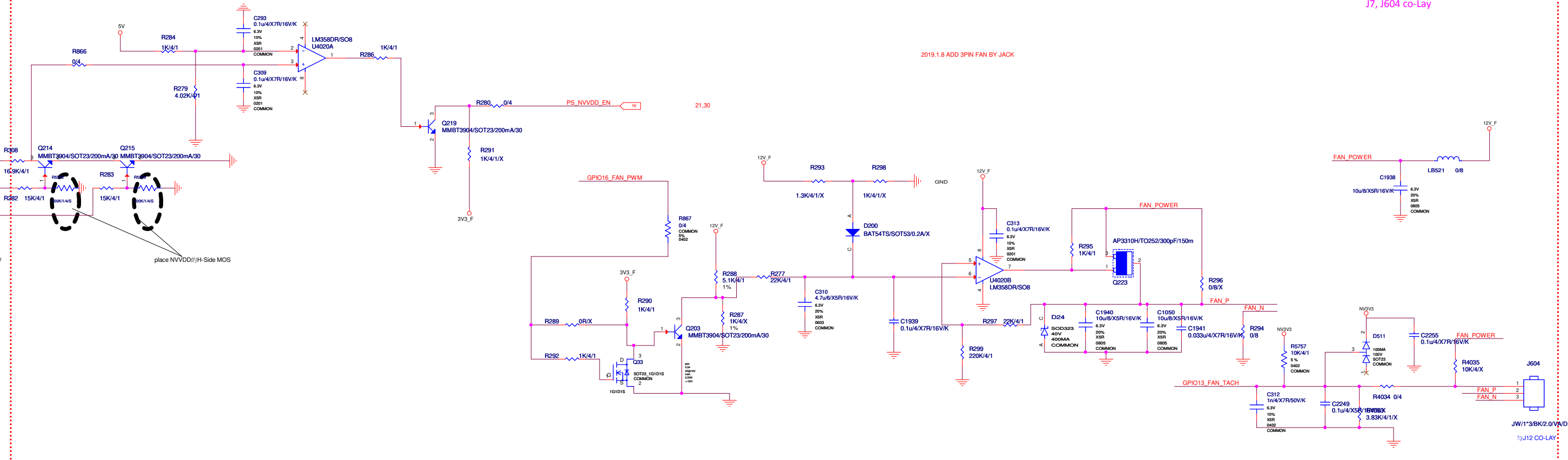
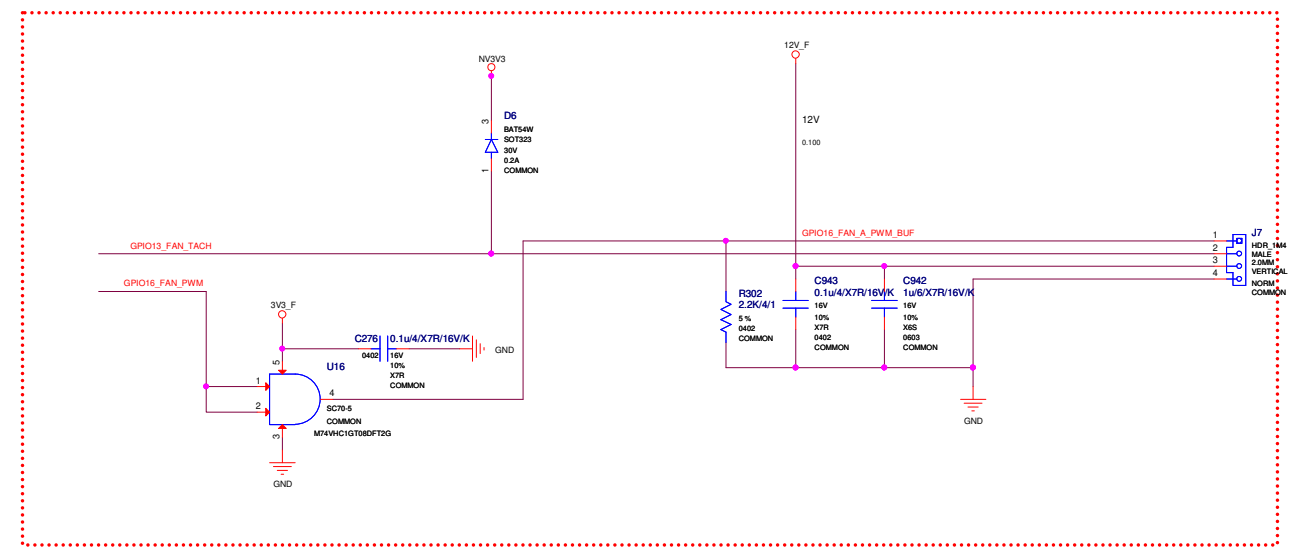
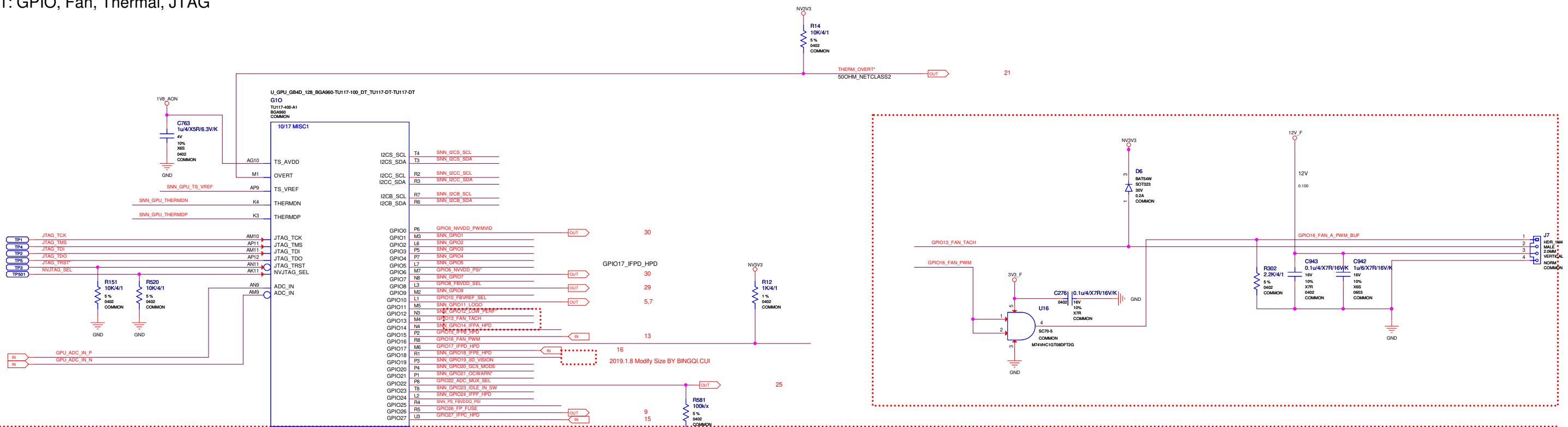


2019.1.8 ADD BY BINGQI.CUI



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MISC1: GPIO, Fan, Thermal, JTAG



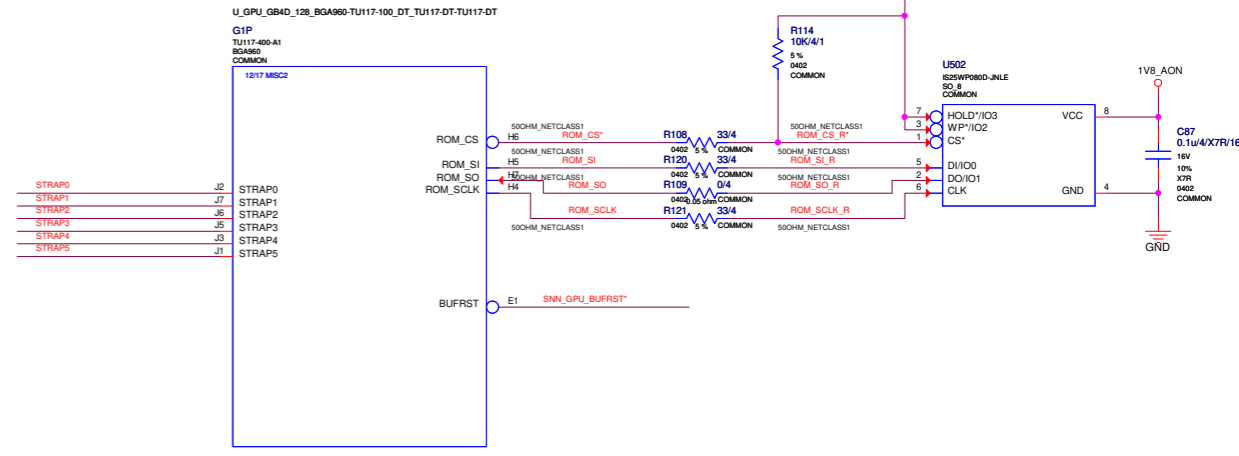
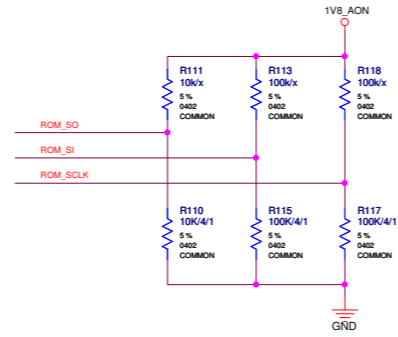
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ASSEMBLY PAGE DETAIL
 -ASSEMBLY_DESCRIPTION-
 MISC1: Fan, Thermal, JTAG, GPIO

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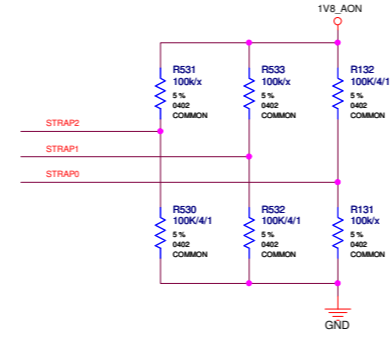
MISC2: ROM, XTAL, Straps

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	xxx1	FS_OVERT ENABLE	Default
L	L	M	xxx0	FS_OVERT DISABLE	

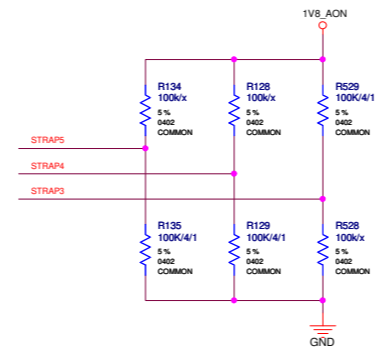


H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4G80325FC-HC25
L	L	H	0001	Micron 8Gb 256Mx32 MT51J256M32HF-80:B
L	H	L	0010	Hynix 8Gb 256Mx32 H5GC8H24AJR-R2C
L	H	H	0011	Hynix 8Gb 256Mx32 H5GQ8H24MJR-R4C
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

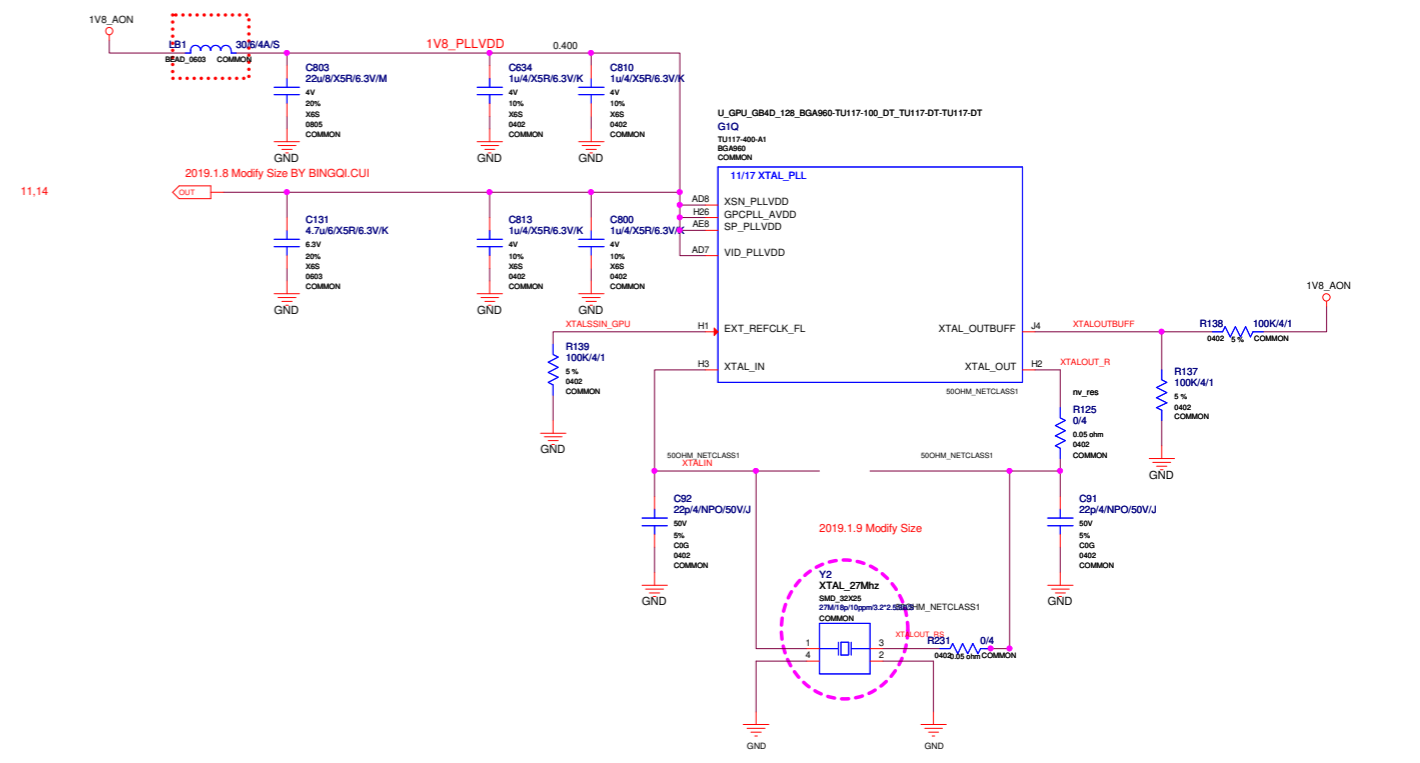
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- MISC2: ROM, XTAL, Straps
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GIGABYTE

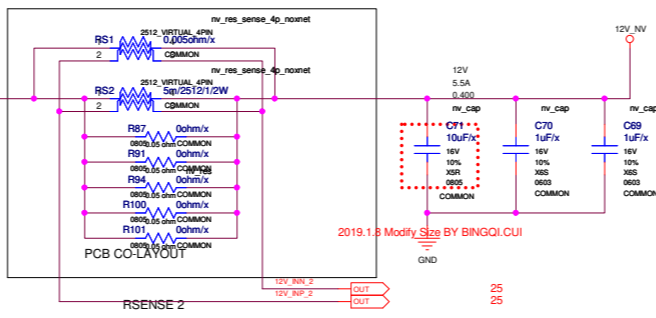
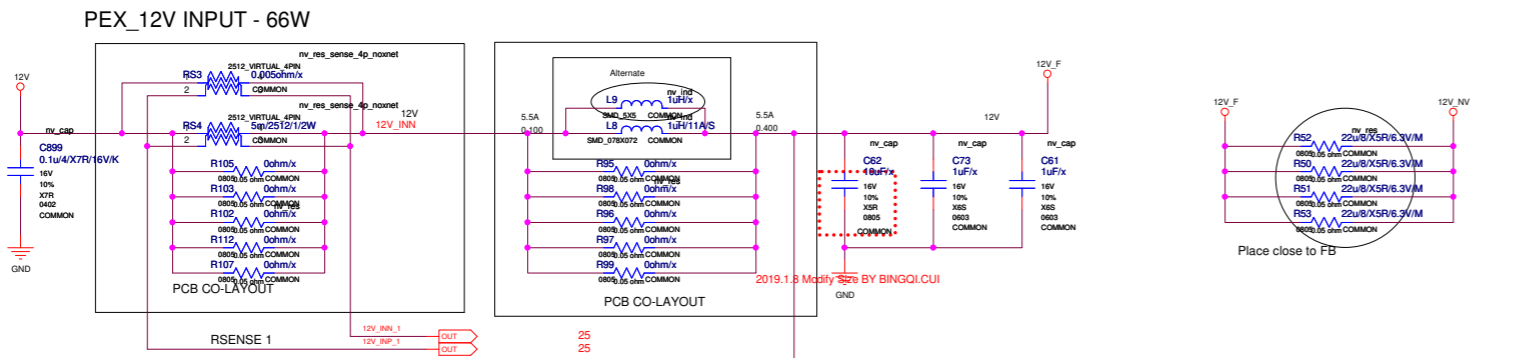
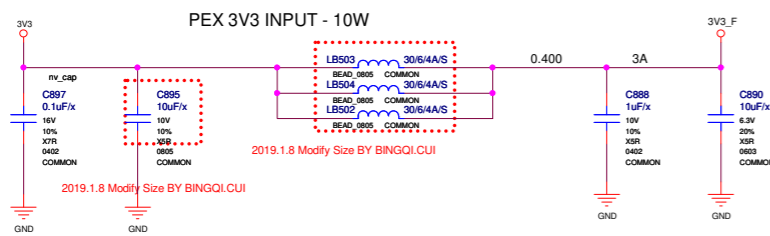
Title: PG174

Size: Custom Document Number: **GV-N16500C-4GD** Rev: 1.0

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Power Inputs and Filtering

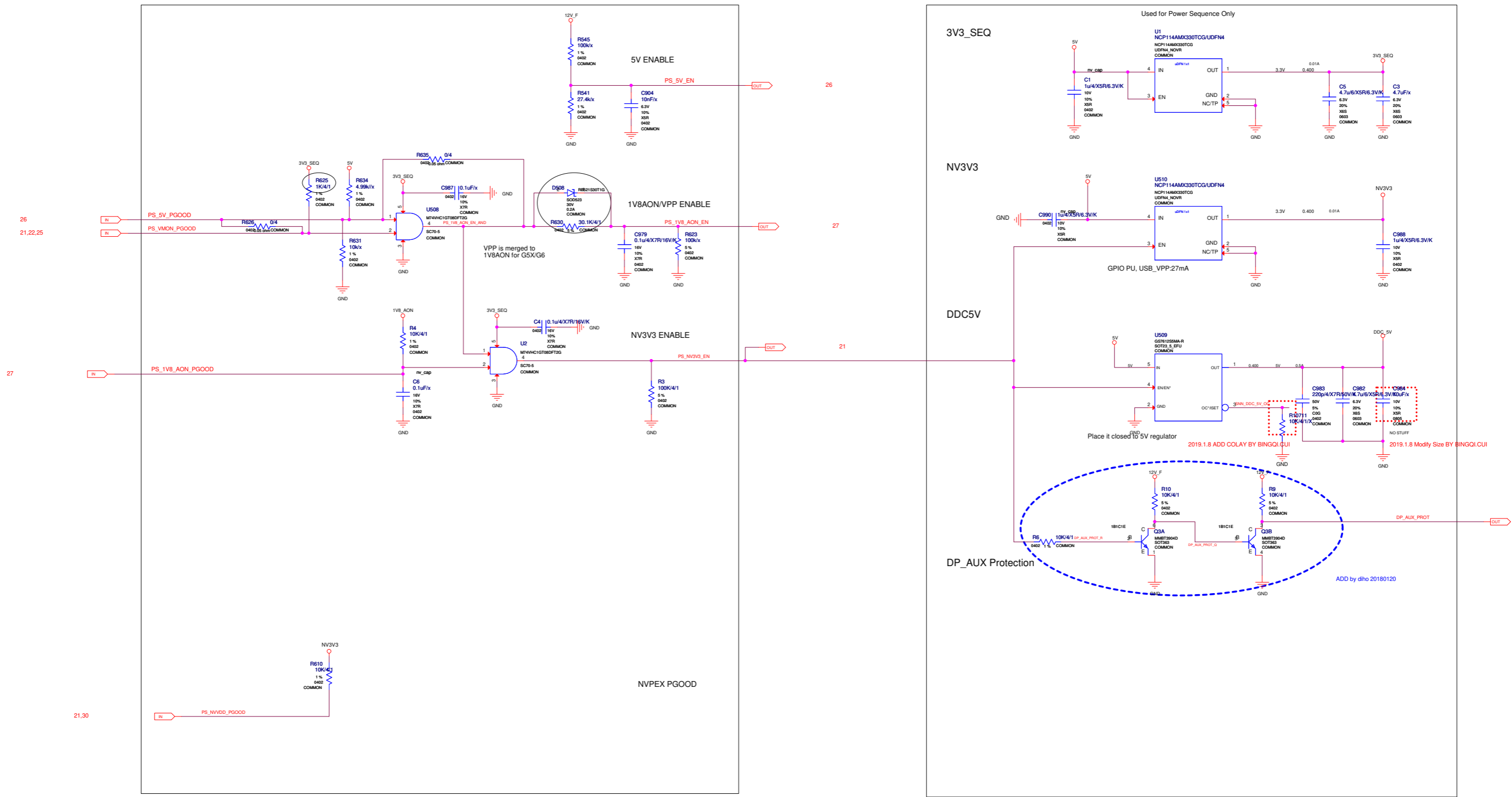


ASSEMBLY PAGE DETAIL -ASSEMBLY_DESCRIPTION- Power Inputs and Filtering

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GIGABYTE		
Title PG174		
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SEQ:5V,1V8,NV3V3 ENABLE



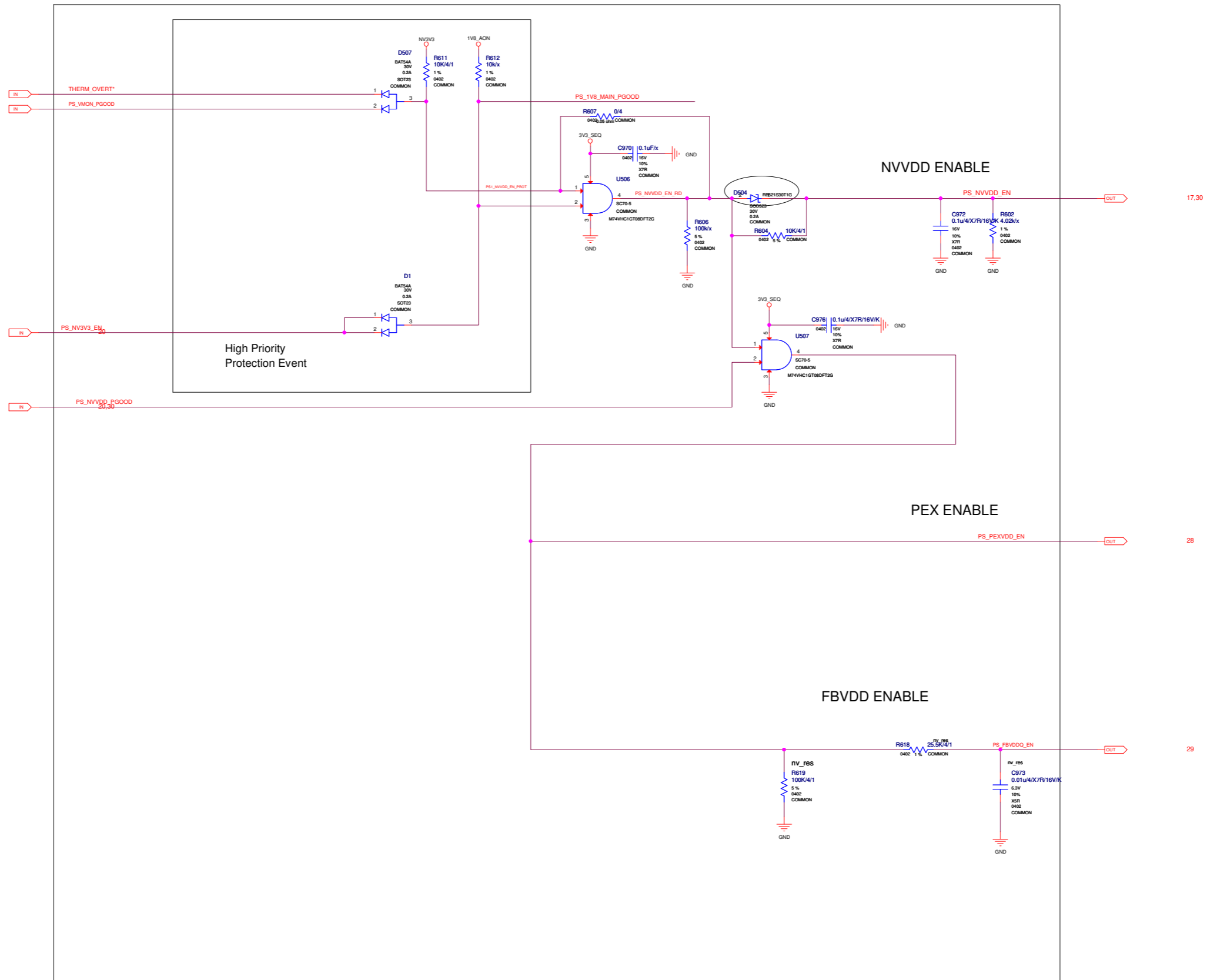
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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- SEQ: 5V, 1V8, NV3V3 ENABLE
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SEQ:NV,PEX,FB ENABLE

17
20,22,25



17,30

28

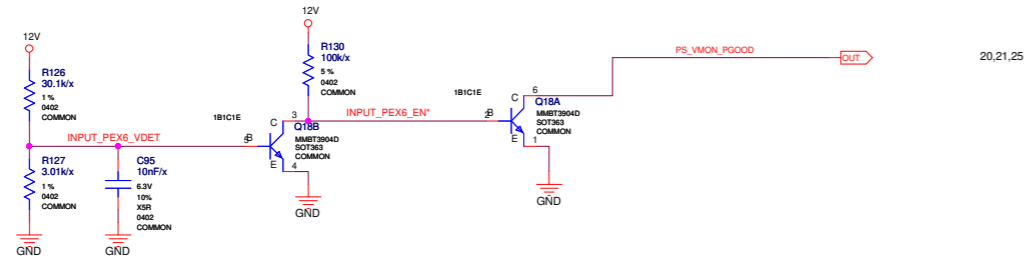
29

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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- SEQ: NV, PEX, FB ENABLE
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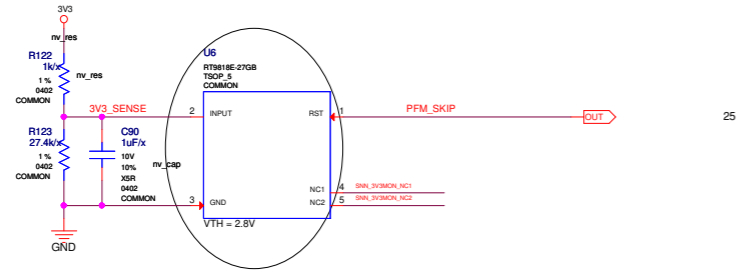
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SEQUENCE: Voltage Monitor



20,21,25

Route the trace to PEX Golden Finger



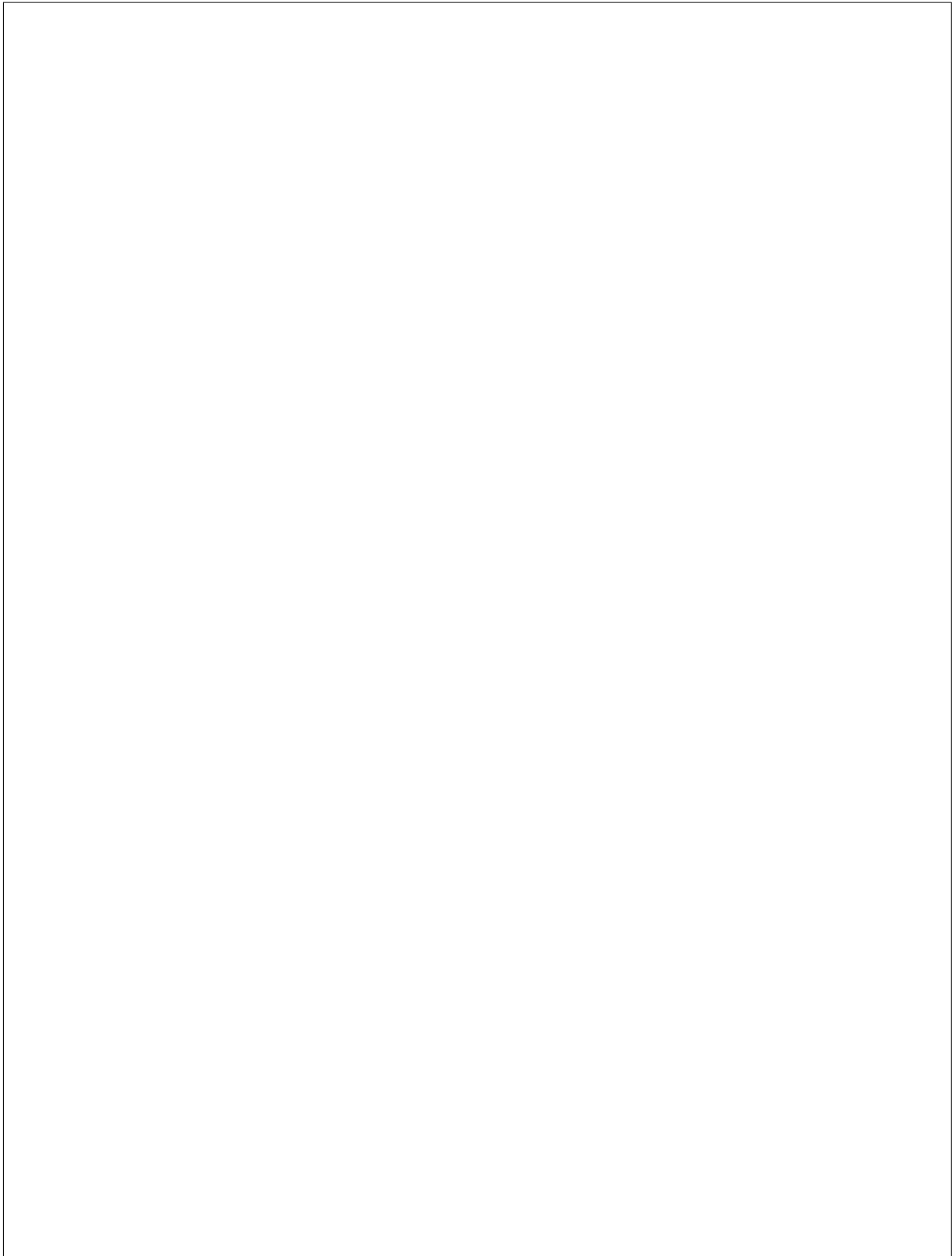
25

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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- SEQ: VOLTAGE MONITOR
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SEQUENCE:Discharge

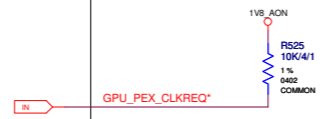


ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> SEQ. DISCHARGE
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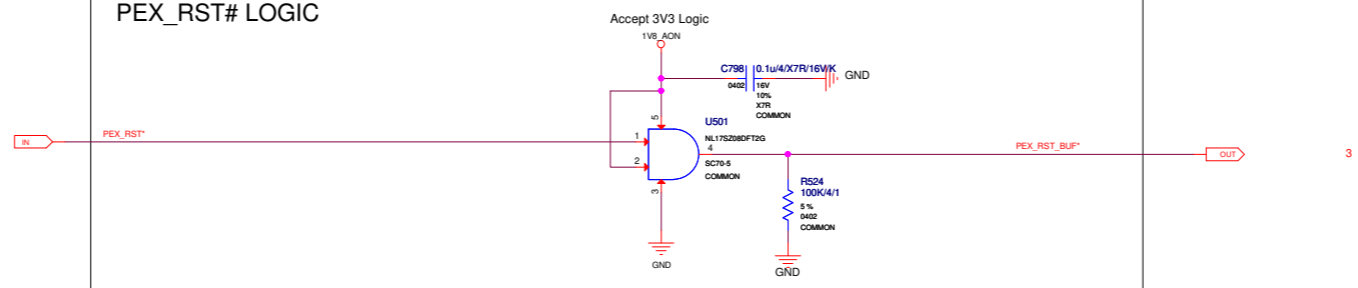
PEX_CLKREQ*



GPU_WAKE*



PEX_RST# LOGIC

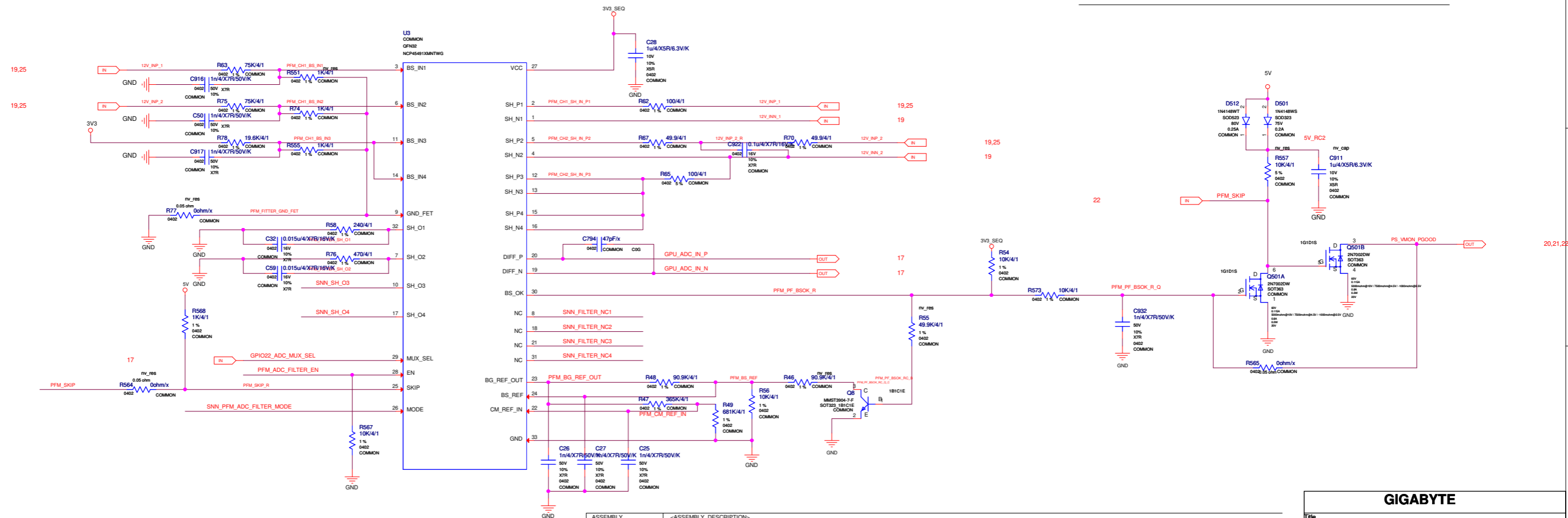


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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- SEQ: MISC
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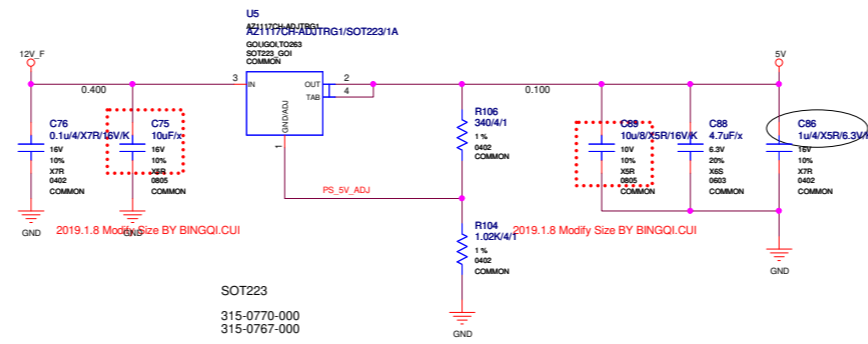
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PWR SENSE

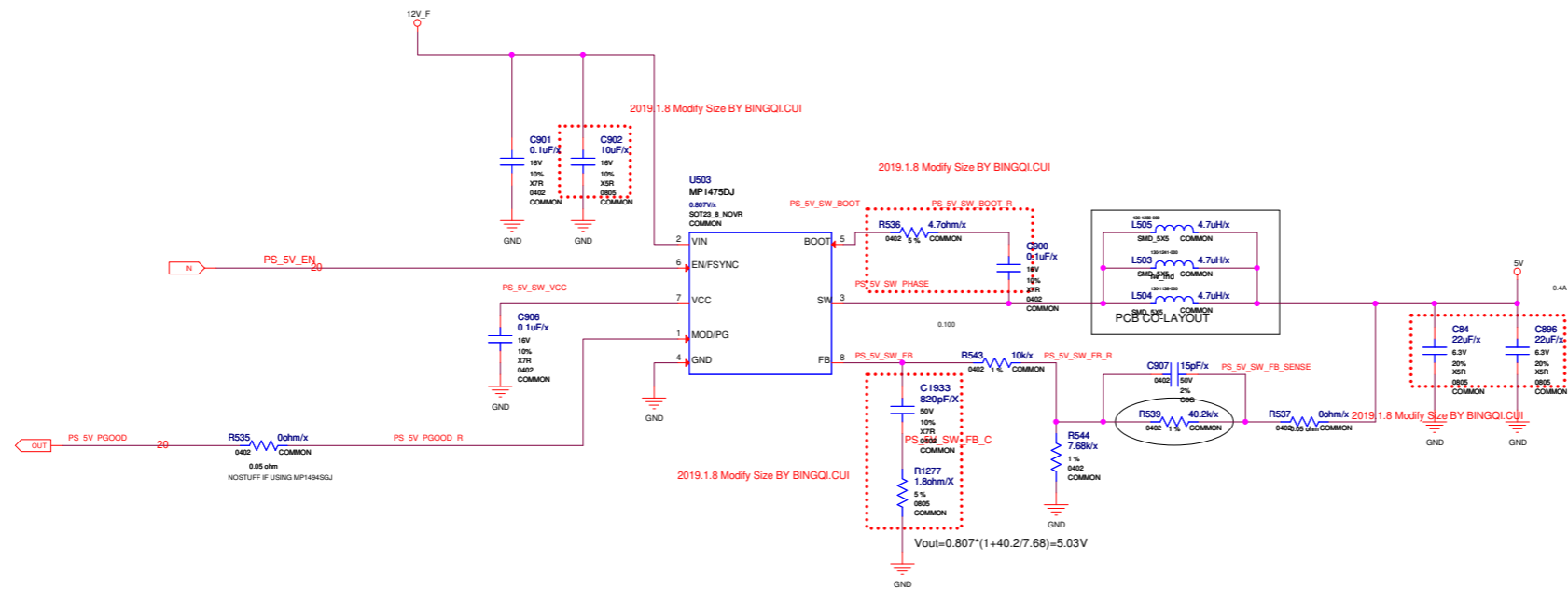


MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



$$V_{out} = 1.25 * (1 + 1020/340) + 60\mu A * 1020 = 5.06V$$



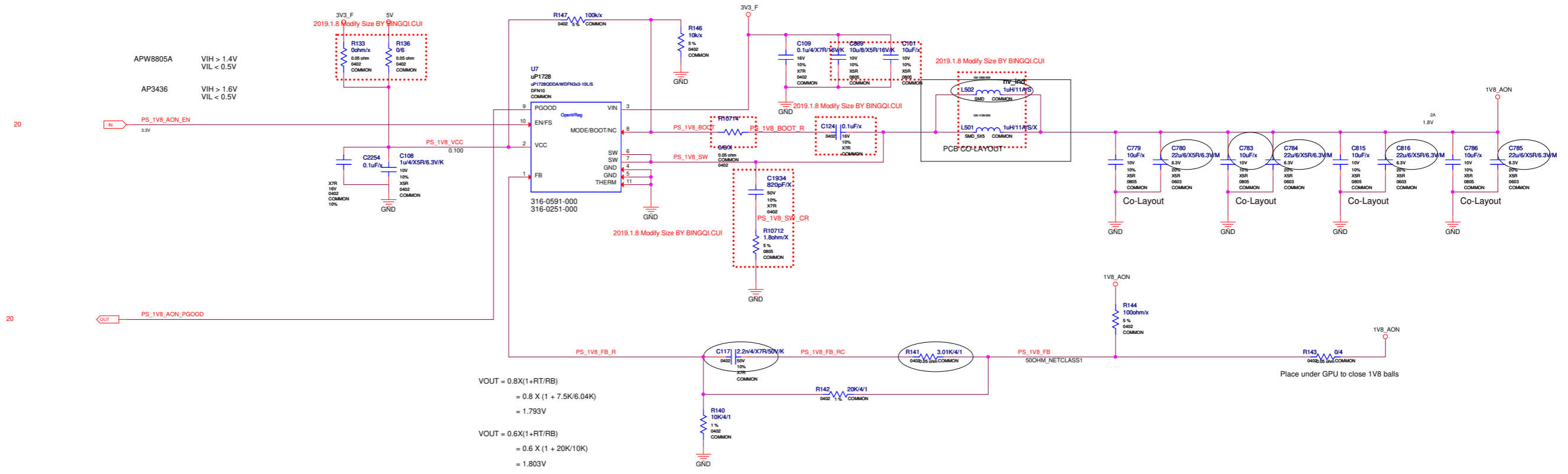
$$V_{out} = 0.807 * (1 + 40.2/7.68) = 5.03V$$

ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- PS: 5V
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PS: 1V8



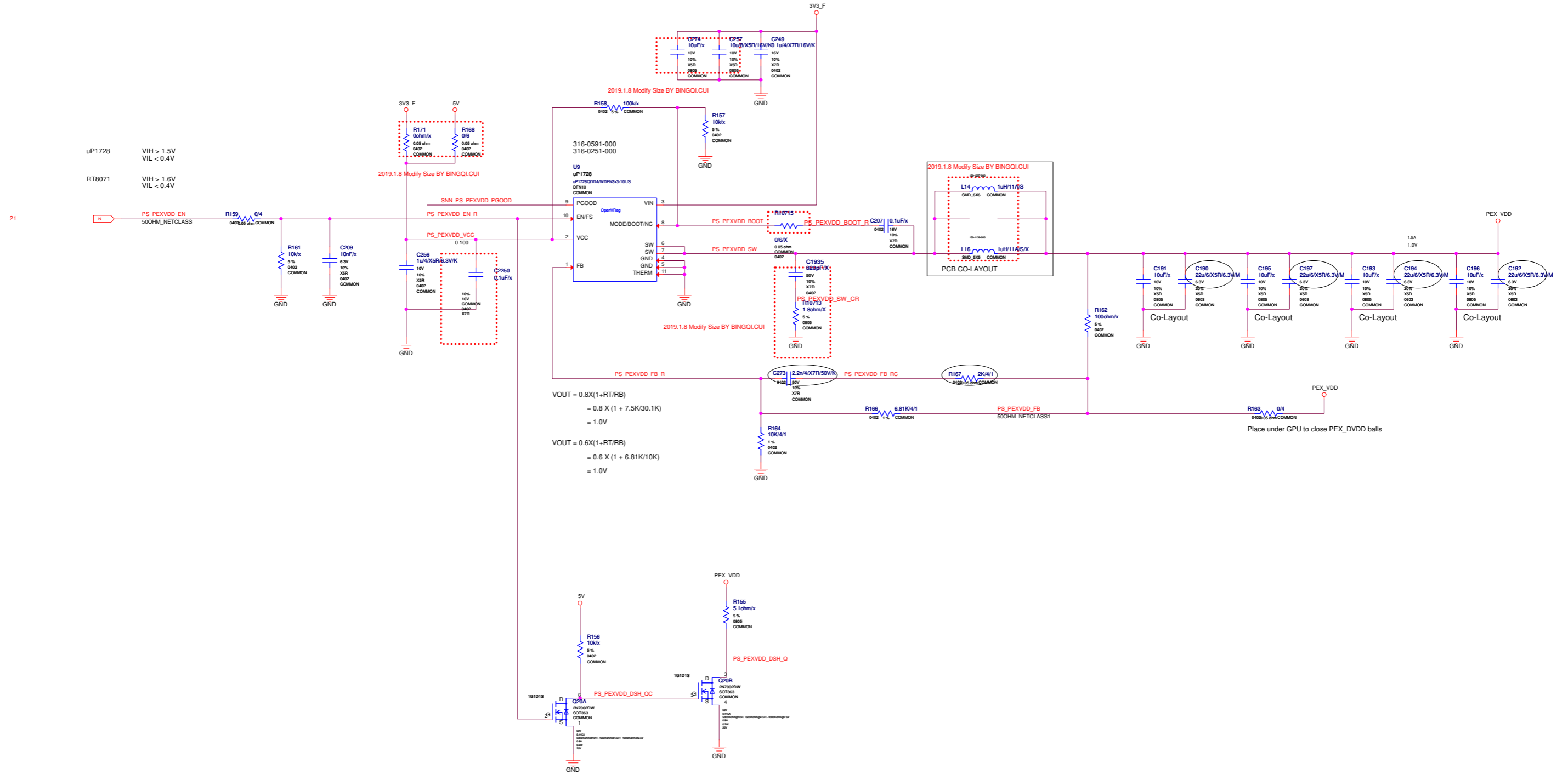
$$\begin{aligned}
 V_{OUT} &= 0.8 \times (1 + R_T/R_B) \\
 &= 0.8 \times (1 + 7.5K/6.04K) \\
 &= 1.793V \\
 V_{OUT} &= 0.6 \times (1 + R_T/R_B) \\
 &= 0.6 \times (1 + 20K/10K) \\
 &= 1.803V
 \end{aligned}$$

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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- PS: 1V8
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PS: PEXVDD

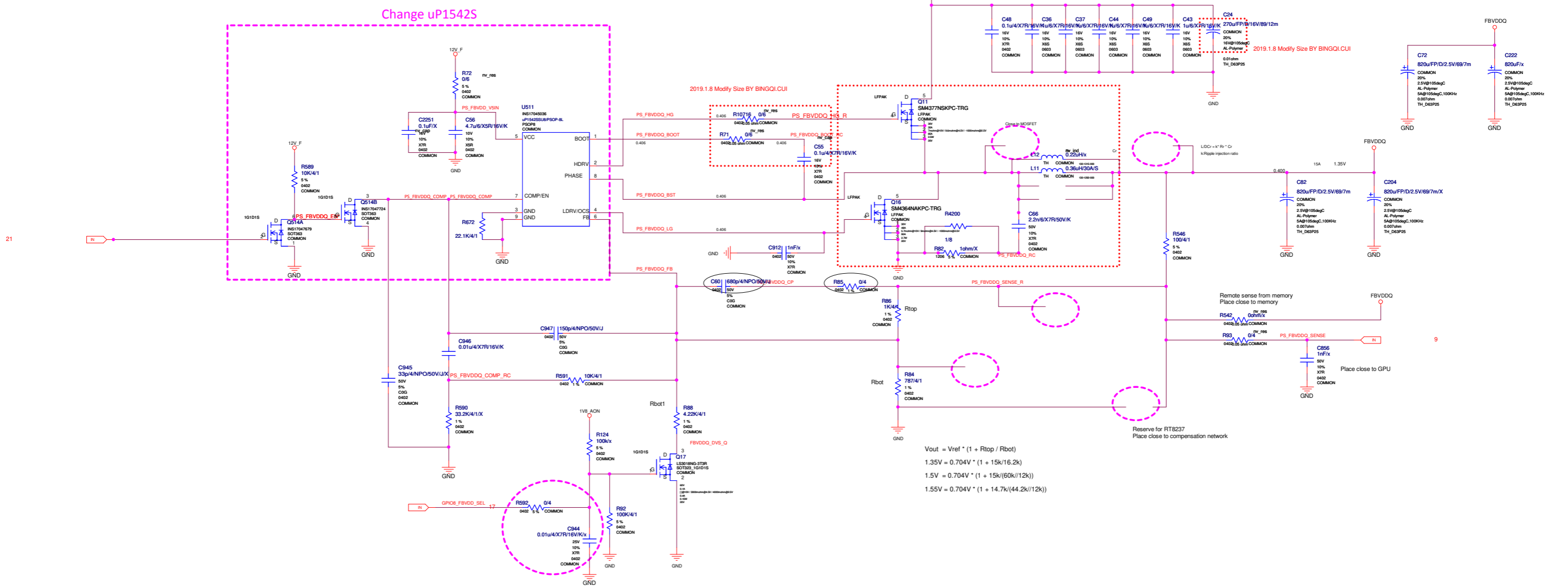


UP1728 VIH > 1.5V
 VIL < 0.4V
 RT8071 VIH > 1.6V
 VIL < 0.4V

ASSEMBLY PAGE DETAIL -ASSEMBLY_DESCRIPTION-
 PS: PEXVDD

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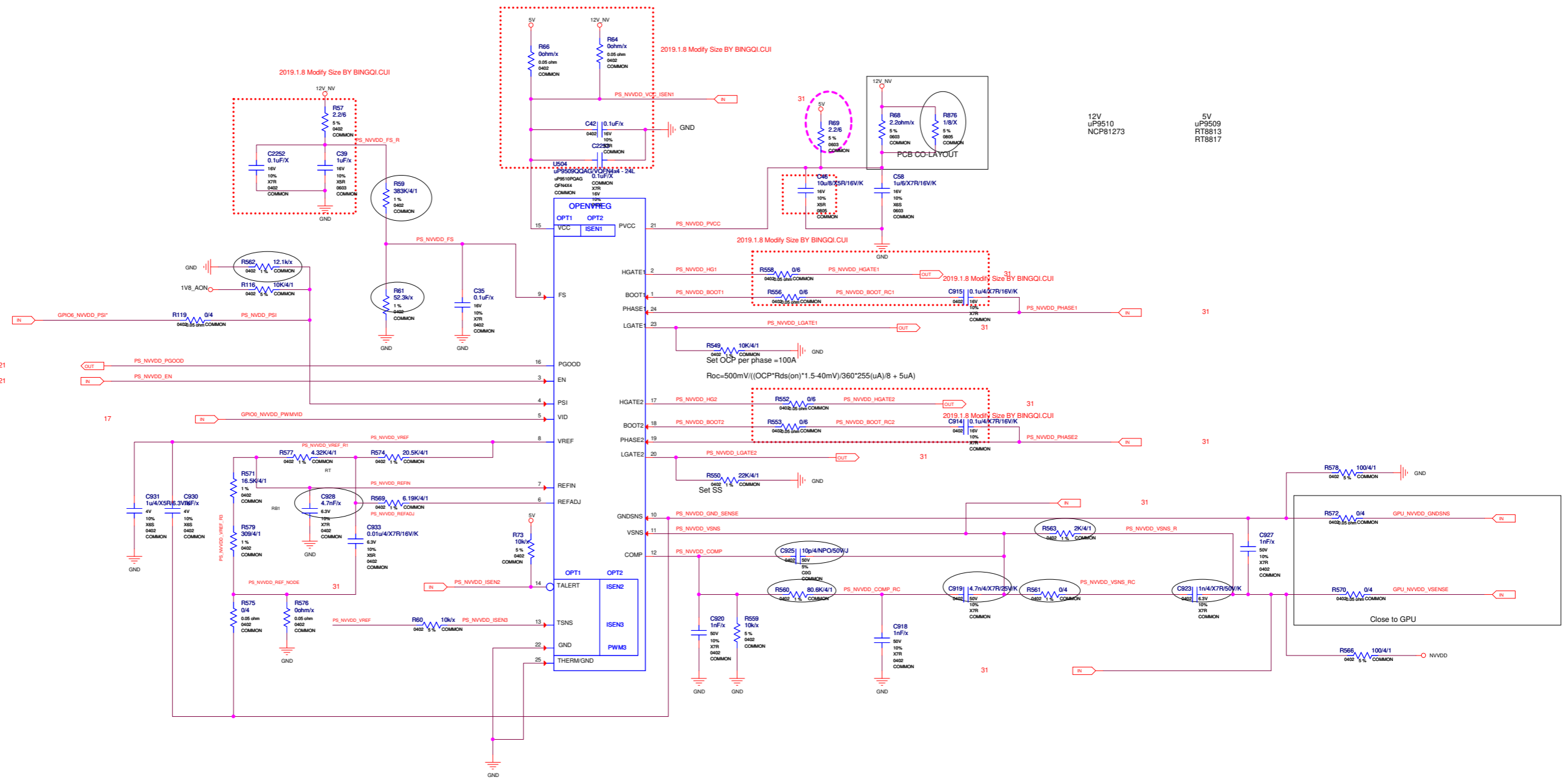
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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- PS: FBVDDQ
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PS: NVVDD OVR2+1

NCP81273 EN VIH >1.5V, VIL < 0.7V
 UP9509/10 EN VIH >1.2V, VIL < 0.6V
 RT8817A EN VIH >1.2V, VIL < 0.6V



NVPN	Name	PVCC(21)	VCC(15)
316-0478-000	NCP81273	12v	LDO_OUT
316-0476-000	up9510	12v	ISENSE
316-0484-000	RT8817A	5v	NC

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Title: PG174

Size: Custom

Document Number: **GV-N16500C-4GD**

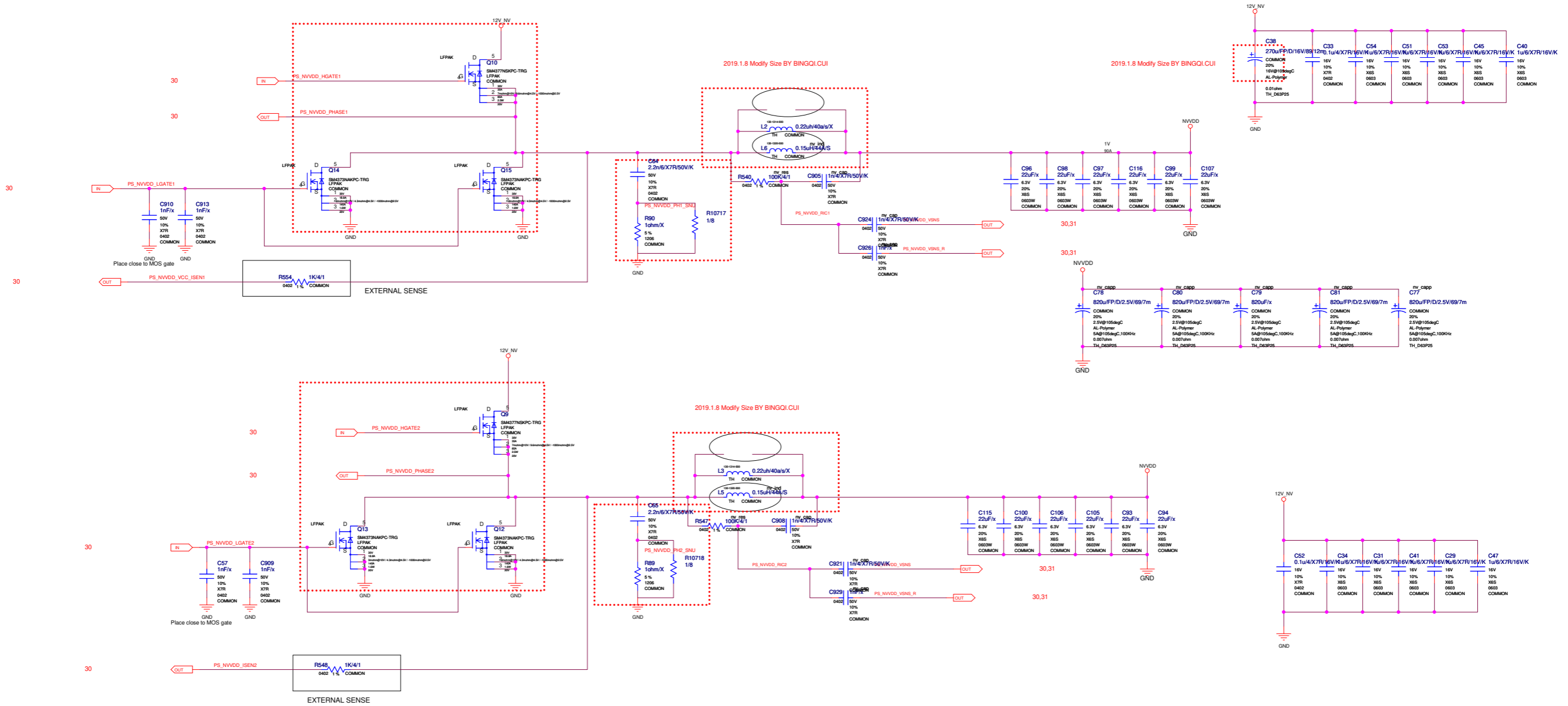
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PS: NVVDD Phase 1,2



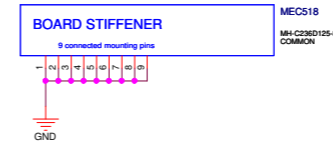
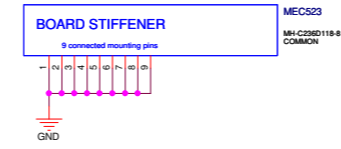
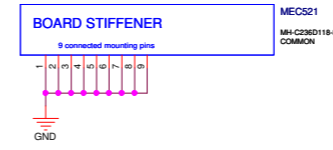
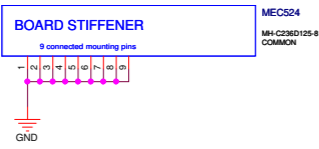
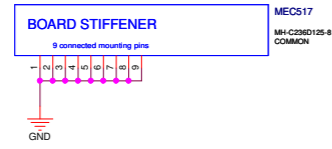
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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- PS: NVVDD Phase 1,2
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Mechanical: Bracket/Thermal Solution

Brackets:



ASSEMBLY PAGE DETAIL <ASSEMBLY_DESCRIPTION>
MECH: Bracket/Thermal

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History

Date	Modify
2019.01.04	First version