

# PG413 A00


## GP104 - 8GB GDDR5X, 256b, 256Mx32 Tall DVI-D + DP + DP + DP/HDMI + DP

### TABLE OF CONTENTS

Page	Description	Page	Description
1	Table of Contents	26	PS: FBVDD
2	Block Diagram	27	PS: NVVDD_OVR8
3	PCI Express	28	PS: Blank Page
4	MEMORY: GPU Partition A/B	29	PS: NVVDD Phase 1-4
5	MEMORY: FBA[31:0]	30	PS: NVVDD Phase 5 & 6
6	MEMORY: FBA[63:32]	31	PS: Blank Page
7	MEMORY: FBB[31:0]	32	PS: Dynamic Power Balance Phases
8	MEMORY: FBB[63:32]	33	PS: Dynamic Power Balance Logic
9	MEMORY: GPU Partition C/D	34	PS: NV3V3, NV12V
10	MEMORY: FBC[31:0]	35	PS: Inputs, Filtering, and Monitoring
11	MEMORY: FBC[63:32]	36	PS: Shutdown and Sequencing
12	MEMORY: FBD[31:0]	37	PS: 12V Current Steering PSI Control and LED
13	MEMORY: FBD[63:32]	38	MECH: Bracket/Thermal
14	GPU PWR and GND		
15	GPU Decoupling		
16	IFPAB DVI-D-DL		
17	IFPE DP		
18	IFPEF DP		
19	IFPC HDMI 2.0/DP		
20	IFPD DP		
21	MIOA/B Interface and Frame Lock		
22	MISC1; Fan, Thermal, JTAG, GPIO, Stereo		
23	MISC2: ROM, XTAL, Straps		
24	PS: 1V8, 1V8_AON		
25	PS: 5V, PEX_VDD		

<b>GIGABYTE™</b>			
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Date: Friday, December 06, 2016	Sheet: 1	of	50

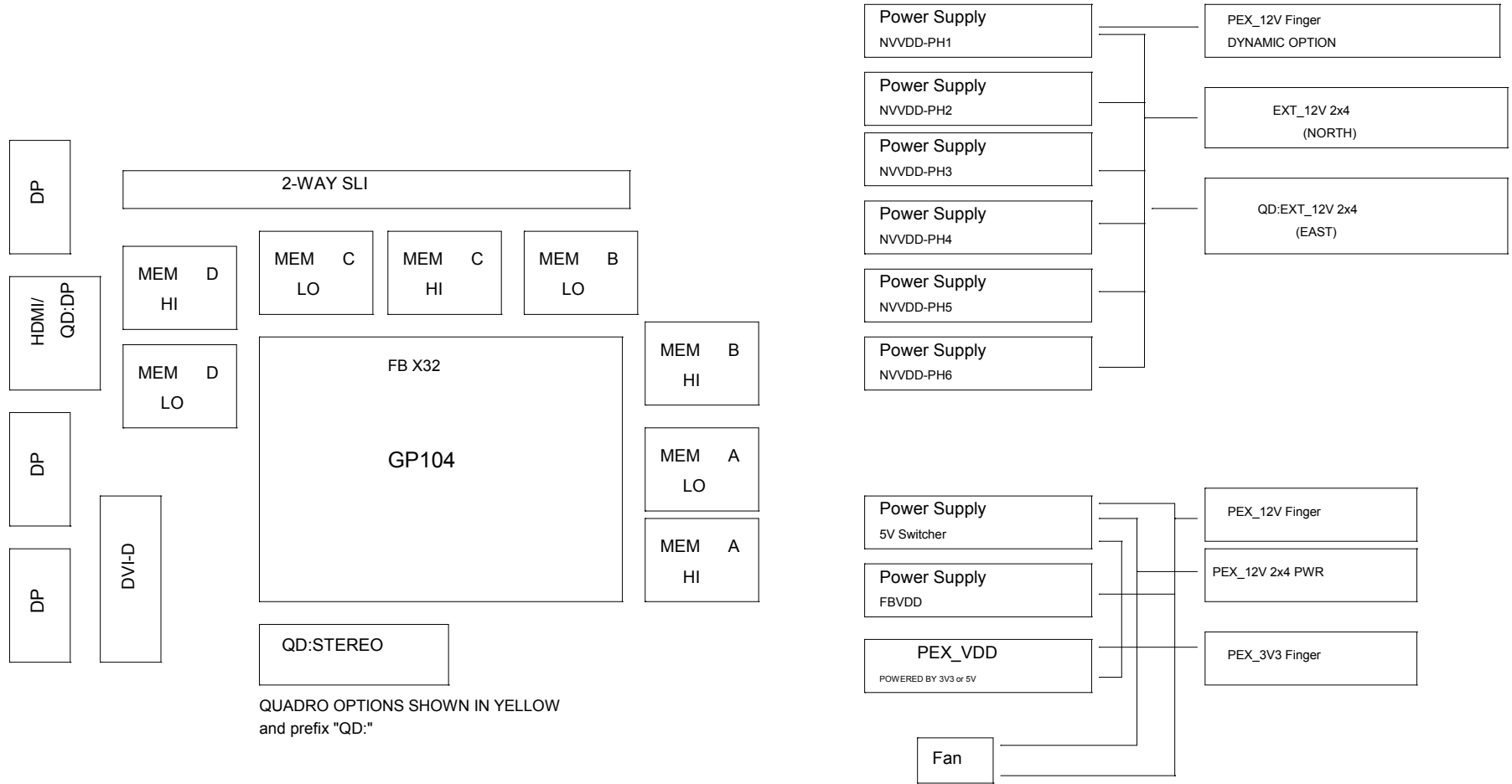
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NV_PN	600-1G413-BASE-000	T OF 38
PCB REV	1G413A00	PAGE
BCM REV	A	DATE
		25-MAR-2016

ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	Table of Contents

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Friday, December 08, 2016 Sheet 2 of 50

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1V\_PN 600-1G413-BASE-000

PCB REV 1G413-ADD PAGE 2 OF 38

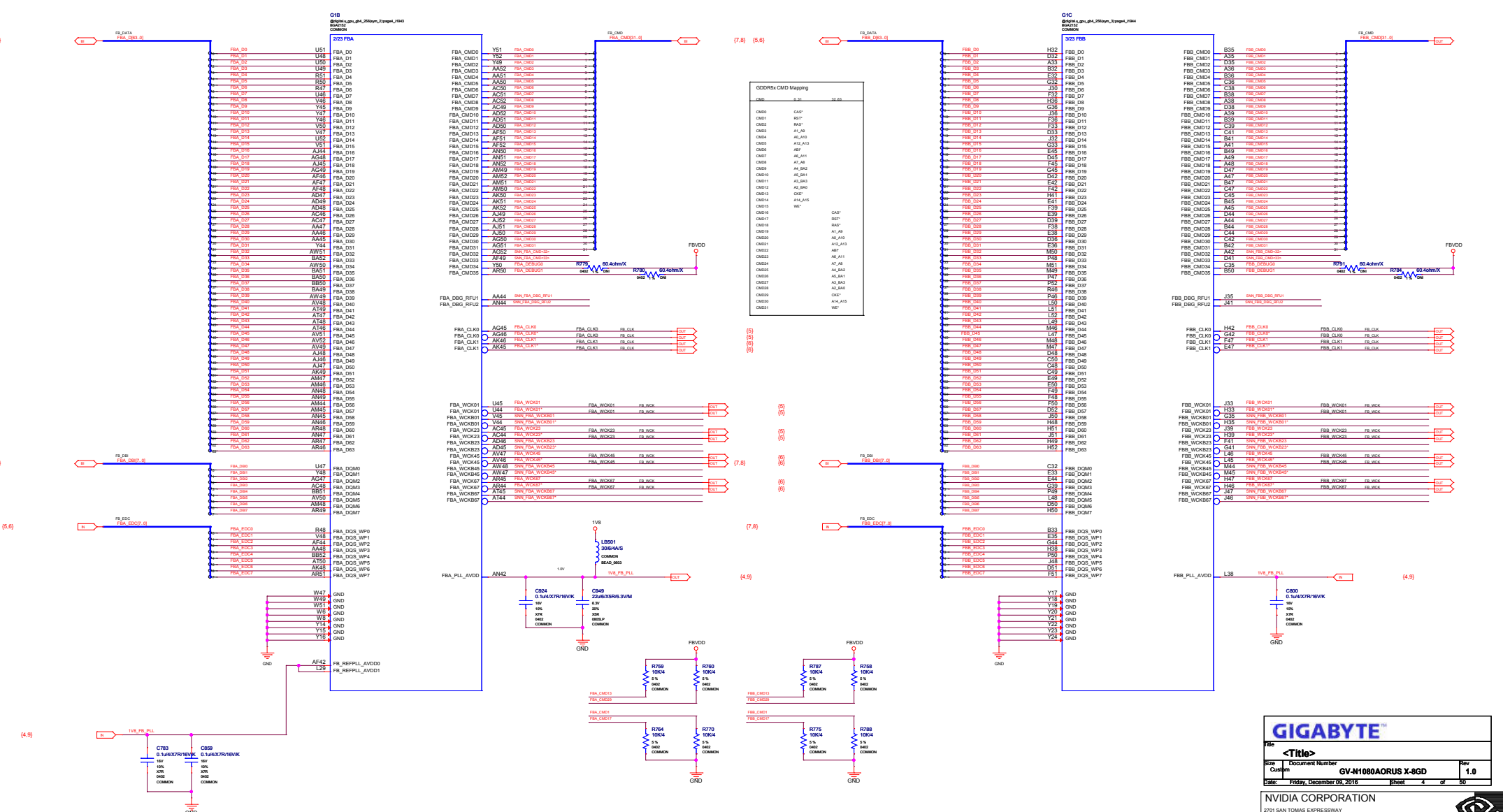
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GDDR5x CMD Mapping

Cmd	Bit	Bit
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0x01	RT*	
0x02	RA*	
0x03	AL*	
0x04	AL*	
0x05	AP*	
0x06	AL*	
0x07	AL*	
0x08	AL*	
0x09	AL*	
0x0A	AL*	
0x0B	AL*	
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Date: Friday, December 09, 2016 Sheet: 4 of 50

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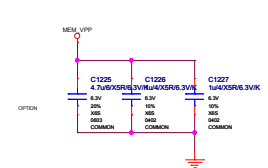
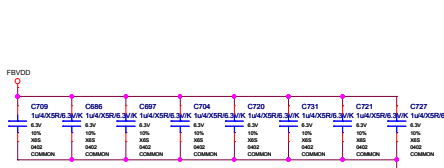
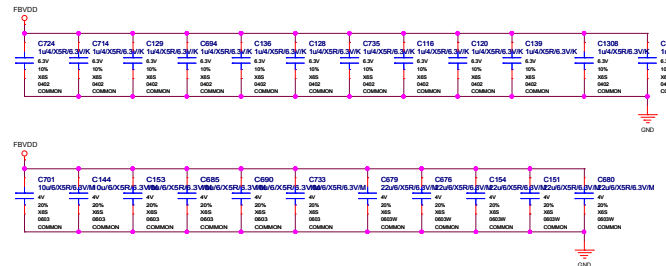
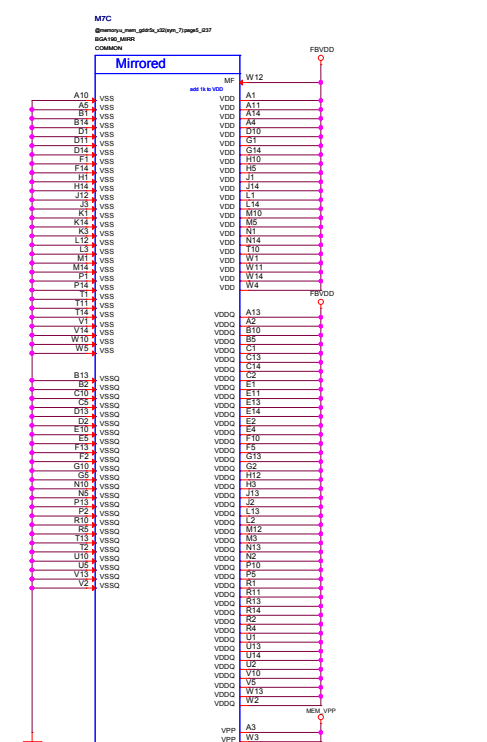
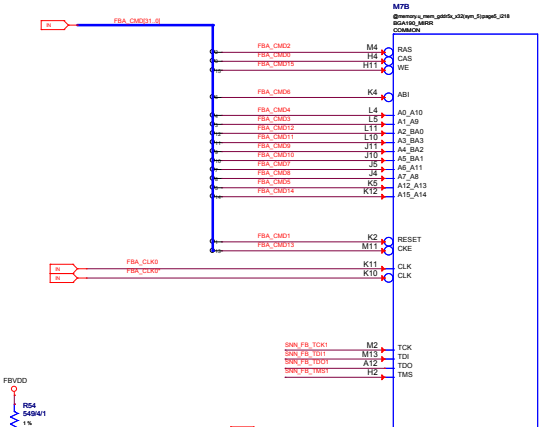
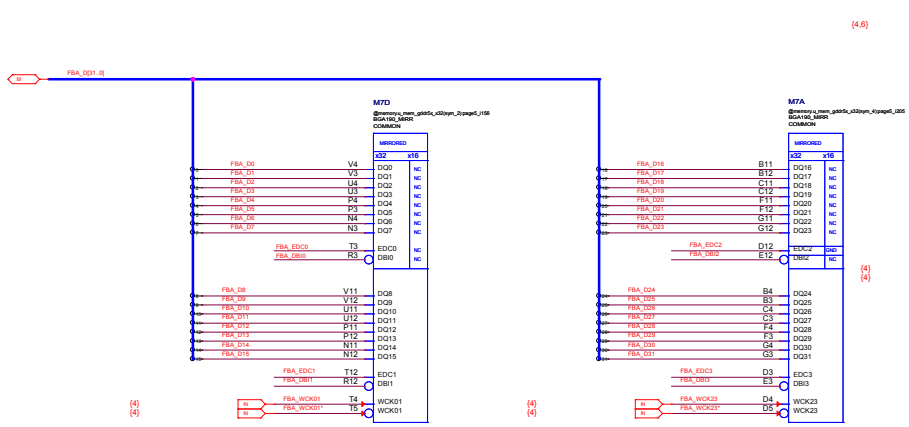
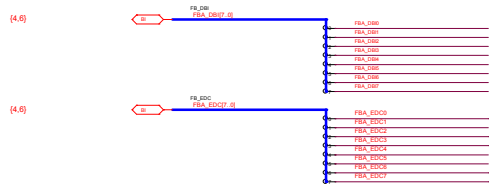
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Model: **600-1G413-BASE-000**

PCB REV: 1G413-000 PAGE: 4 OF 38  
SOM REV: A DATE: 28-MAR-2016

ASSEMBLY DESCRIPTION: MEMORY: GPU Partition A/B

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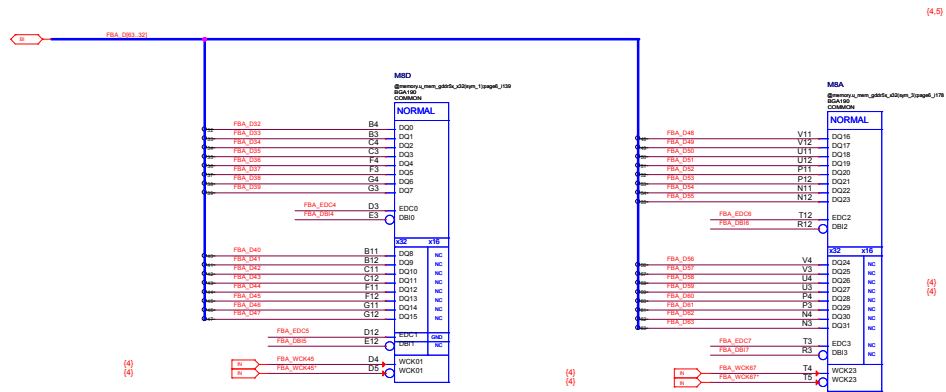
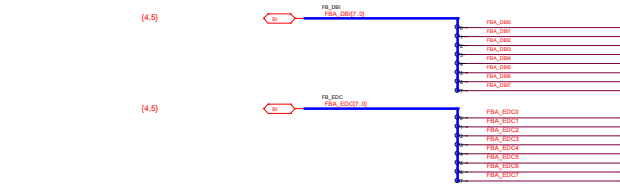
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 Date: **Friday, December 09, 2016** Sheet **5** of **10**

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PCB REV	1G413-ADD	PAGE	5 OF 38
ECN REV	A	DATE	25-MAR-2016

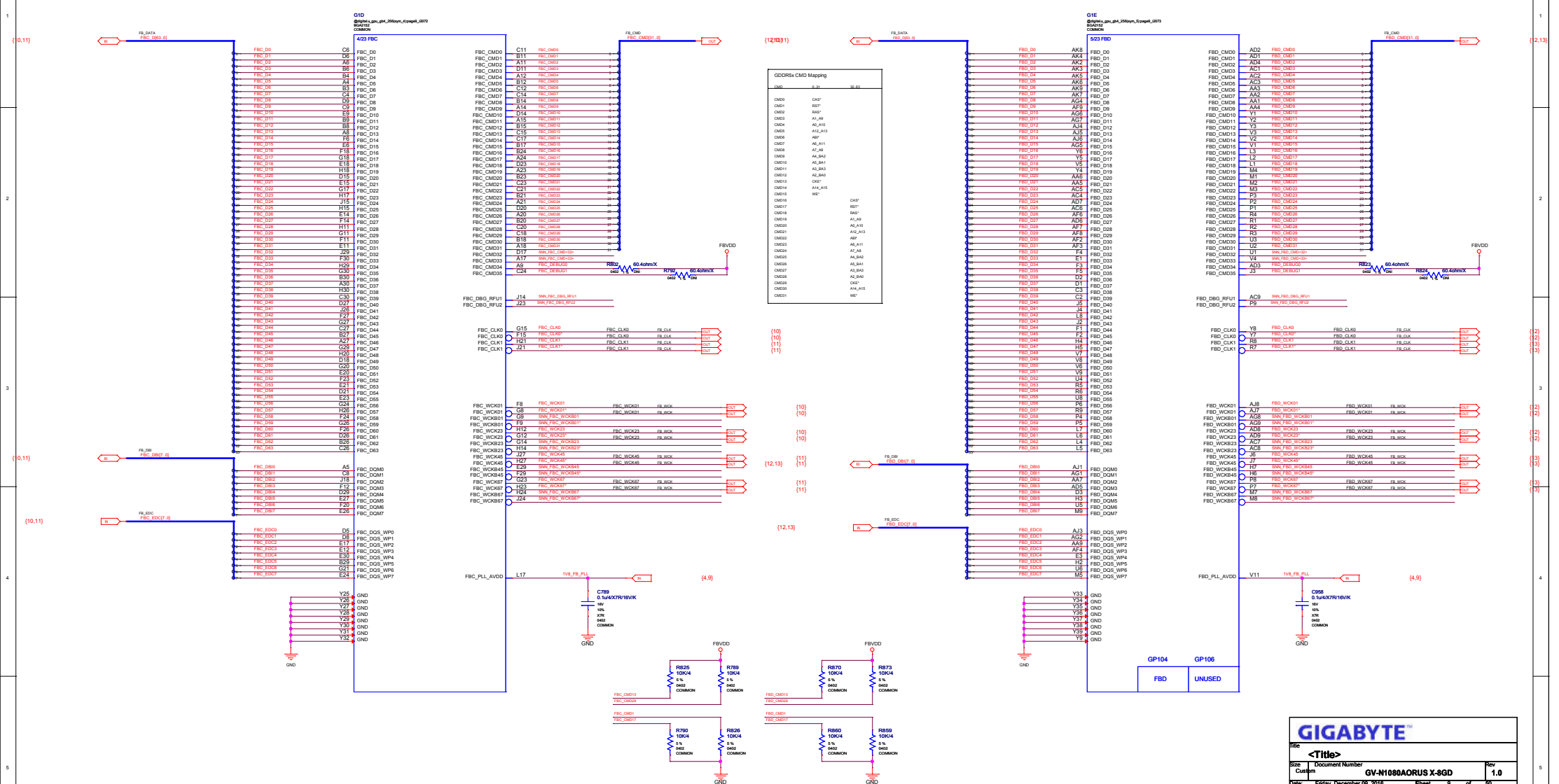
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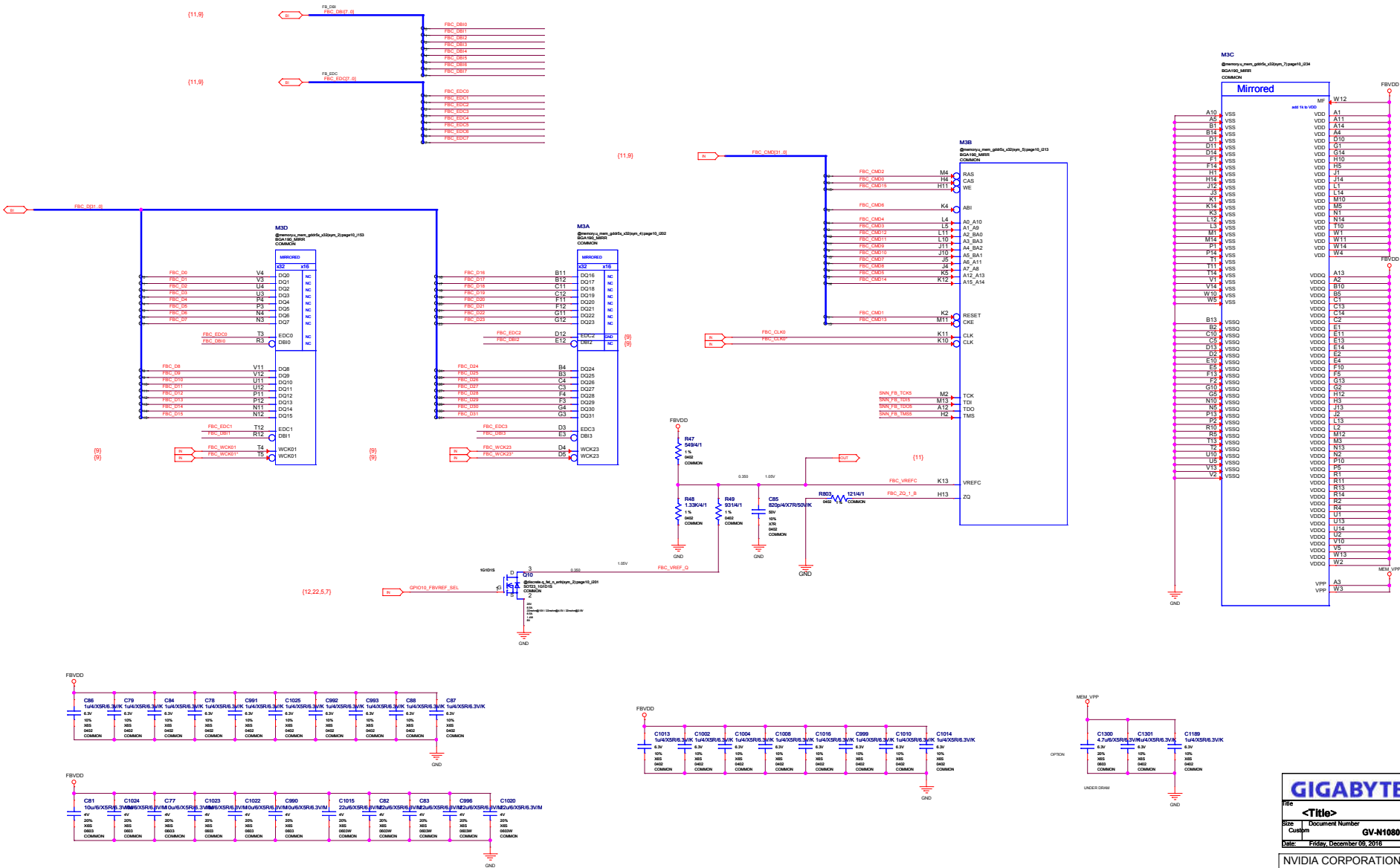
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Size: **GV-N1080AORUS X-8GD** Rev: **1.0**

Date: **Friday, December 05, 2016** Sheet: **9** of **50**

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Part Number: **600-1G413-BASE-000**

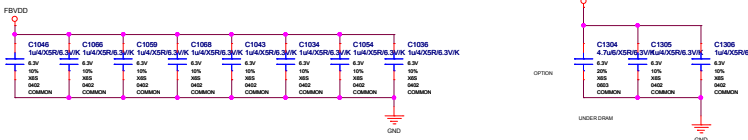
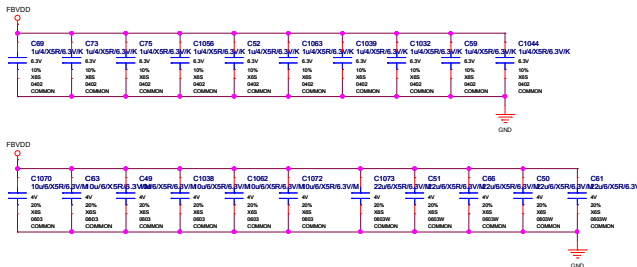
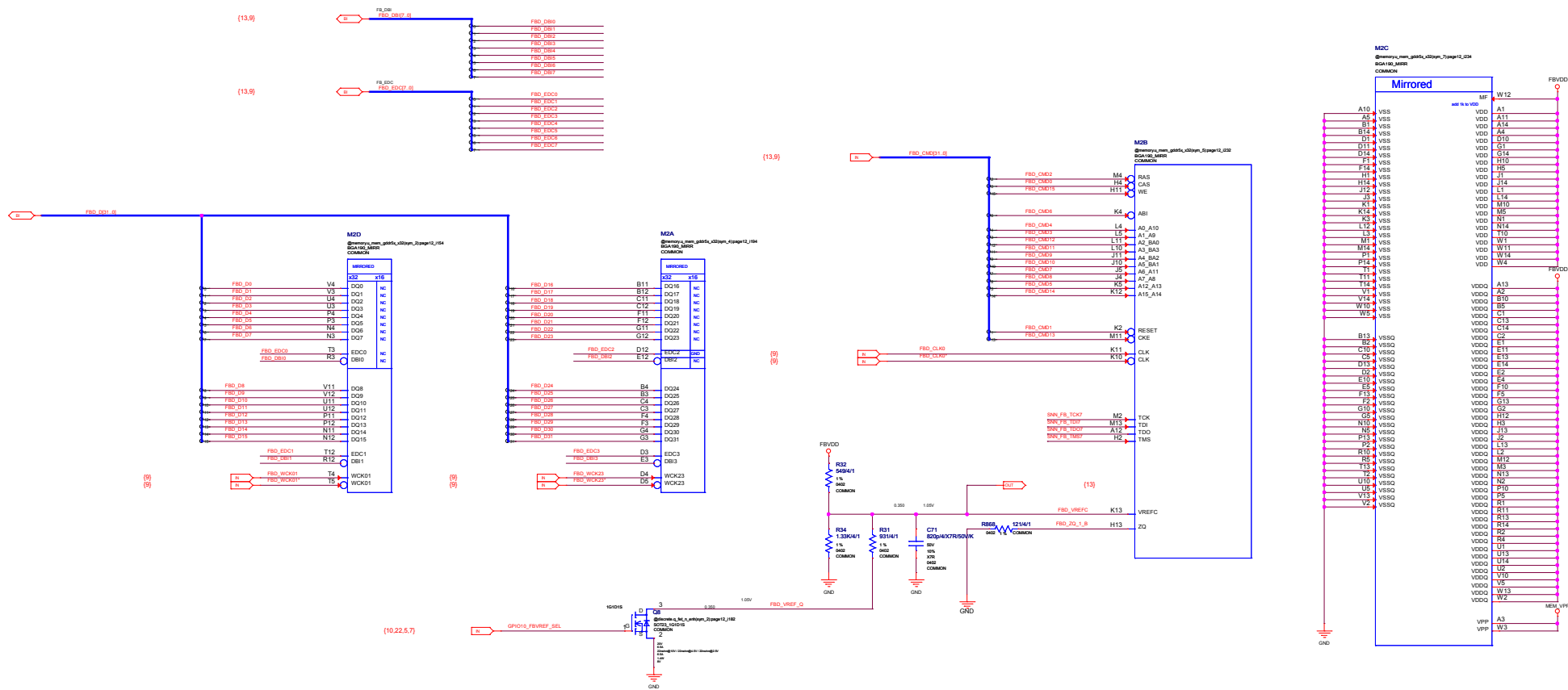


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**GIGABYTE**  
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 Date: Friday, December 09, 2016 Sheet: 10 of 50

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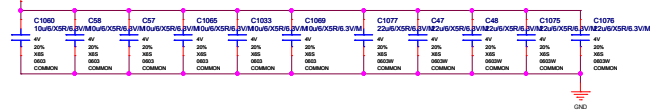
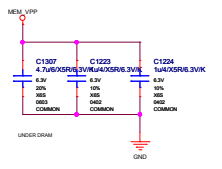
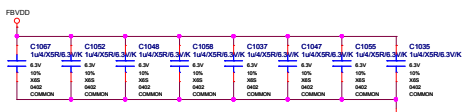
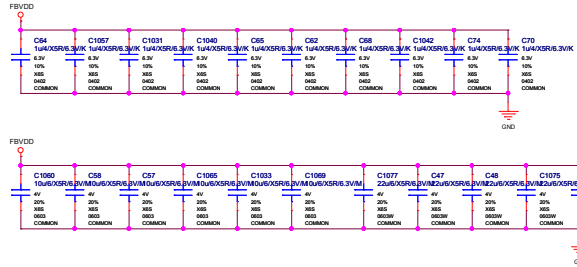
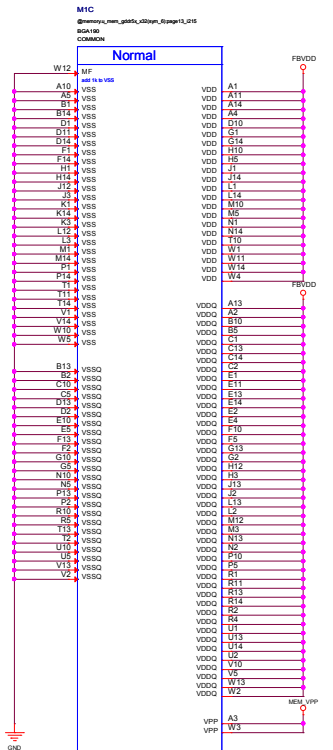
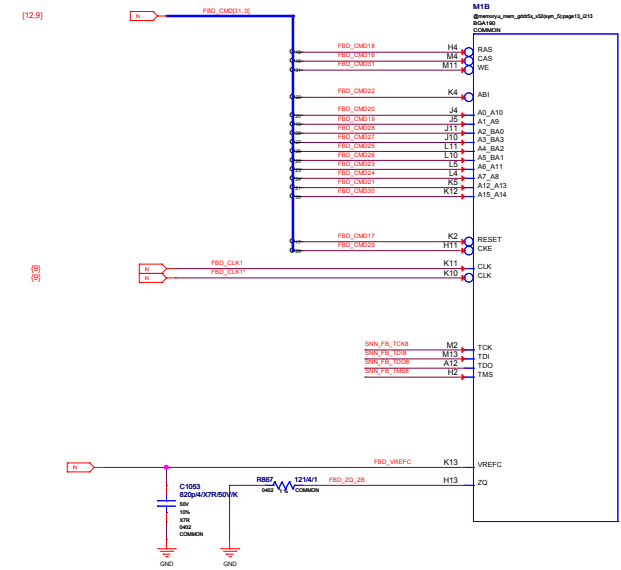
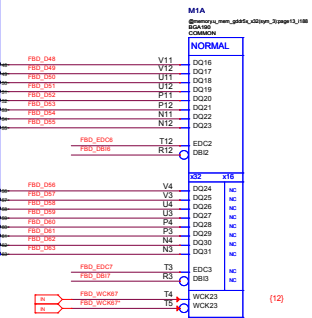
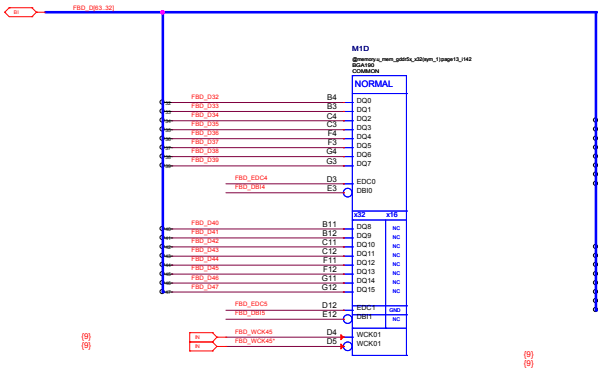
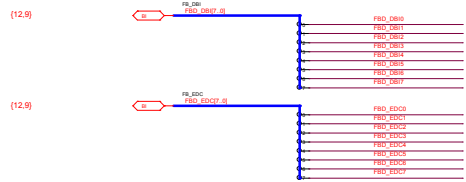
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Date	Friday, December 09, 2016	Sheet 12 of 50

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14V_PN	600-1G413-BASE-000	
PCB REV	1G413-A00	PAGE 12 OF 38
ECOM REV	A	DATE 25-MAR-2016

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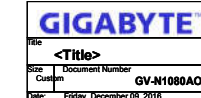
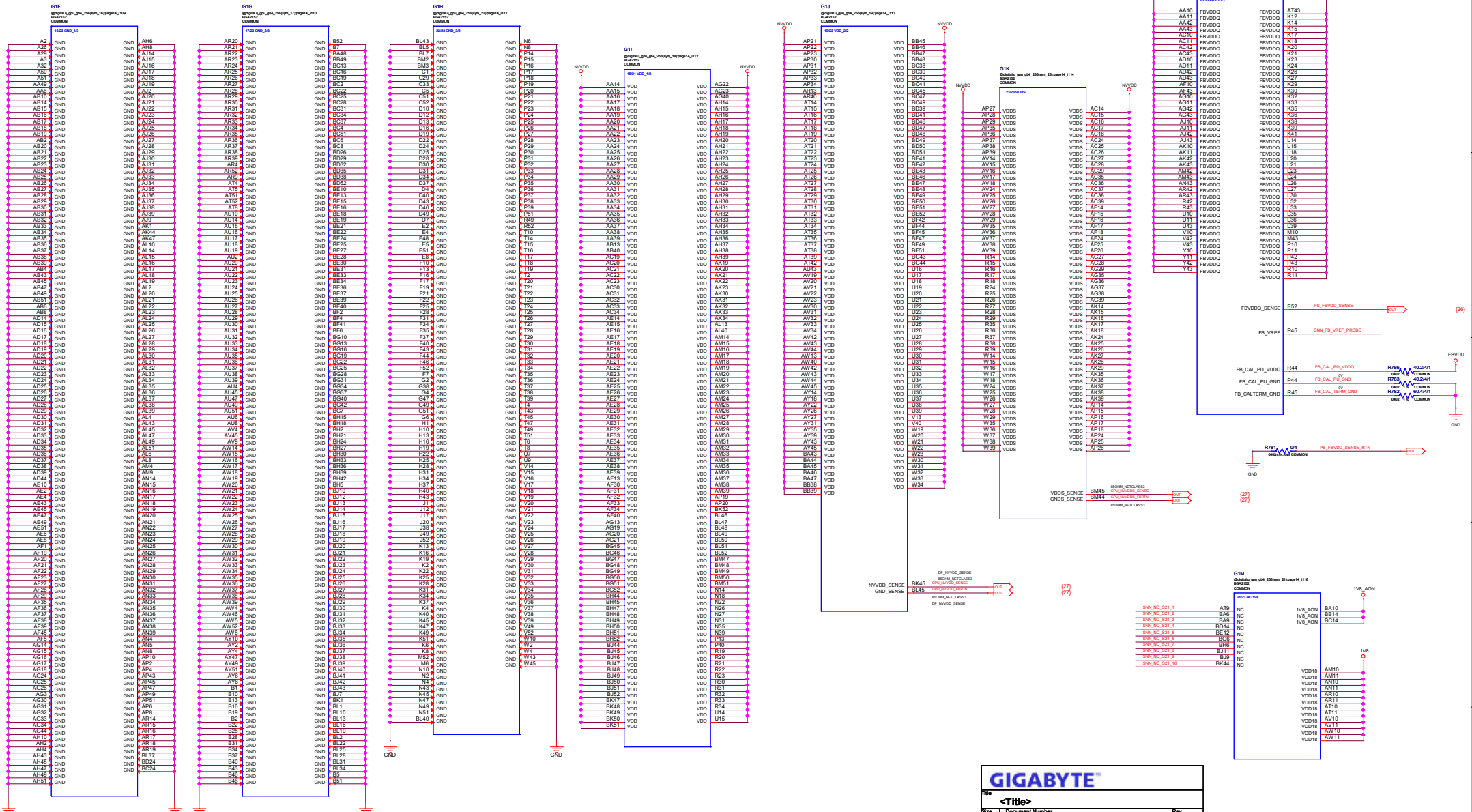
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 Size: 16GB  
 Document Number: **GV-N1080AORUS X-8GD**  
 Rev: **1.0**  
 Date: Friday, December 08, 2018 Sheet 13 of 50

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Part Number: **600-1G413-BASE-000**

PCB REV	1G413-000	PAGE	13 OF 38
ECOM REV	A	DATE	25-MAR-2018

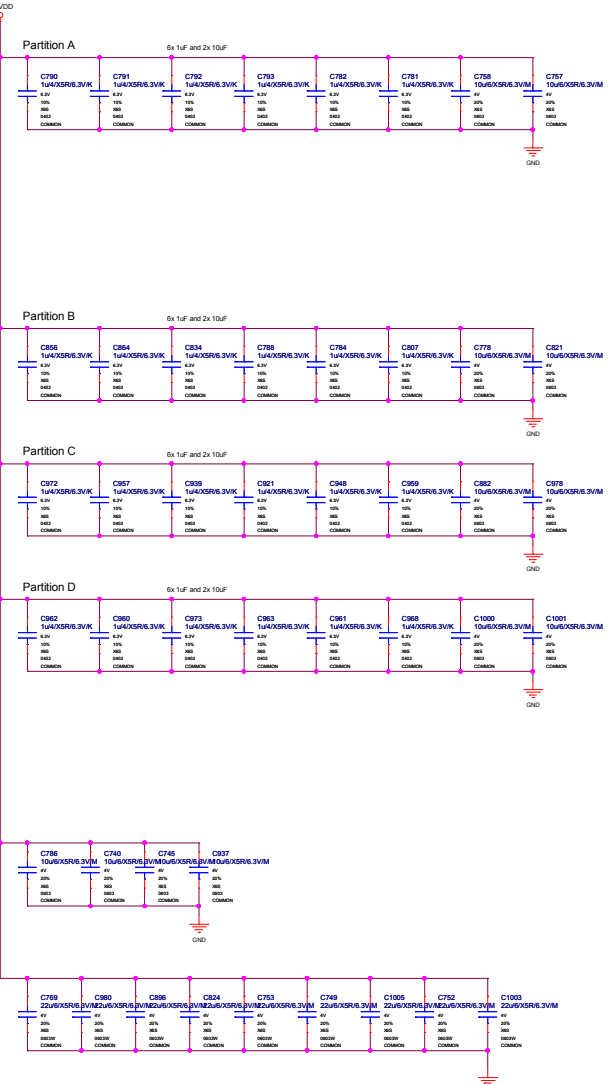
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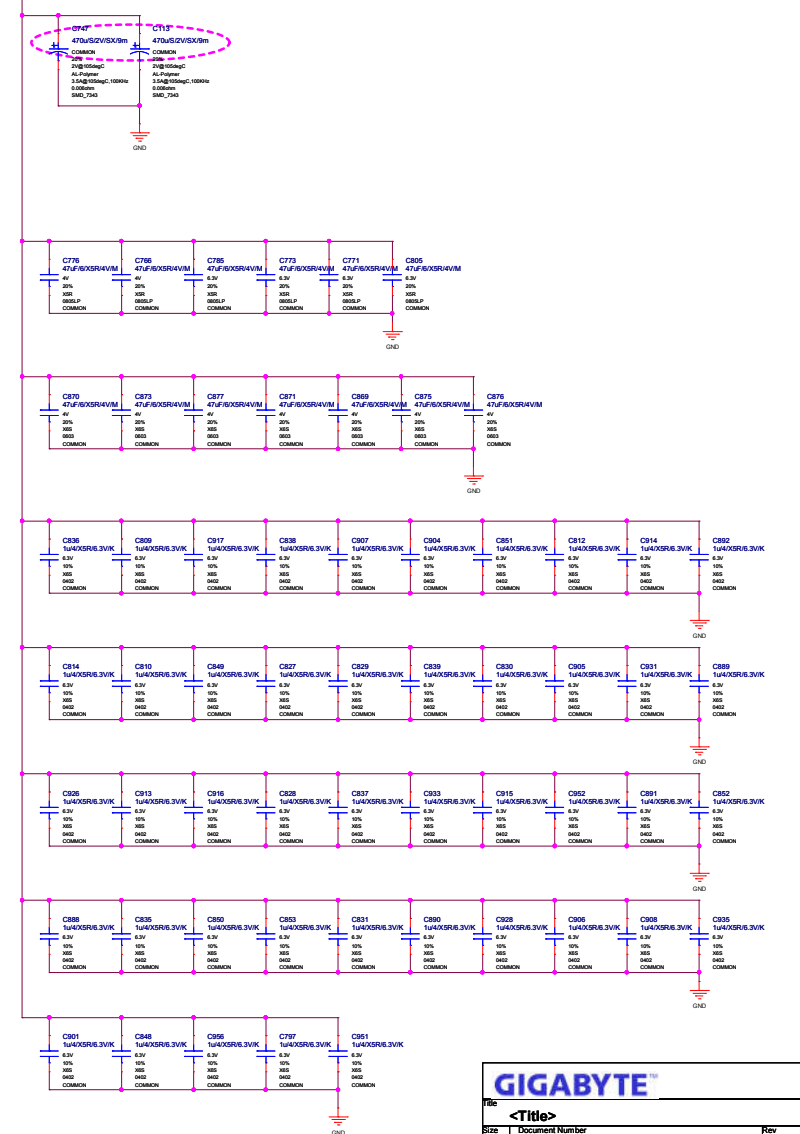
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 Date: Friday, December 06, 2016  
 Page: 14 of 50

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 NV\_PN: 800-1G43-BASE-000  
 PCB REV: 1G43-A00  
 BOM REV: A  
 PAGE: 14 OF 38  
 DATE: 28-MAR-2016

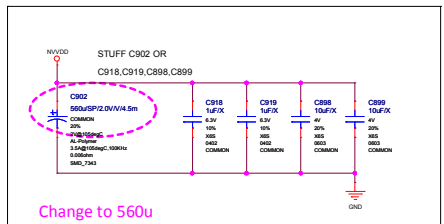
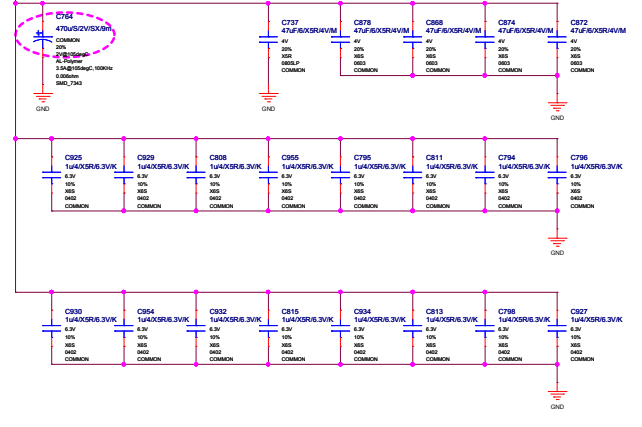
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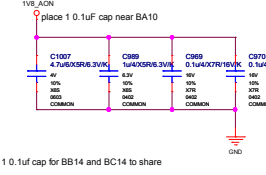
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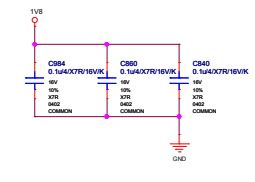
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VDD18



**GIGABYTE**

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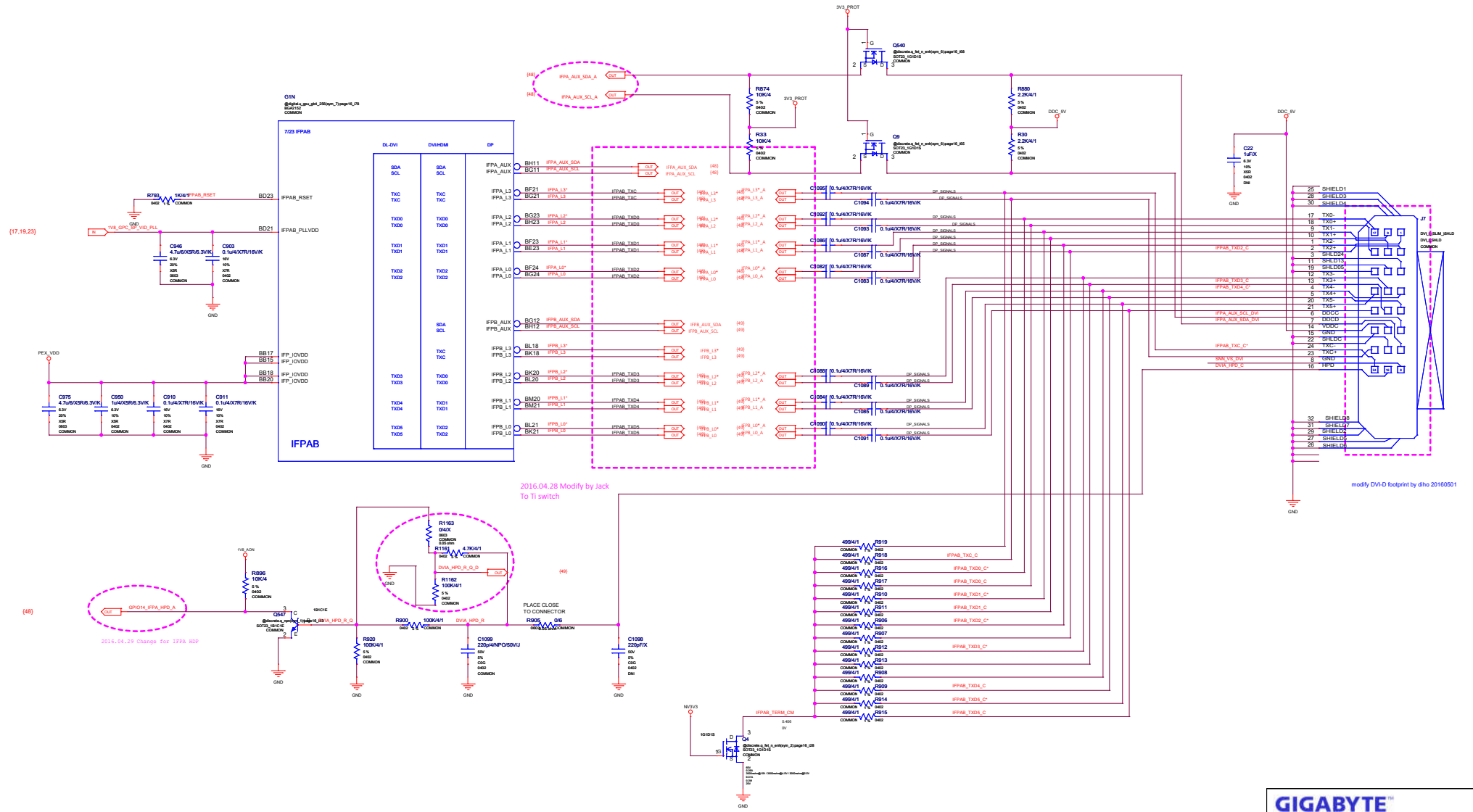
Date: Friday, December 25, 2016 Sheet: 15 of 21

ASSEMBLY DESCRIPTION: GPU Decoupling

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2701 SAN TOMAS EXPRESSWAY  
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Rev_P/N	600-1G413-BASE-000	PAGE	15 OF 38
PCB REV	1G413-A00	DATE	25-MAR-2016
ECOM REV	A		

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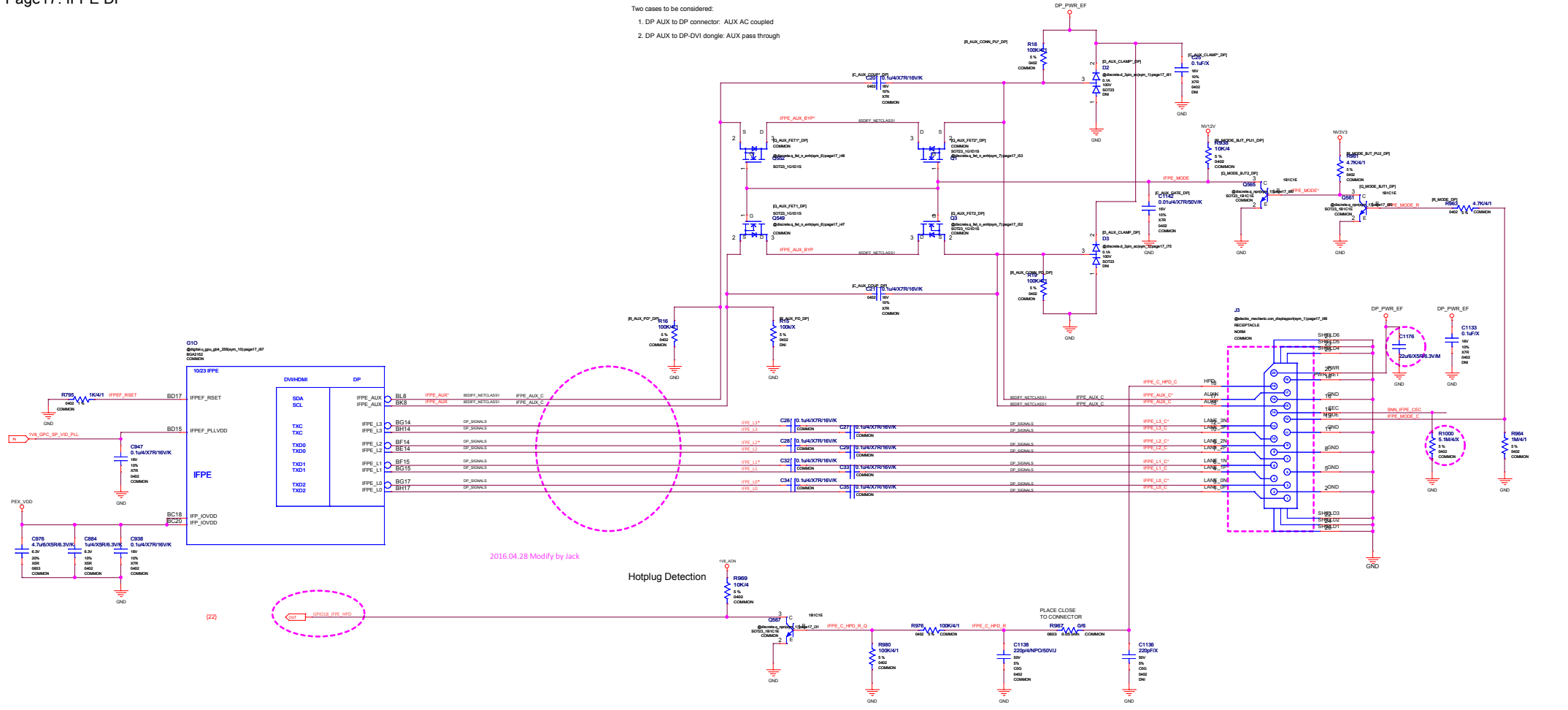
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Date: Friday, December 09, 2016	Sheet: 18 of 10
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INVENTOR: <b>16V_PN</b> 600-1G413-BASE-000 PCB REV: 1G413-ADD BOM REV: A	
PAGE: 16 OF 38	DATE: 25-MAR-2016

ASSEMBLY DESCRIPTION	IFPAB DVI-D-DL
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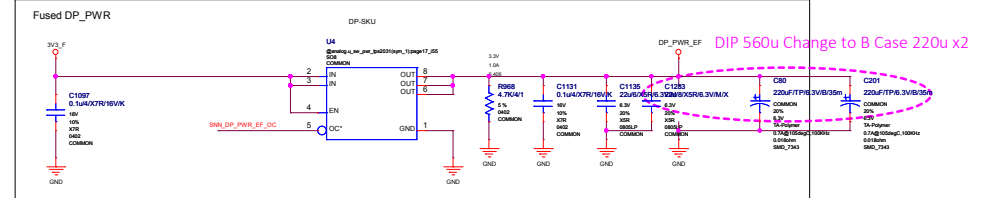


- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
  2. DP AUX to DP-DVI dongle: AUX pass through



2016.04.28 Modify by Jack

Hotplug Detection



<b>GIGABYTE</b>	
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Size	Document Number
Custom	GV-N1080AORUS X-9GD
Date	Friday, December 09, 2016
Sheet	17 of 50

ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IFPE DP

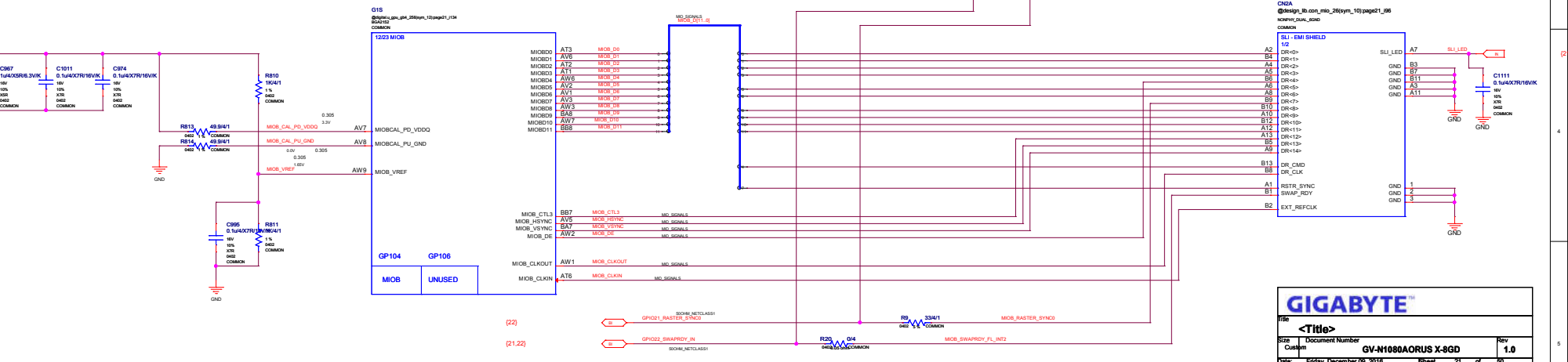
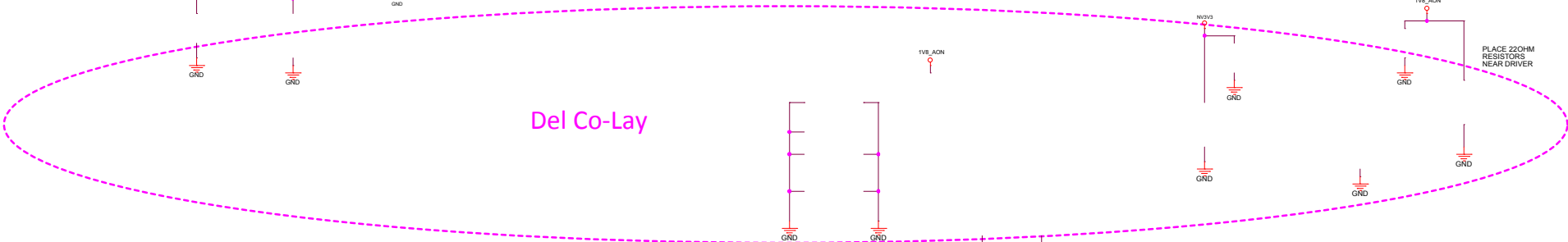
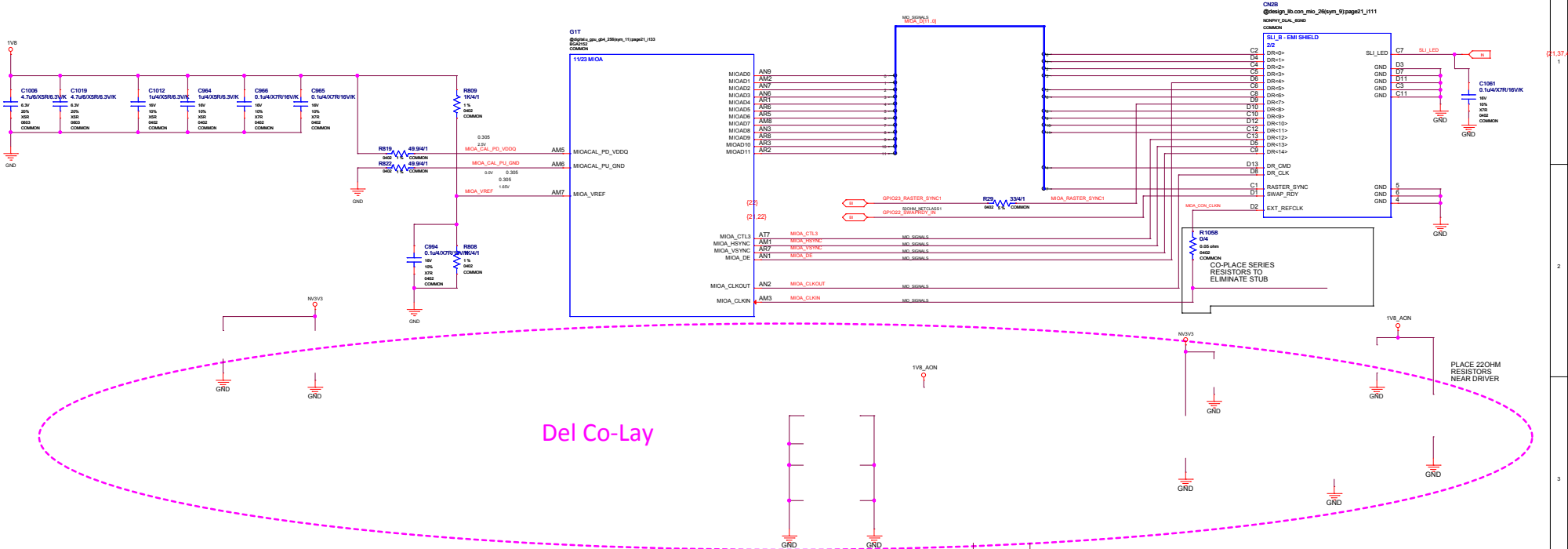
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2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
PN	600-1G413-BASE-000
PCB REV	1G413-000
FORM REV	A
PAGE	17 OF 38
DATE	25-MAR-2016

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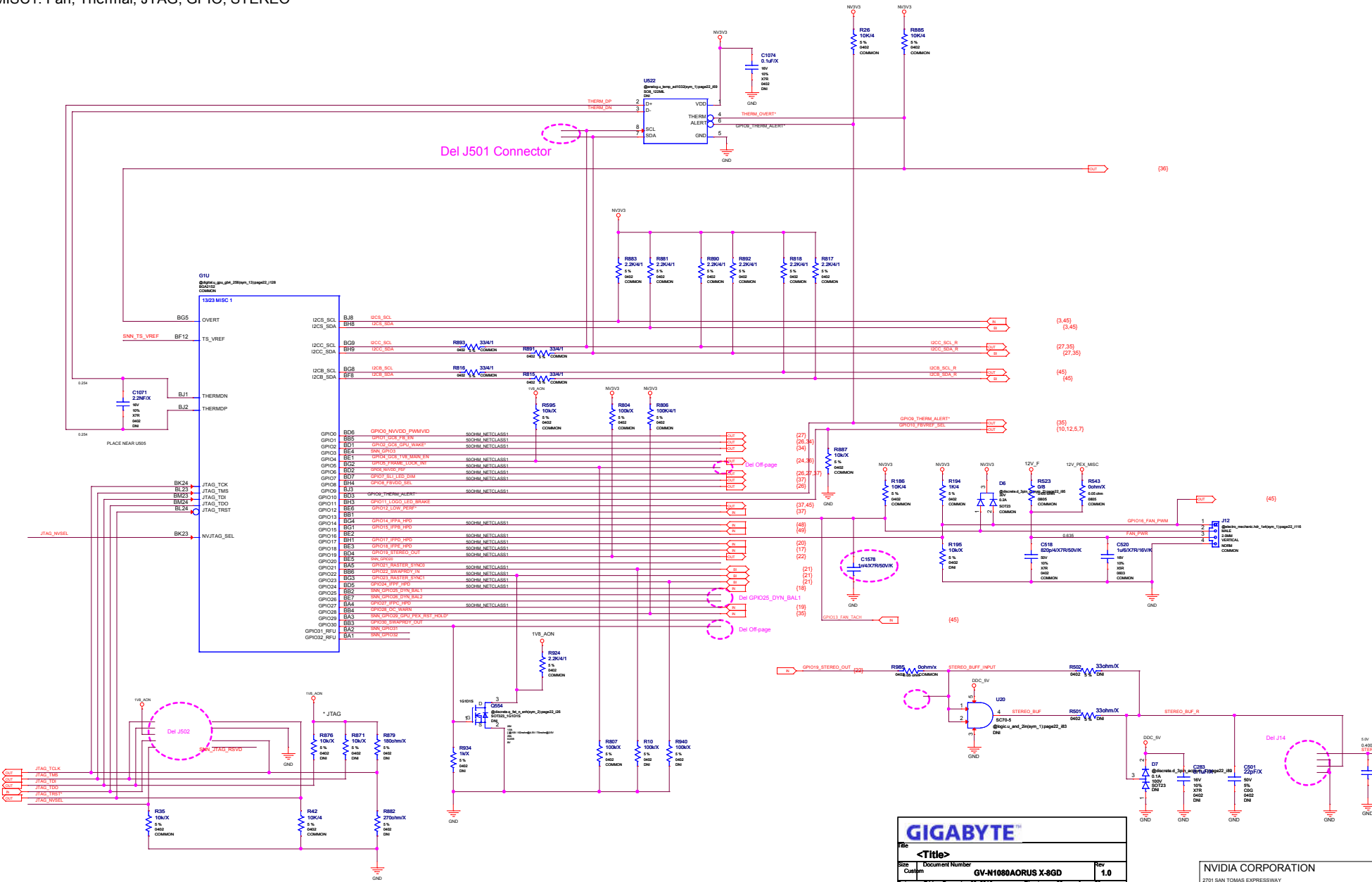


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 Date: Friday, December 09, 2016

Document Number: **GV-N1060AORUS X-8GD**  
 Rev: 1.0  
 Sheet: 21 of 30

ASSEMBLY DESCRIPTION: MIOA/B Interface and Frame Lock



GPU Pinout Table:

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GPIO1	BD5	GPIO1_DDC_PFE_VBE	500mΩ NETCLASS1
GPIO2	BD1	GPIO2_GPIO_DRV_VBE	500mΩ NETCLASS1
GPIO3	BE4	GPIO3_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO4	BE1	GPIO4_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO5	BC2	GPIO5_FANBE_VBE	500mΩ NETCLASS1
GPIO6	BD2	GPIO6_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO7	BD7	GPIO7_SCL_LED_DRV	500mΩ NETCLASS1
GPIO8	BD4	GPIO8_FANVDD_SEE	500mΩ NETCLASS1
GPIO9	BE3	GPIO9_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO10	BD3	GPIO10_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO11	BE5	GPIO11_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO12	BE9	GPIO12_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO13	BE1	GPIO13_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO14	BC4	GPIO14_FAN_PFE	500mΩ NETCLASS1
GPIO15	BD1	GPIO15_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO16	BE2	GPIO16_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO17	BD1	GPIO17_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO18	BE3	GPIO18_GPIO_PFE_VBE	500mΩ NETCLASS1
GPIO19	BD4	GPIO19_GPIO_PFE_VBE	500mΩ NETCLASS1
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GPIO21	BE5	GPIO21_GPIO_PFE_VBE	500mΩ NETCLASS1
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GPIO99	BE1	GPIO99_GPIO_PFE_VBE	500mΩ NETCLASS1
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Size	Document Number	Rev
Class	GV-N1080AORUS X8GD	1.0
Date	Feb 25, December 28, 2016	Sheet 22 of 30

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IN\_VL\_PN 600-1G413-BASE-000

PCB REV 1G413-A00 PAGE 22 OF 38  
BOM REV A DATE 25-MAR-2016

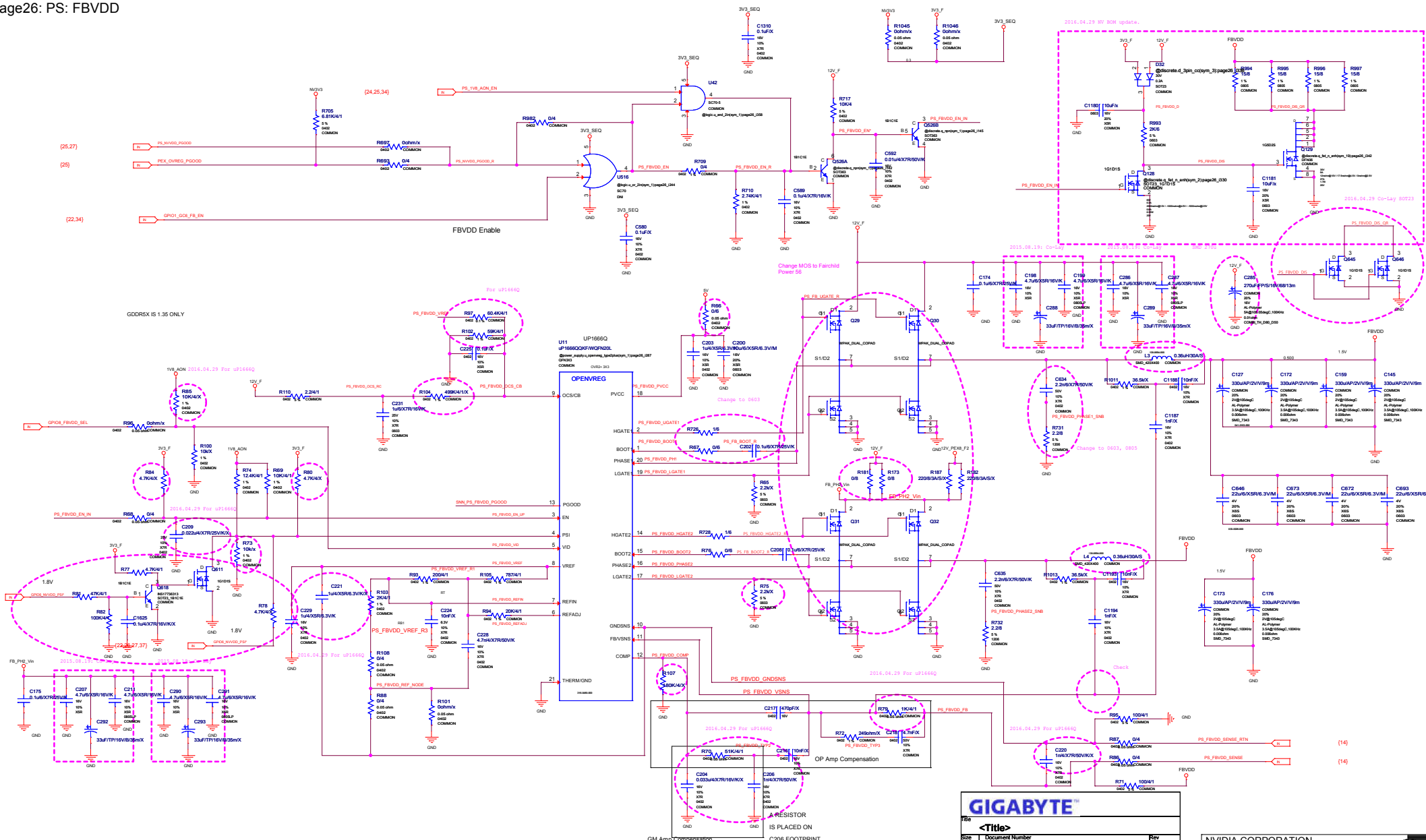
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Rev: 1.0

DATE: Friday, December 08, 2016

SHEET: 26 of 59

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Date	Friday, December 09, 2016	Sheet 28 of 50

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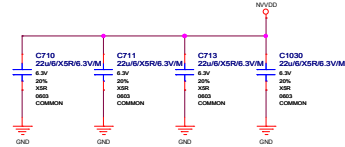
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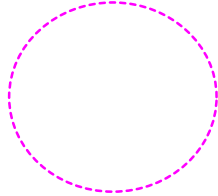
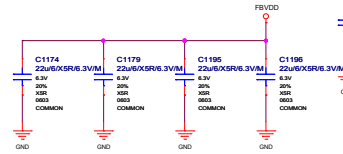
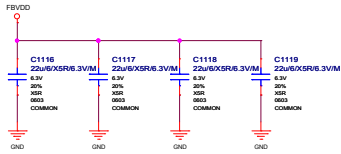
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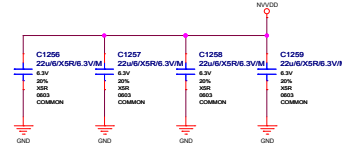


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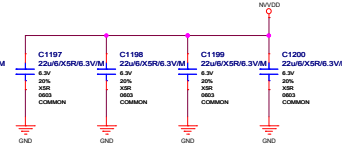


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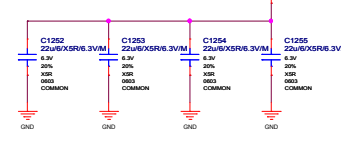
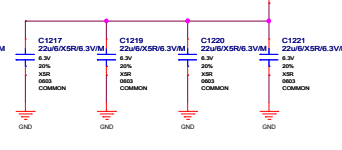
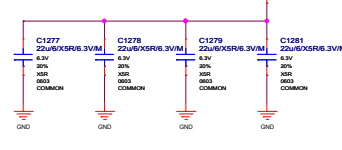
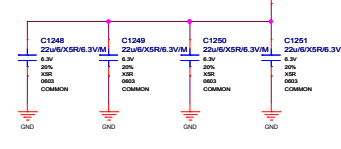
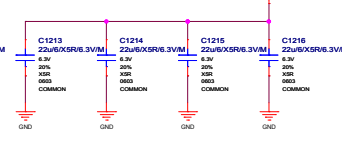
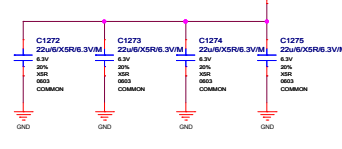
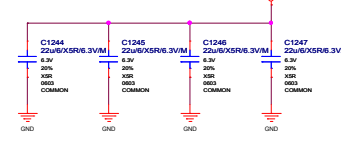
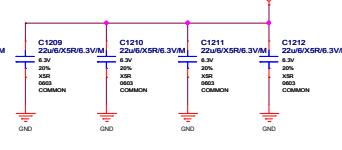
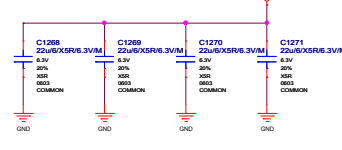
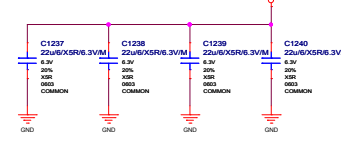
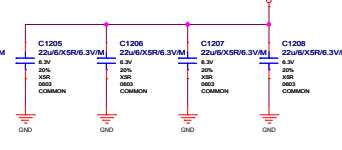
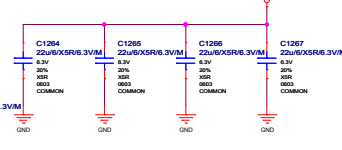
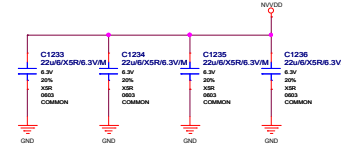
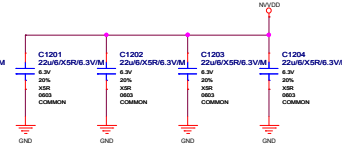
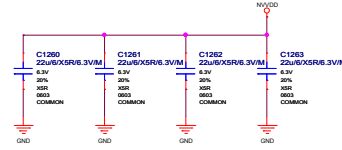
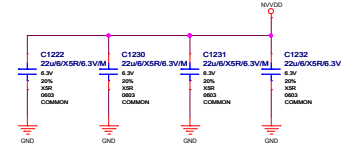
Output Choke side



Output Choke side



Output Choke side



**GIGABYTE**  
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 Date: Friday, December 09, 2016 Sheet: 29 of 50

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1V\_PN: 600-1G413-BASE-000  
 PCB REV: 1G413-ADD PAGE: 29 OF 38  
 BOM REV: A DATE: 25-MAR-2016

ASSEMBLY	*ASSEMBLY DESCRIPTION*
PAGE DETAIL	PS: NVDD Phase 1-4

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Date: <b>Friday, December 09, 2016</b>		Sheet <b>30</b> of <b>50</b>


<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	<b>600-1G413-BASE-000</b>	PAGE	30 OF 38
PCB REV	TG413-ADD	DATE	25-MAR-2016
ECN REV	A		

ASSEMBLY	*ASSEMBLY DESCRIPTION*
PAGE DETAIL	PS: NVVDD Phase 5 & 6

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Date	Friday, December 09, 2016	Sheet	31 of 80

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NV_PN	<b>600-1G413-BASE-000</b>	PAGE	31 OF 38
PCB REV	TG413A00	DATE	25-MAR-2016
ECM REV	A		

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Date	Friday, December 09, 2016	Sheet 32 of 80

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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	PS: Dynamic Power Balance Phases

NV_PN	<b>600-1G413-BASE-000</b>	PAGE	32 OF 38
PCB REV	TG413A00	DATE	25-MAR-2016
ECM REV	A		

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Date	Friday, December 09, 2016	Sheet 33 of 50

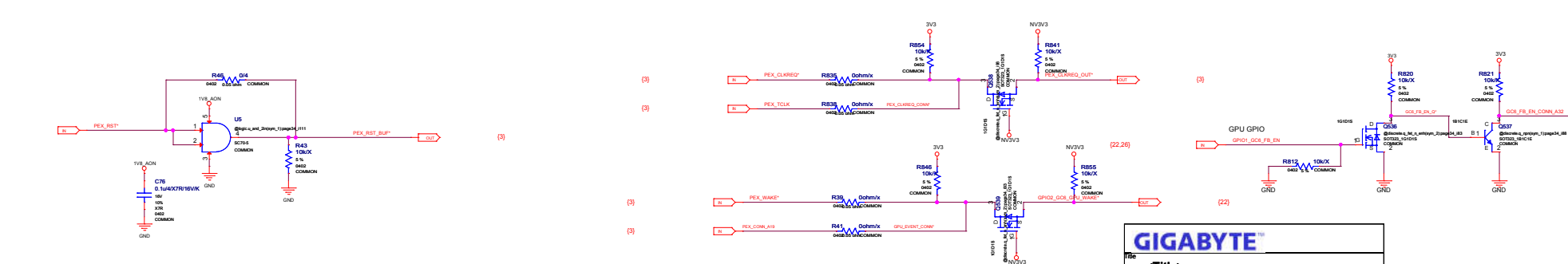
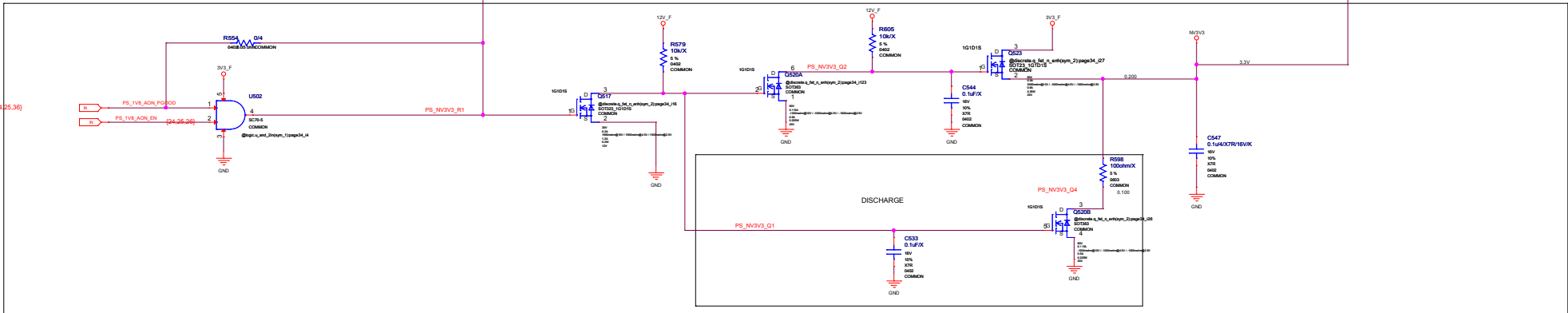
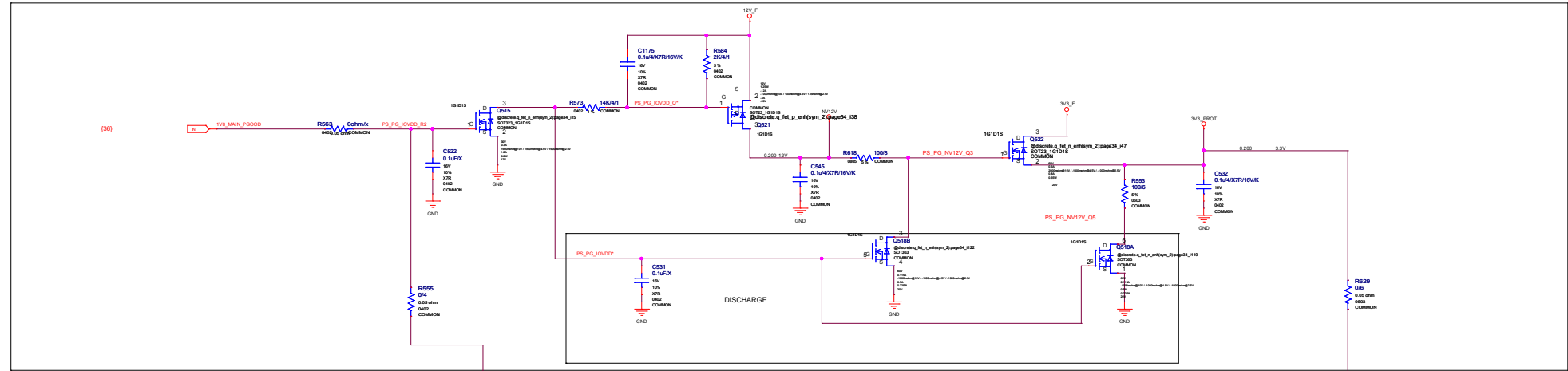
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PAGE DETAIL	PS: Dynamic Power Balance Logic

NV_PN	<b>600-1G413-BASE-000</b>	PAGE	33 OF 38
PCB REV	1G413-ADD	DATE	25-MAR-2016
ECM REV	A		

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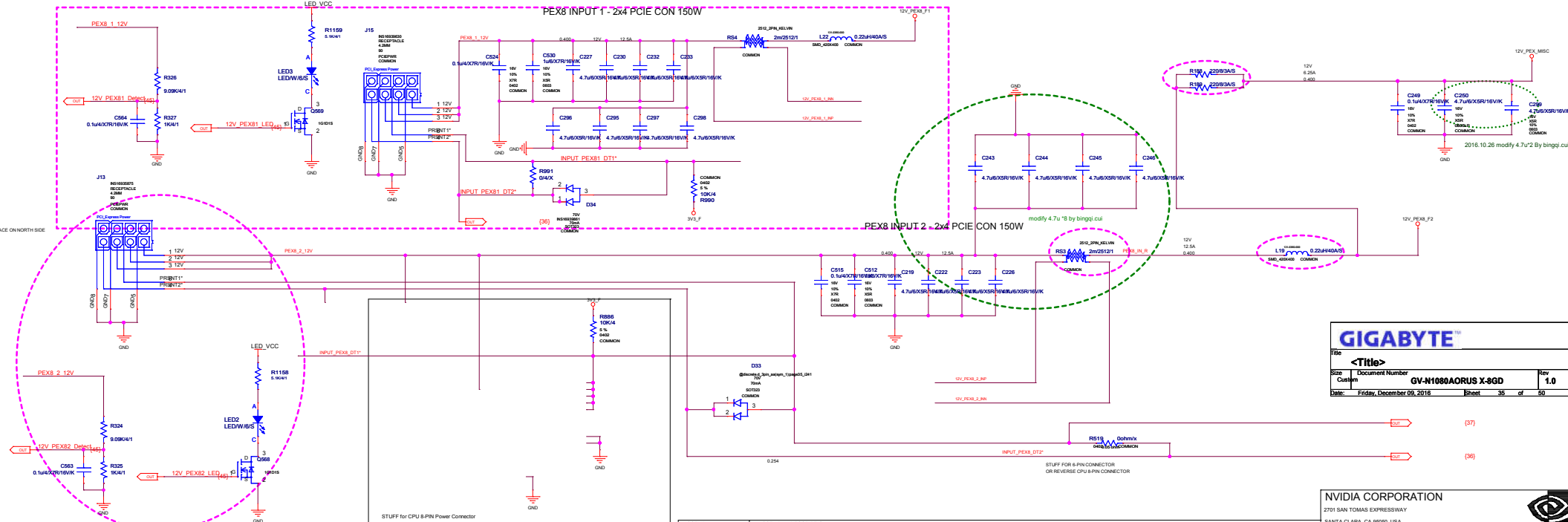
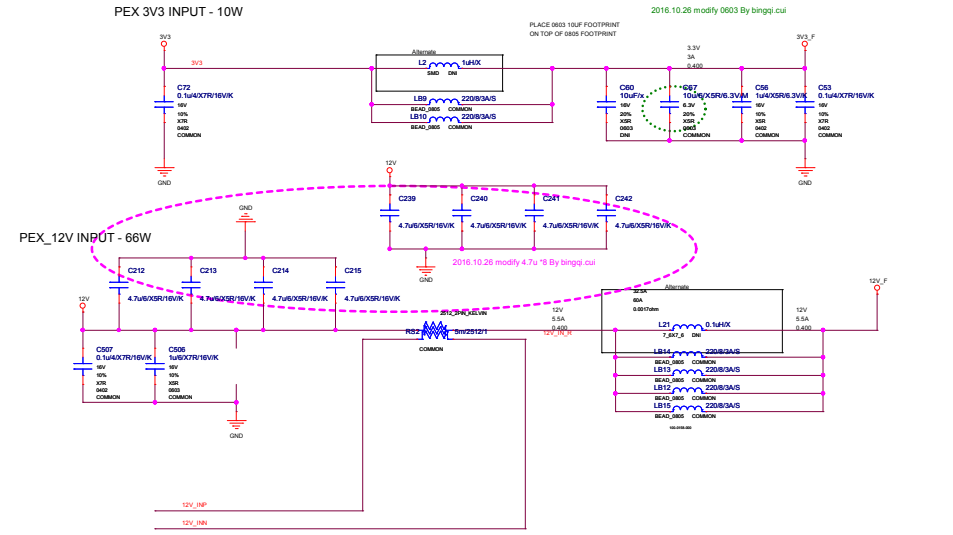
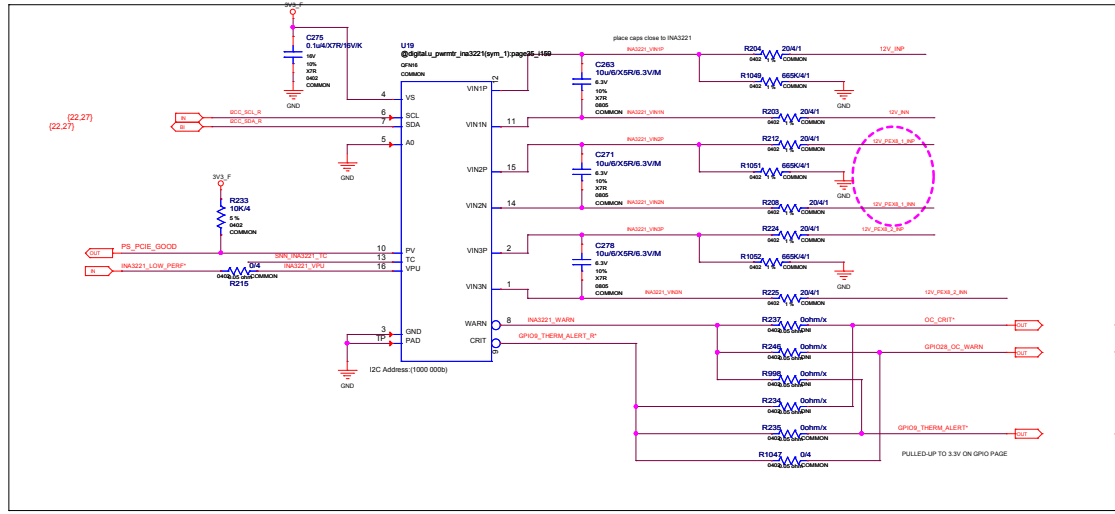
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Rev	1.0	
Date	Friday, December 05, 2016	Sheet 34 of 50

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: NV3V3, NV12V

NV_PN	600-1G413-BASE-000	PAGE	34 OF 38
PCB REV	1G413-000	DATE	25-MAR-2016
ECN REV	A		

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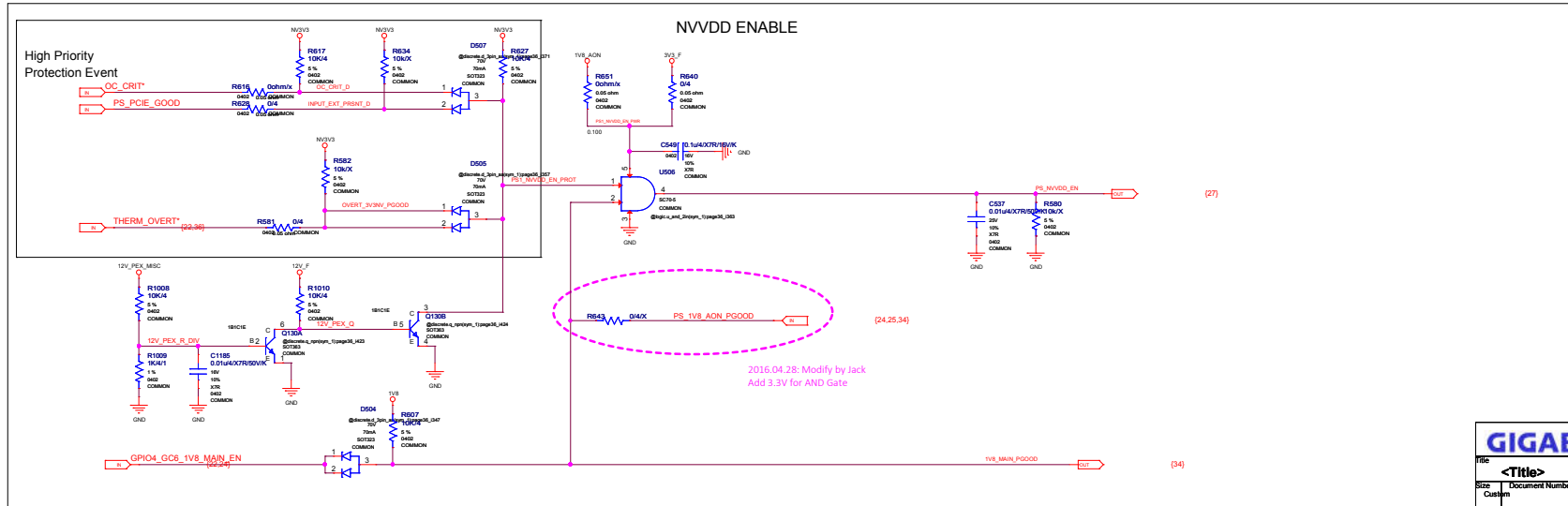
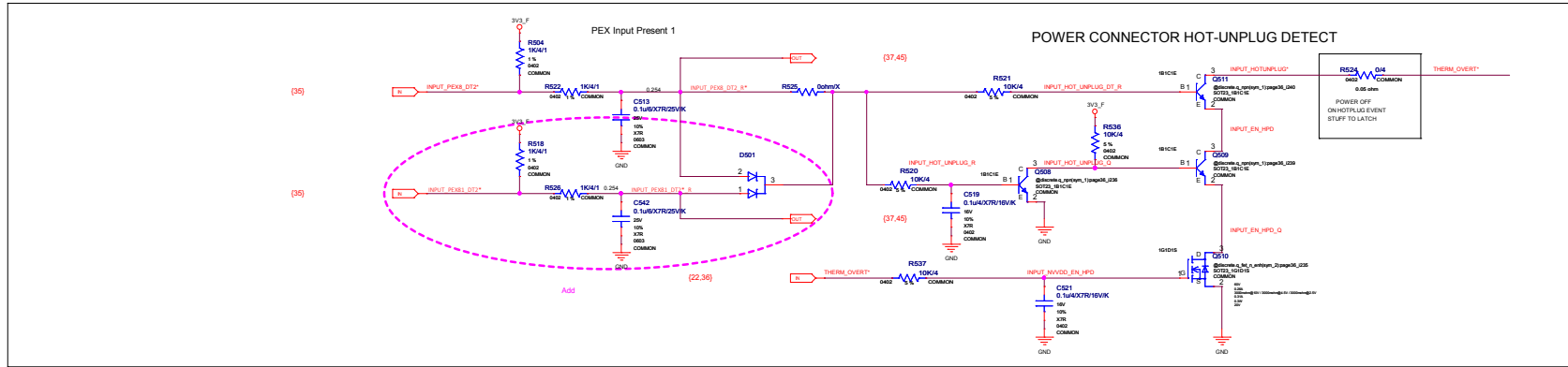


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Date:	Friday, December 09, 2016	Sheet 35 of 50

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INV_P/N	600-1G413-BASE-000	
PCB REV	1G413-A00	PAGE 35 OF 38
ECOM REV	A	DATE 25-MAR-2016



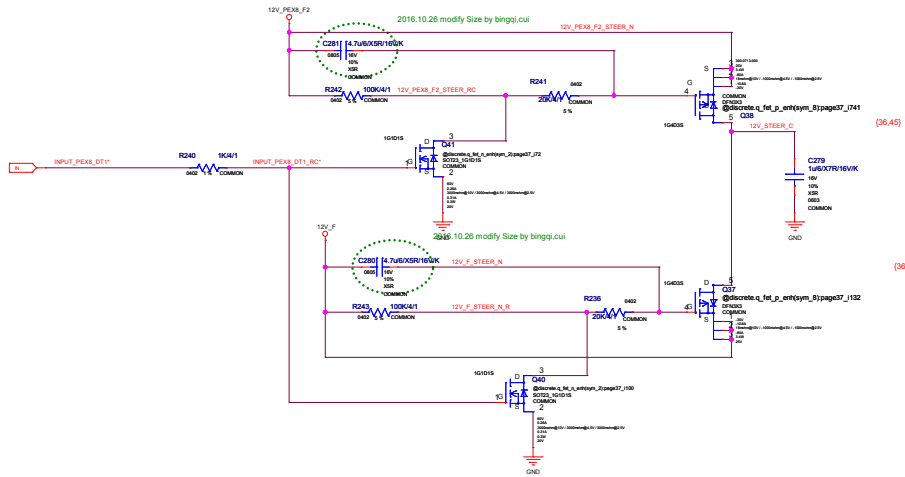
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PCB REV	1G413-A00	PAGE 36 OF 38
ECOM REV	A	DATE 25-MAR-2016

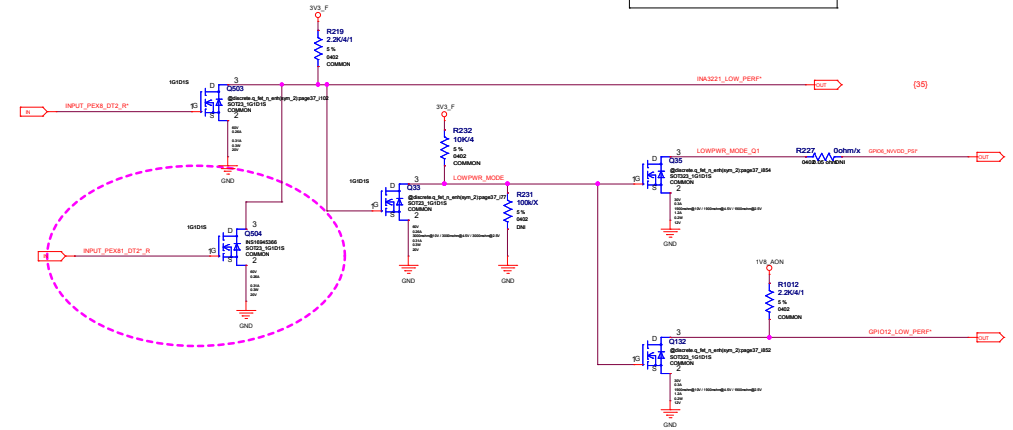
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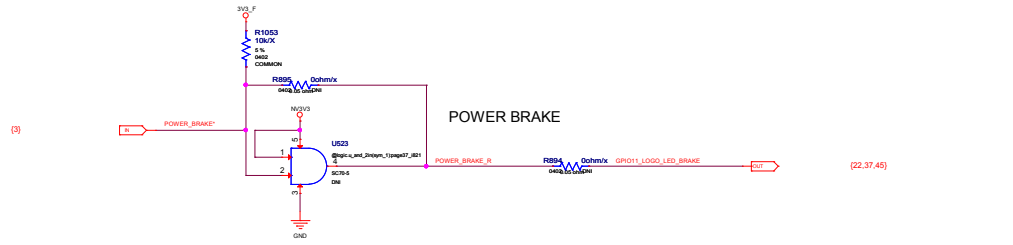
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PEX Input - Power Level/PSI\* Control

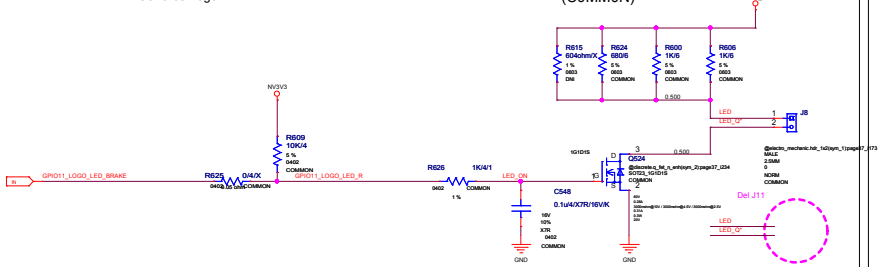


POWER BRAKE



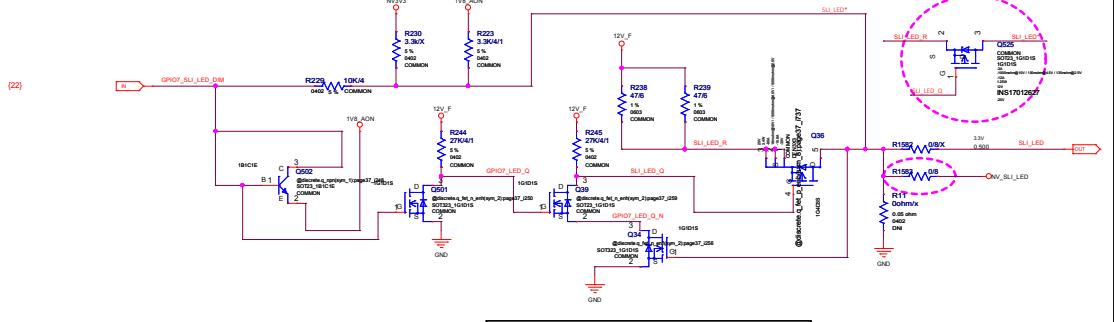
GeForce Logo LED

LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)

Add經濟料SOT23



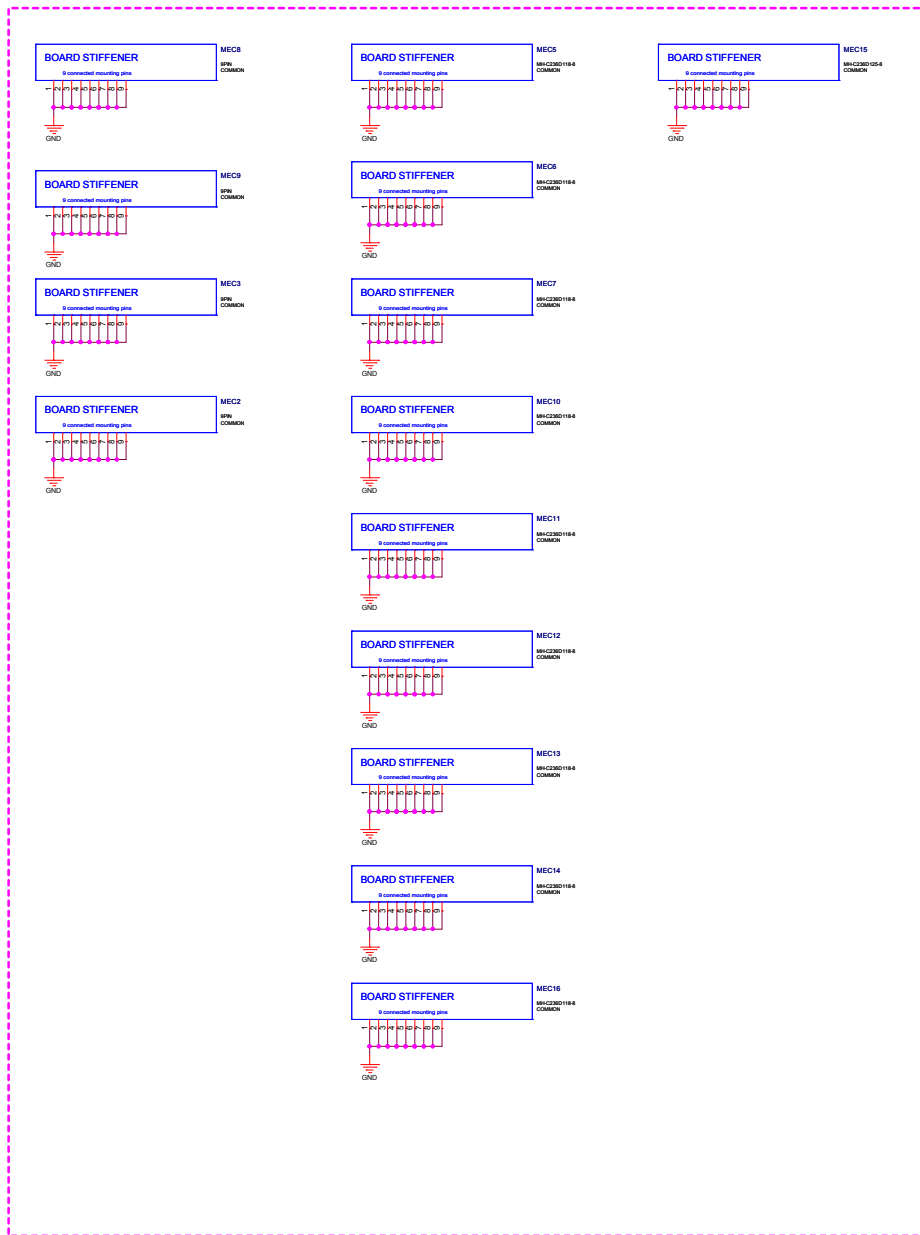
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 Date: Friday, December 08, 2016 Page: 37 of 50

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INV\_PN: 600-1G413-BASE-000  
 PCB REV: 1G413-A00  
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Rev  
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**GV-N1080AORUS X-8GD**  
 Rev  
**1.0**  
 Date  
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 of  
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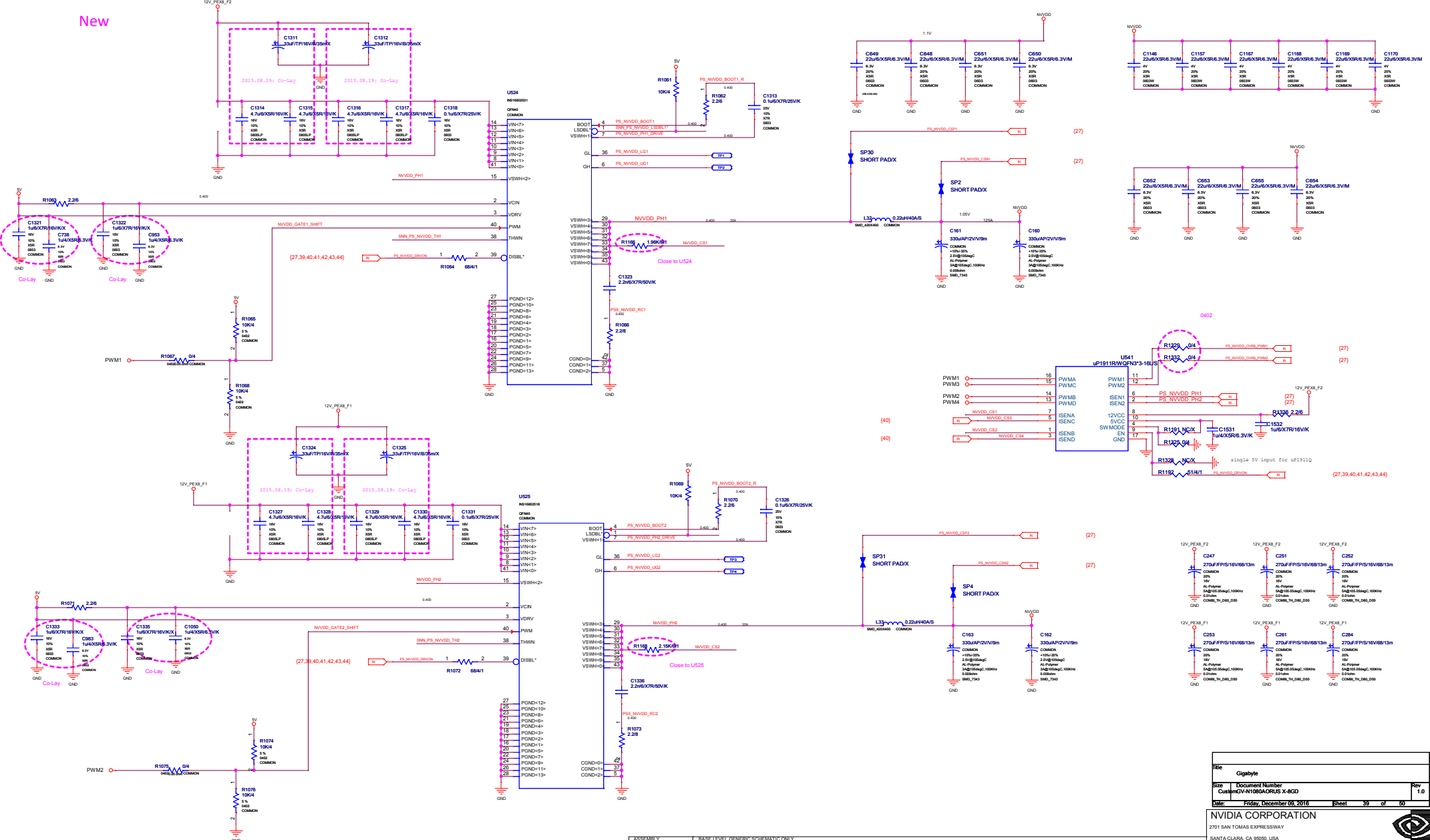


NV_PN	600-1G413-BASE-000	PAGE	38 OF 38
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ECOM REV	A		

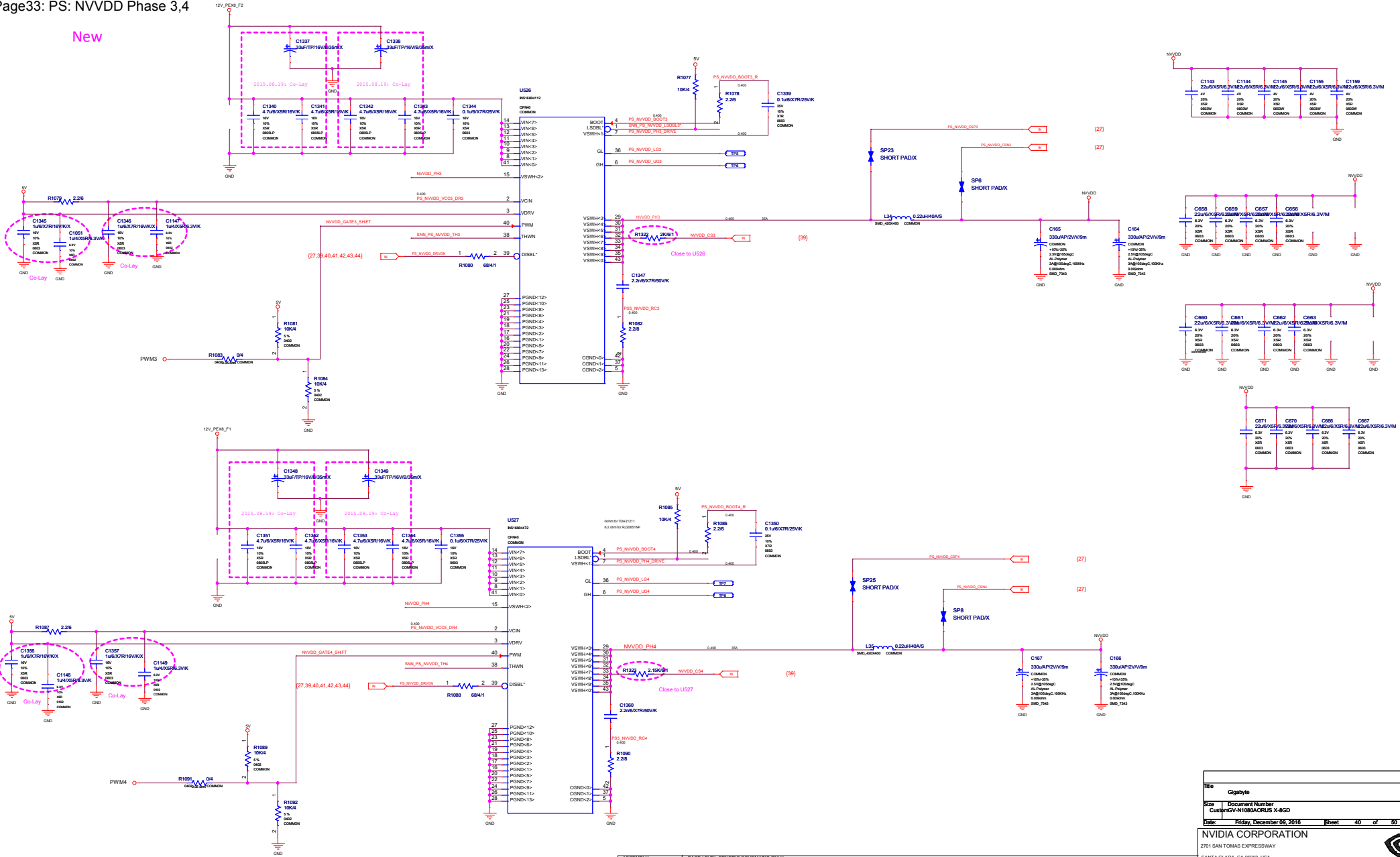
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New



New



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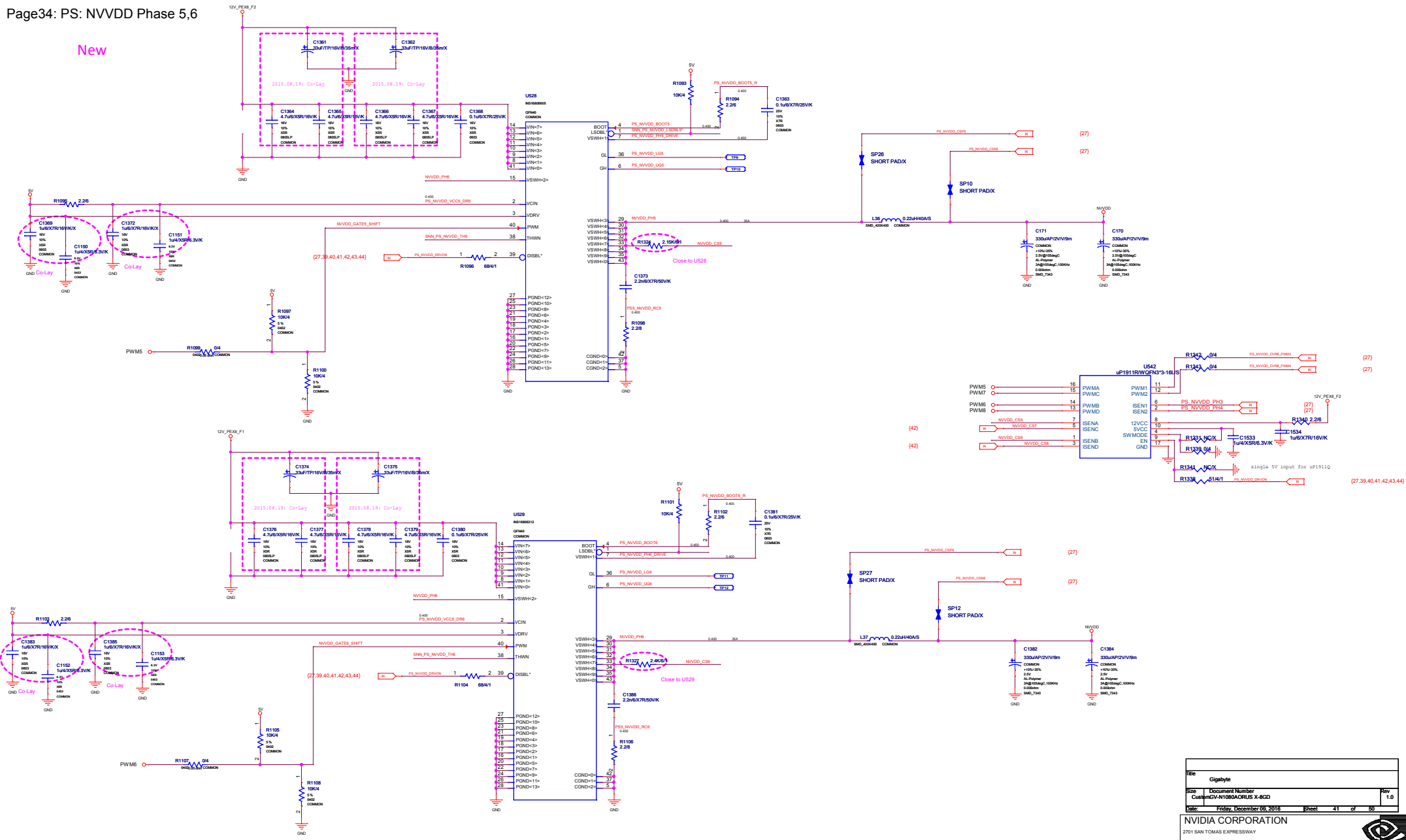
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Date:	Friday, December 05, 2016	Sheet	40 of 80
NVIDIA CORPORATION			
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FILE REV	PH0000304	PAGE	33 OF 45
BOM REV	A	DATE	21-APR-2015





New



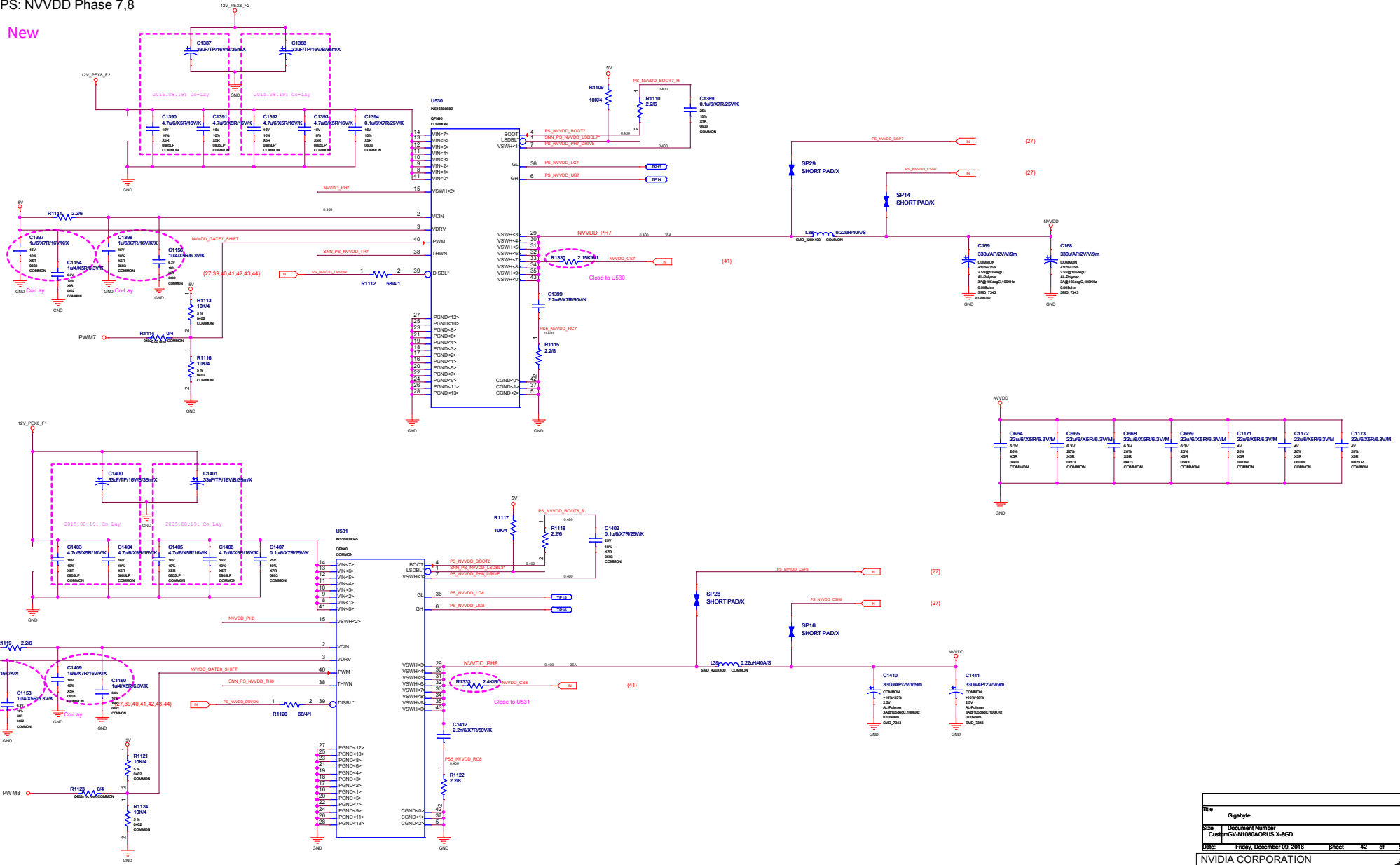
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NV_PN	600-1G600-BASE-QS1	
PCB REV	PS0001024	PAGE 34 OF 45
BOM REV	A	DATE 21-APR-2015

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New



CO-LAYOUT: CHOOSE UA OR UB

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY  
 PASTE DETAIL: PS: NVVDD Dynamic Switch Phases

File		Gigabyte	
Size	Customer Number	Document Number	Rev
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Date:	Friday, December 05, 2015	Sheet	42 of 80

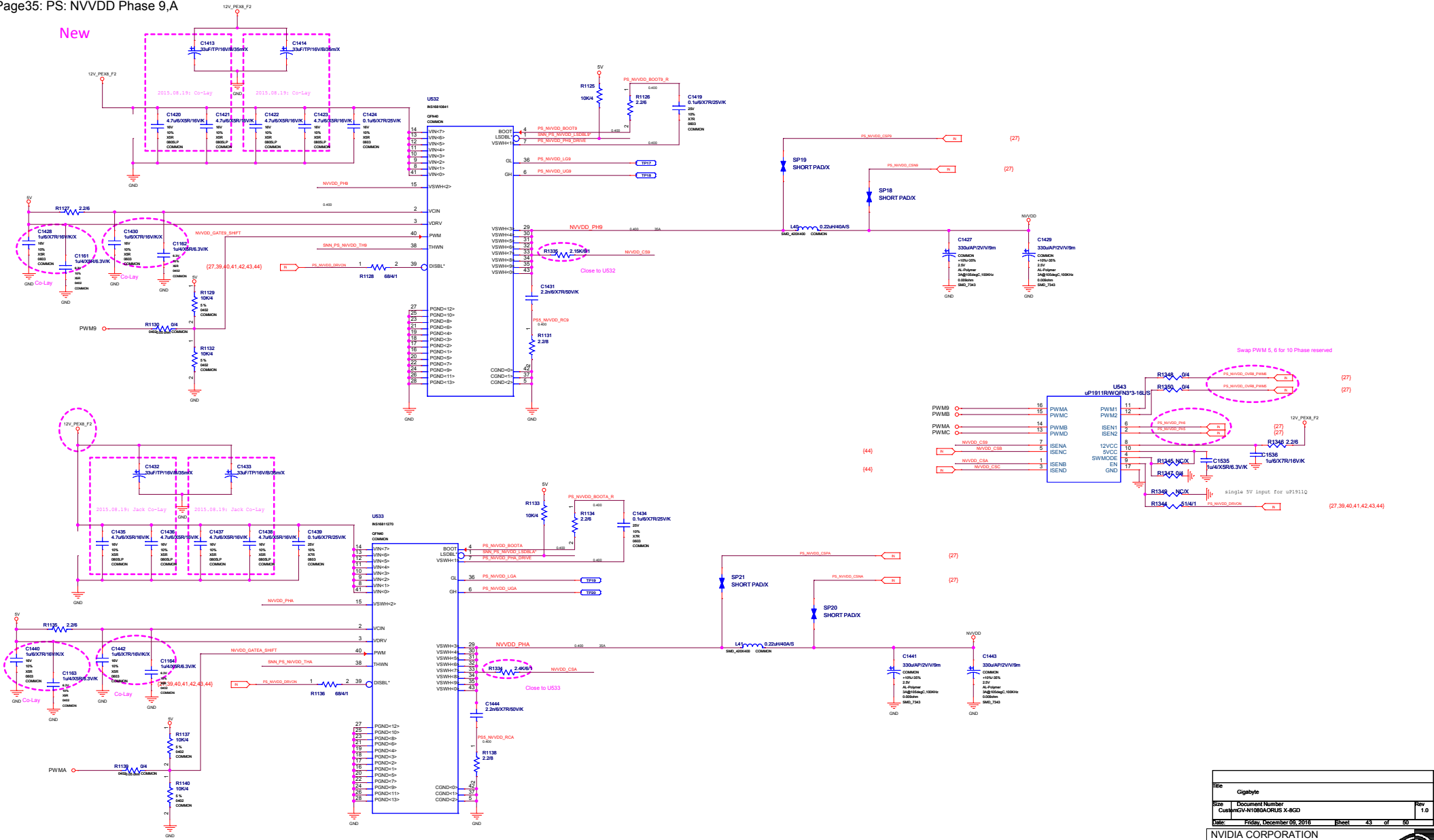
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NV_PN	600-1G600-BASE-QS1	PAGE	35 OF 45
PCB REV	PS000180Z	DATE	21-APR-2015
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New



CO-LAYOUT: CHOOSE UA OR UB

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 PDATE DETAIL: PS: NVVDD Dynamic Switch Phases

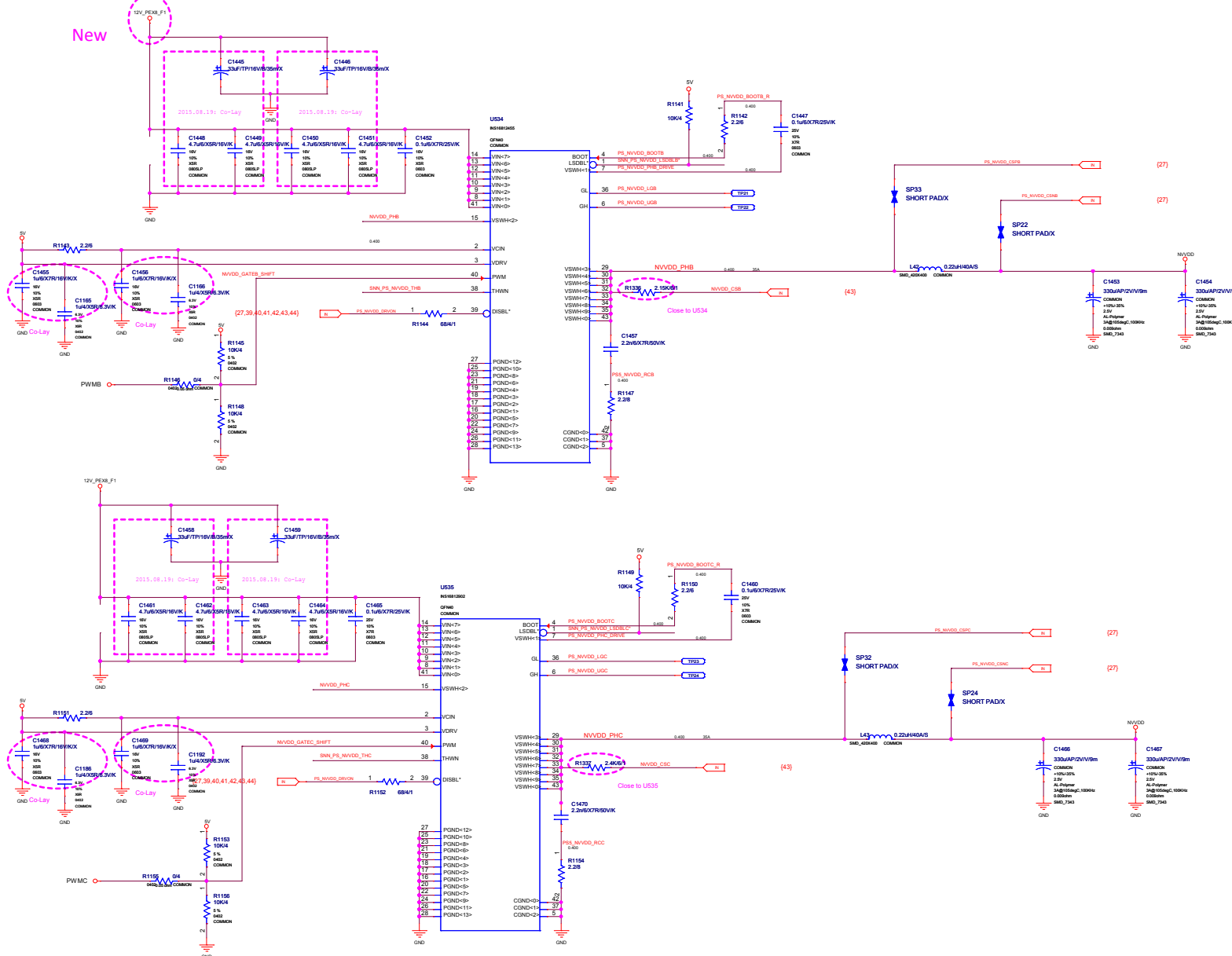
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Date:	Friday, December 05, 2016	Sheet	43 of 80

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NV_PN	600-1G600-BASE-QS1		
PCB REV	P380030Z	PAGE	35 OF 45
BOM REV	A	DATE	21-APR-2015

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CO-LAYOUT: CHOOSE UA OR UB

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY  
 PASTE DETAIL: PS: NVVDD Dynamic Switch Phases

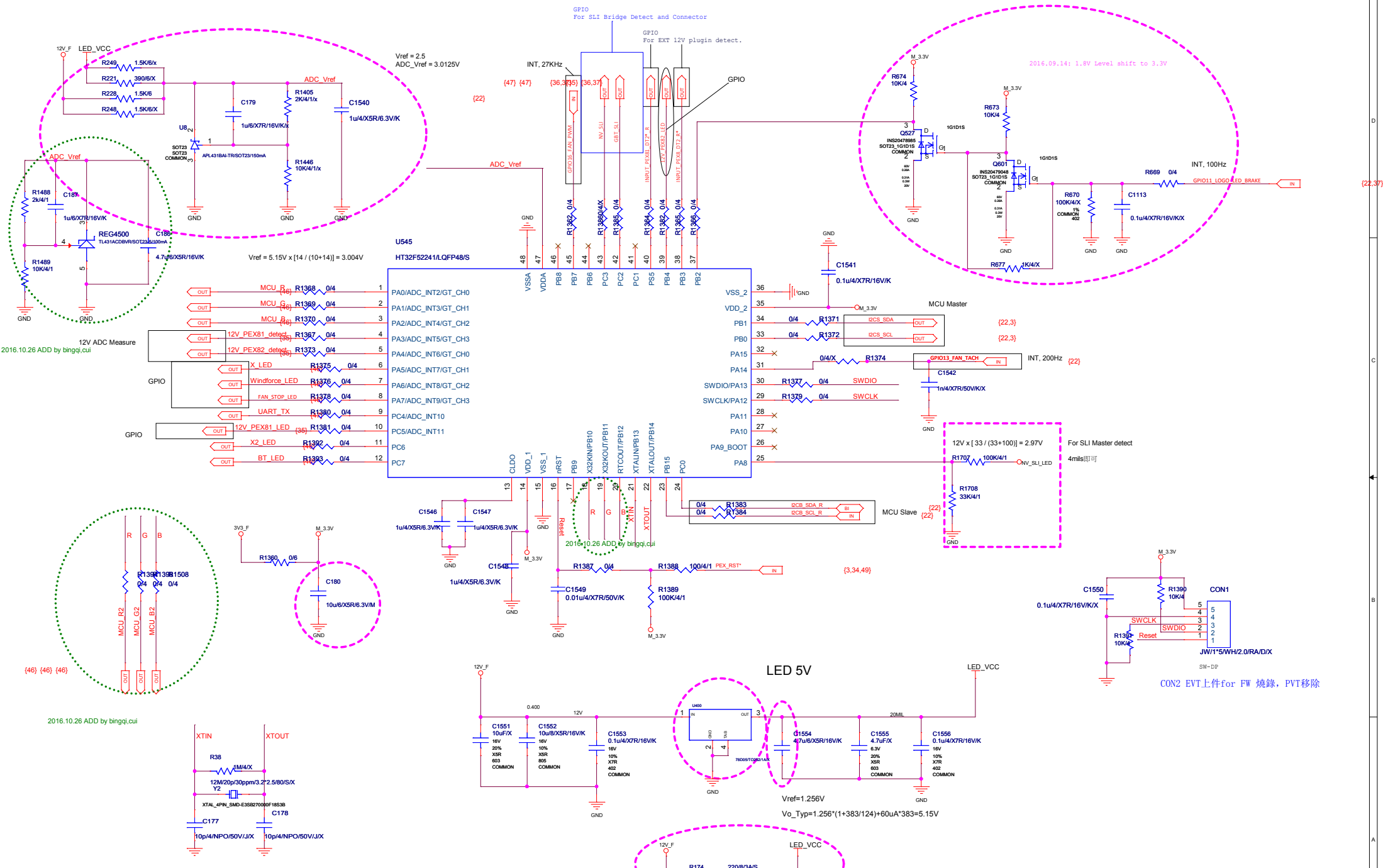
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Customer	NV1080AORUS X-8GD		
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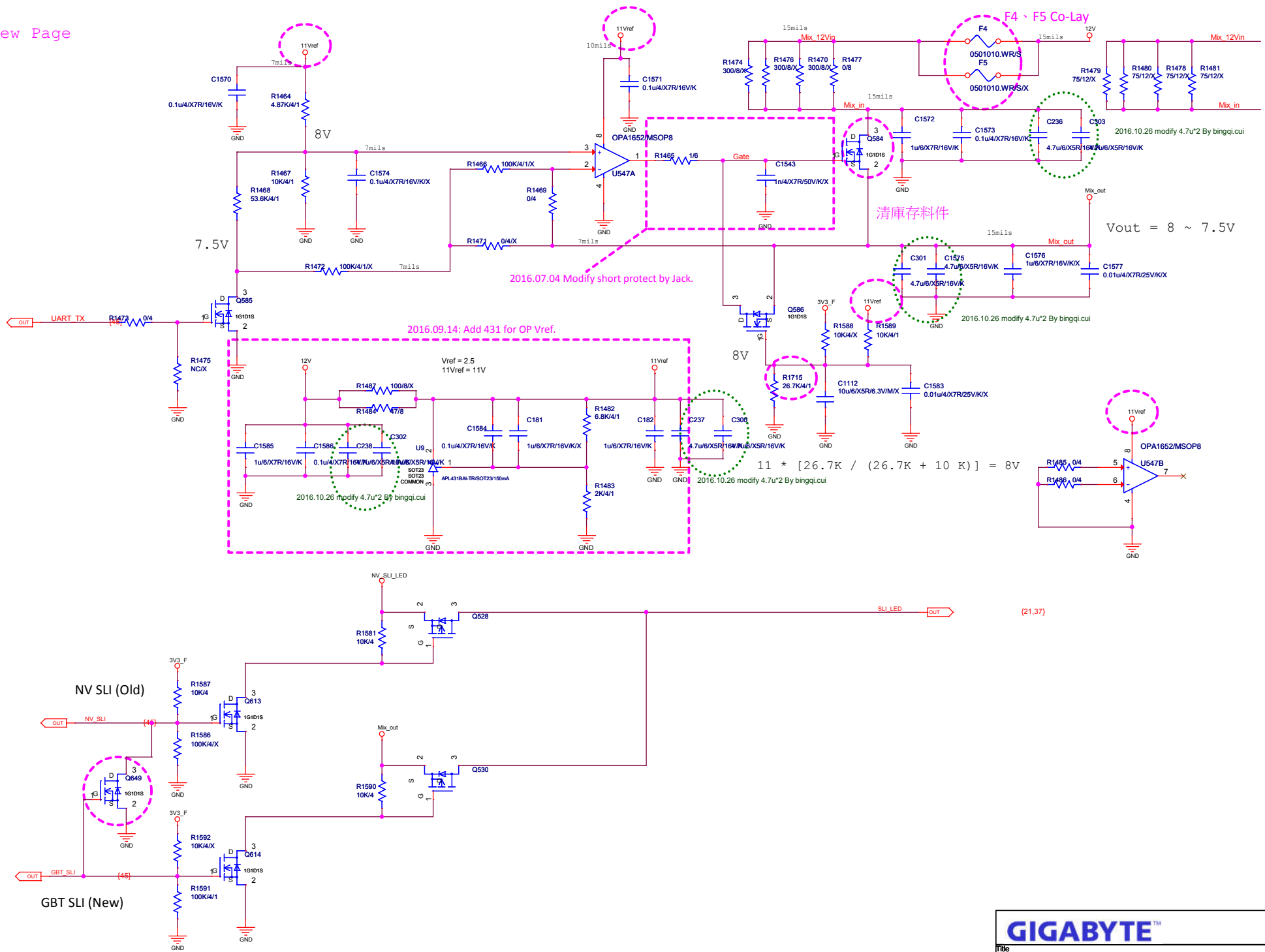


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BOM REV	A	DATE	21-APR-2015

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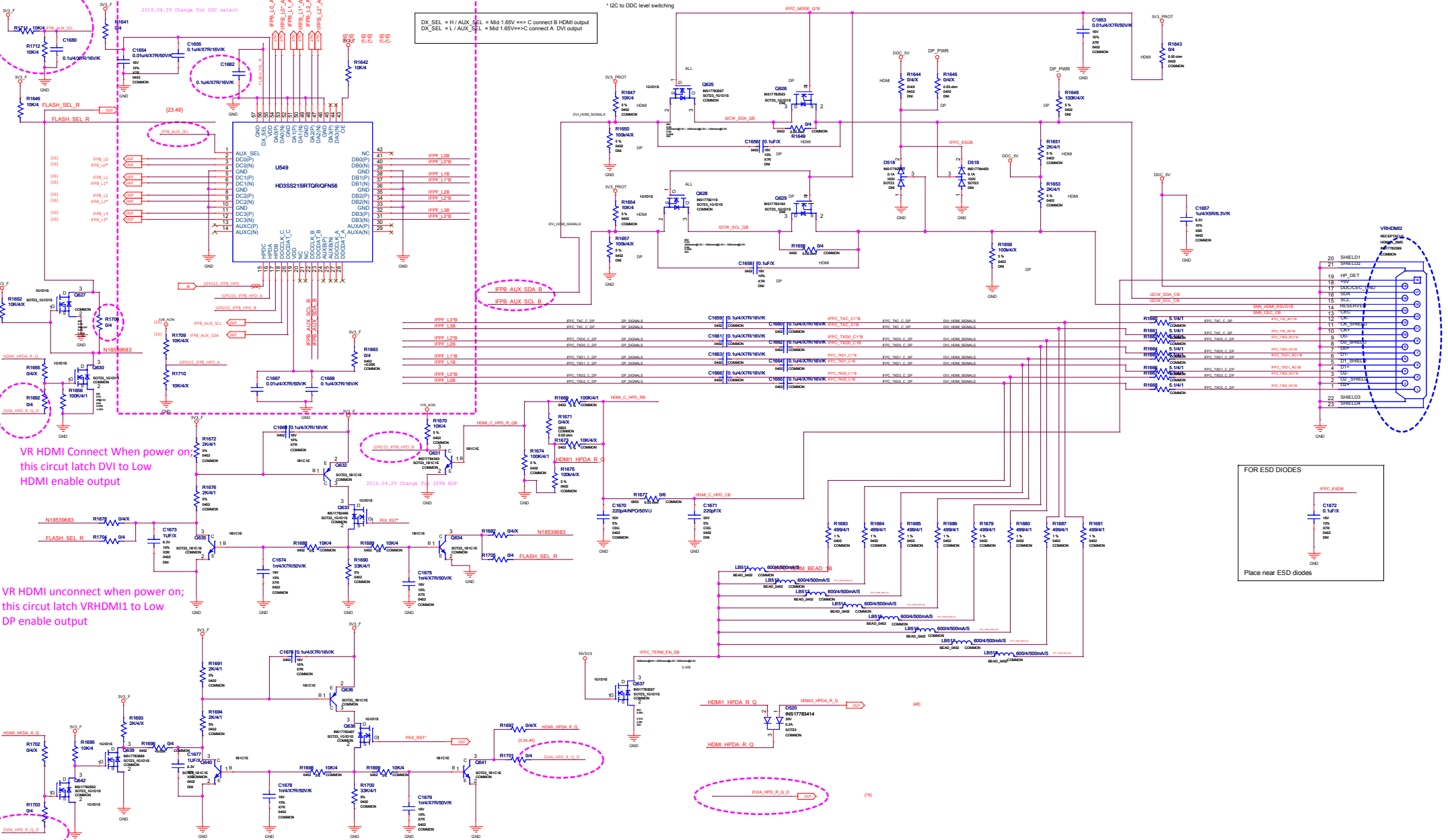






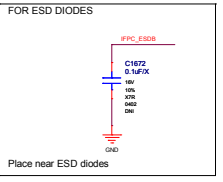






VR HDMI Connect When power on;  
this circuit latch DVI to Low  
HDMI enable output

VR HDMI unconnect when power on;  
this circuit latch VRHDMI1 to Low  
DP enable output



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## History

Date	Modify
2016.04.04	First version
2016.05.04	0.21 modify DVI vs VRHDMI switch
2016.06.16	2.0 Only modify PCB text REV 0.21 to 2.0
2016.07.04	0.6 Modify P.47 Q586 Mix_out protect.
2016.08.26	2.01 Only modify PCB text REV 0.21 to 2.0
2016.09.24	0.7 modify From 2.01, Modify P.47 OP Vref.