PG611 C00

12GB GDDR5X, 384b, 256Mx32

TALL DVI-D + DP + DP + HDMI/DP + DP

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PART_DWG	800-1G611-BASE-300		
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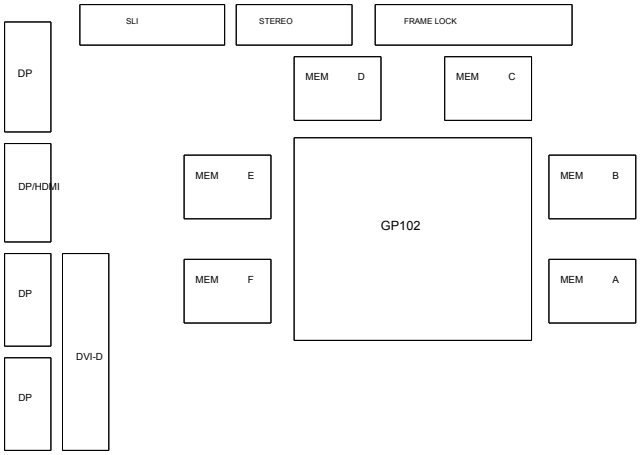
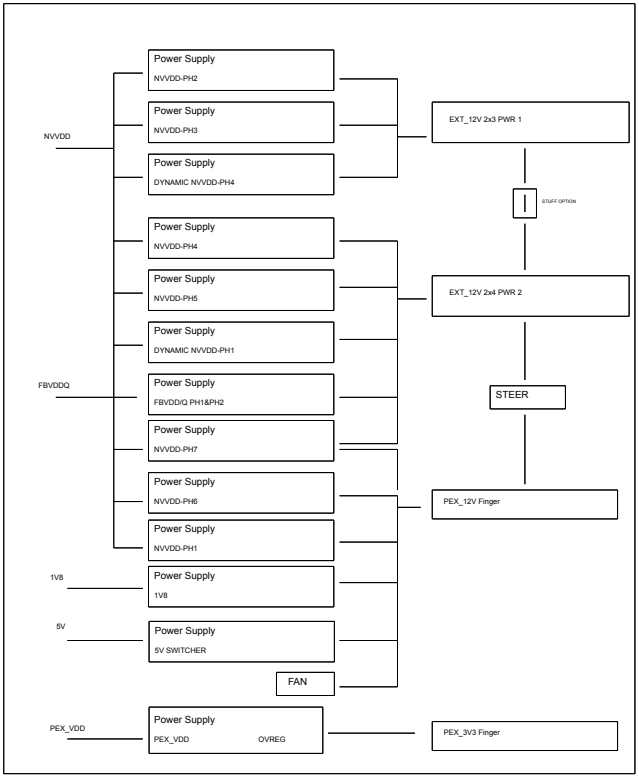
Page2: Block Diagram





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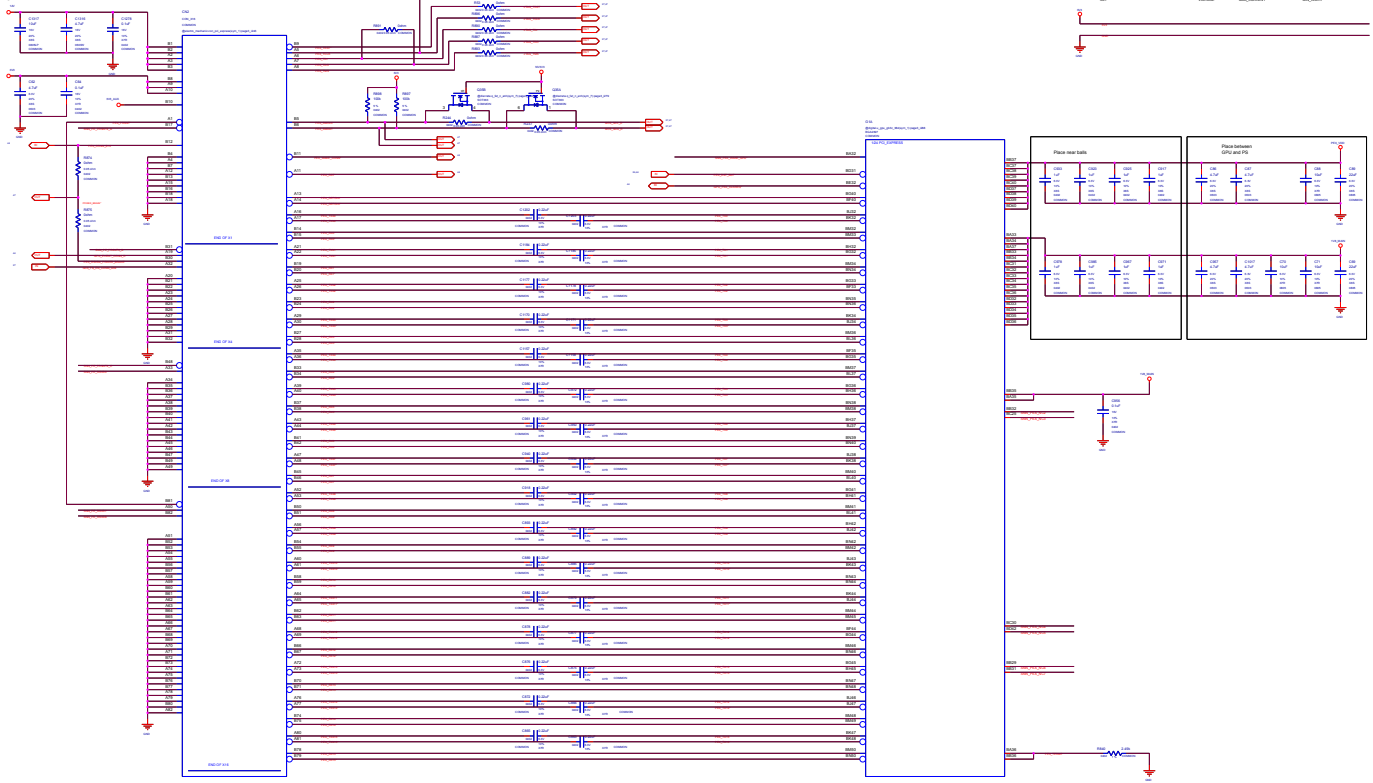
Page3: PCI Express



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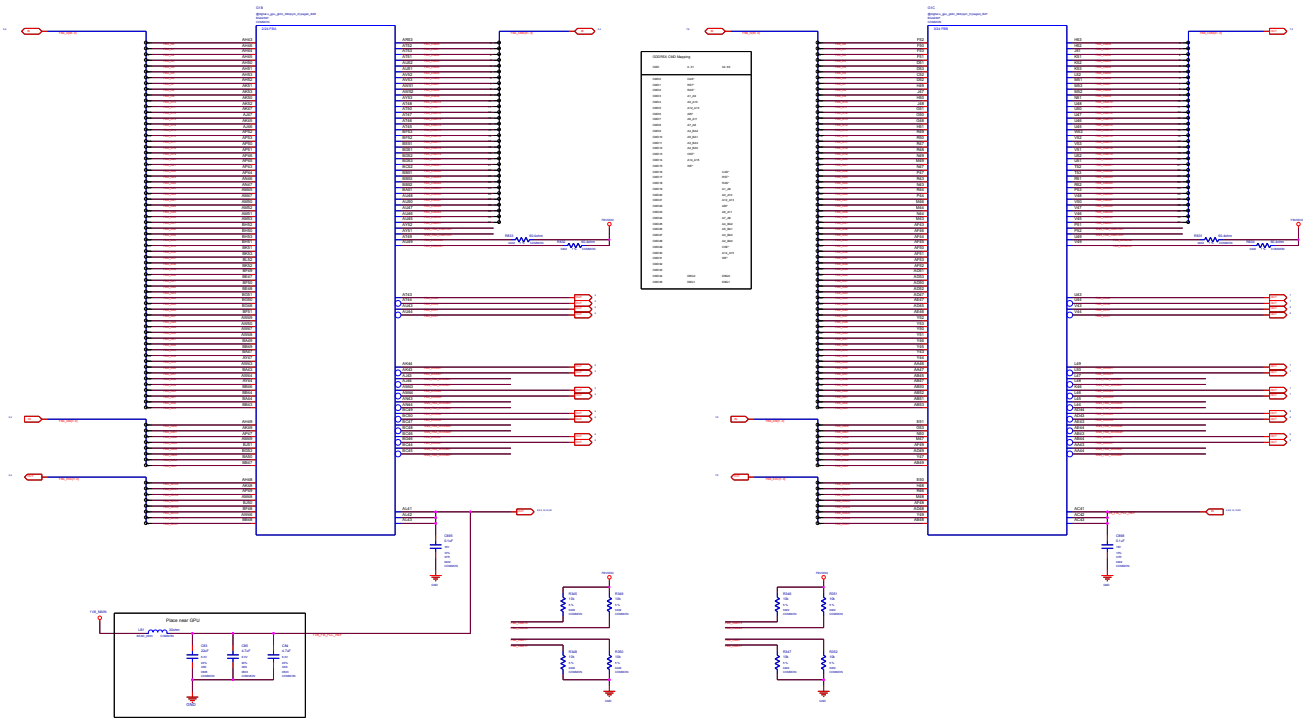
Page4: MEMORY: GPU Partition A/B



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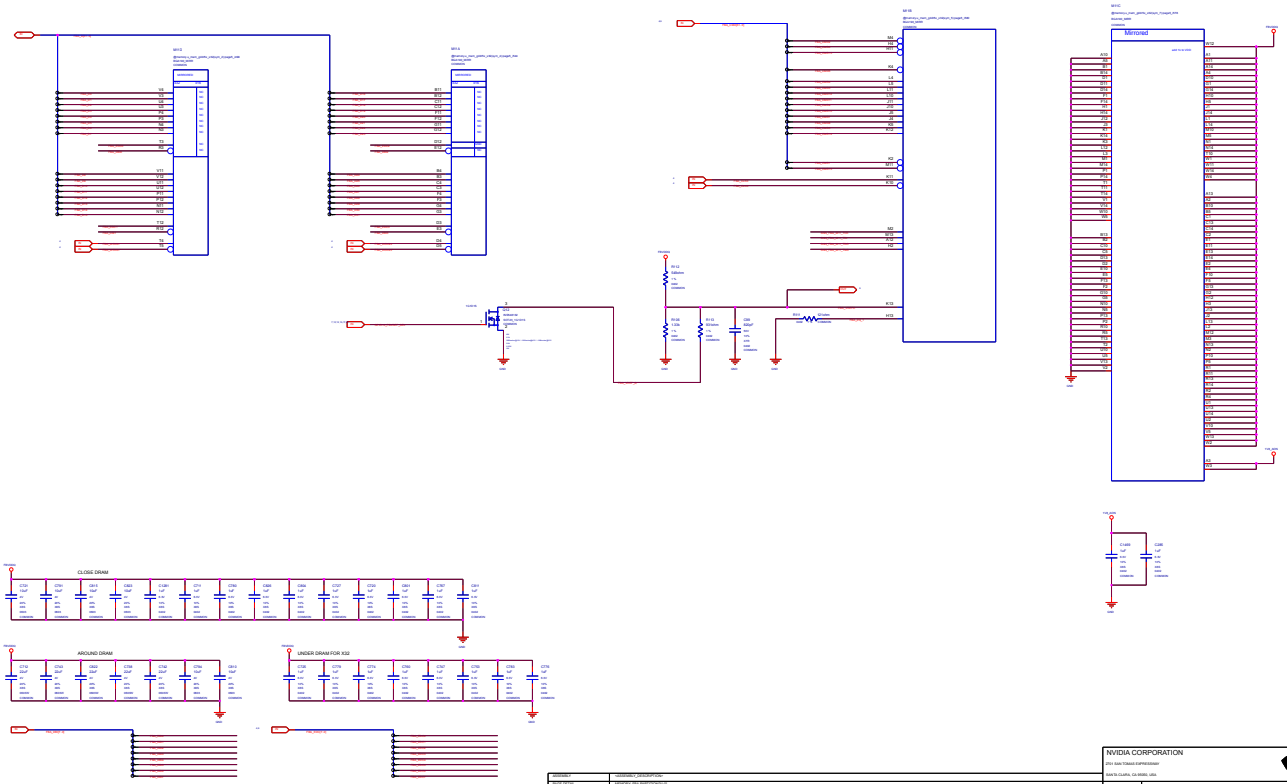

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PAGE 28 FBA	MEMORY: FBA PART-PAGE-15

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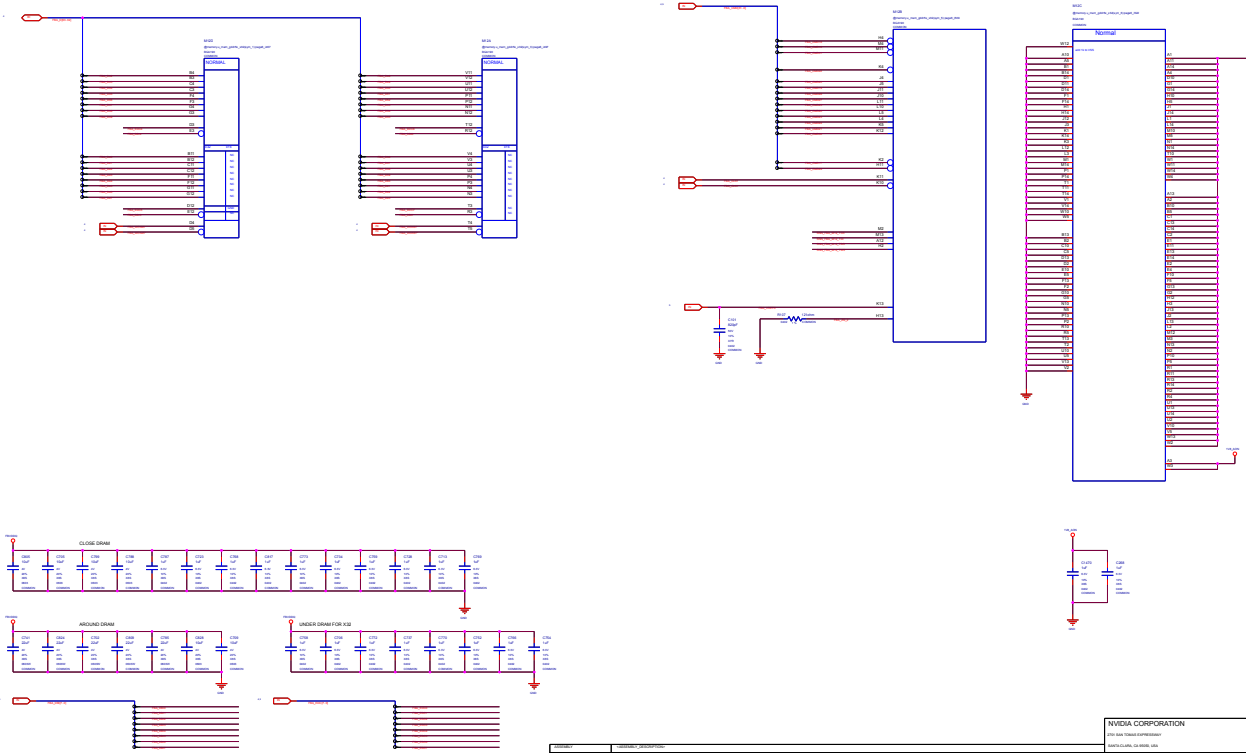
Page6: MEMORY: FBA Partition 63..32



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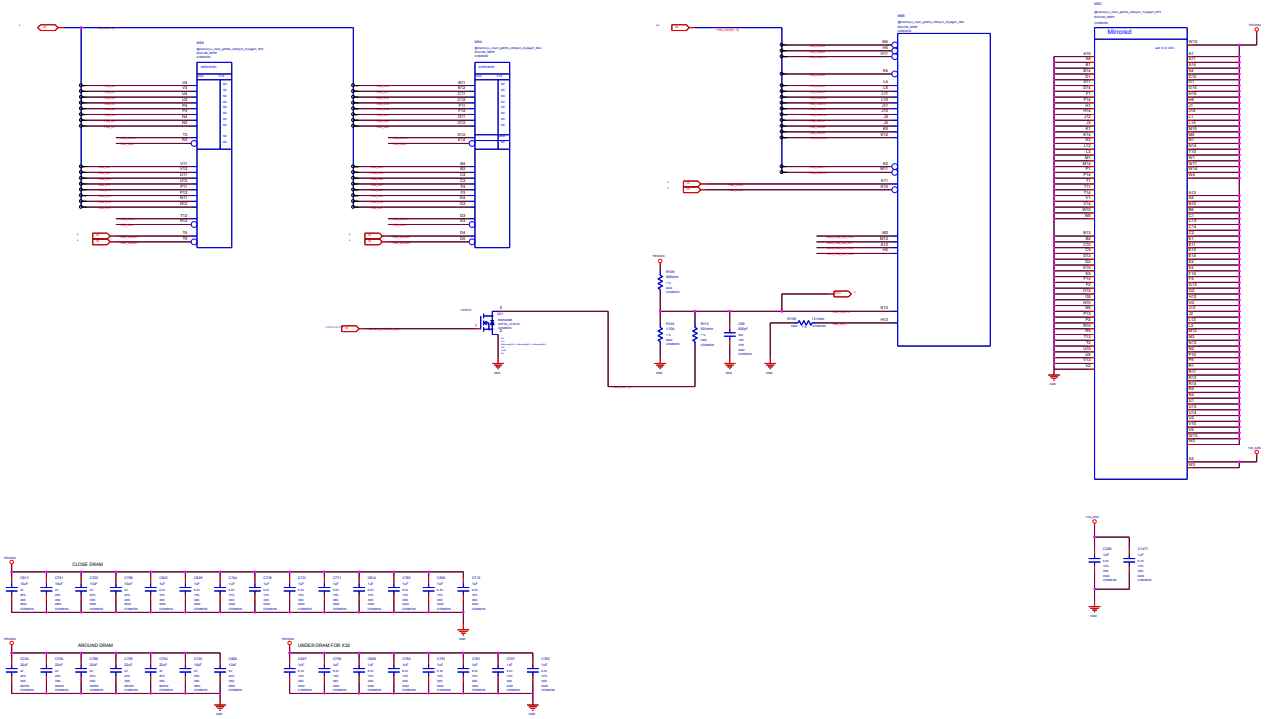
Page7: MEMORY: FBB Partition 31..0



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ASSEMBLY	ASSEMBLY_DESCRIPTION=
PART OF PN#	MEMORY FBB PARTITION31..0

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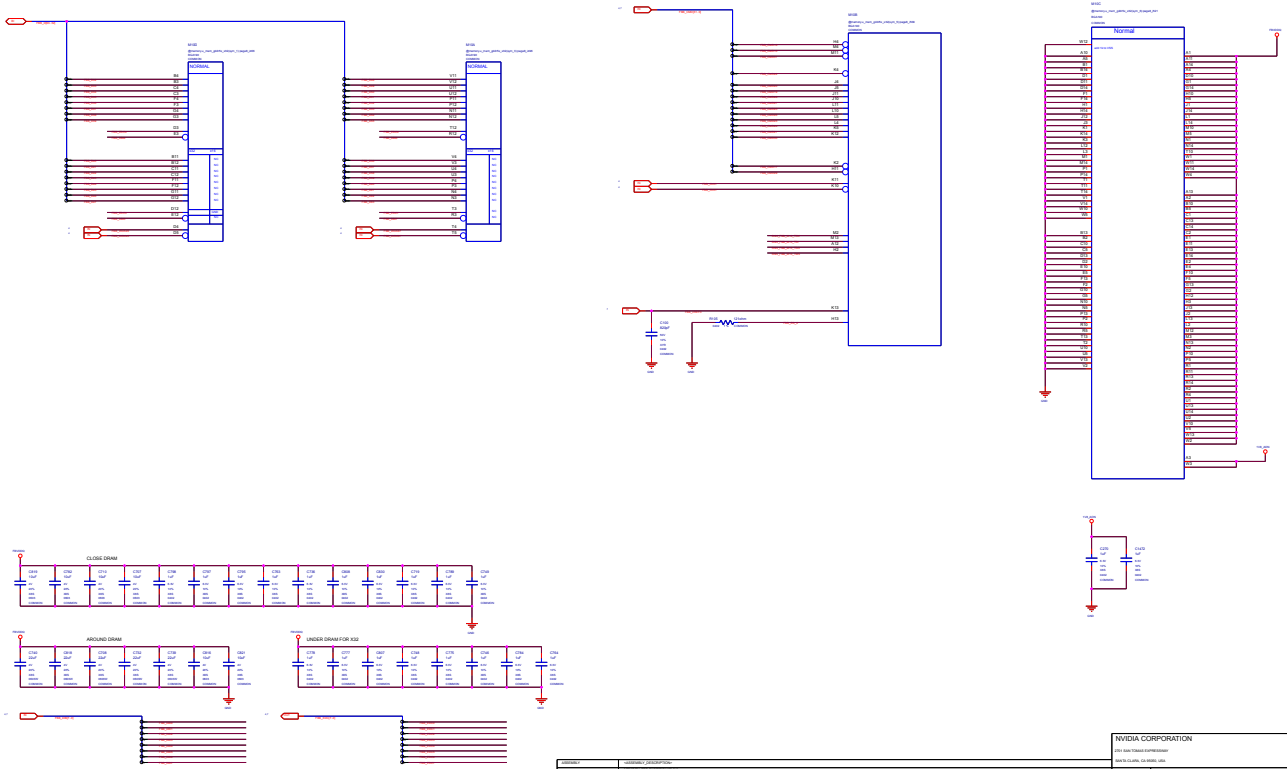
Page8: MEMORY: FBB Partition 63..32



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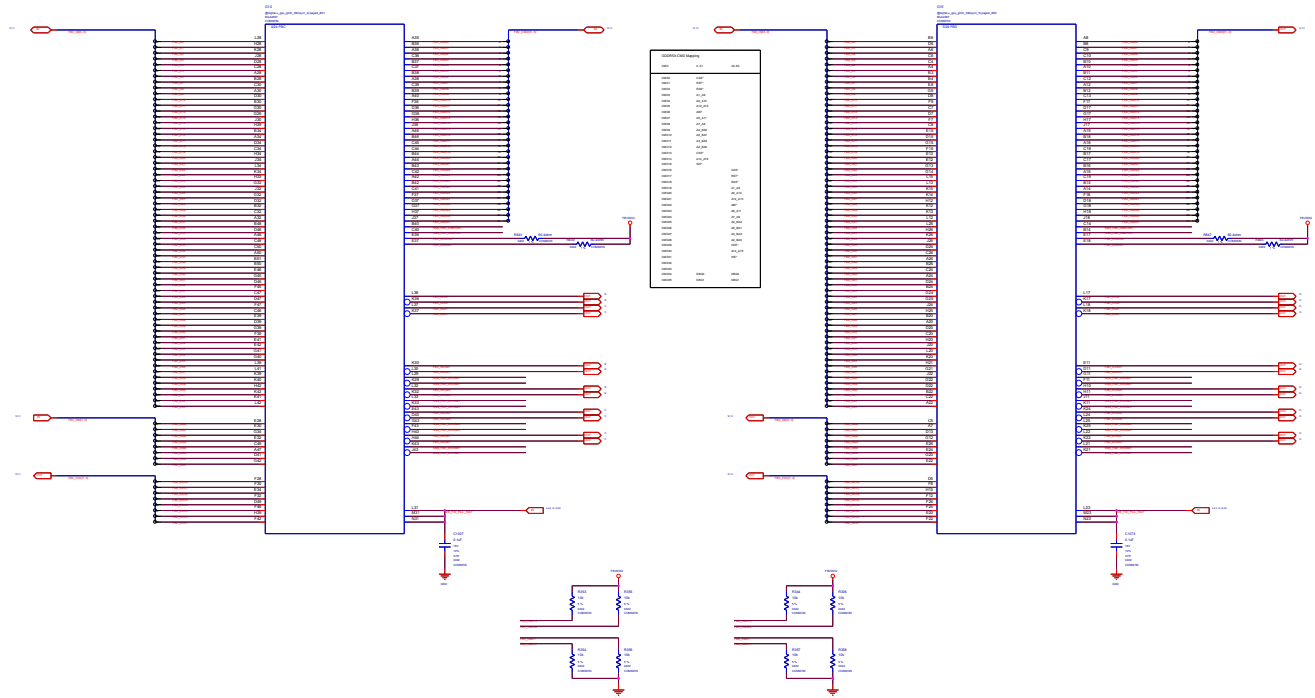
Page9: MEMORY: GPU Partition C/D



PROPRIETARY	WARNING / DISCRIPTION:		
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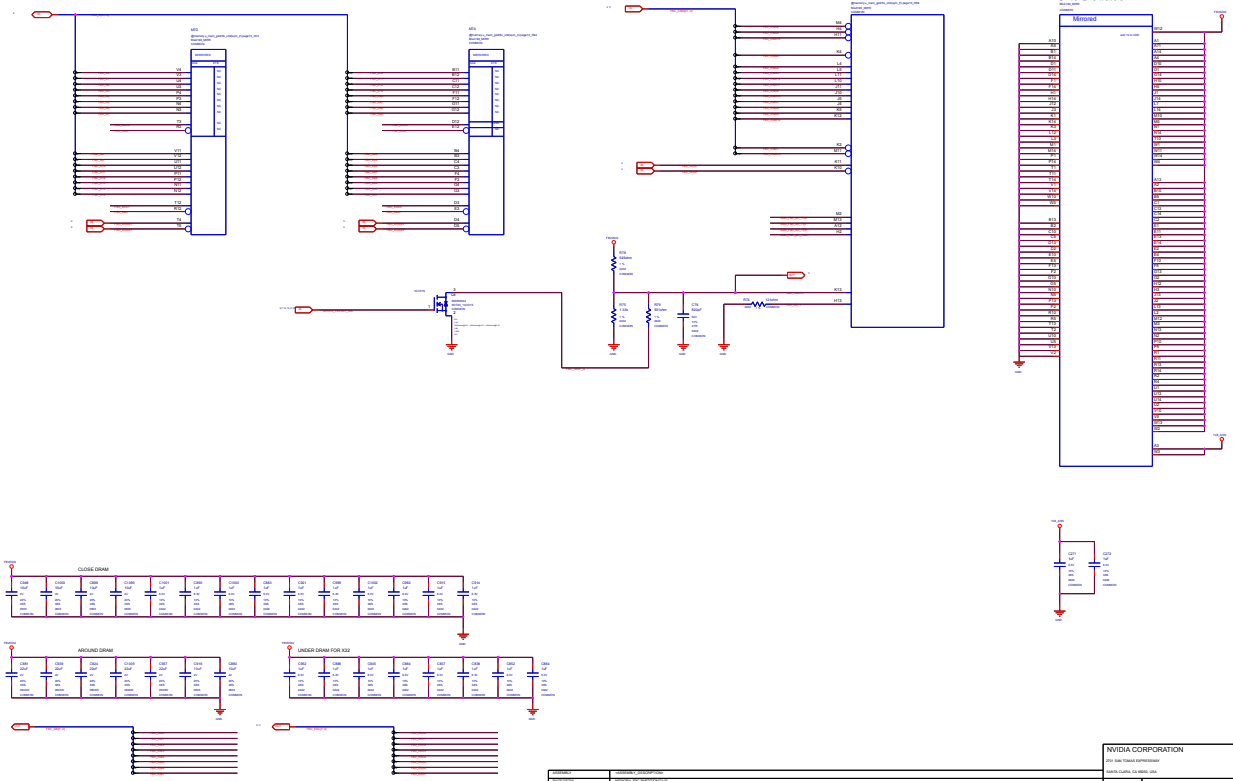
Page10: MEMORY: FBC Partition 31..0



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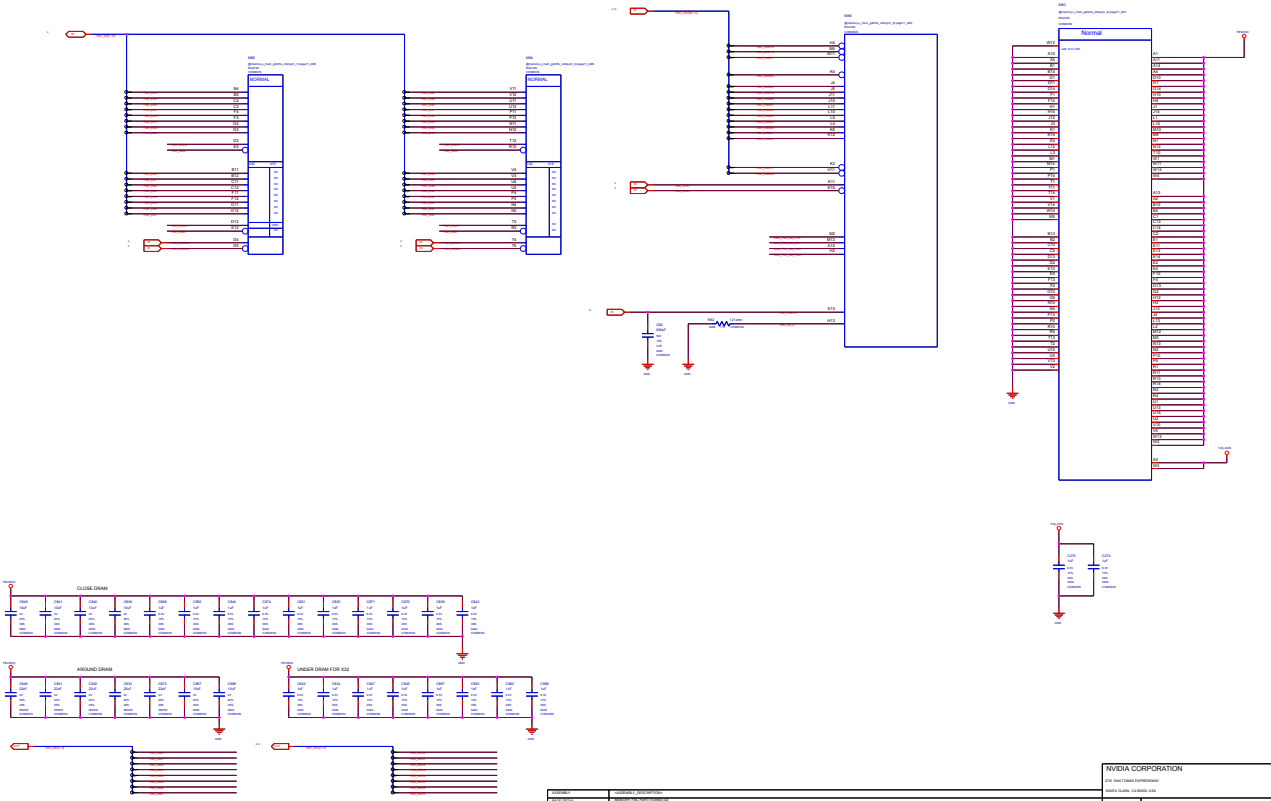
Page11: MEMORY: FBC Partition 63..32



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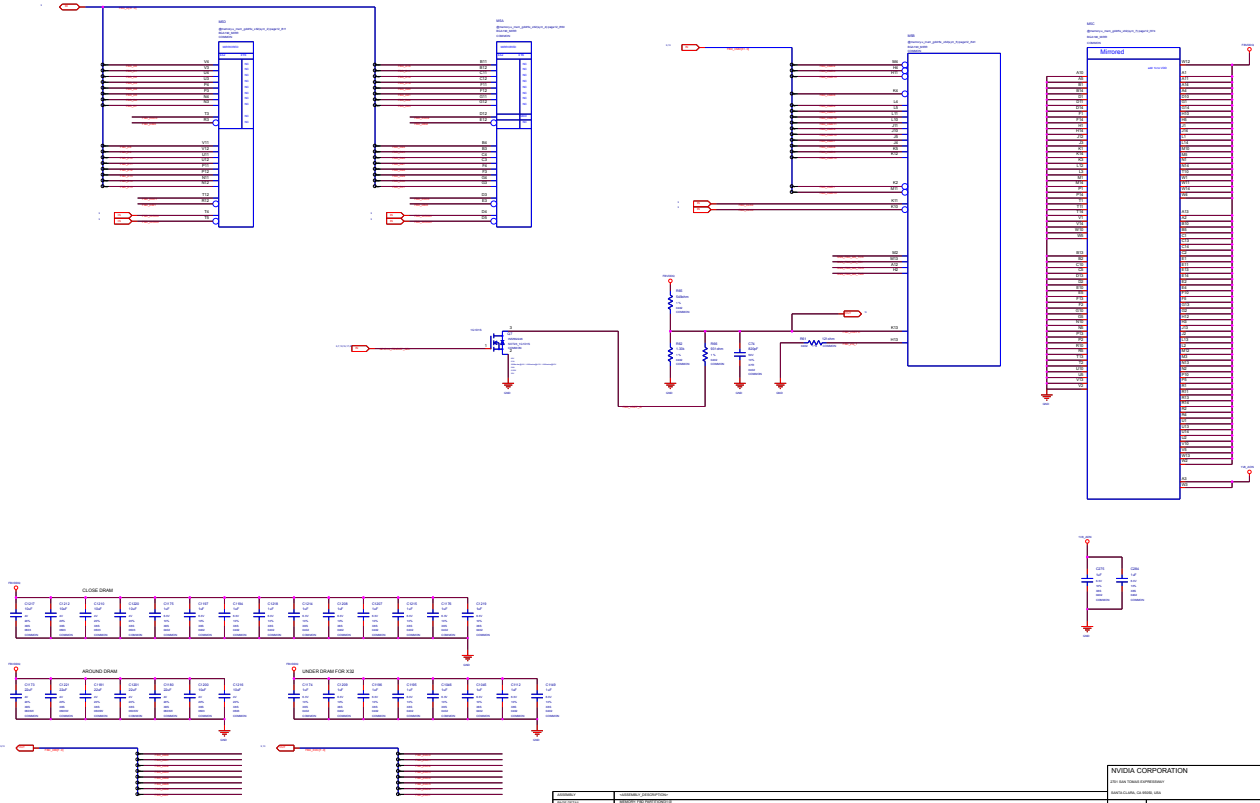

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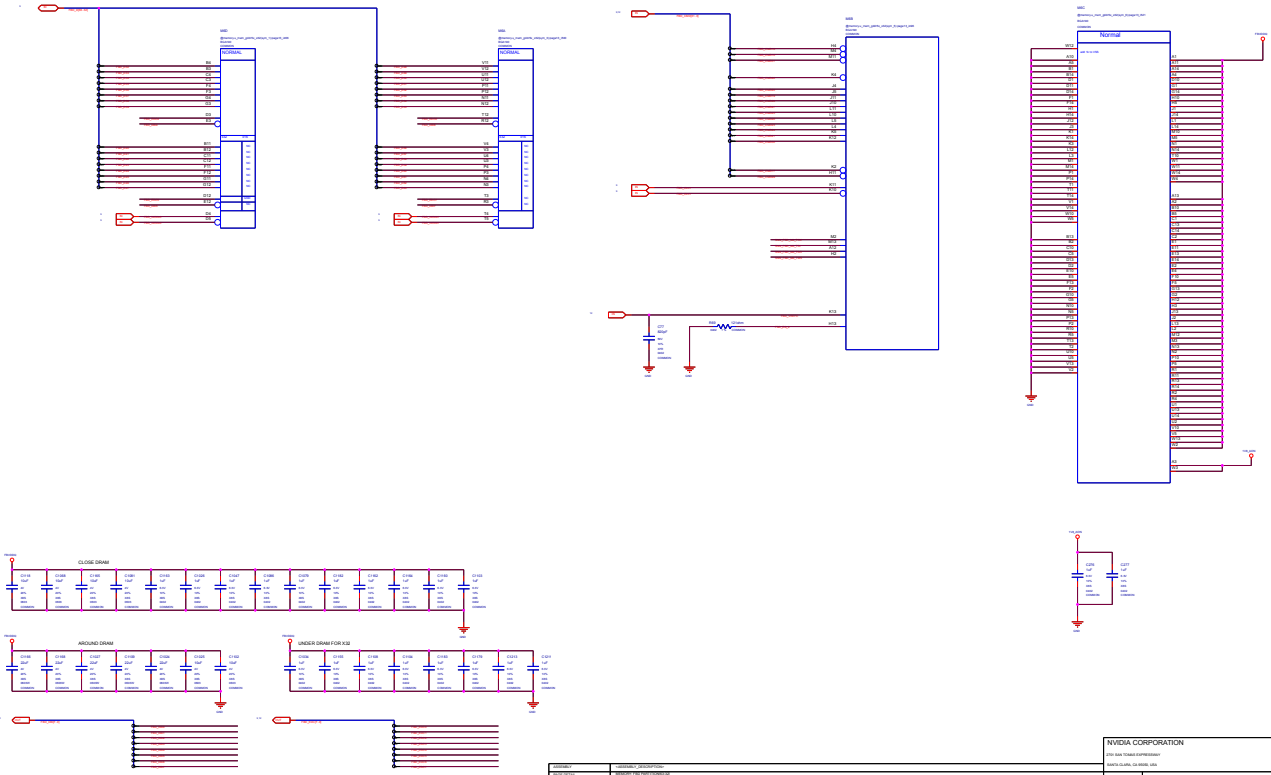
Page13: MEMORY: FBD Partition 63..32



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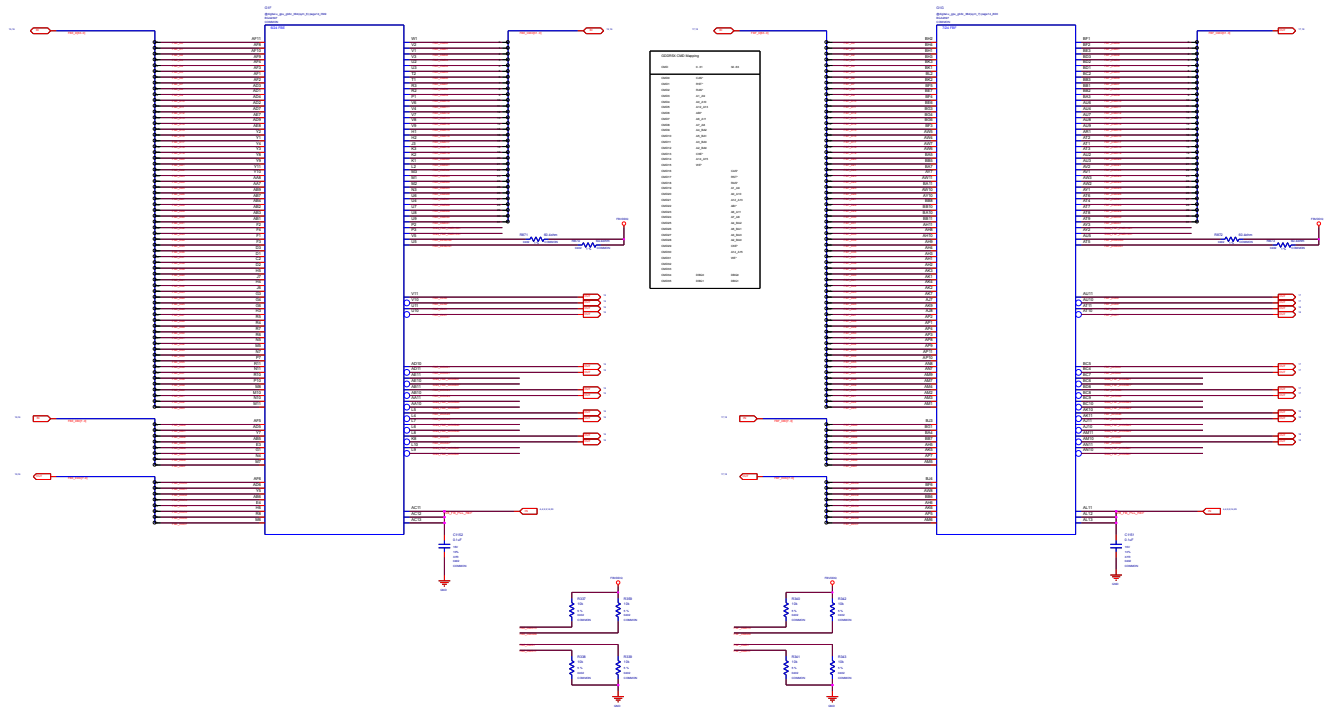
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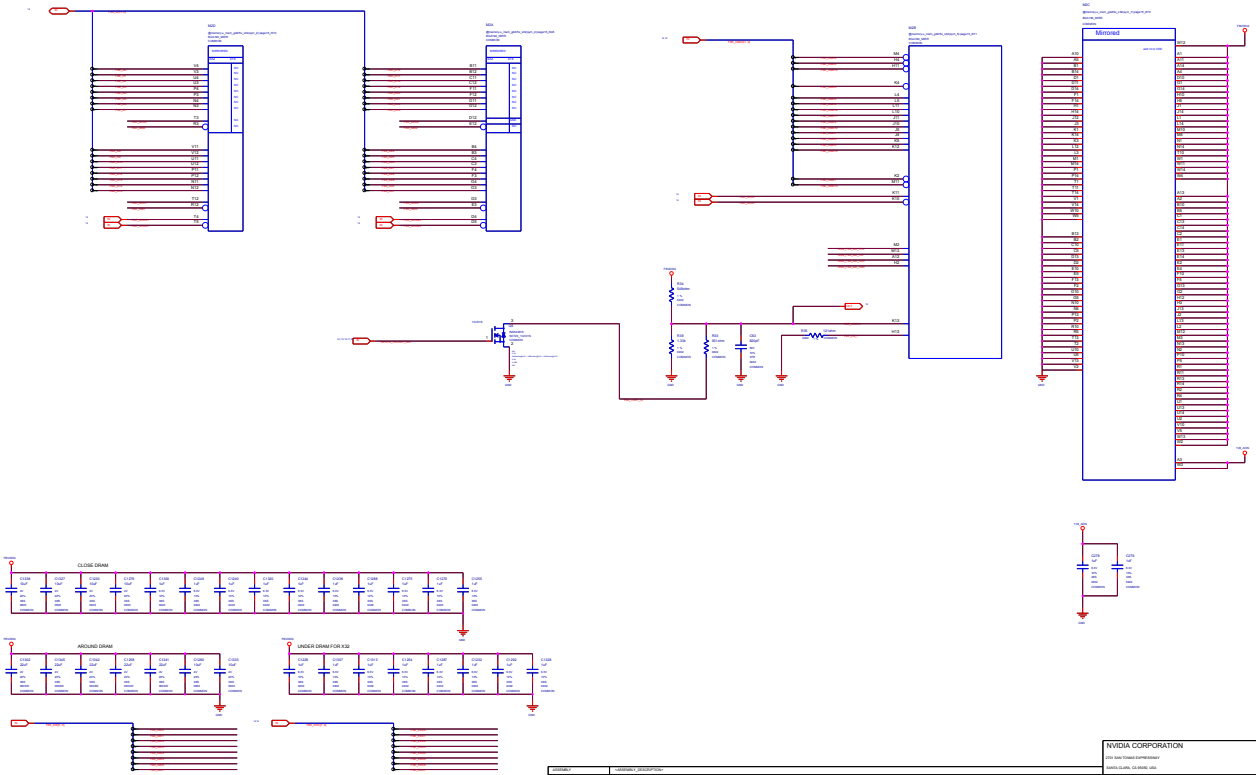

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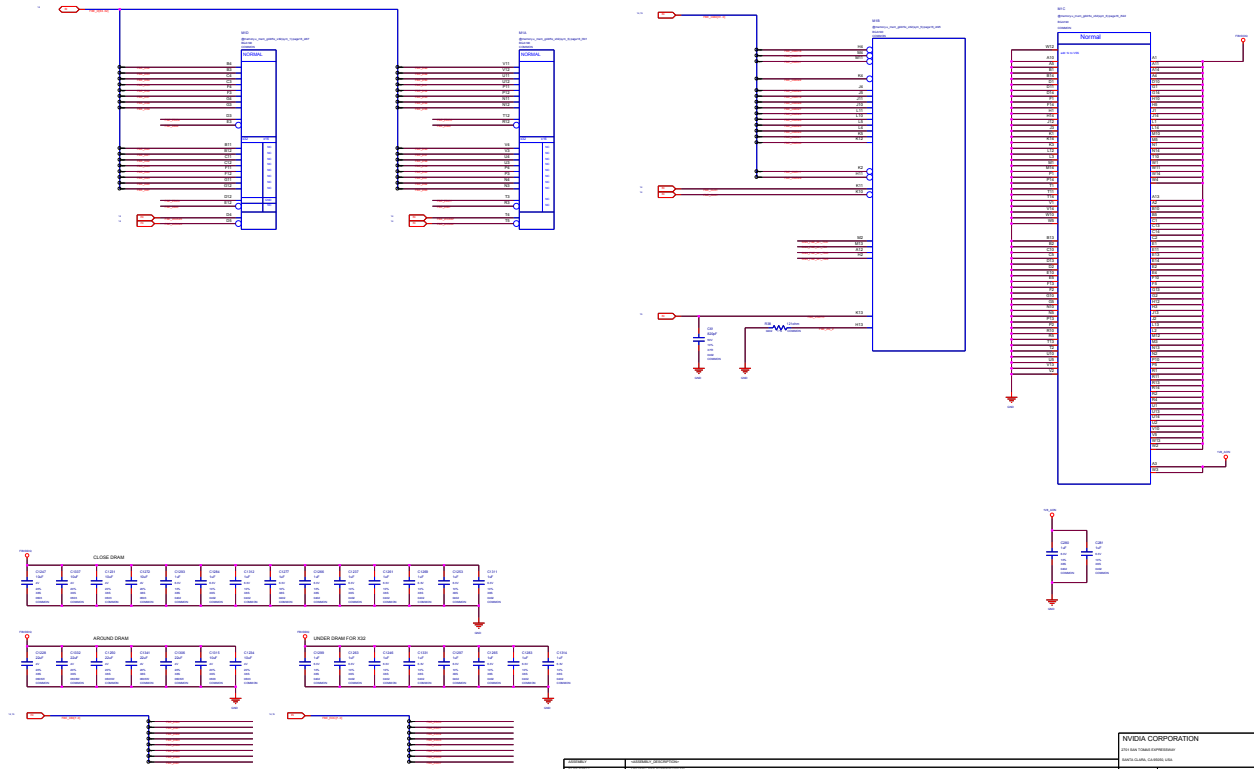

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PAGE TITLE	MEMORY: FBE PARTITION63-32

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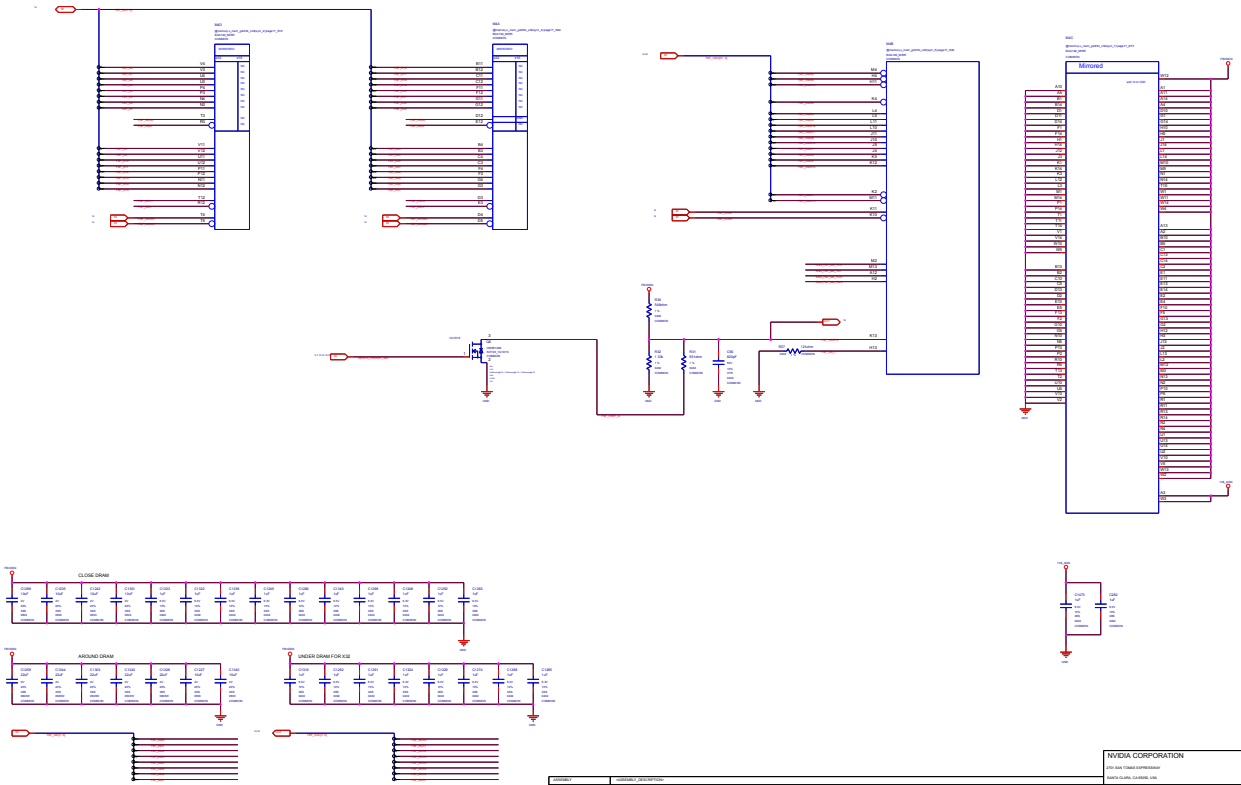

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE 18 OF 54	MEMORY: FBF PART-FIXED 18

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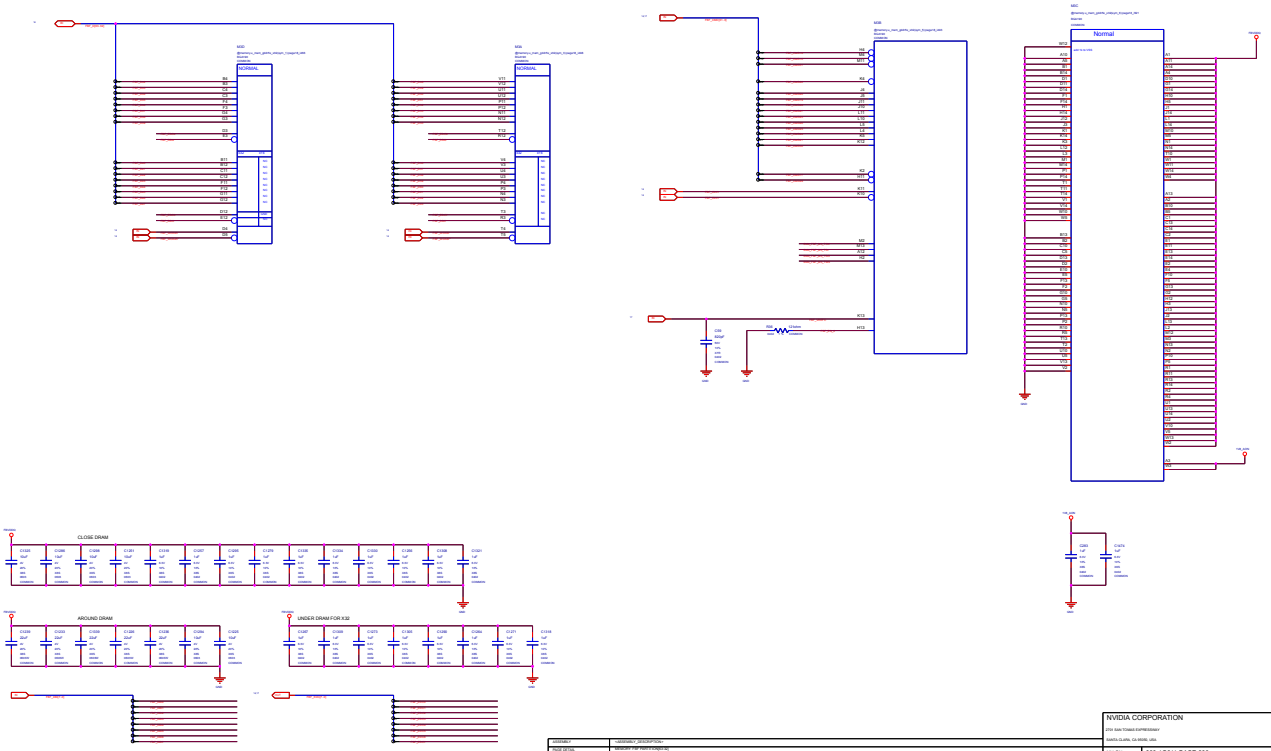
NV_PN	600-1G611-BASE-300		
PLANNER	PCB11 DATE	PAGE	17 OF 48
SCM REV	A	DATE	28-SEP-2016



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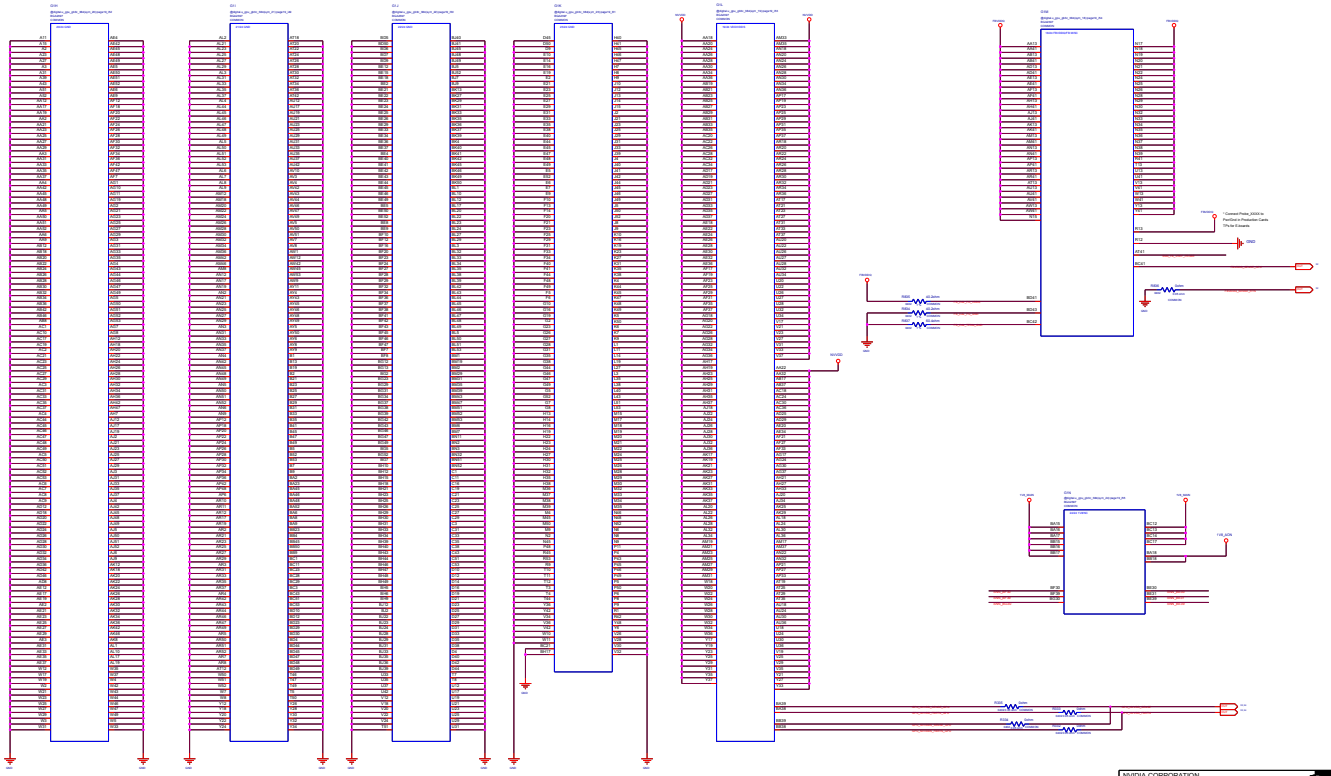
NV_PN	600-1G611-BASE-300		
PCB REV	PCB P1 CODE	PAGE	18 OF 68
SCM REV	A	DATE	08-SEP-2010

Page19: GPU PWR and GND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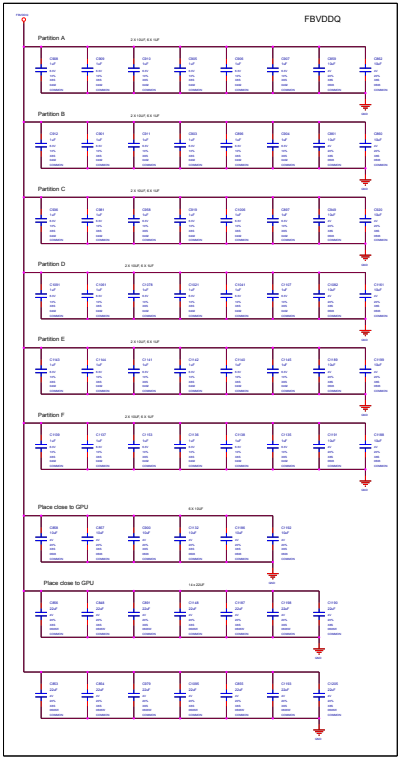
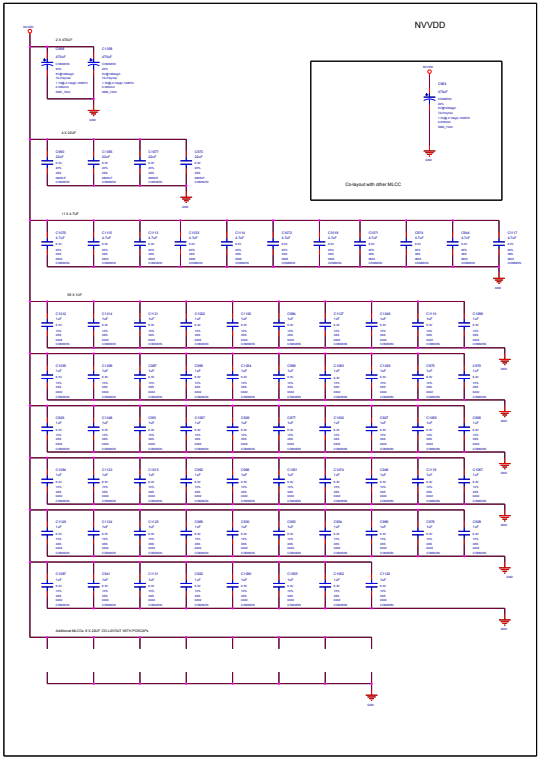
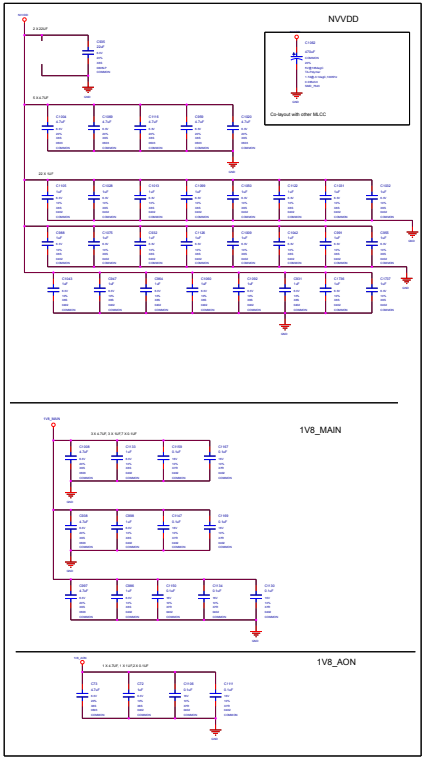
Page20: GPU Decoupling







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PROJECT	PROJECT-CODE	PAGE	20 OF 34
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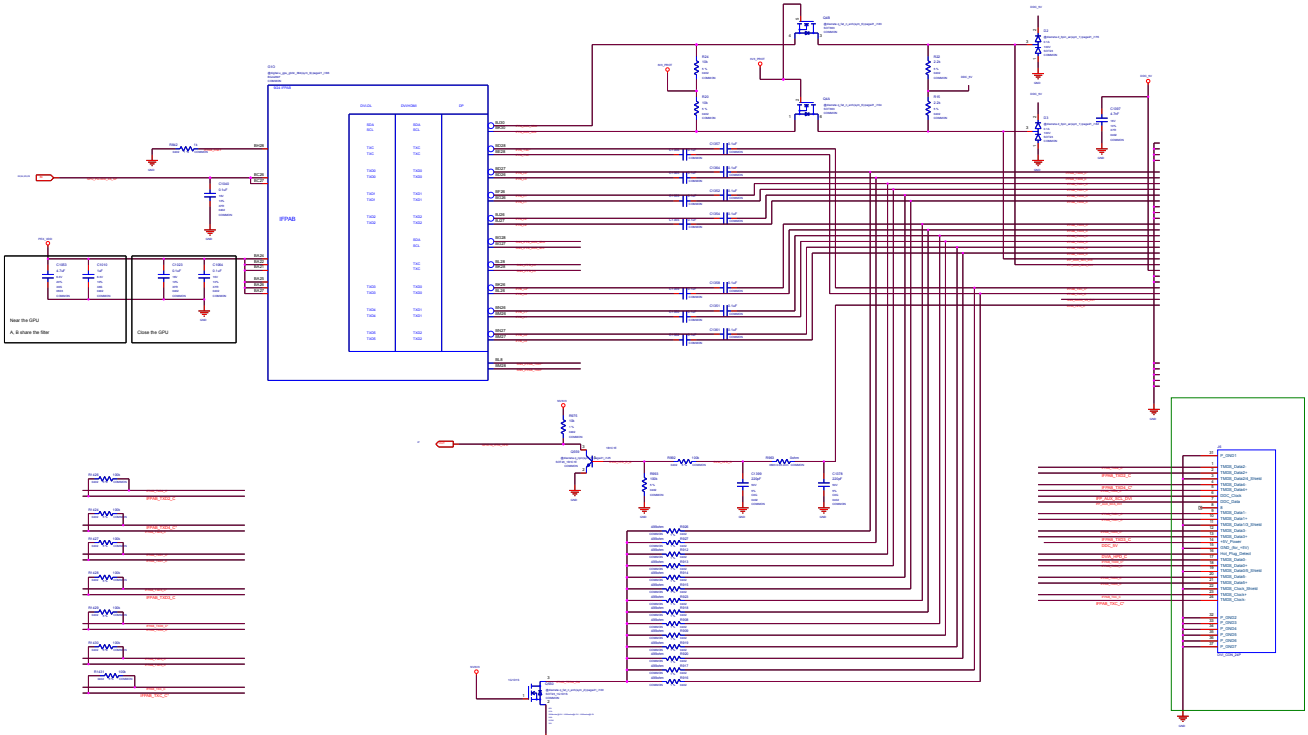

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MODEL/NAME	NV50/G84N-V_DVI-DCRT-DDM
PAGE CONTENT	IFPAB DVI-D-DL

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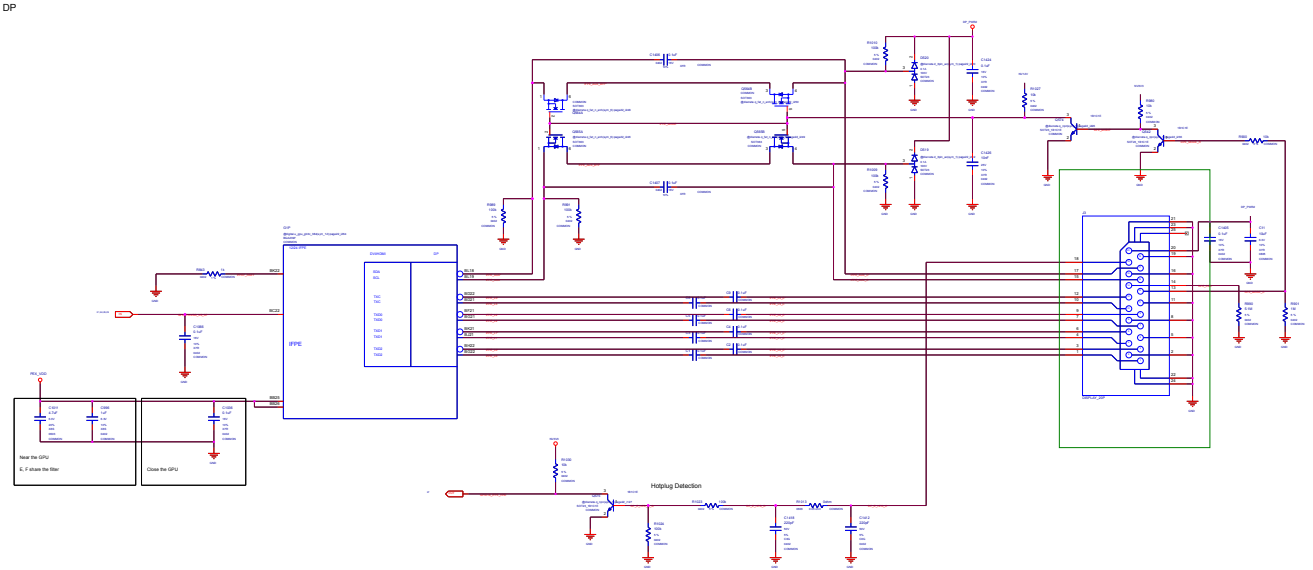
PCB REV	PROJECT CODE	PAGE	21 OF 28
SCHEMREV	A	DATE	28-SEP-2006

Page22: IFPE DP



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PAGE EDITED:	DPE DP

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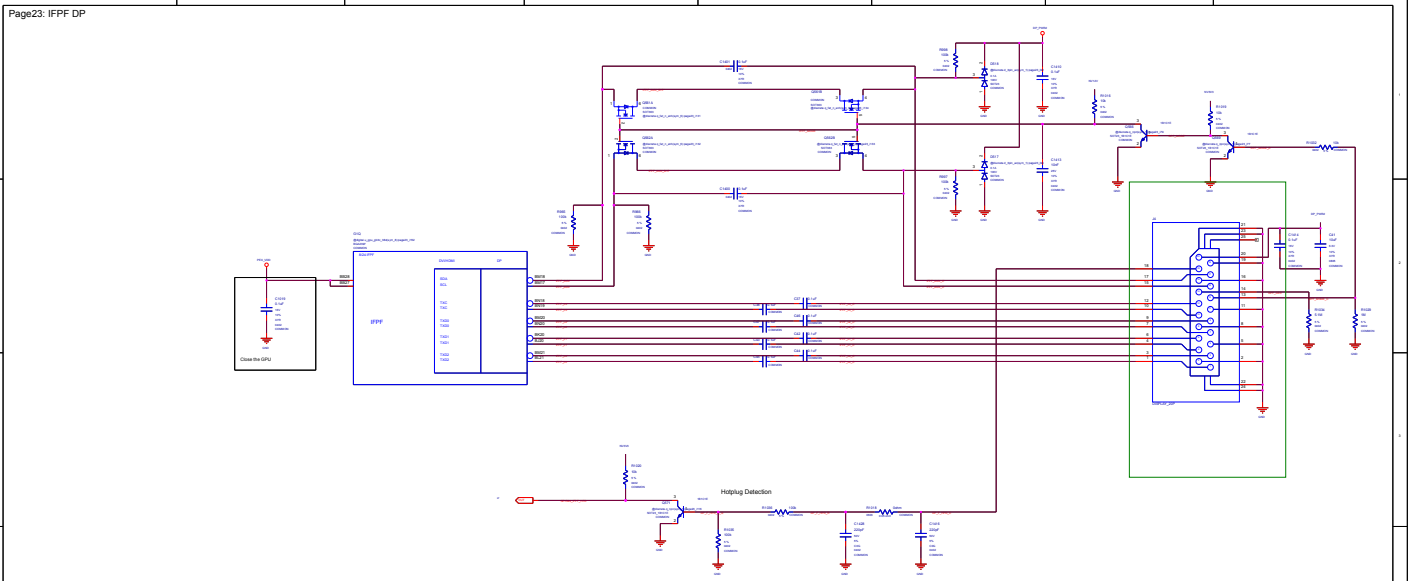
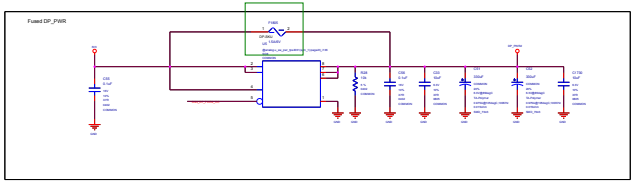
CAD REV	A	DATE	2010-07-07-15

Page23: IFPF DP





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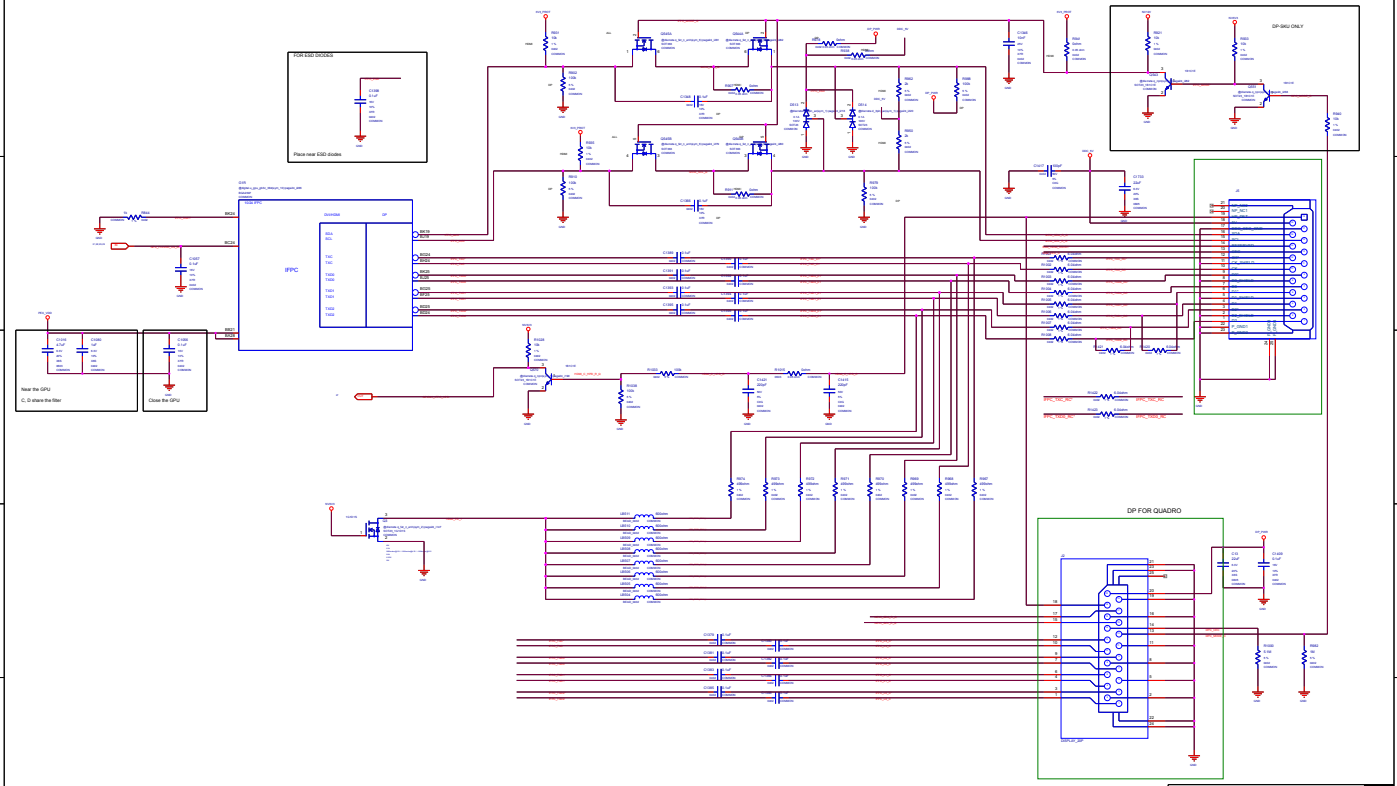
Page24: IFPC HDMI 2.0/DP



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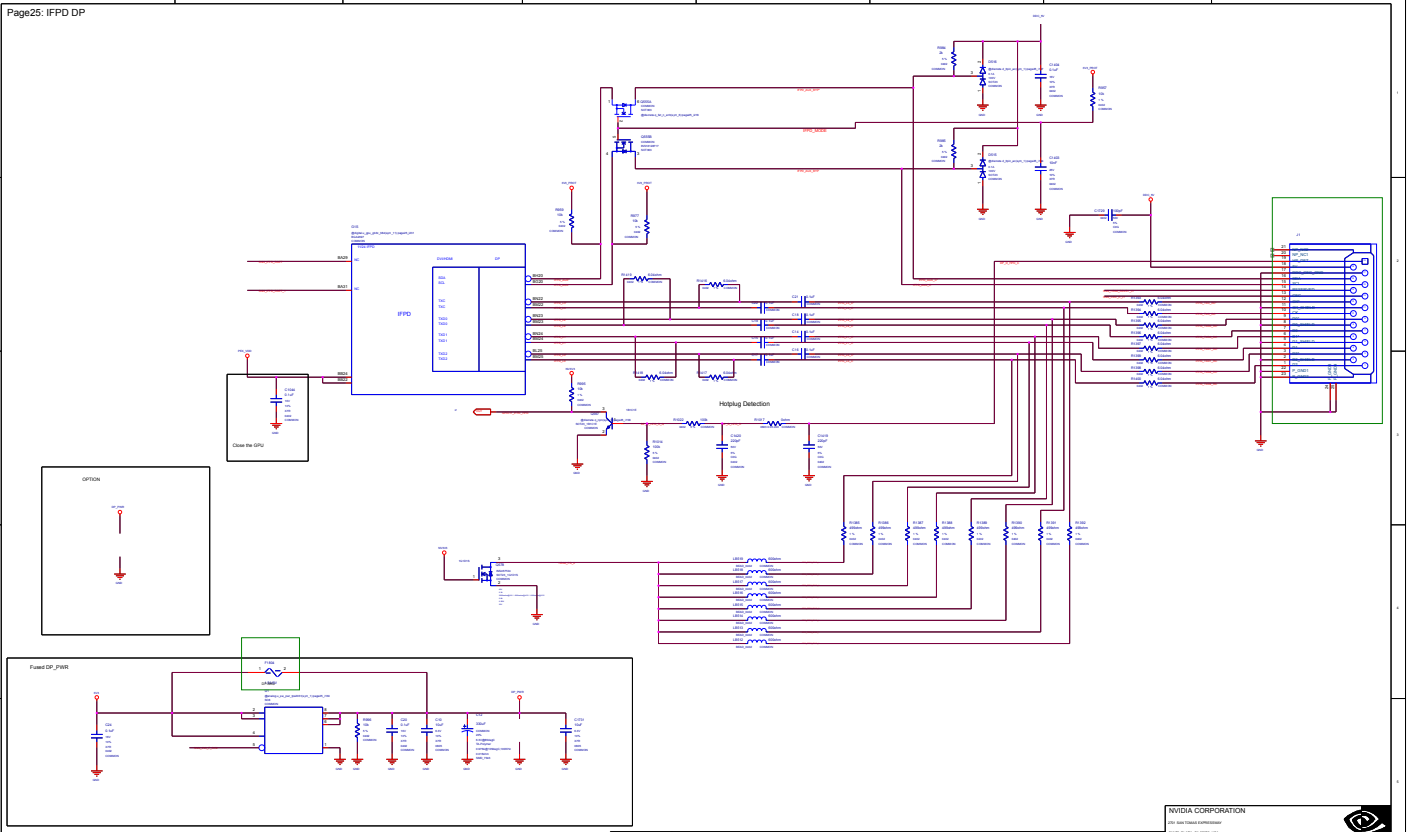
NV_PN	800-10611-BASE-300		
PCB REV	PCBDFT-1600	PAGE	25 OF 28
SCHEMA	0	DATE	08:08:08 2016

Page25: IFPD DP



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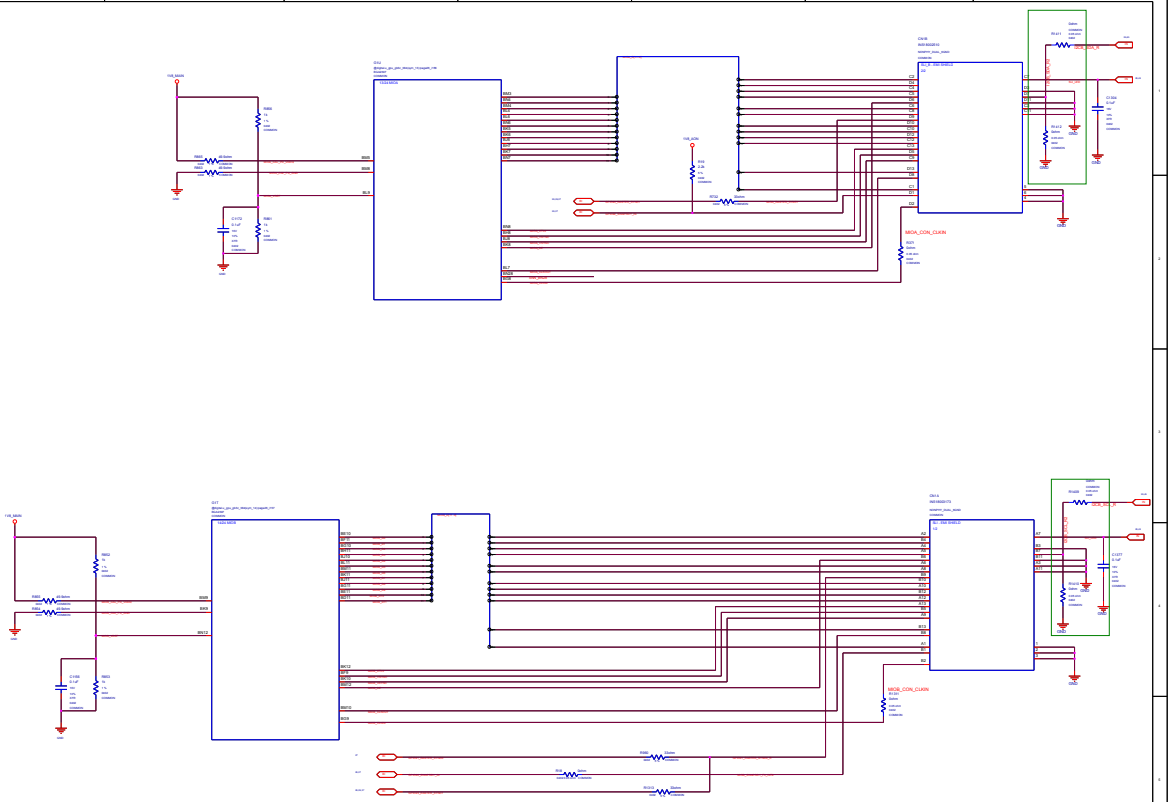
Page26: MIOA/B Interface and FRAME LOCK



WARRANTY	<WARRANTY_DESCRIPTION>
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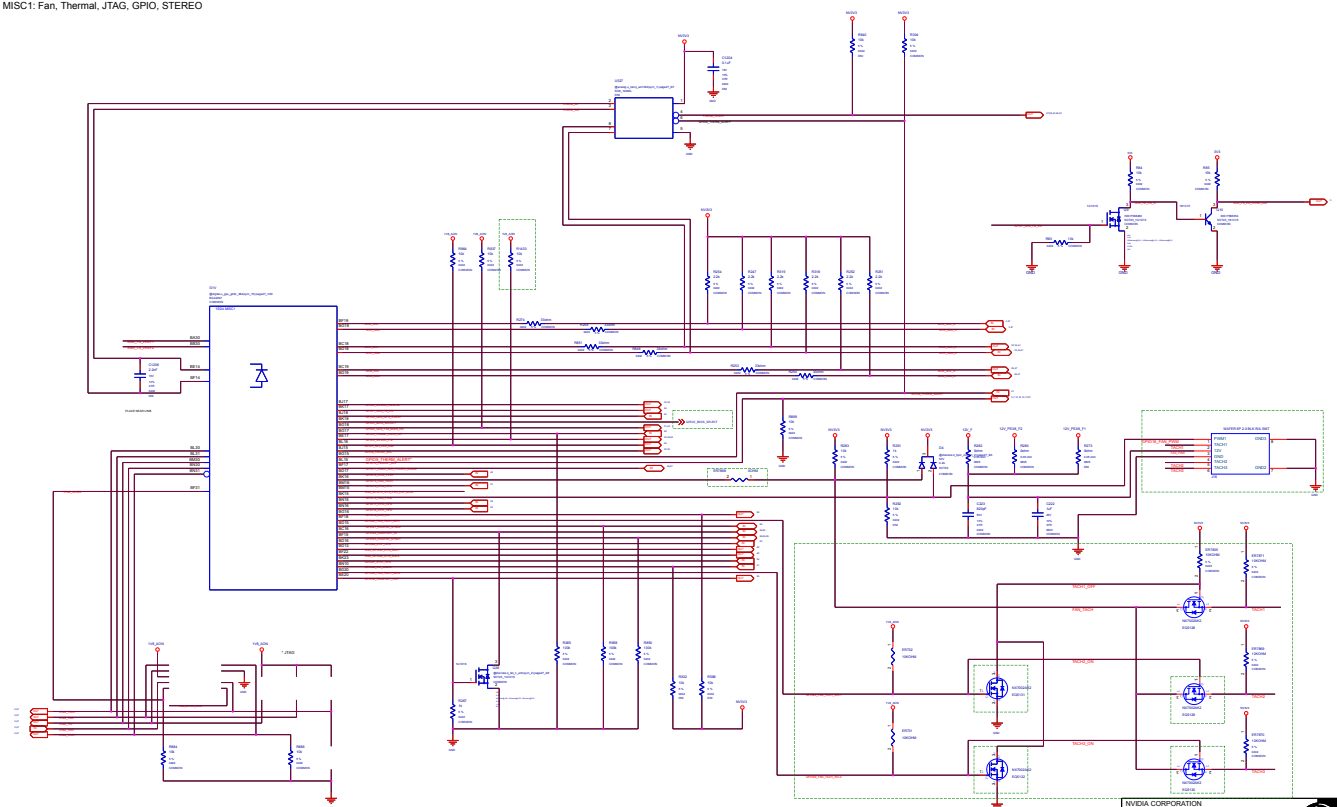
Date/Time	X	Date	04-SEP-2018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Page28: MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	L	H	00001	
L	H	L	00010	MICRON 12Gbps REV.B
L	H	H	00011	
H	L	L	00100	

ROM_SO	ROM_SI	ROM_SCLK	SCR_EXPOSEDQ[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SCR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

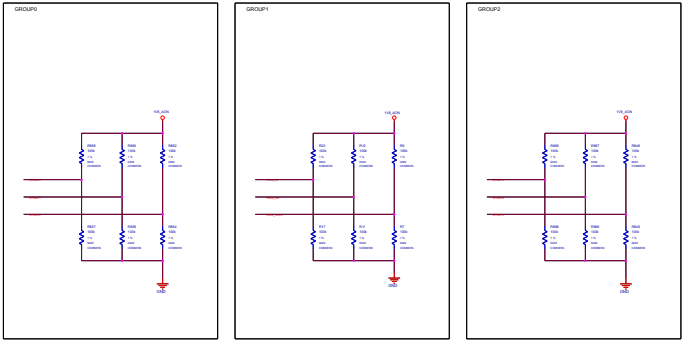
H=High :Tied to 1.8V
M=Middle Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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ASSEMBLY	
PAGE 28 OF 64	MISC: ROM, STRAPS

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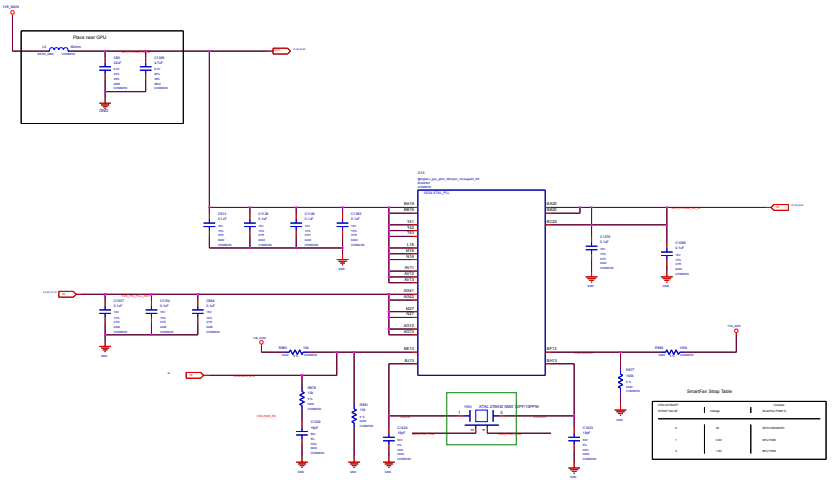
PCB REV	PCB11.0-B0	PAGE	28 OF 28
SCM REV	A	DATE	20-SEP-2016

Page29: MISC2: XTAL, PLL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: XTAL, PLL

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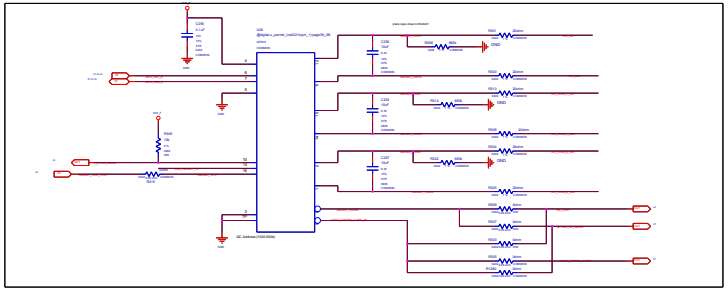
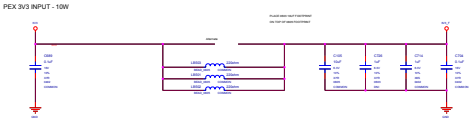
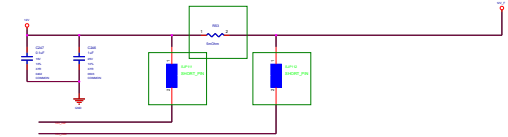
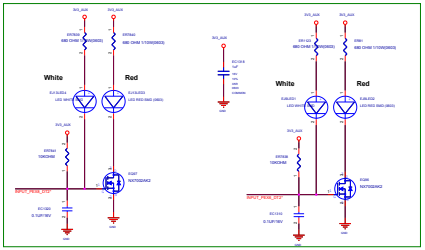
SCM REV	0	DATE	08:58PM 06-07-16

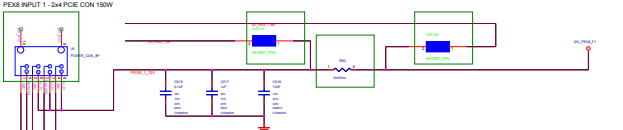
Page41: PS: Inputs, Filtering, and Monitoring

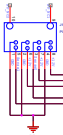


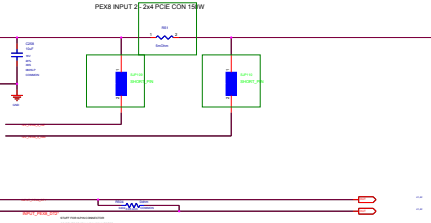












ASSEMBLY:	ASSEMBLY_DESCRIPTION:
P6081-0216a	PS: Inputs Filtering, and Monitoring

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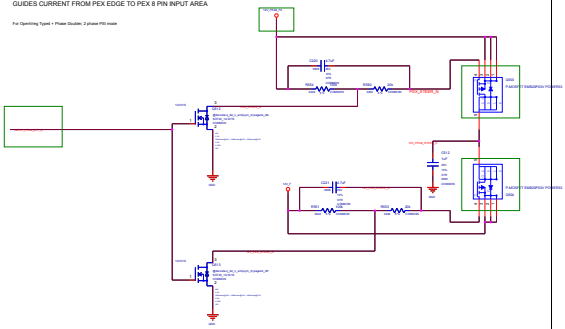
Page42: PS: 12V Current Steering & Hot Unplug Detect

QUADRO/TESLA:

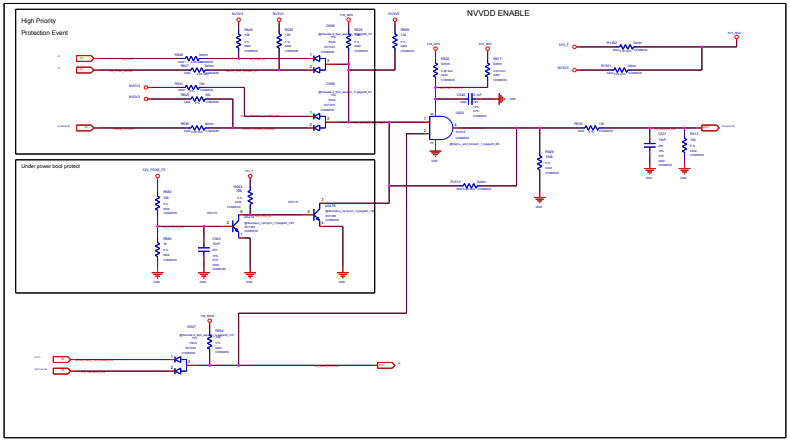
12V CURRENT STEERING (UNDER POWER BOOT):

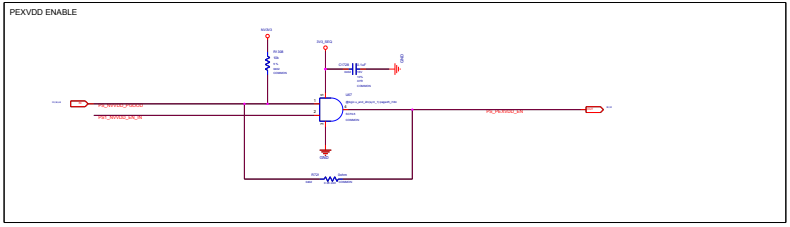
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVolting Typed + Phase Doubler, 2 phase PSI mode


12V_PEX_EDGE_IN
Q512
Q513
Q514
Q515
R512
R513
R514
R515
C512
C513
C514
C515
12V_PEX_EDGE_OUT
12V_PEX_EDGE_OUT_F
12V_PEX_EDGE_OUT_F_F
12V_PEX_EDGE_OUT_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F
12V_PEX_EDGE_OUT_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F_F

Page43: PS: NVVDD ENABLE





ASSEMBLY	A-0101A8-P_0100_RPT1GHz
PAGE OF 100	PS: NVVDD ENABLE

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SCHEMATIC	A	DATE	28-SEP-2015

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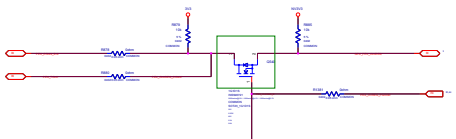
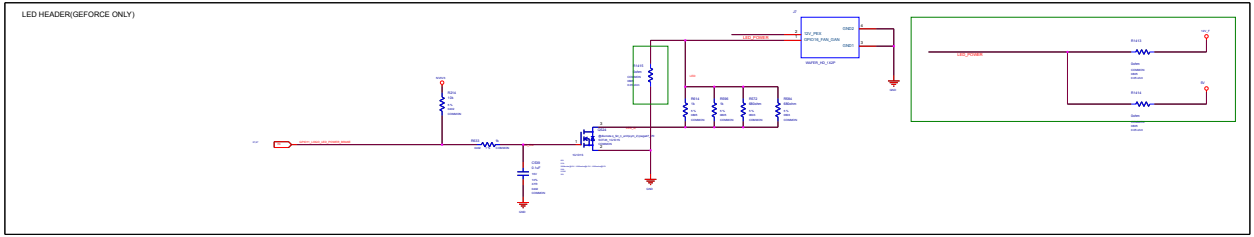
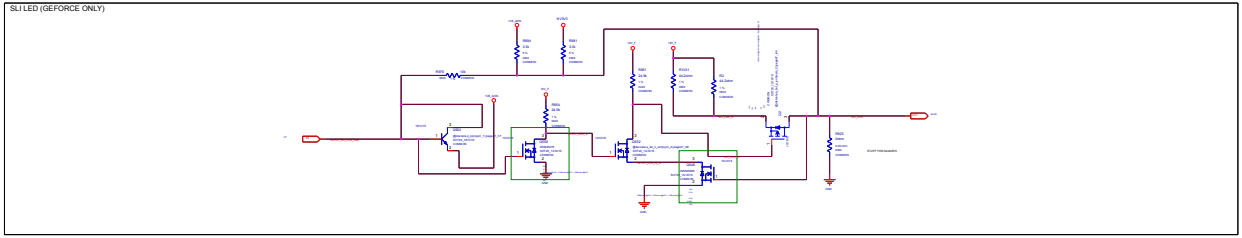
PEX_CLKREQ*



Page45:GEFORCE LED & SLI LED





ASSEMBLY	ASSEMBLY_DESCRIPTION
PBGE-22164	GEFORCE-LED-BRD Rev-001

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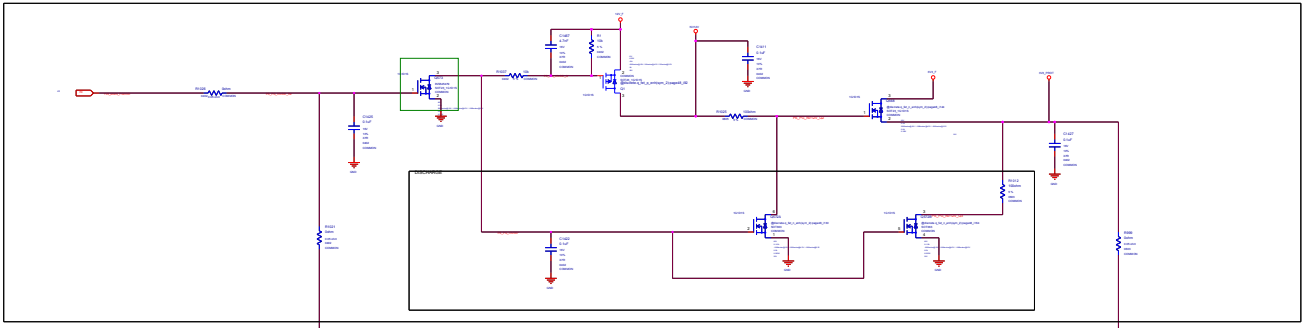
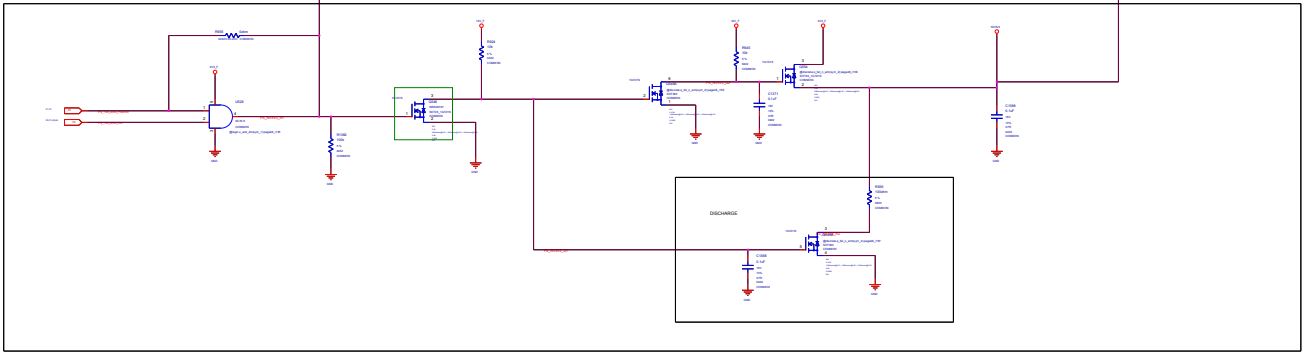
NV_PN	800-1G611-BASE-300		
TITLE REV	TITLE01-000	PAGE	45 OF 84
DRAWN BY		DATE	20-SEP-2010





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS:NV3V3, NV12V

DILI: NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS". THE MATERIALS MAY CONTAIN ERRORS AND OMISSIONS. VOLUTIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

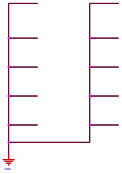
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_ZIN	800-1G611-BASE-300		
PCB REV	PCB11.0 DEC	PAGE	63 OF 98
ECN REV	0	DATE	30-SEP-2016

Brackets:

Bracket Screw

GPU HEATLINK

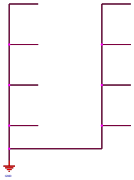
Mechanical Holes Symbol



GPU Stiffener (BRING-UP COOLER)

STIFFENER

GPU HOLES SYMBOL



QUAL COOLER STIFFENER

BOARD BACK PLATE

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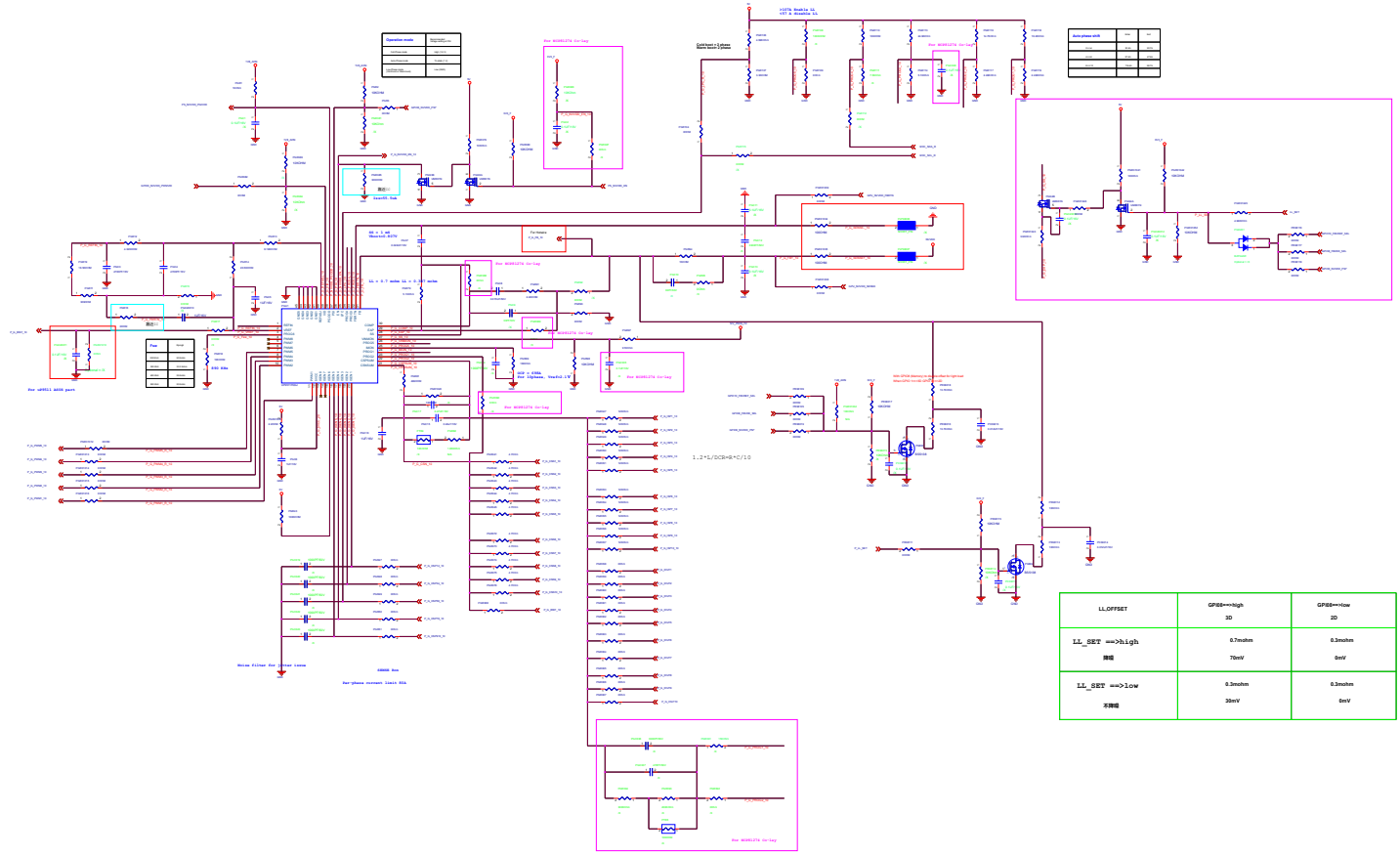
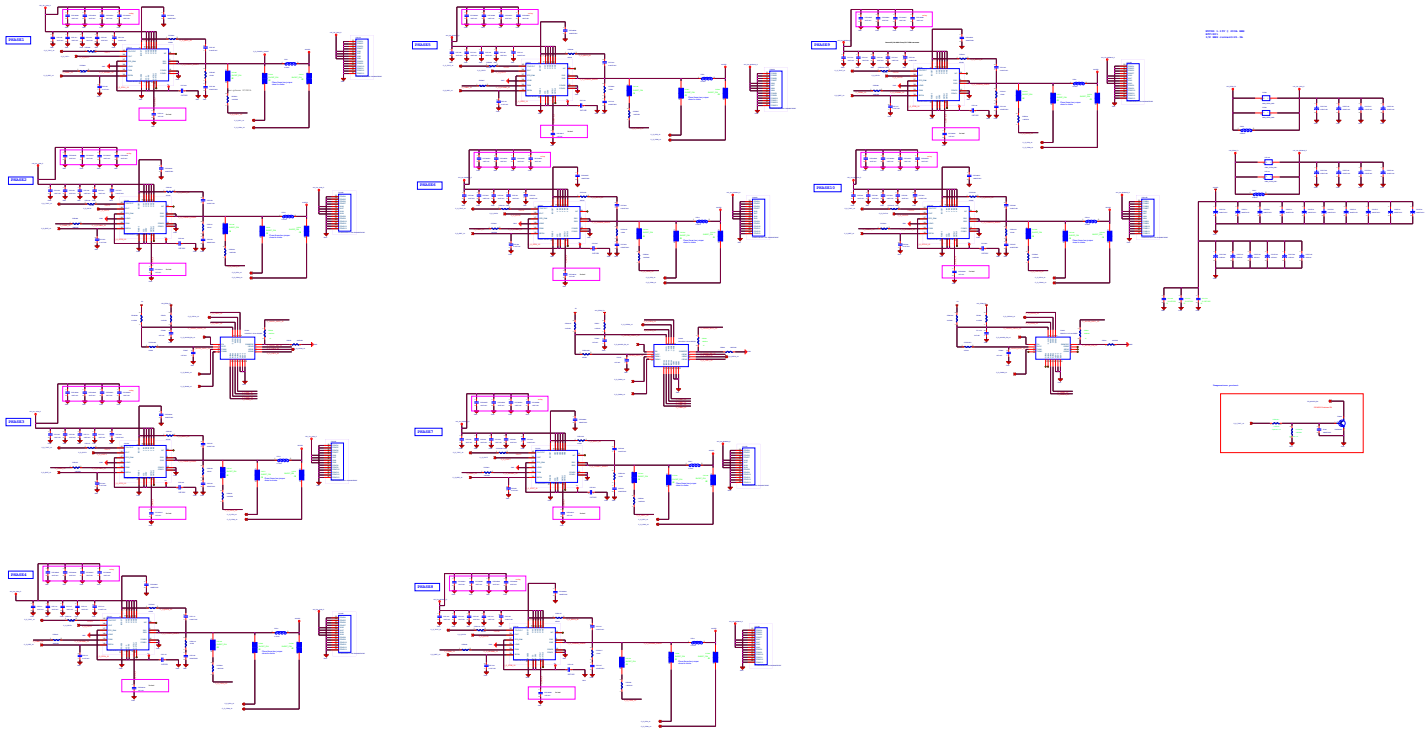
ASSEMBLY	~ASSEMBLY_DESCRIPTION~
FROM DFTAR	MECH

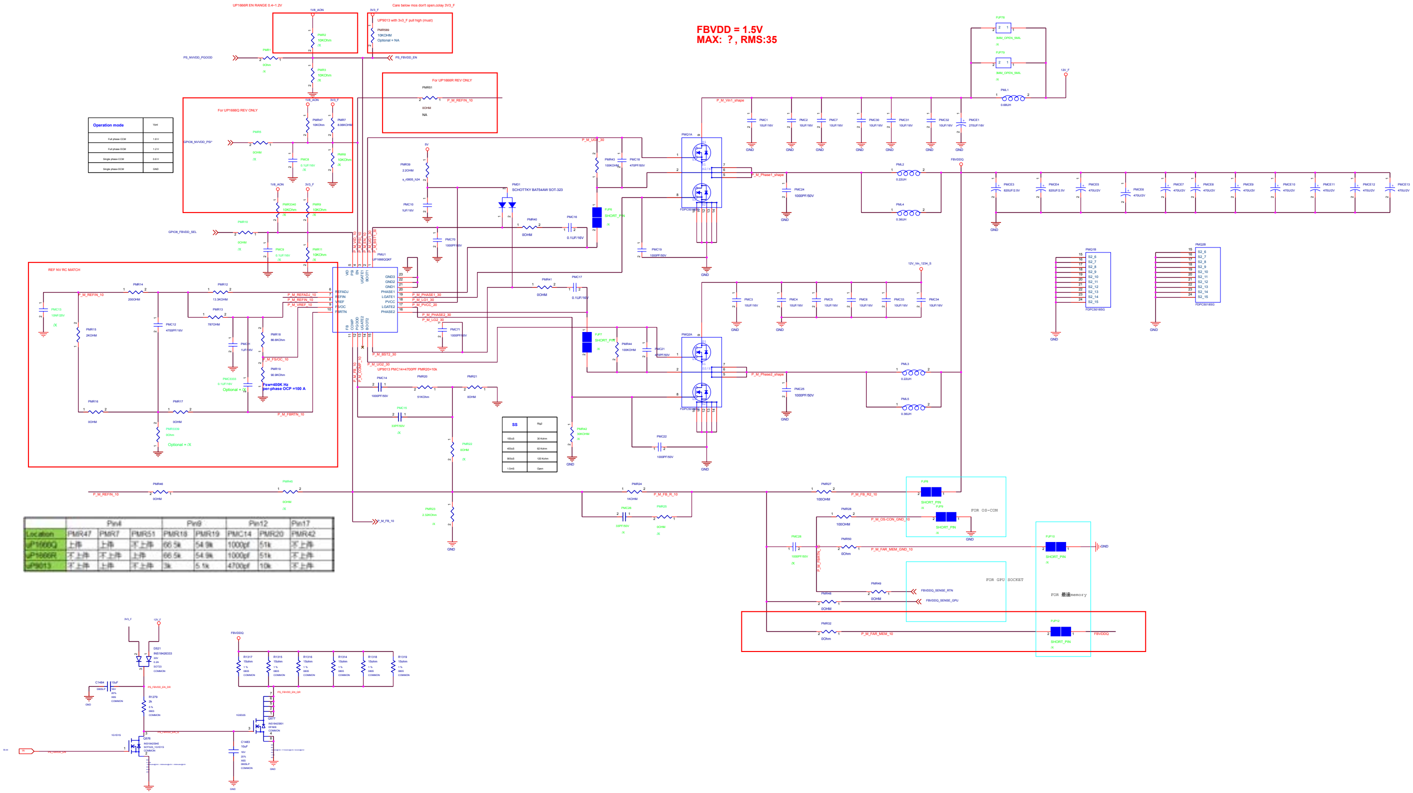
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95051 USA

NV_PN	800-1G611-BASE-300		
PCB REV	PCBPN-DASH	PAGE	48 OF 48
NOM REV	0	DATE	30-SEP-2016



LL_OFFSET	GPIO0==high 3D	GPIO0==low 2D
LL_SET ==>high 降幅	0.7mohm 70mV	0.3mohm 0mV
LL_SET ==>low 不降幅	0.3mohm 30mV	0.3mohm 0mV

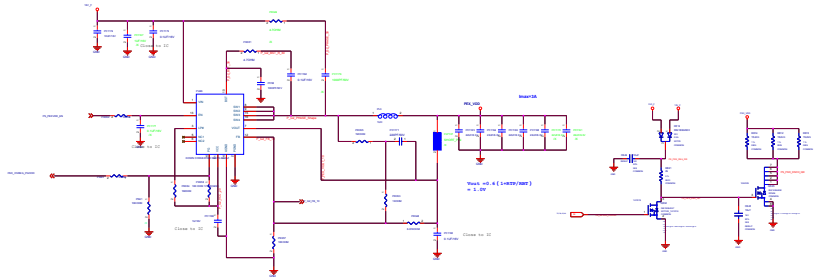


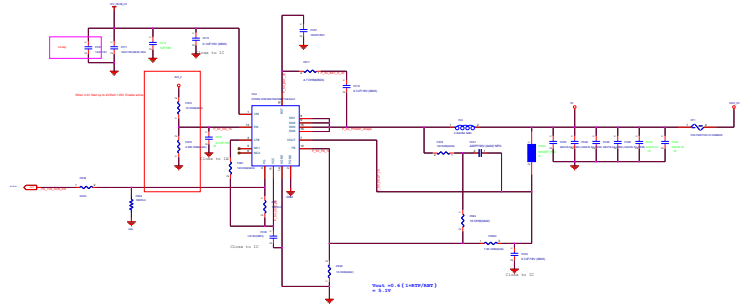


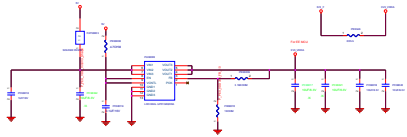
Operation mode	Vpsi
Full phase CCM	1.8 V
Full phase DCM	1.2 V
Single phase CCM	0.6 V
Single phase DCM	GND

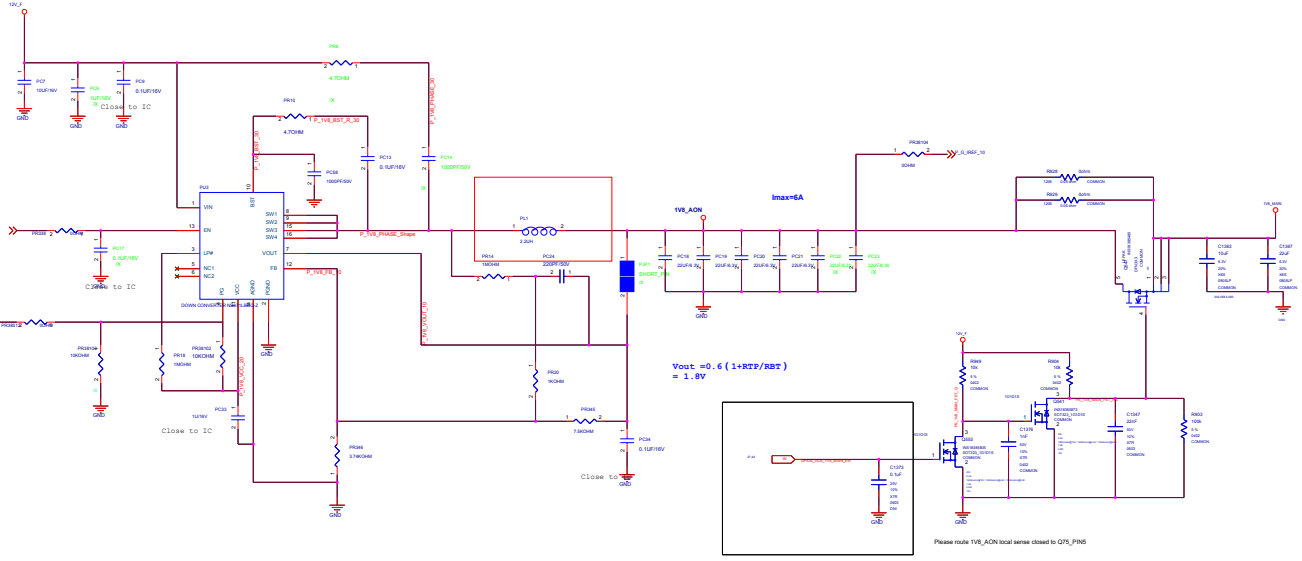
SS	Rig2
150uS	30 Kohm
450uS	62 Kohm
900uS	120 Kohm
1.5mS	Open

	Pin4			Pin9		Pin12		Pin17
Location	PMR47	PMR7	PMR51	PMR18	PMR19	PMC14	PMR20	PMR42
uP1666Q	上件	上件	不上件	66.5k	54.9k	1000pf	51k	不上件
uP1666R	不上件	不上件	上件	66.5k	54.9k	1000pf	51k	不上件
uP9013	不上件	上件	不上件	3k	5.1k	4700pf	10k	不上件

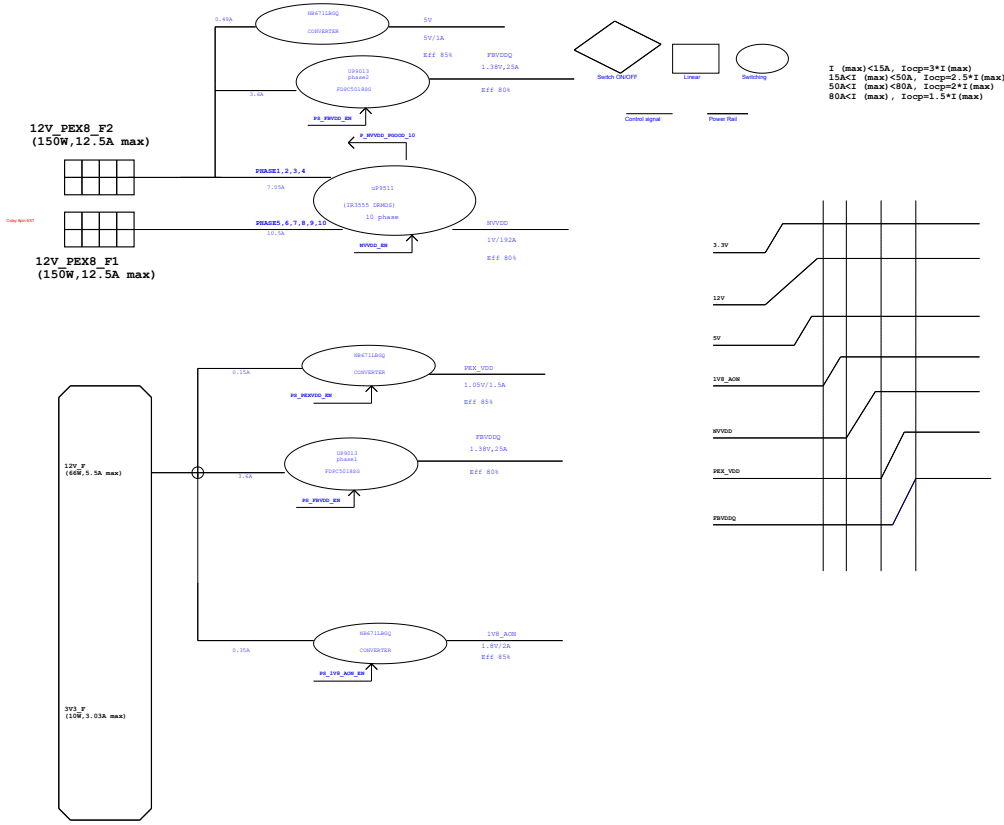

Vout =0.6 [1+R79/R87]
= 1.0V
Close to IC

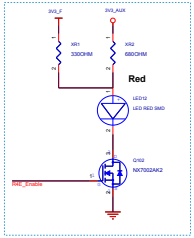

Vout =0.6 [1+R79/R87]
= 5.1V
Close to IC

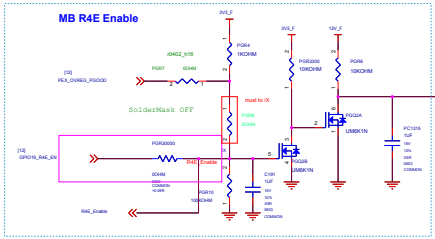

Vo=0.8V[1+Rtop/Rbot]
=0.8V*[1+2.16K/1K]=2.3V

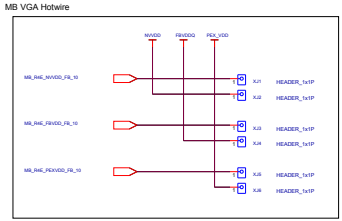

12V_F
PC7
10UF/16V
PC8
10UF/16V
PC9
0.1UF/16V
Close to IC
PR8
4.7OHM
PR10
4.7OHM
P_1V8_BST_R_33
PC13
0.1UF/16V
PC14
1000PF/50V
PC58
1000PF/50V
PU3
VIN
EN
LPW
NC1
NC2
BST
SW1
SW2
SW3
SW4
VOUT
FB
PG
VCC
AGND
PGND
DOWN CONVERTER
PS_1V8_ACN_EN
PR238
PC17
0.1UF/16V
Close to IC
P_1V8_PHASE_Shape
PS_1V8_ACN_PGOOD
PR281
PR281R
19KOHM
PR18
1MOHM
PR18102
10KOHM
PC33
1U/16V
P_1V8_ACC_33
PR346
3.74KOHM
PL1
2.2UH
PR14
1MOHM
PC24
220PF/50V
P_1V8_VOUT_10
PR20
9KOHM
PR345
7.5KOHM
PC34
0.1UF/16V
Close to IC
1V8_AON
Imax=6A
PC18
22UF/6.3V
PC19
22UF/6.3V
PC20
22UF/6.3V
PC21
22UF/6.3V
PC22
22UF/6.3V
PC23
22UF/6.3V
PR281R4
20OHM
_0_REF_10
PR29
20mm
PR28
20mm
COMMON
1V8_MAIN
C1383
10uF
C1387
22uF
Vout =0.6(1+RTF/RBT)
= 1.8V
12V_F
PR49
10k
PR50
10k
COMMON
C1379
10uF
C1347
22uF
R603
100k
COMMON
C1379
0.1uF
Please route 1V8_AON local sense closed to Q75_PIN5

Page59: PS: Power Flow







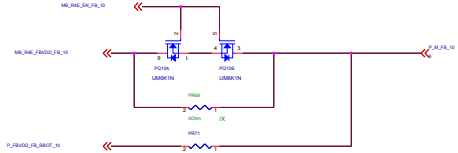


SOFT START (VR11)

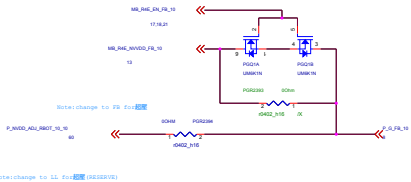
1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
   VID[5:1]=11000 to set 0.9125V

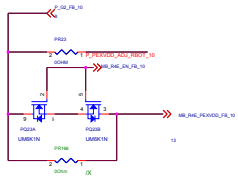
P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V



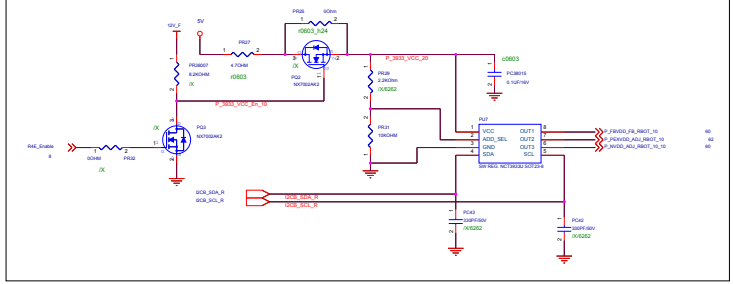
For MB R4E的預留超壓電路

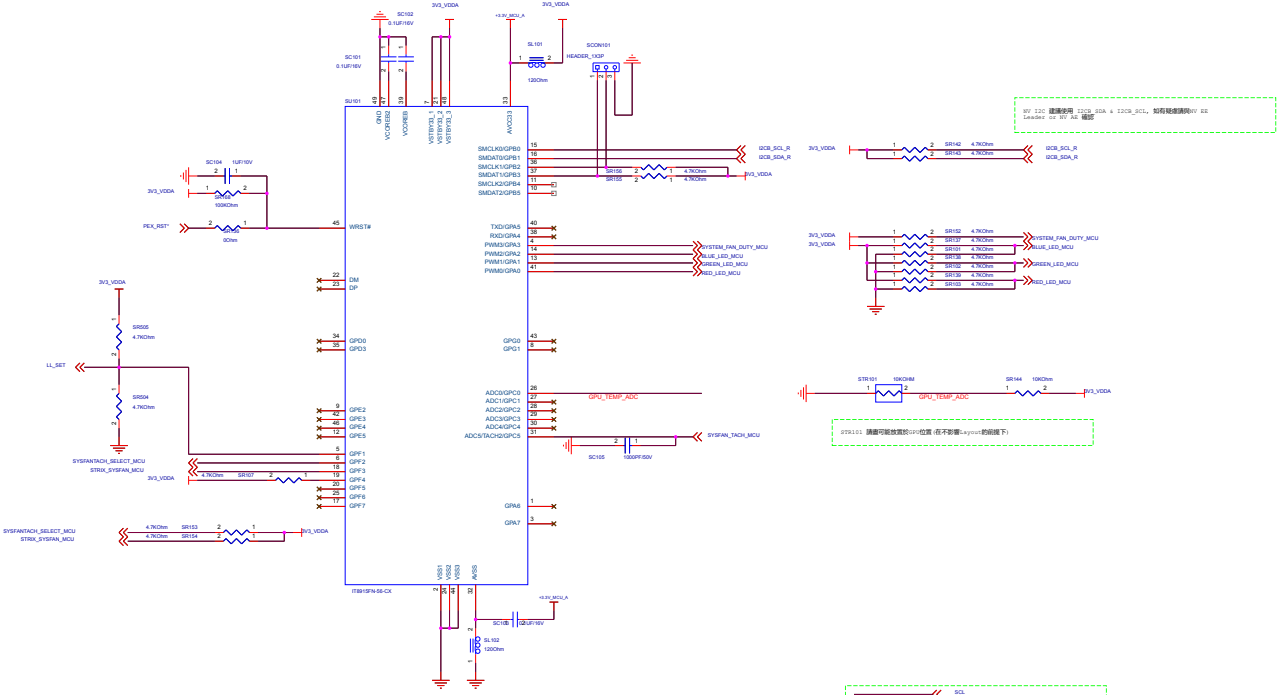




NCT3933U Over Voltage

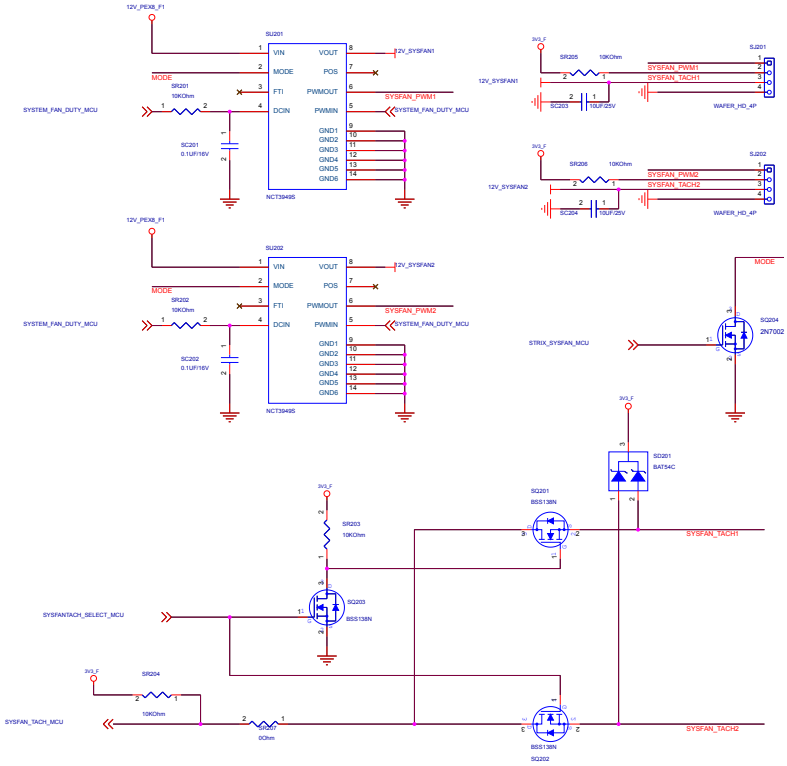
```
Address : 0x2A
```

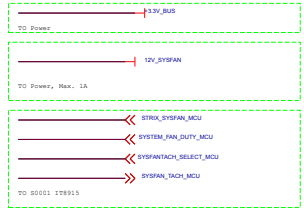




STRIX_SYSFAN_MCU	Mode
L	NORMAL
H(Default)	STRIX

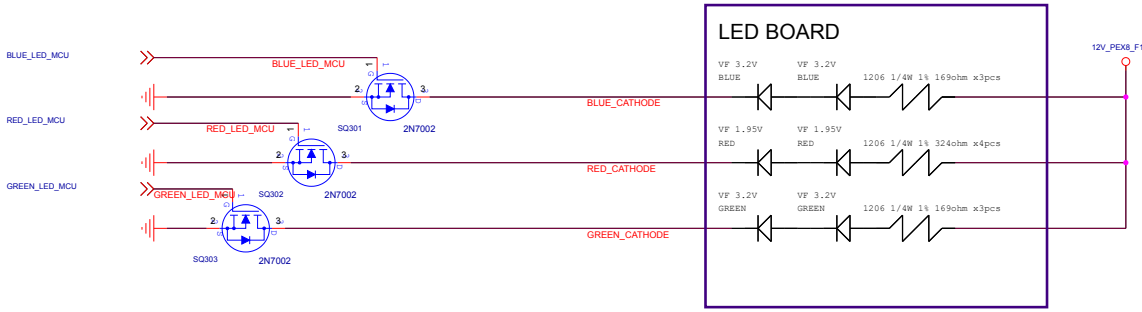
SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H(Default)	SYSFAN_TACH2

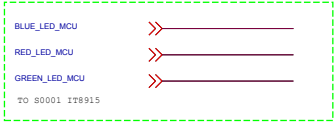




STRIX_SYSFAN_MCU	Mode
L	NORMAL
H (Default)	STRIX

SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H (Default)	SYSFAN_TACH2

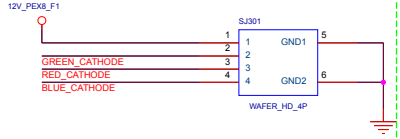




COVER LED線路

示意圖

連接座旁請註明 12V G R B



背板ROG LED線路

5V_LED

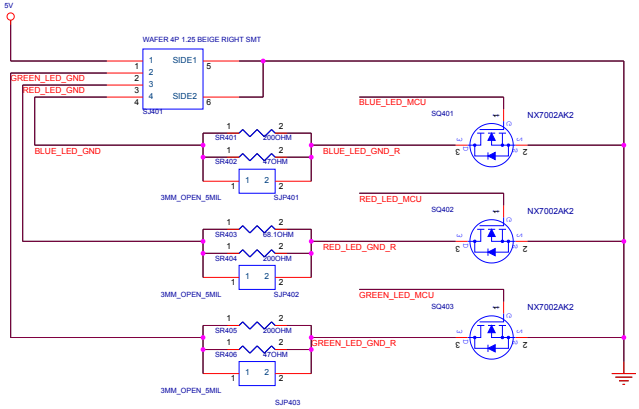
TO Power

BLUE_LED_MCU

RED_LED_MCU

GREEN_LED_MCU

TO S0001 IT8915



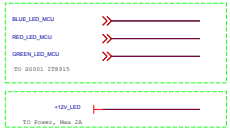
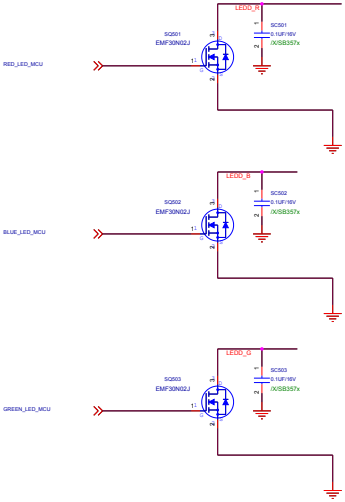
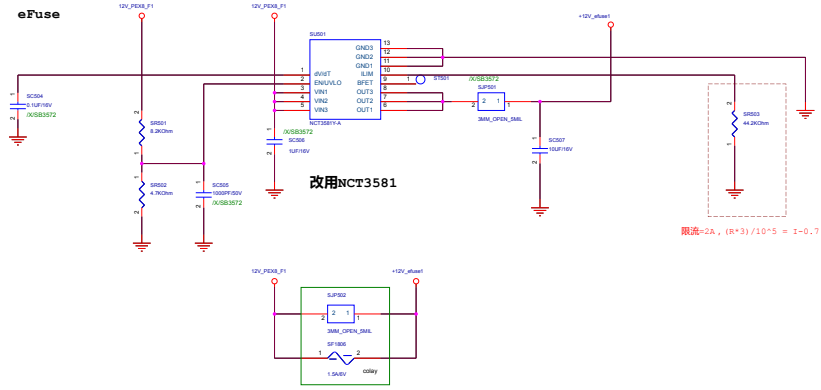

BLUE_LED_MCU
RED_LED_MCU
GREEN_LED_MCU
TO S0001 IT8915
+12V_LED
TO Power, Max 2A

示意圖
連接座旁請註明 12V G R B
RGB Header
RGB_HEADER
+12V_efuse1
LED0_B
LED0_R
LED0_G
HEADER_1MP


LED0_R
SQ501
EMF30N02J
SC501
0.1UF/16V
/X/SB357x
RED_LED_MCU
LED0_B
SQ502
EMF30N02J
SC502
0.1UF/16V
/X/SB357x
BLUE_LED_MCU
LED0_G
SQ503
EMF30N02J
SC503
0.1UF/16V
/X/SB357x
GREEN_LED_MCU


eFuse
12V_PEX8_F1
SU501
GND3
GND2
GND1
ILIM
BFET
OUT3
OUT2
OUT1
dVdt/ET
ENUVLO
VIN1
VIN2
VIN3
NCT3581Y-A
SC504
0.1UF/16V
/X/SB3572
SR501
6.2KOhm
SR502
6.7KOhm
SC505
1000PF/50V
/X/SB3572
SC506
1UF/16V
/X/SB3572
ST501
/X/SB3572
SJP501
3MM_OPEN_SMIL
+12V_efuse1
SC507
10UF/16V
SR503
44.2KOhm
改用NCT3581
限流=2A，(R*3)/10^5 = I-0.7
SJP502
3MM_OPEN_SMIL
SF1806
1.5A/6V
collay