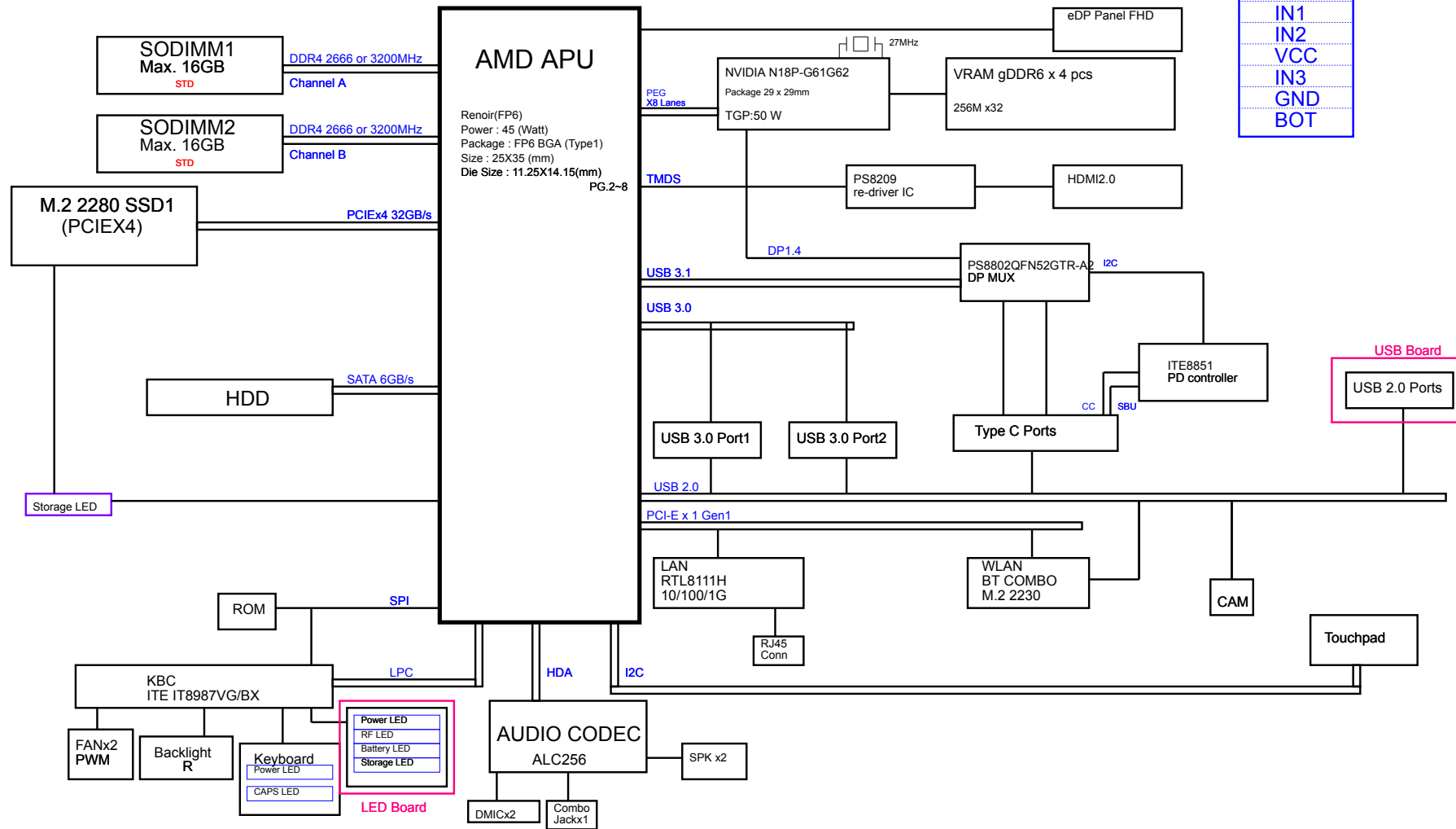


Asus " FX506IH&II/FX706IH&II_AMD+N18P -G61/G62 Block Diagram

01

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



APU PCIE

03

FR6
216N0P9F6
U1B

PCIE

FR6 REV 0 92
PART 2 OF 13

dGPU

dGPU

GLAN

GLAN

WLAN

WLAN

HDD

HDD

M.2 SSD1

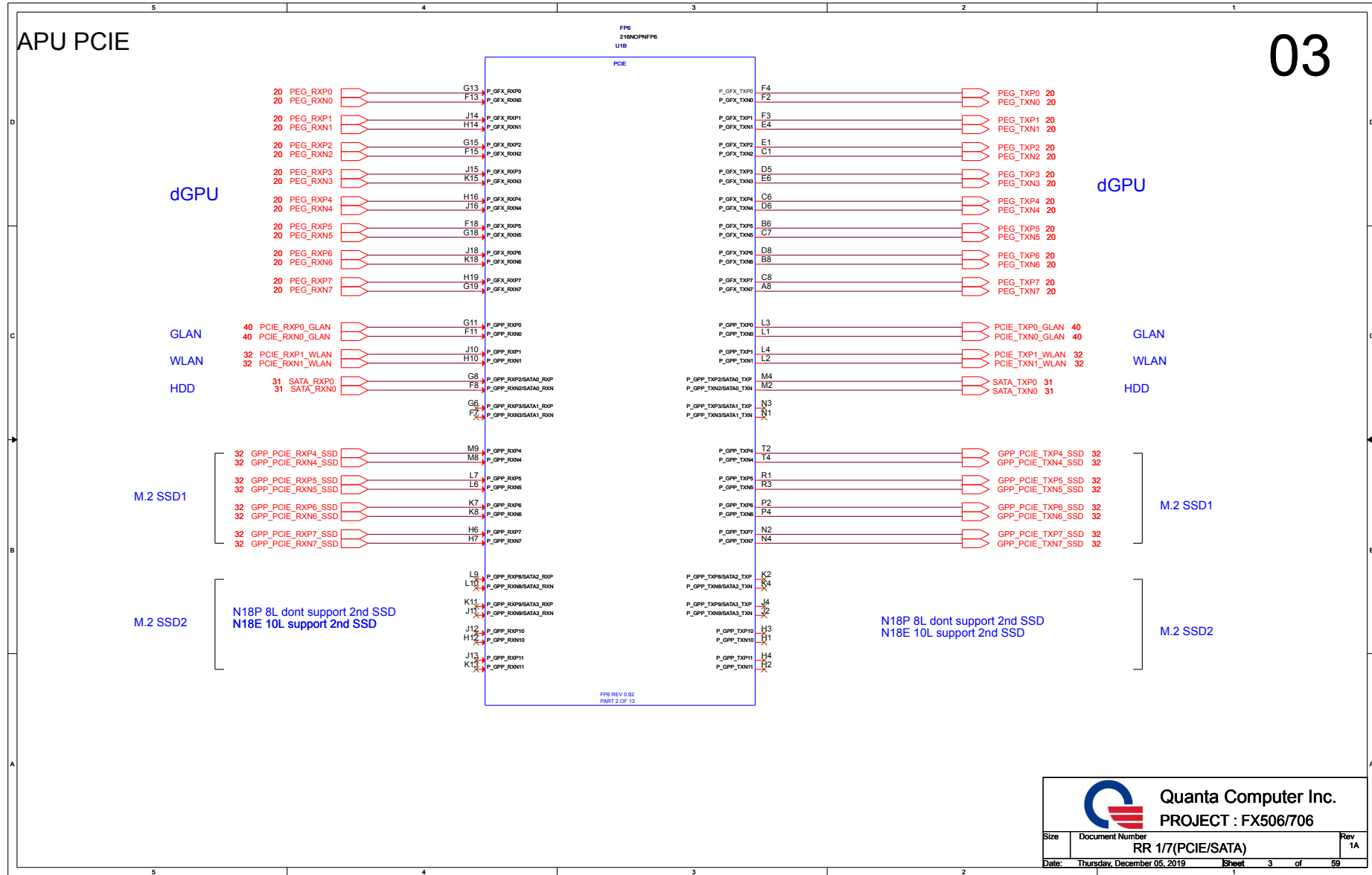
M.2 SSD1


M.2 SSD2

M.2 SSD2

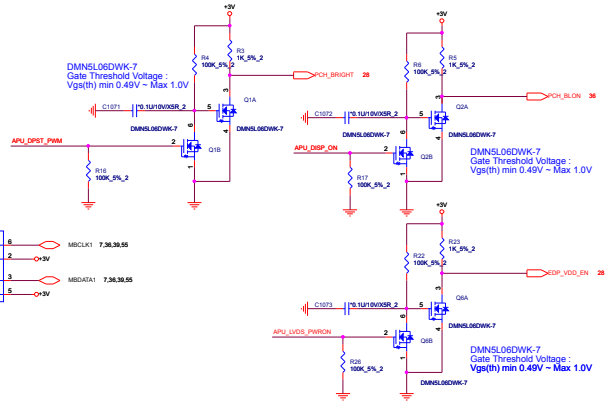
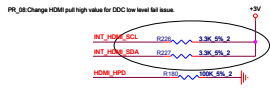
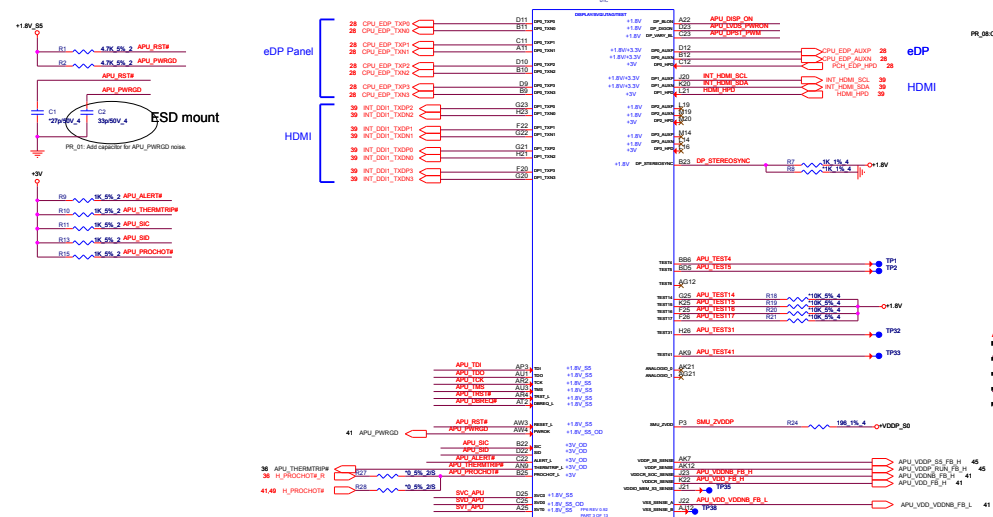
N18P 8L dont support 2nd SSD
N18E 10L support 2nd SSD

N18P 8L dont support 2nd SSD
N18E 10L support 2nd SSD

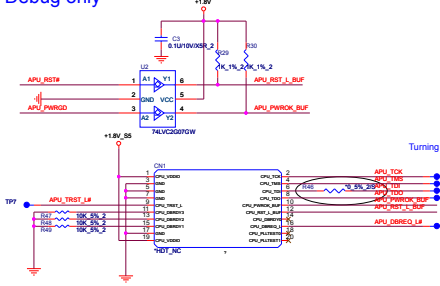
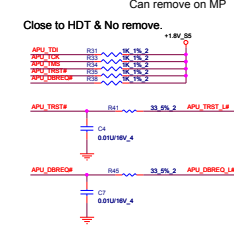



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PROJECT : FX506/706

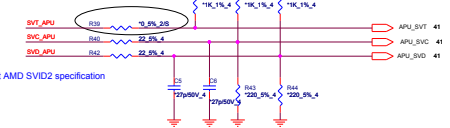
Size	Document Number	Rev
	RR 1/7(PCIE/SATA)	1A
Date: Thursday, December 05, 2019	Sheet	3 of 59



HDT+ Connector for Debug only

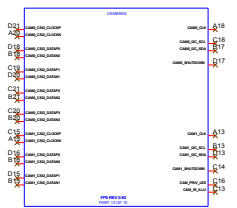


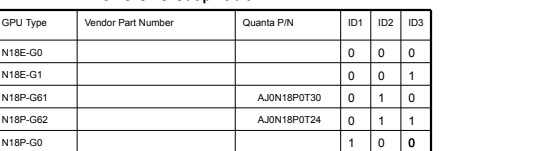
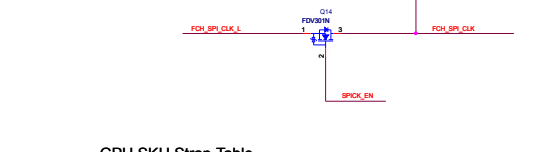
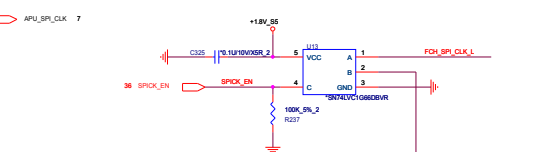
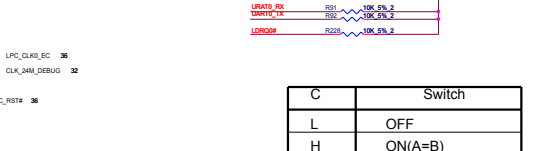
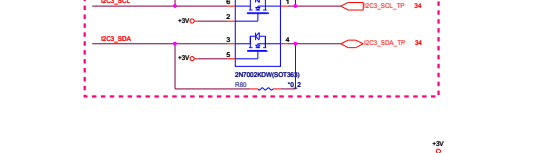
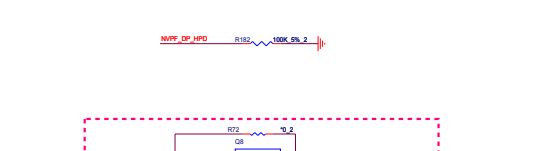
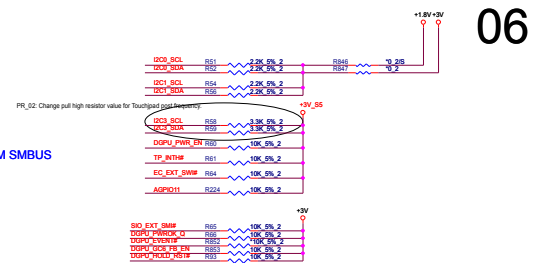
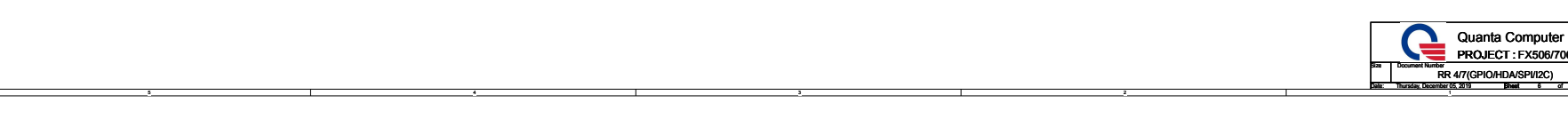
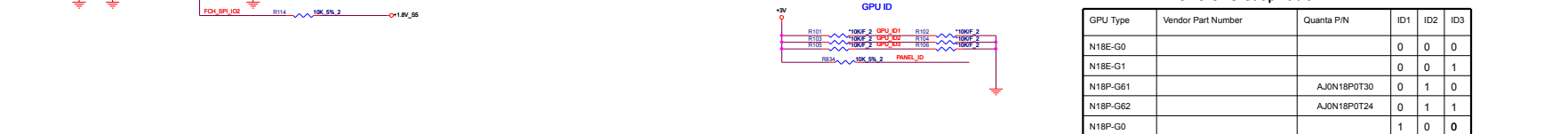
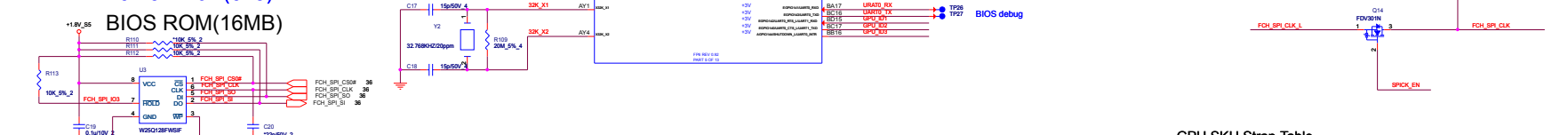
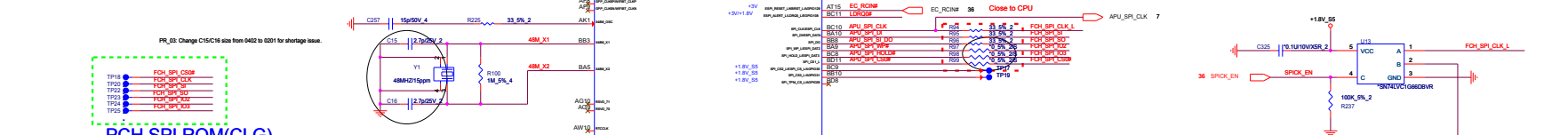
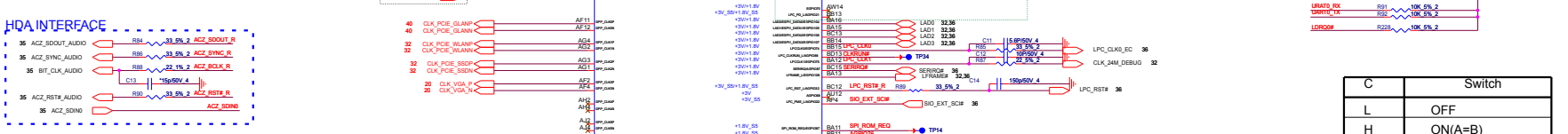
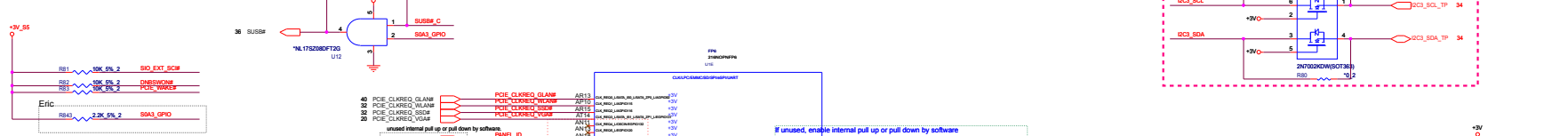
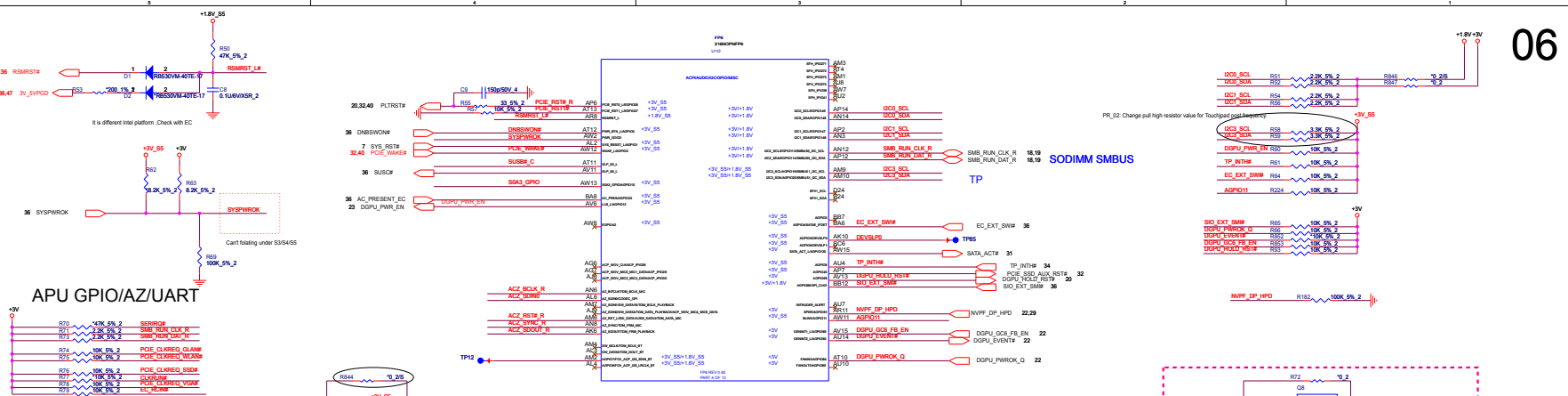
APU Serial VID



Boot-VID code

SVC	SVD	VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8





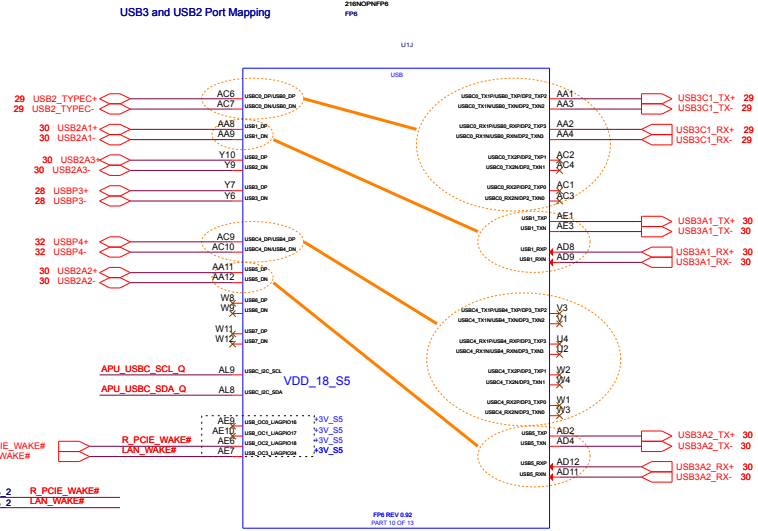
C	Switch
L	OFF
H	ON(A=B)

GPU SKU Strap Table

GPU Type	Vendor Part Number	Quanta P/N	ID1	ID2	ID3
N18E-G0			0	0	0
N18E-G1			0	0	1
N18P-G61		AJON18POT30	0	1	0
N18P-G62		AJON18POT24	0	1	1
N18P-G0			1	0	0

USB2 Port	Function
USB0	TYPE-C
USB1	U3B PORT1
USB2	USB2 P1
USB3	Camera
USB4	Bluetooth
USB5	U3B PORT2
USB6	
USB7	

Type C
U3B P1
USB2 P1
Camera
Bluetooth
U3B P2

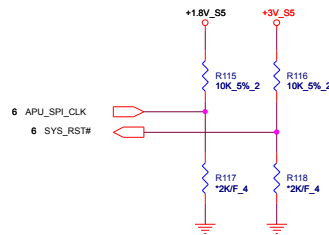


USB TYPE C

U3B Port1

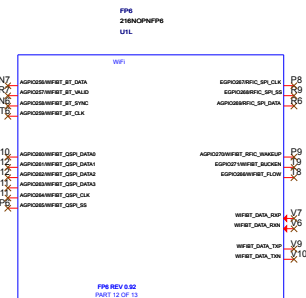
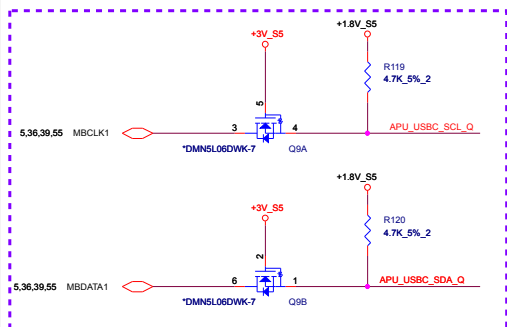
U3B Port2


STRAPS PINS



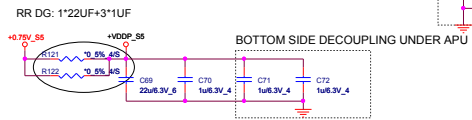
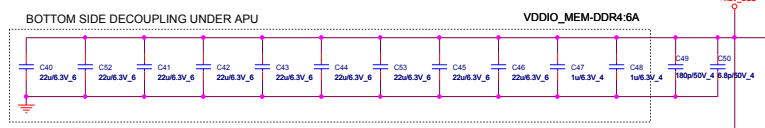
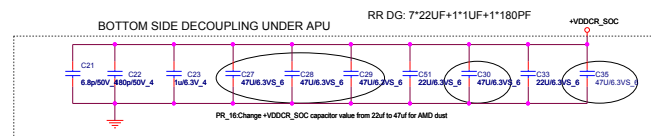
REQUIRED STRAPS

	APU_SPI_CLK	SYS_RST#
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks DEFAULT	normal reset mode DEFAULT
PULL LOW	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



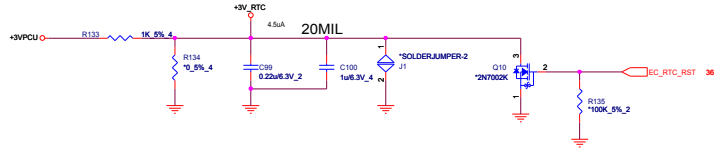
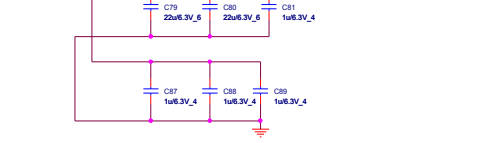
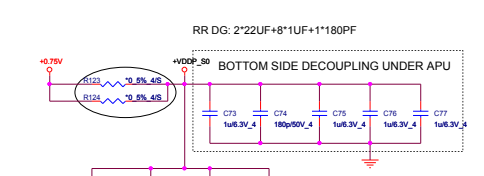
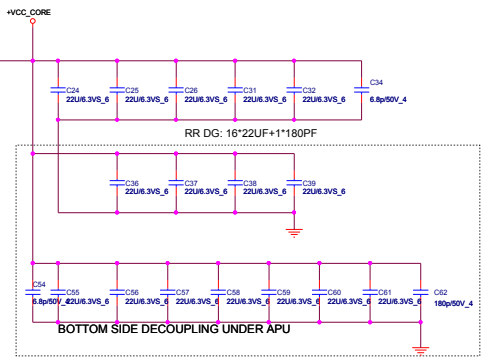
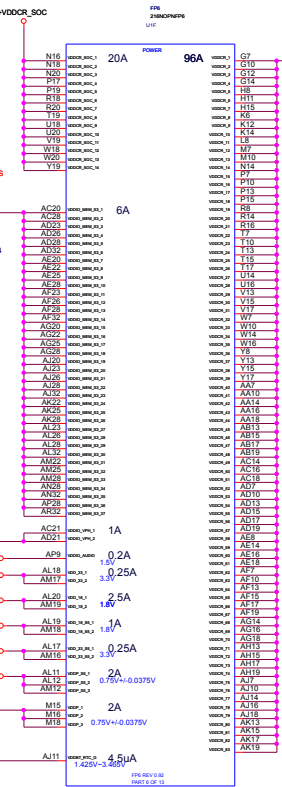
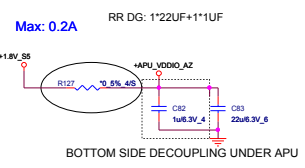
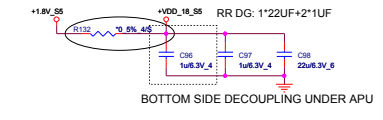
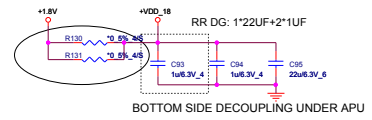
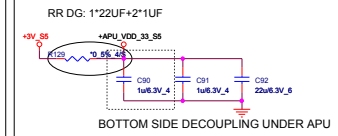
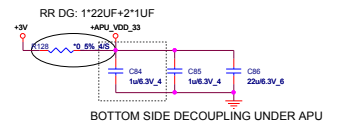

Quanta Computer Inc.
 PROJECT : FX506/706
 RR 5/7(USB/STRAP)
 Date: Thursday, December 05 2019 Sheet 7 of 59 Rev 1A

APU POWER



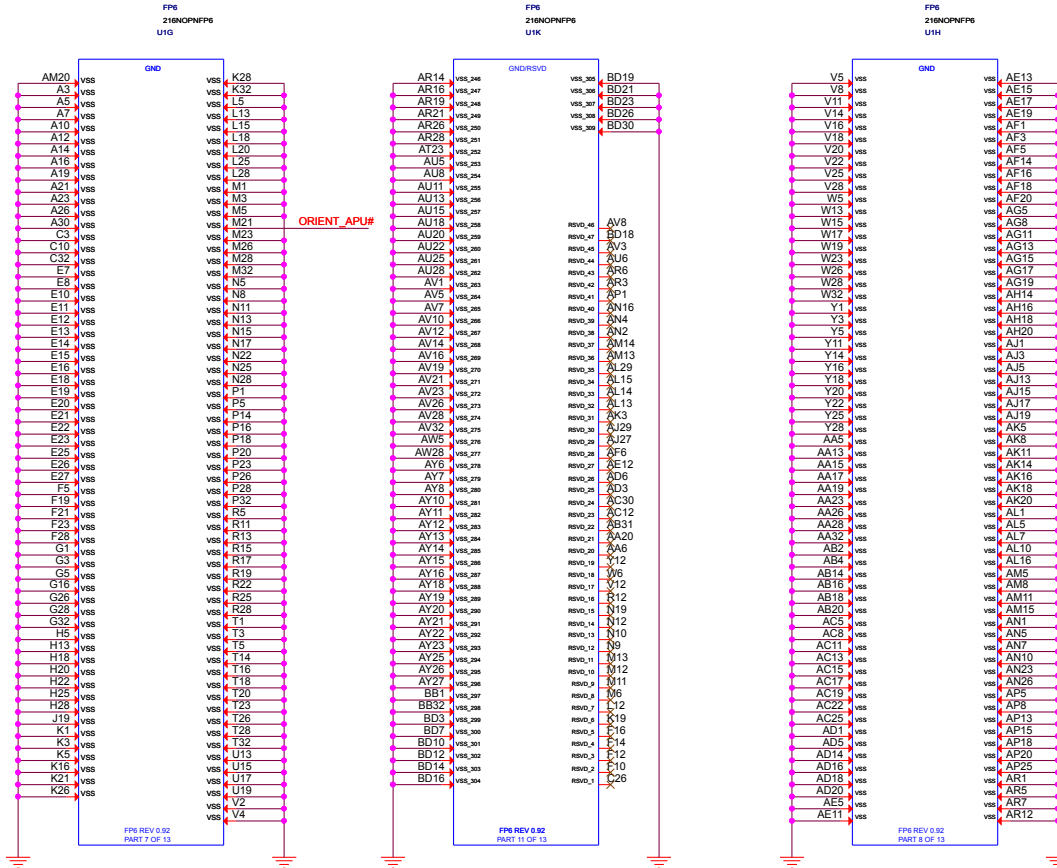
If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or COG dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.


VDDIO_VPH is a dedicated power supply for DisplayPort 0. When DPMS is used for eDP, connect VDDIO_VPH to VDDIO_MEM_S3 source (1.1V LPDDR4x or 1.2V DDR4) to improve battery life.

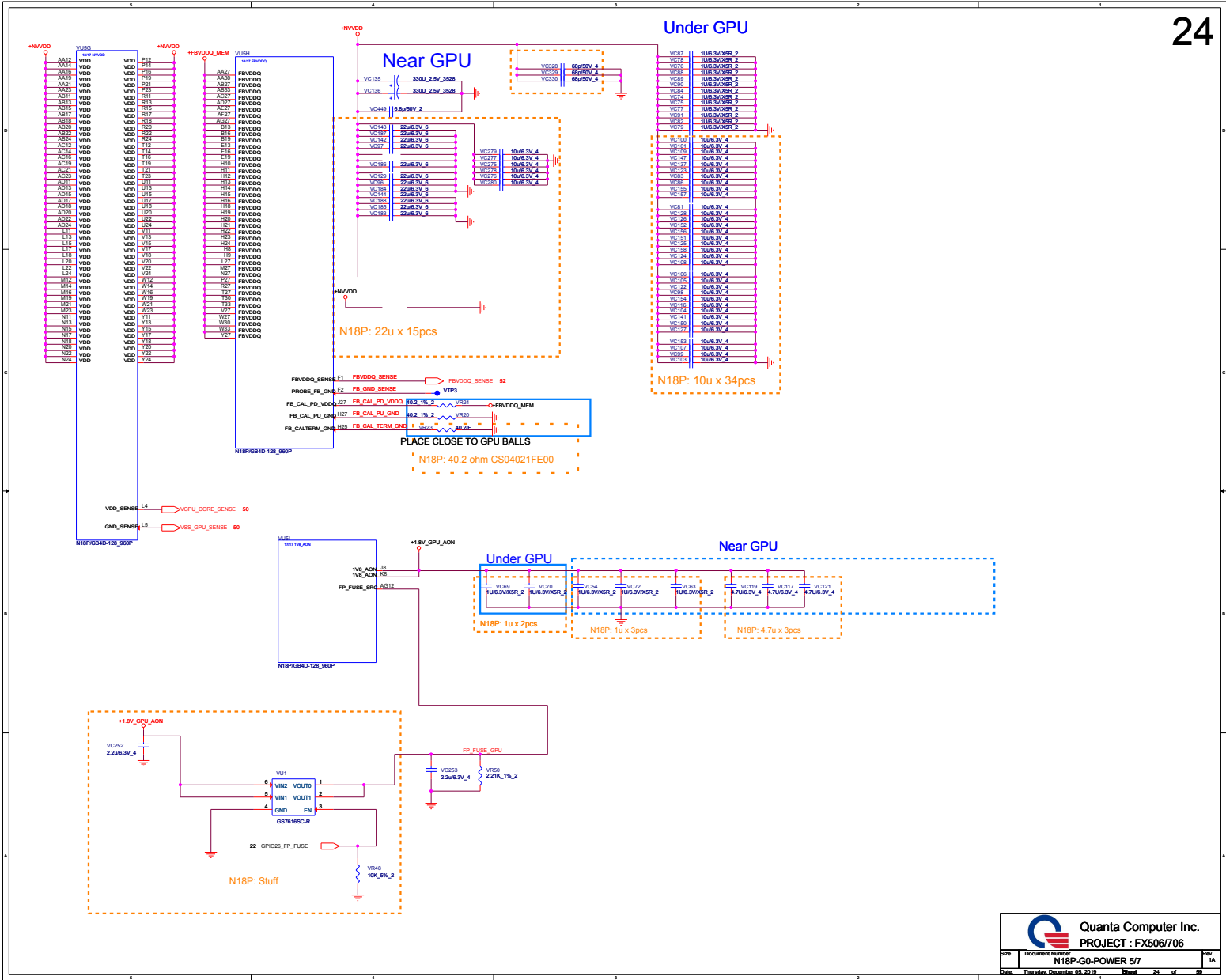


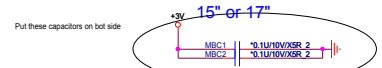
APU GND

9



 Quanta Computer Inc. PROJECT : FX506/706		Rev 1A
Date: Thursday, December 05, 2019		Sheet 9 of 59



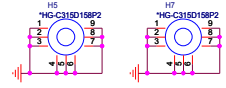


	15"	17"
MBC1	0	1
MBC2	0	0

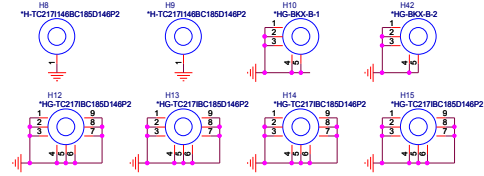
FAN



CPU



CPU / GPU brket



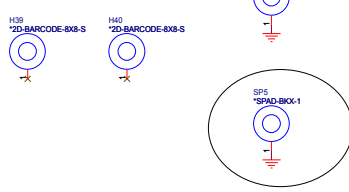
Audio



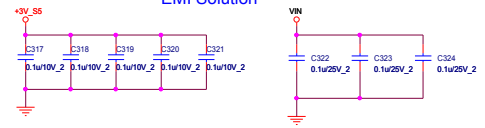
USB2 PAD



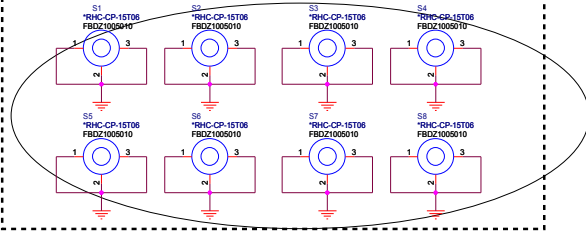
2D barcode



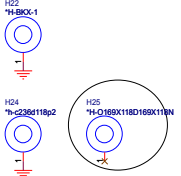
EMI Solution



DDR4 clip PAD

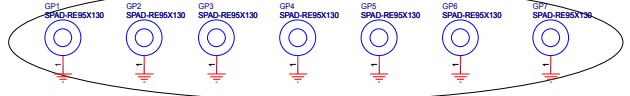


Type C

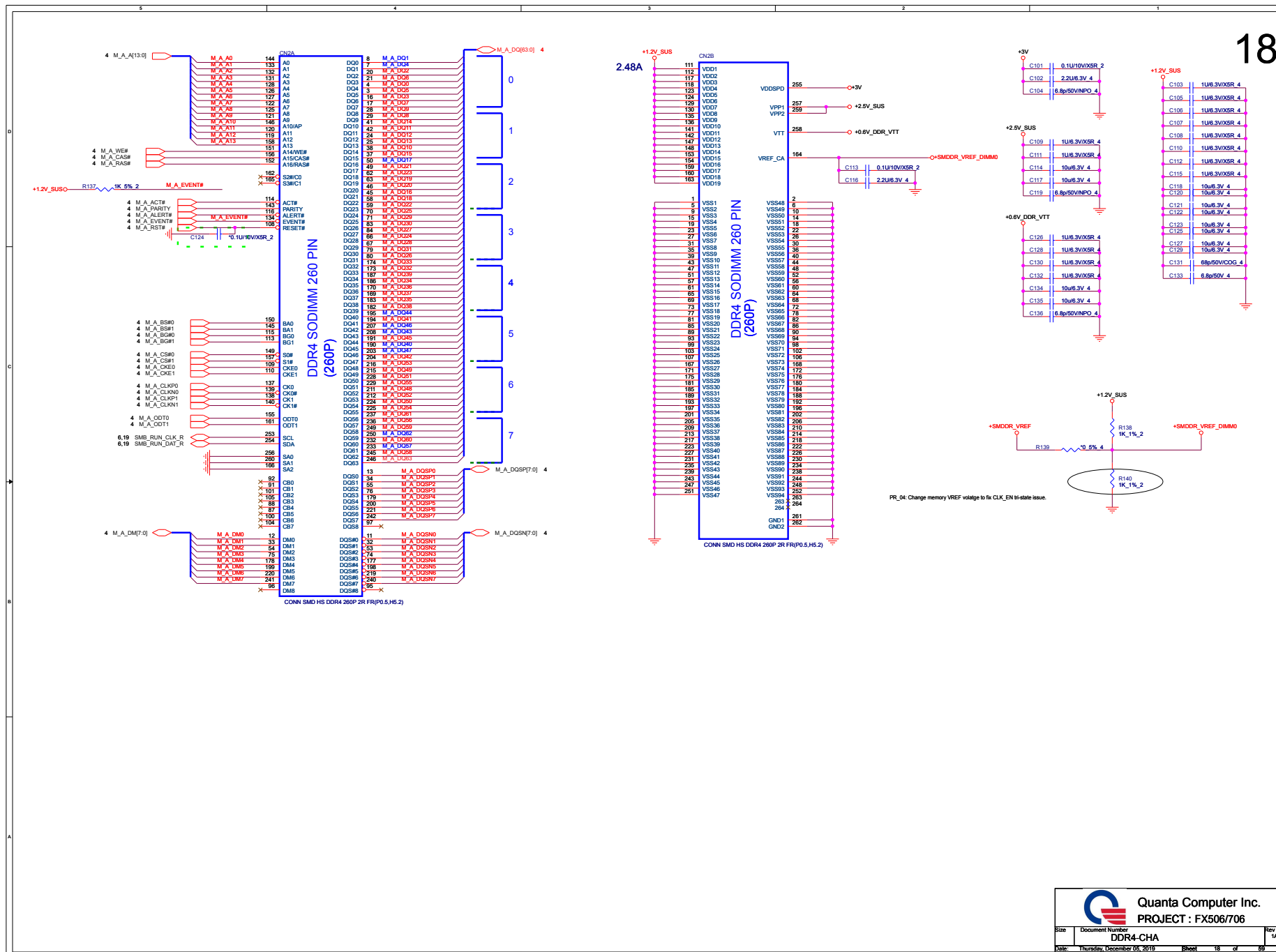


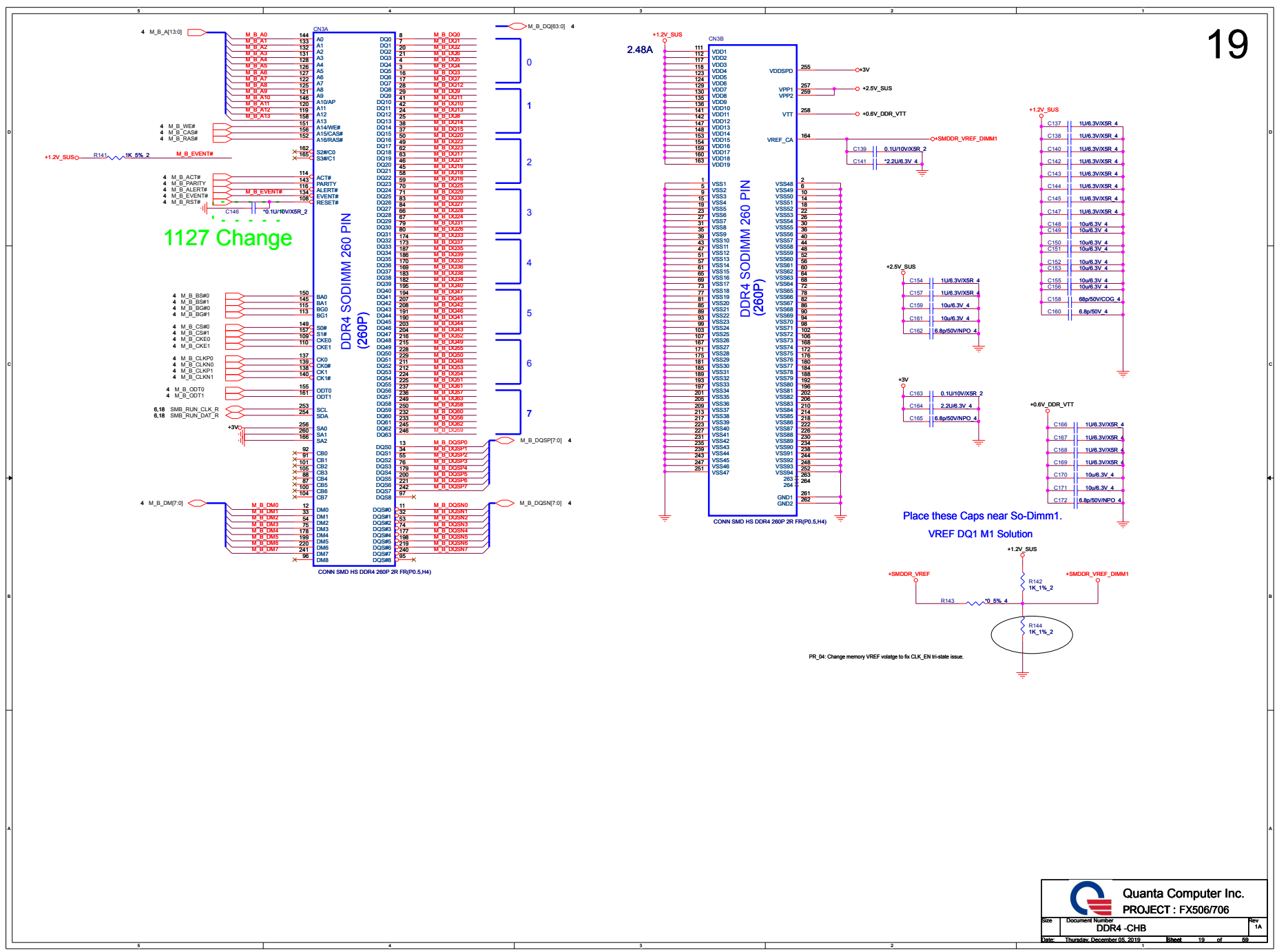
VRAM GP

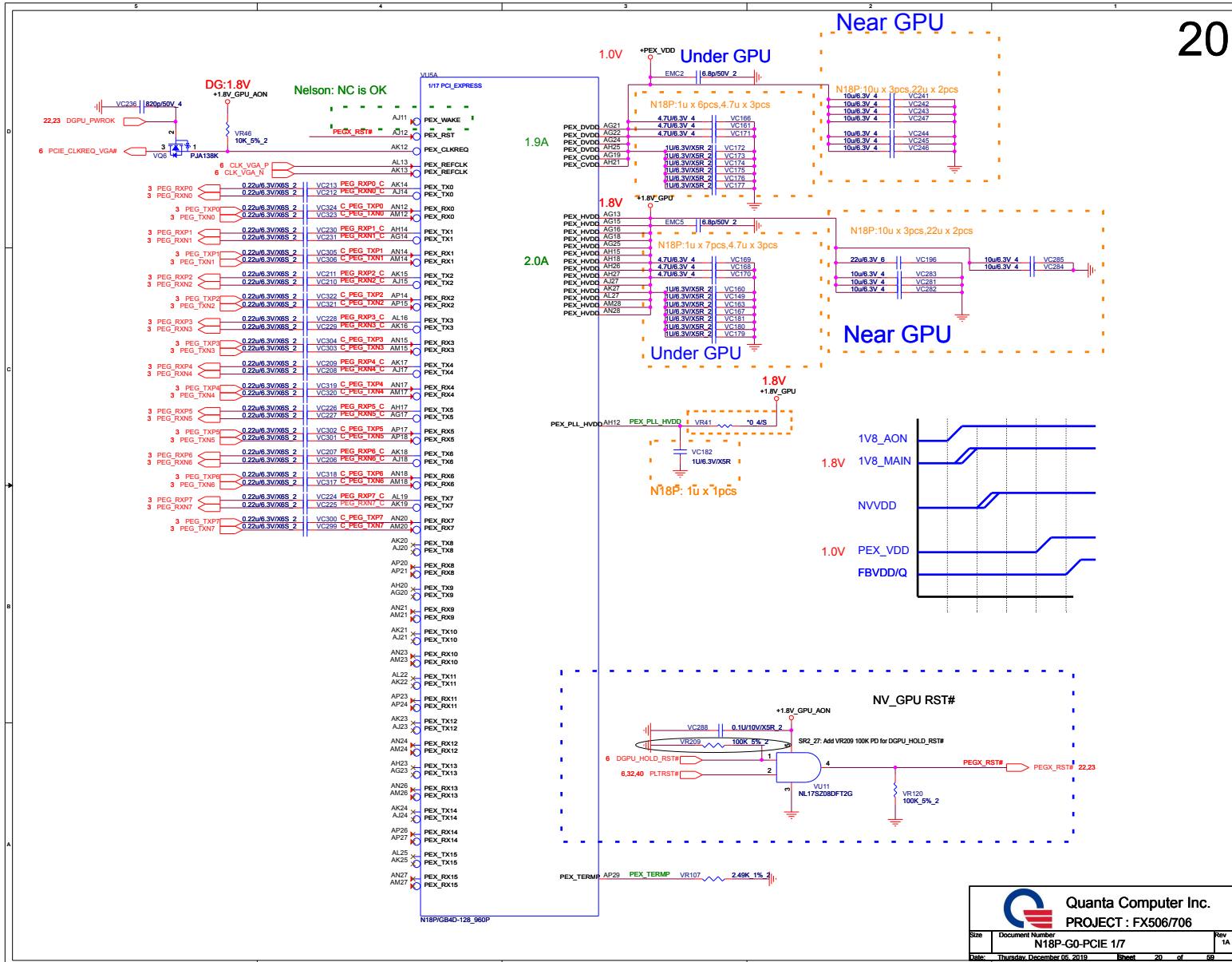
PR_18 Change gasket from 2mm to 1.5mm

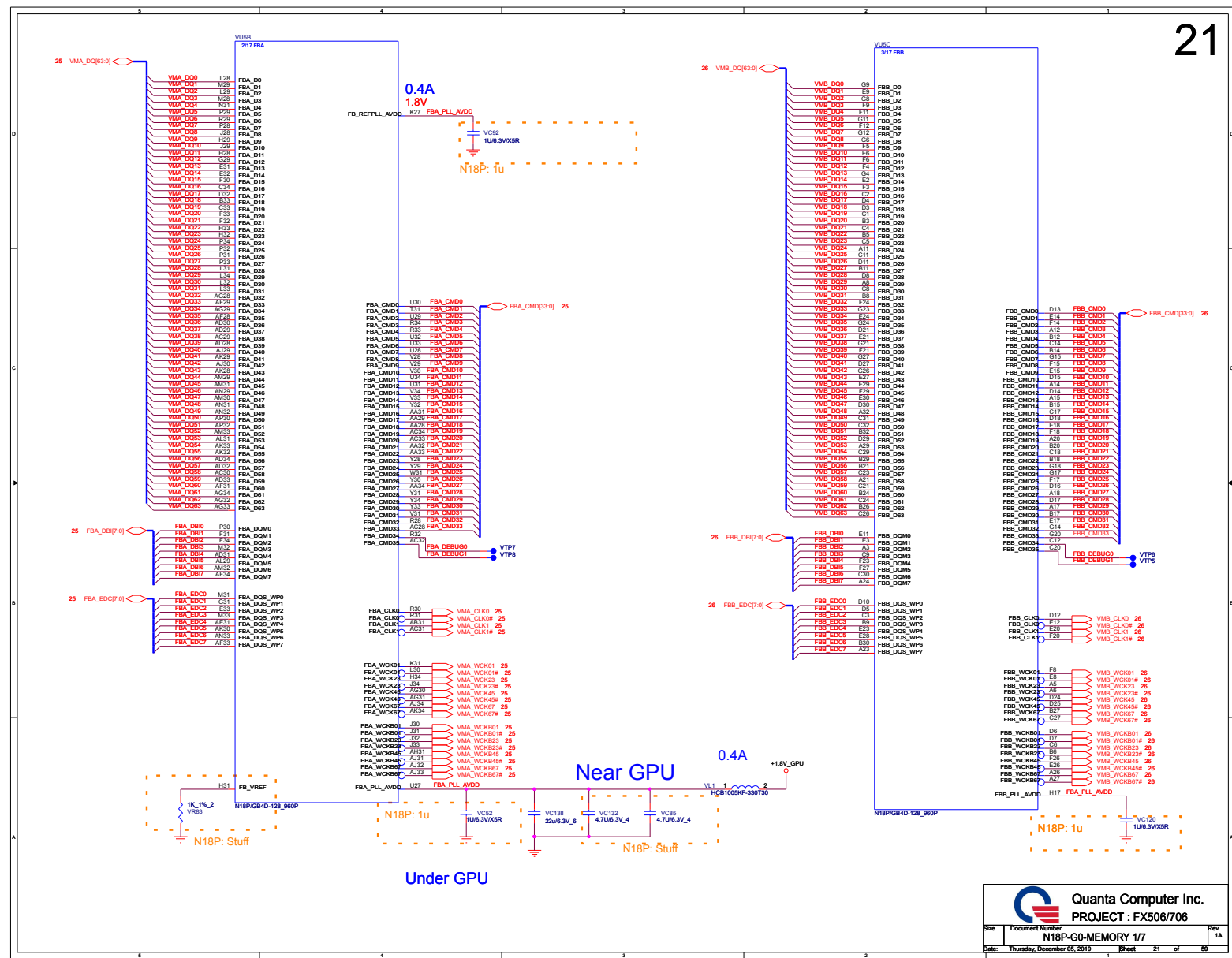


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Size	Document Number	<Doc>	<Rev>
Date:	Thursday, December 06, 2018	Sheet	17 of 59

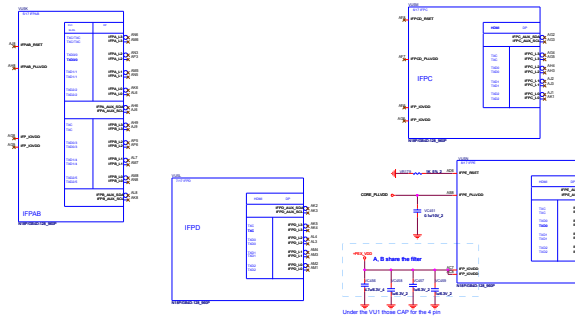








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PROJECT : FX506/706
Size: Document Number: N18P-G0-MEMORY 1/7
Date: Thursday, December 05, 2019 11:07:11 AM Page 21 of 89



STRAP[3] VRAM Table for N18P-GS2H1 QDDR6 Recommended Memories

Strap	Decomposition	Memory	Memory Size	Quanta Part	Frequency
00	0000000000000000	Memory	4GB	QDDR6-16000-1.6A	1.600000
01	0000000000000001	Memory	4GB	QDDR6-16000-1.6A	1.600000

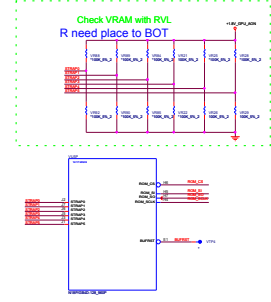
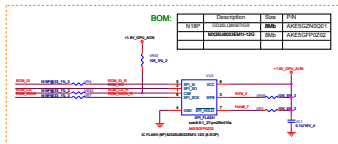
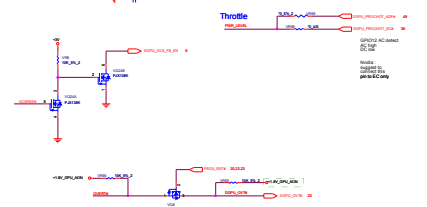
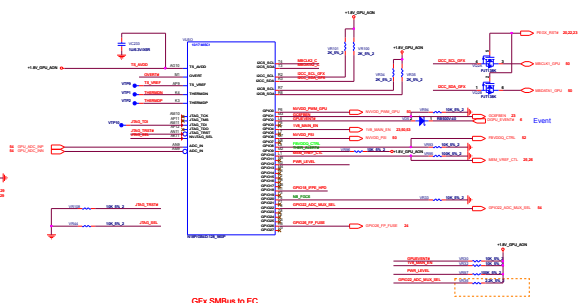
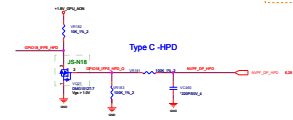
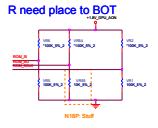


Table 5.3 RAMCFG

STRAP1	STRAP2	STRAP3	RAMCFG Setting Number
L	L	L	0 (0x000)
L	L	H	1 (0x001)
L	L	L	2 (0x002)
L	L	H	3 (0x003)
L	L	L	4 (0x004)
L	L	H	5 (0x005)
L	L	L	6 (0x006)
L	L	H	7 (0x007)
L	L	L	8 (0x008)
L	L	H	9 (0x009)
L	L	L	10 (0x00A)



N18P: Stuff

Table 14.2 GPIO Descriptions for GBAC-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	WAKE_GPIO_VID	O	PMW output to control WAKE	0 to 10k pull-up to VDD
GPIO1	GPIO_G0_01_EN	O	FS Enable for G0.1	Open Drain 10k pull-down
GPIO2	GPIO_G0_02_EN	O	GPIO wake signal for G0.2	10k pull-up to VDD, open drain active
GPIO3	WAKE_GPIO_PWDN	O	PMW output to control the 3.3Vd power supply	0 to 10k pull-down
GPIO4	GPIO_G0_04_EN	O	GPIO power sequencing for G0.1.1	Open Drain 10k pull-up to VDD
GPIO5	TRN_LCK	I	Active Low Frame Lock	Open Drain 10k pull-up to VDD

Table 14.2 GPIO Descriptions for GBAC-128 Packages (Continued)

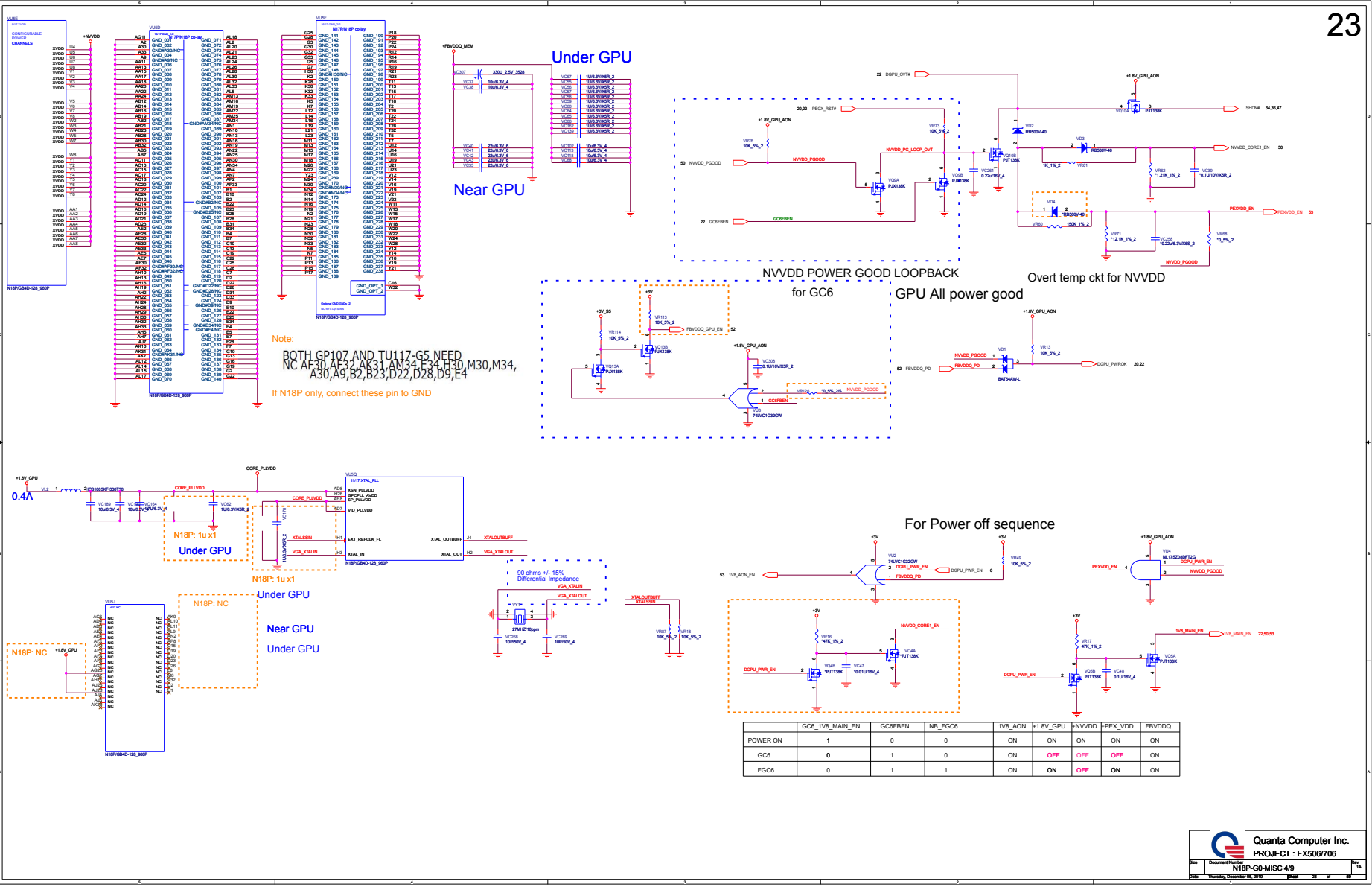
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	WAKE_GPIO	O	PMW Shading Drive	10k pull-up to VDD, 10k pull-down
GPIO7	LED_R_STM	O	Panel backlight enable	10k pull-up to VDD, 10k pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	10k pull-up to VDD, 10k pull-down
GPIO9	THRM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10k pull-up to VDD
GPIO10	MEM_VDD_CTL	O	Memory Voltage Control	10k pull-up to VDD
GPIO11	LED_VDD	O	LED Power enable	10k pull-up to VDD
GPIO12	GPIO_VDD	O	GPIO Power enable	10k pull-up to VDD
GPIO13	LED_RST	O	LED Power Reset	Panel backlight enable
GPIO14	HPD_01N	I	Hot Plug Detect for 01N	Inverted Input. See Figure 14.1
GPIO15	HPD_01N	I	Hot Plug Detect for 01N	Inverted Input. See Figure 14.1
GPIO16	GPIO_RST_JACK	O	System side PWR reset monitor	10k pull-up to VDD, 10k pull-down
GPIO17	HPD_01N	I	Hot Plug Detect for 01N	Inverted Input. See Figure 14.1
GPIO18	HPD_01N	I	Hot Plug Detect for 01N	Inverted Input. See Figure 14.1
GPIO19	3D_VISION_L1R	O	3D Vision L1R signal	10k pull-down
GPIO20	GPIO_VDD	I/O		
GPIO21	GPIO_VDD	I/O		

Table 14.2 GPIO Descriptions for GBAC-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO22	GPIO_VDD	I/O		
GPIO23	GPIO_VDD	I/O		
GPIO24	GPIO_VDD	I/O		
GPIO25	GPIO_VDD	I/O		
GPIO26	GPIO_VDD	I/O		
GPIO27	GPIO_VDD	I/O		

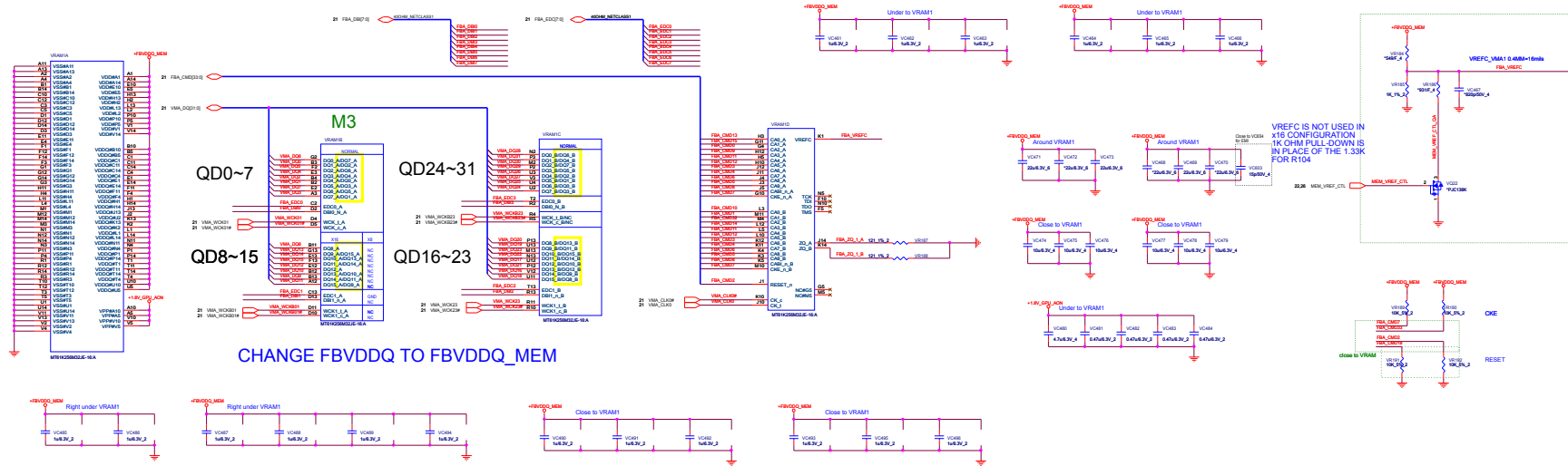
GPIO Descriptions for GBAC-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO28	GPIO_VDD	I/O		

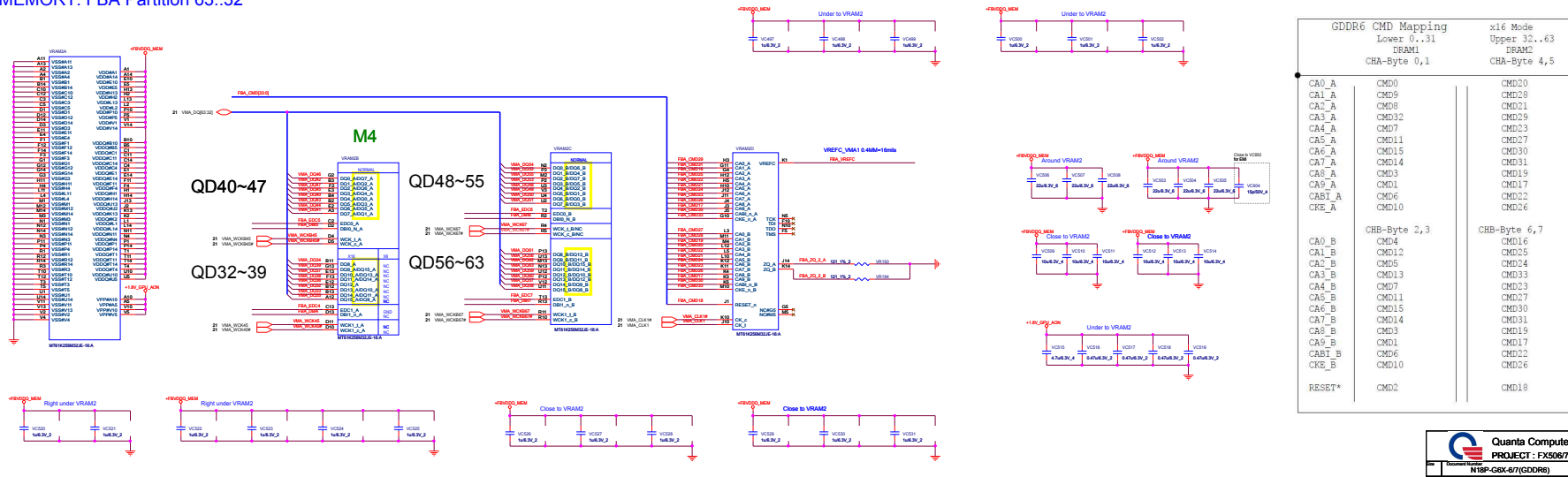


	GC6_V8_MAIN_EN	GC6FFEN	NB_FG6	V8_AON	H1.8V_GPU	NVDDQ	PEX_VDD	FWDDO
POWER ON	1	0	0	ON	ON	ON	ON	ON
GC6	0	1	0	ON	OFF	OFF	OFF	ON
FG6	0	1	1	ON	ON	OFF	ON	ON

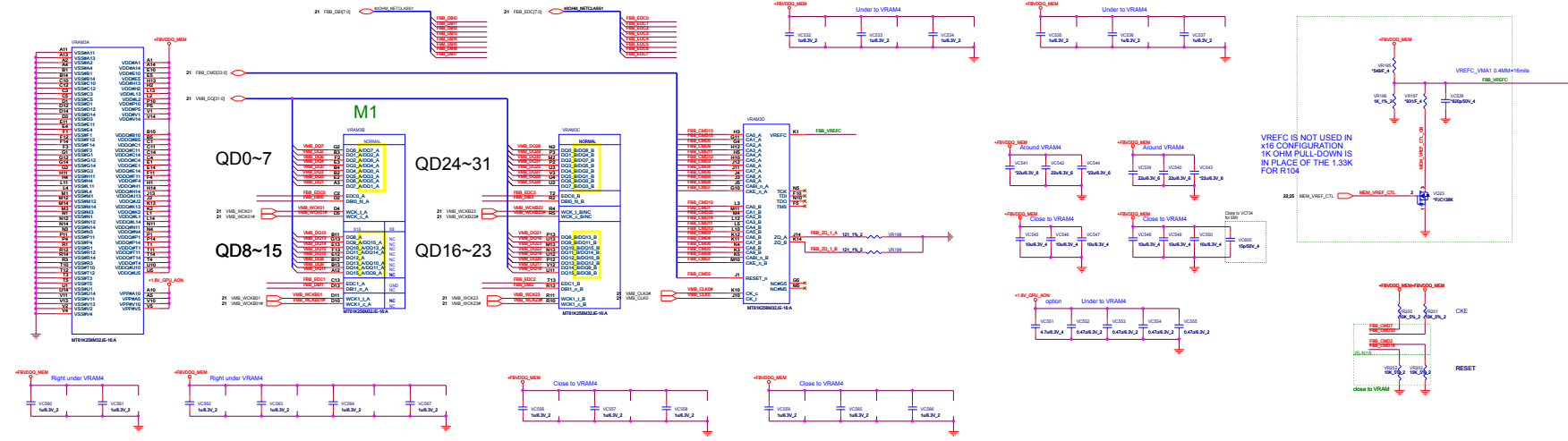
MEMORY: FBA Partition 31..0



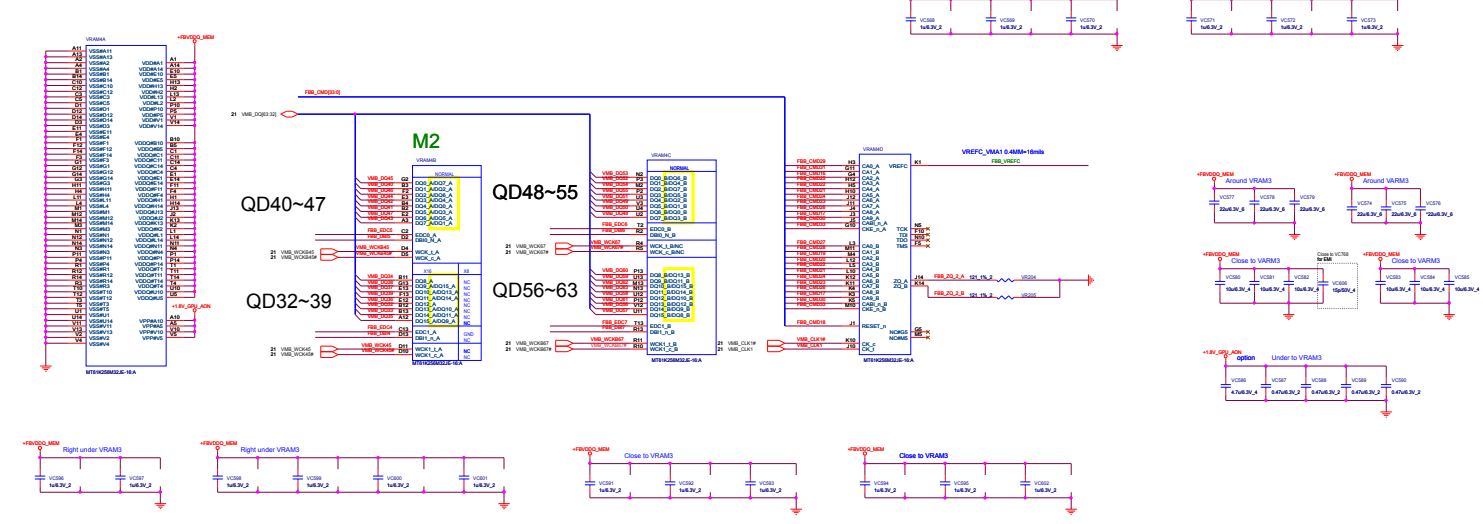
MEMORY: FBA Partition 63..32



MEMORY: FBB Partition 31..0

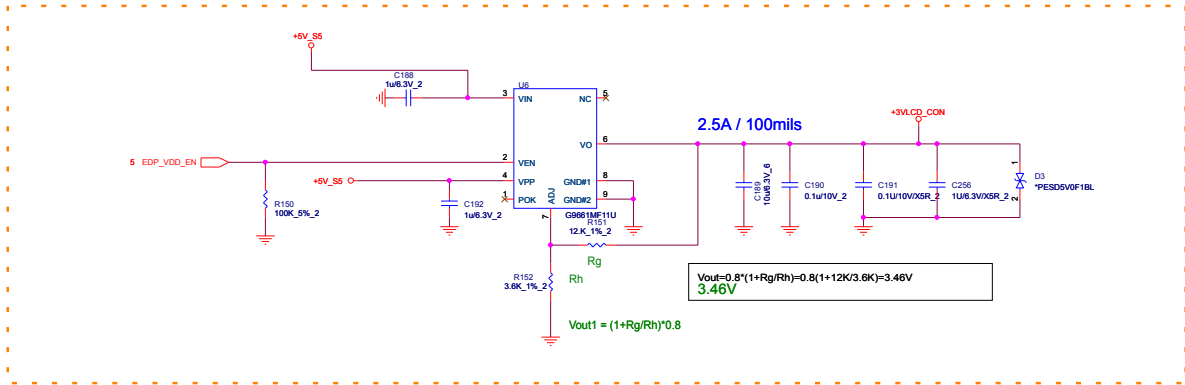
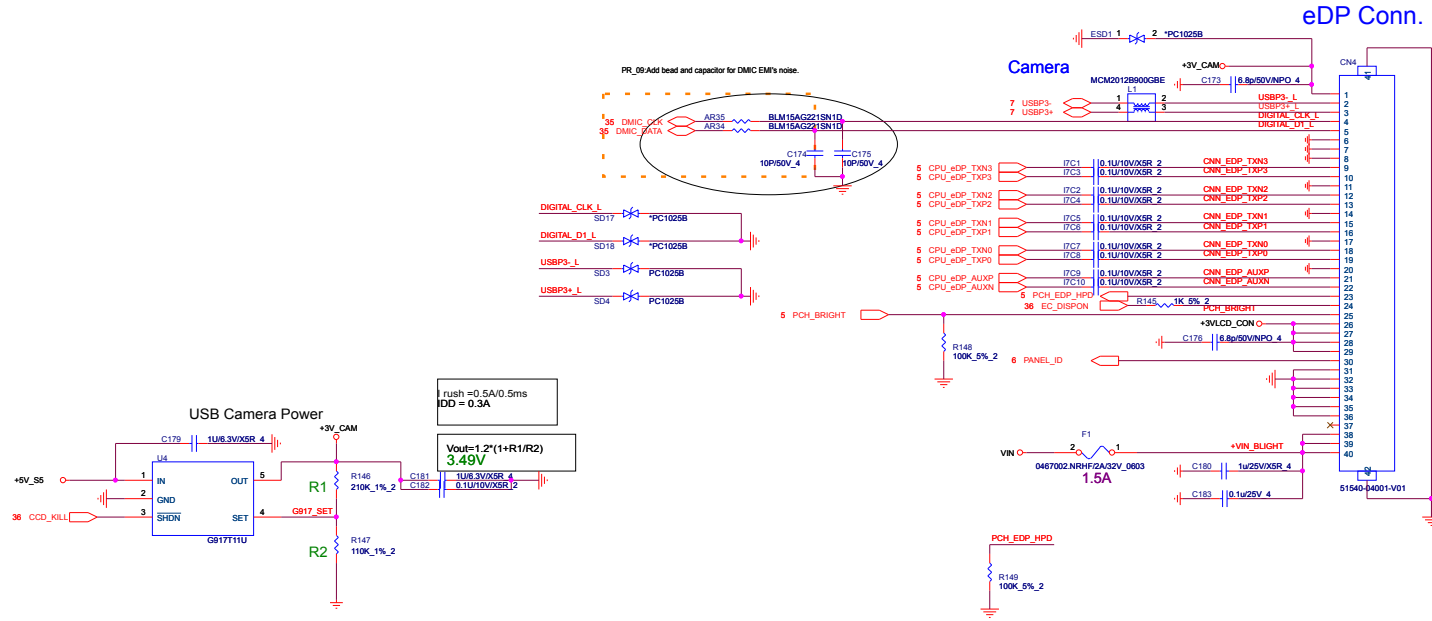


MEMORY: FBB Partition 63..32

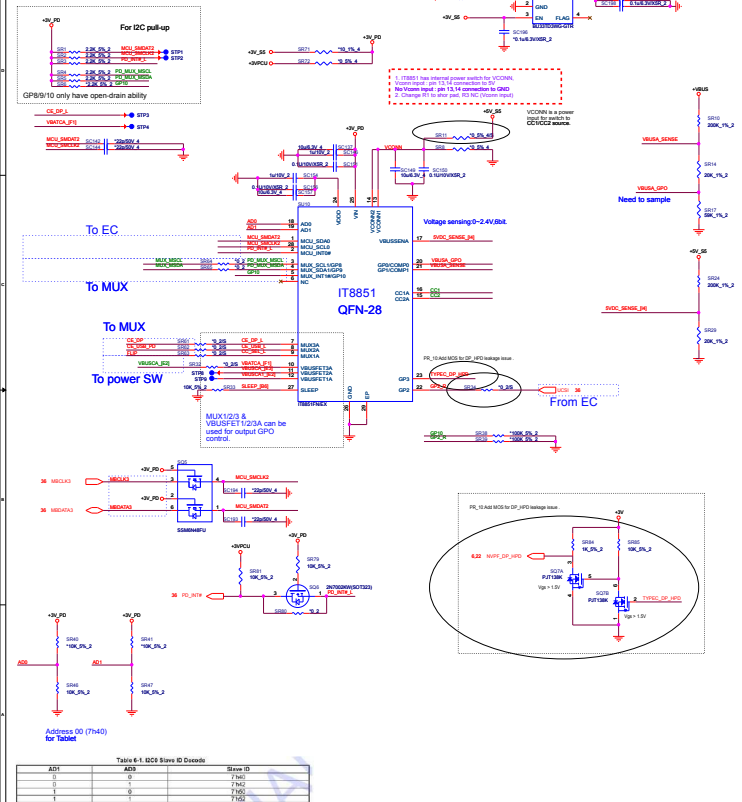


GDDR6 CMD Mapping

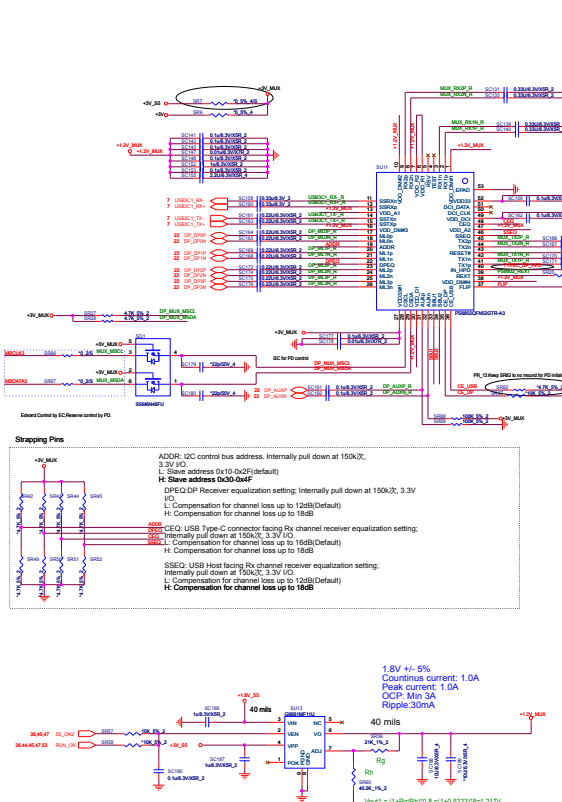
Lower 0..31		Upper 32..63	
DRAM1		DRAM2	
CHA-Byte 0,1	CHB-Byte 0,1	CHA-Byte 4,5	CHB-Byte 4,5
CA0_A	CMD0	CA0_B	CMD0
CA1_A	CMD9	CA1_B	CMD9
CA2_A	CMD8	CA2_B	CMD8
CA3_A	CMD32	CA3_B	CMD32
CA4_A	CMD7	CA4_B	CMD7
CA5_A	CMD11	CA5_B	CMD11
CA6_A	CMD15	CA6_B	CMD15
CA7_A	CMD14	CA7_B	CMD14
CA8_A	CMD3	CA8_B	CMD3
CA9_A	CMD1	CA9_B	CMD1
CAB1_A	CMD6	CAB1_B	CMD6
CAB2_A	CMD10	CAB2_B	CMD10
CHB-Byte 2,3		CHB-Byte 6,7	
CA0_B	CMD4	CA0_B	CMD16
CA1_B	CMD12	CA1_B	CMD26
CA2_B	CMD5	CA2_B	CMD24
CA3_B	CMD13	CA3_B	CMD33
CA4_B	CMD7	CA4_B	CMD23
CA5_B	CMD11	CA5_B	CMD27
CA6_B	CMD15	CA6_B	CMD30
CA7_B	CMD14	CA7_B	CMD31
CA8_B	CMD3	CA8_B	CMD19
CA9_B	CMD1	CA9_B	CMD17
CAB1_B	CMD6	CAB1_B	CMD22
CAB2_B	CMD10	CAB2_B	CMD26
RESET*	CMD2	RESET*	CMD18



PD Controller



DP MUX



Type C

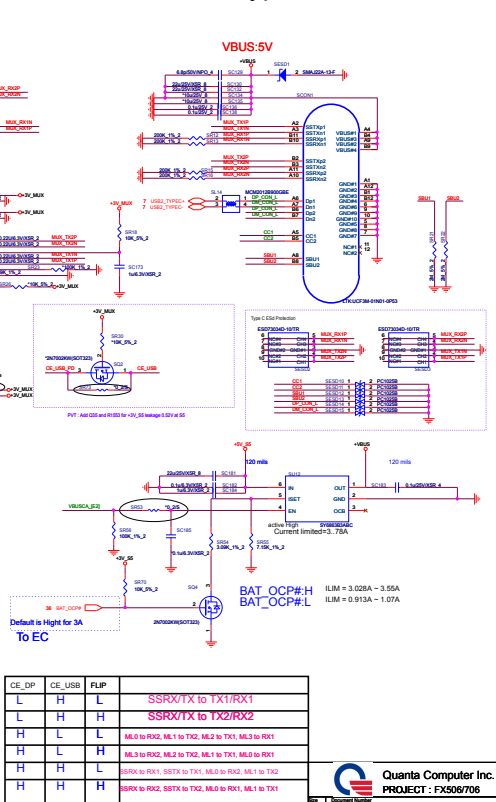


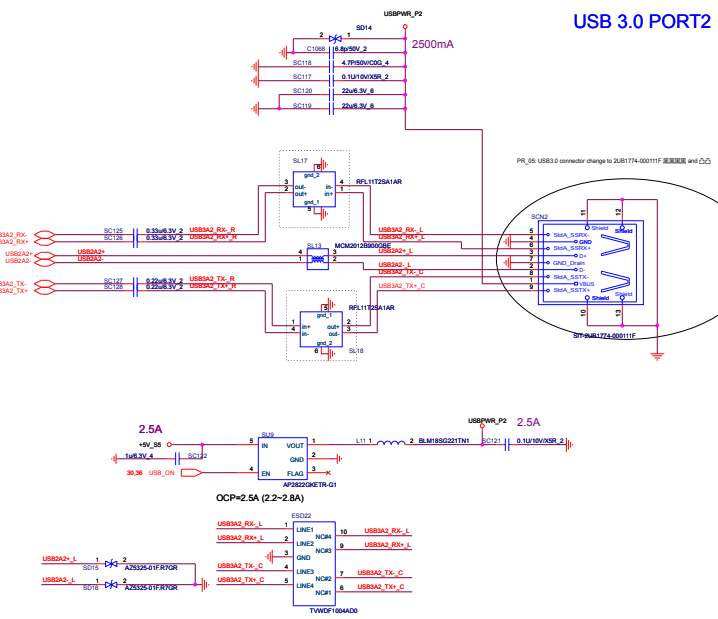
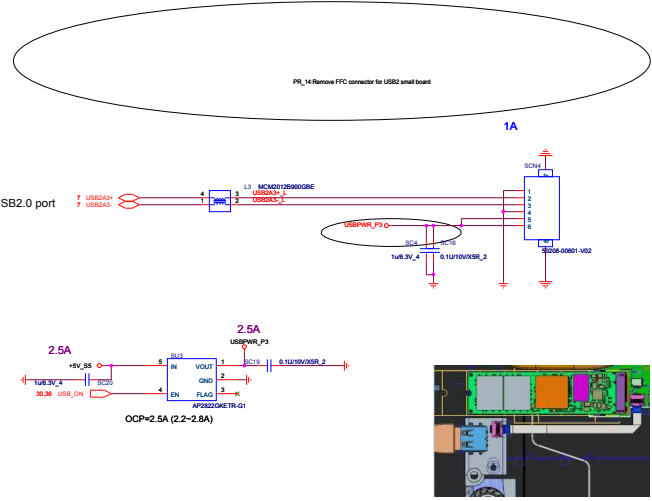
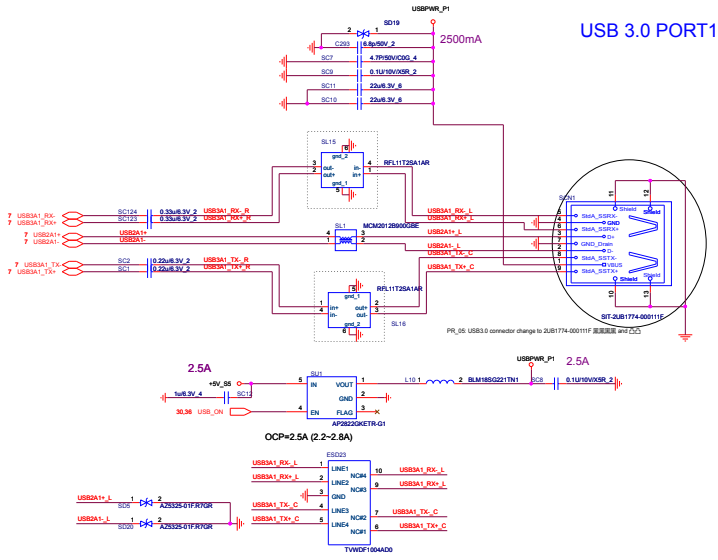
Table 6-1: I2C Slave ID Decodes

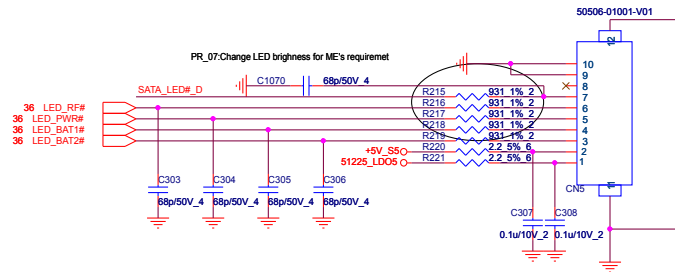
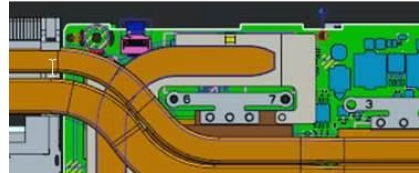
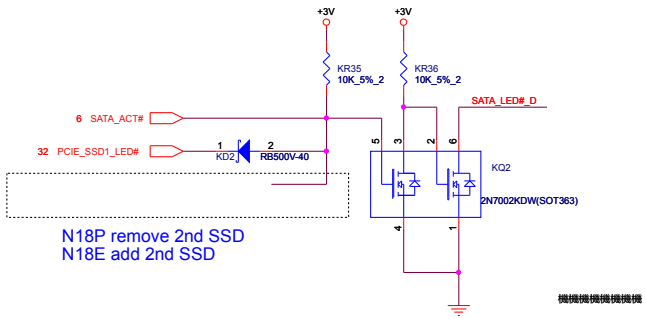
MSB	MSB	Slave ID
0	0	7100
0	1	7102
1	0	7100
1	1	7102

CE_DP	CE_USB	FLIP	SSRX/TX to TX1/RX1
L	H	L	SSRX/TX to TX1/RX1
L	H	H	SSRX/TX to TX2/RX2
H	L	L	ML0 to RX2, ML1 to TX2, ML2 to TX1, ML3 to RX1
H	L	H	ML0 to RX2, ML1 to TX2, ML2 to TX1, ML3 to RX1
H	H	L	SSRX to RX1, SS7X to TX1, ML0 to RX2, ML1 to TX2
H	H	H	SSRX to RX2, SS7X to TX2, ML0 to RX1, ML1 to TX1

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Type C & DP & DP MUX

The part should not contain any substance which is specified in RoHS 2002.

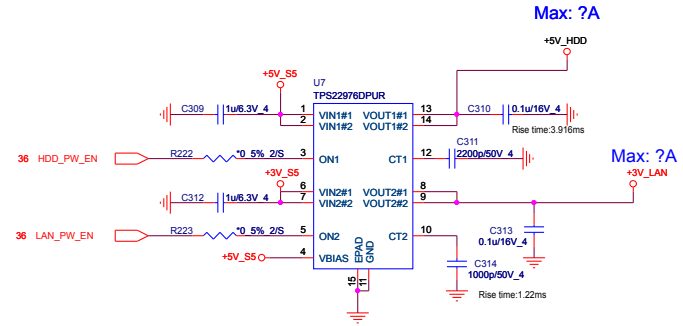
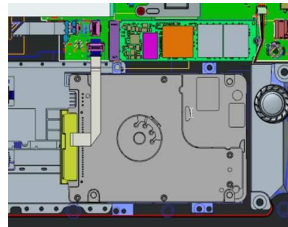
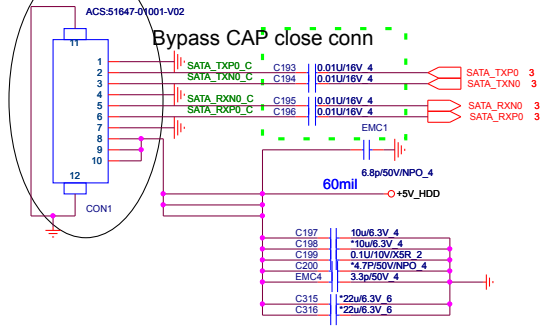




SATA HDD FFC

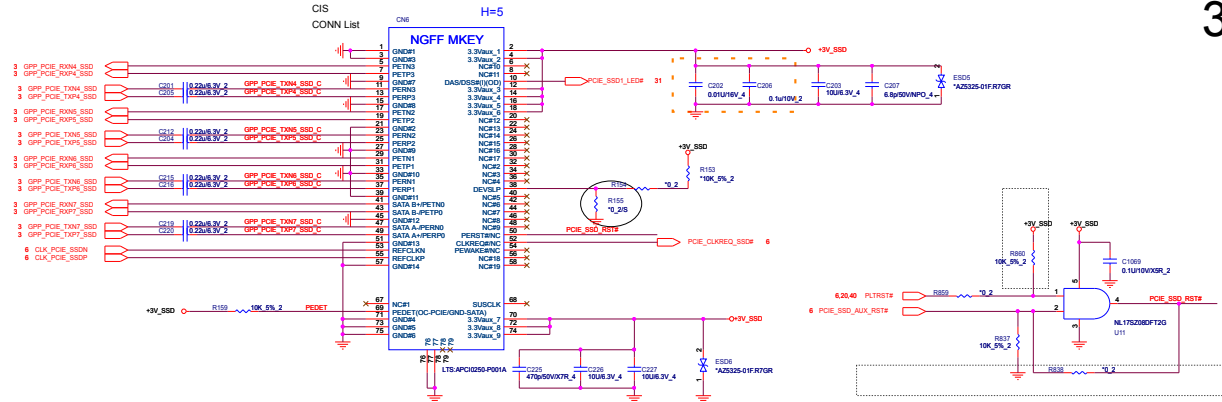
CIS PR_06:HDD Connector pin define swap by ME's requirement

CONN List

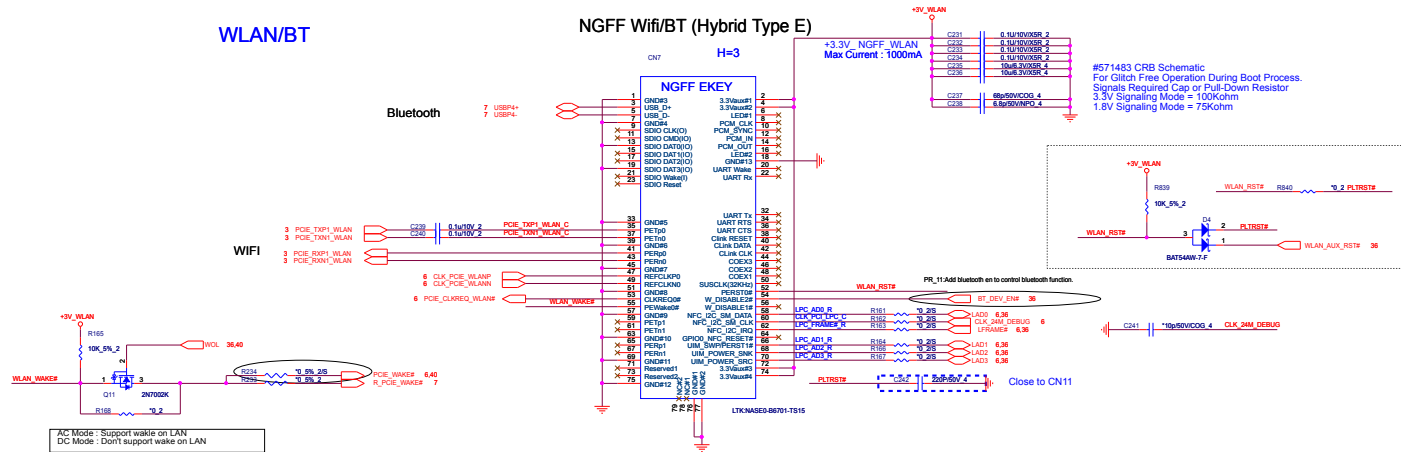


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SSD



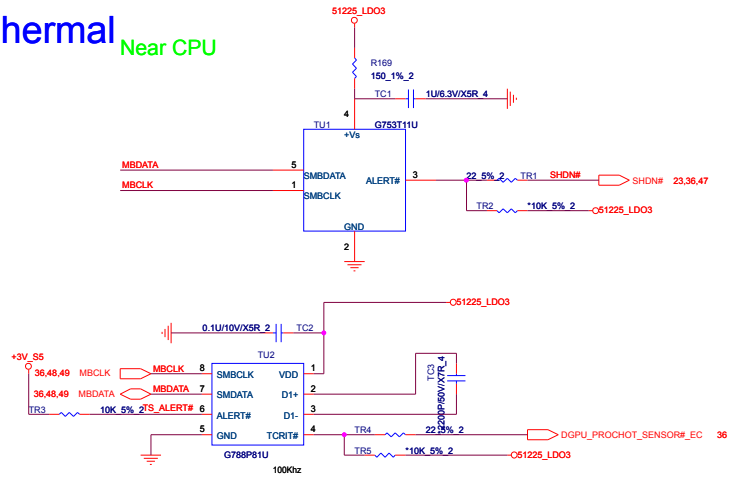
WLAN/BT



Ac Mode : Support wake on LAN
Dc Mode : Don't support wake on LAN

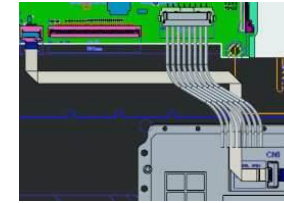
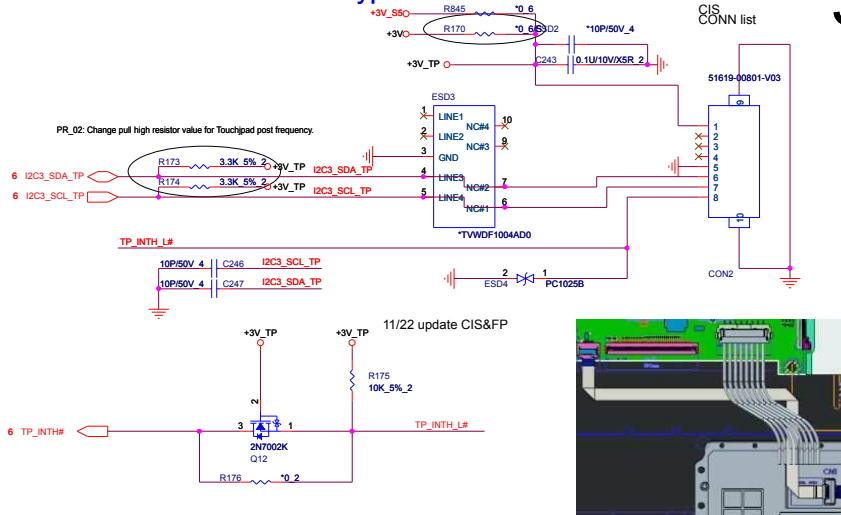
Thermal

Near CPU

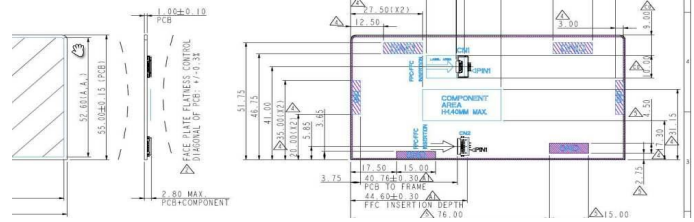


Touch Pad Connector AA type

30

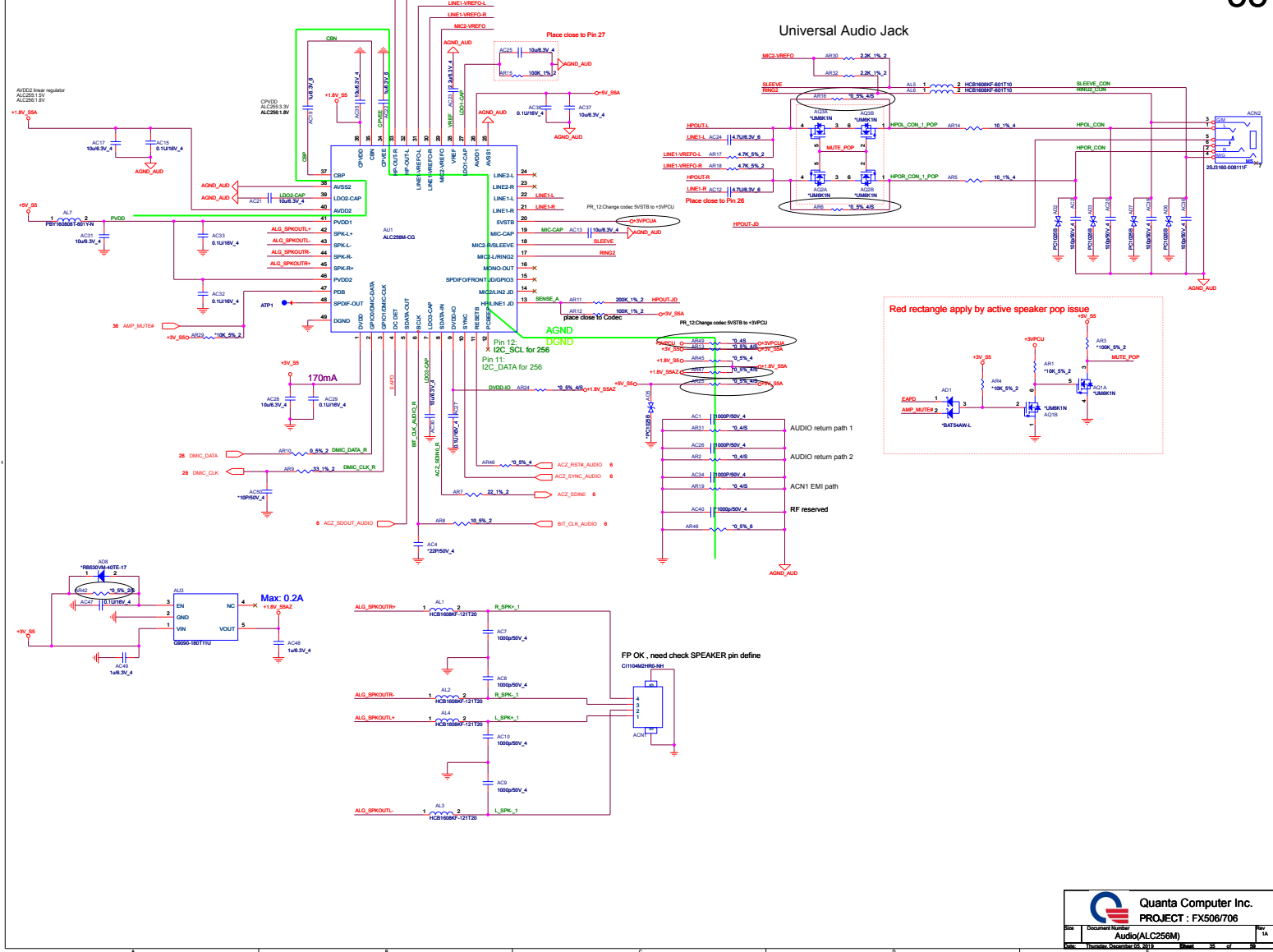


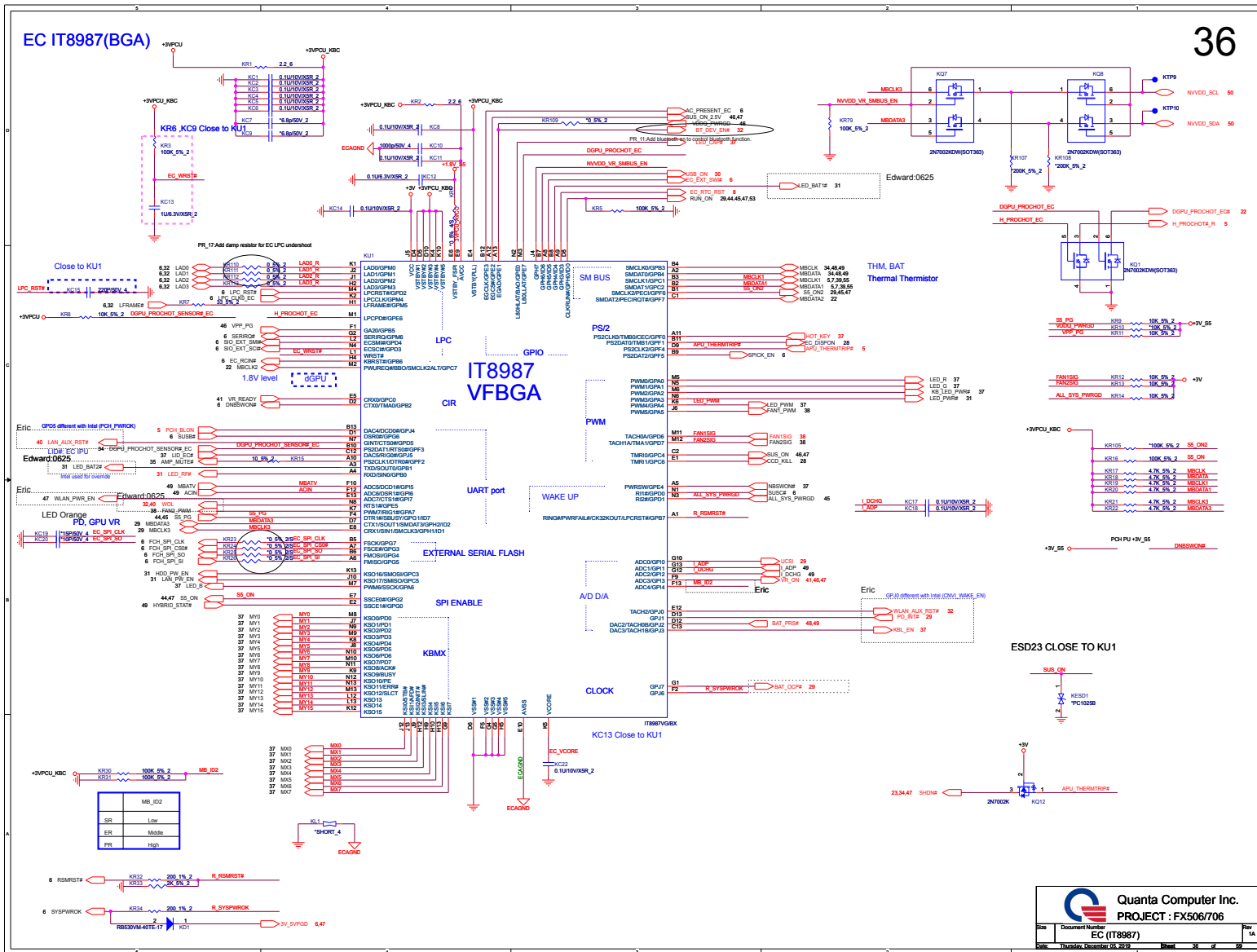
CN1	CN2	UPDATE DESCRIPTION	REMARK	STATUS	APPROVED		
PIN NO.	PIN DEFINE*	PIN NO.	PIN DEFINE*	EVAL-021011-2-1	MODIFY FLATNESS		MIRE
1	TPINT*	1	GND	EVAL-021011-03-0	DESIGNING FOR OPTIMIZE X2 8		RICKY
2	I2C_SCL	2	GND	EVAL-021011-03-1	MODIFY COMPONENT AREA SIZE ADD GND PAD		RICKY
3	I2C_SDA	3	SWR	EVAL-021011-03-1	ADJUST GND PAD LOCATION, REMOVE PIN1		RICKY
4	GND	4	SWL	REV-ADD 2011-03-11	INITIAL RELEASE		RICKY
5	PS2_DT			ANV-AD1 2011-05-03	REPOSITION DEPTH W/REP TO FRM		RICKY
6	PS2_CLK			ANV-REV 2011-07-19	REV LABEL AREA		ALEX
7	NC			ANV-REV 2011-07-20	MODIFY LABEL POSITION		ALEX
8	VDD_3.3V						



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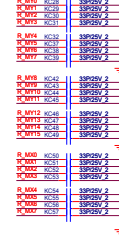
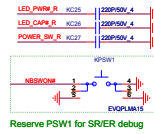
Size	Document Number	Rev
	TP/Thermal	1A
Date:	Thursday, December 05, 2019	Sheet 34 of 59





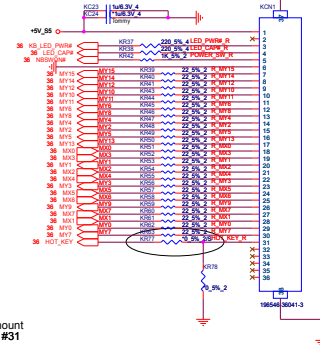
KEYBOARD Con.

37



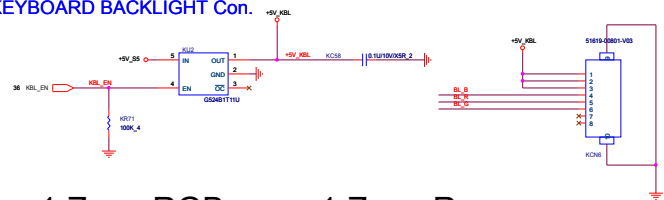
Add 22ohm for ESD

4/6: Add KR129 0ohm no-mount and KR130 0ohm on KCN1#31

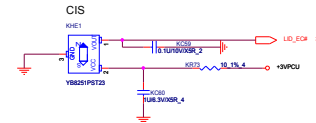


OK

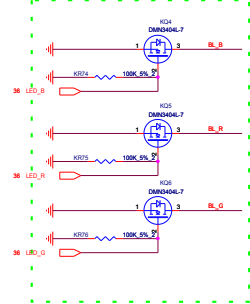
KEYBOARD BACKLIGHT Con.



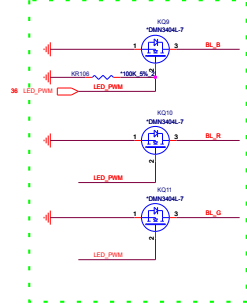
ESD23 CLOSE TO KHE1



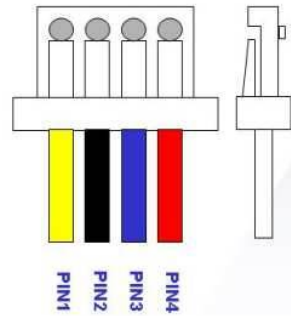
1 Zone RGB



1 Zone R

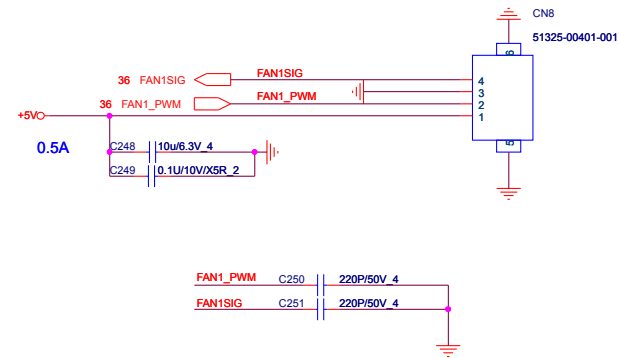


4Pins Fan Connector Pins Definition

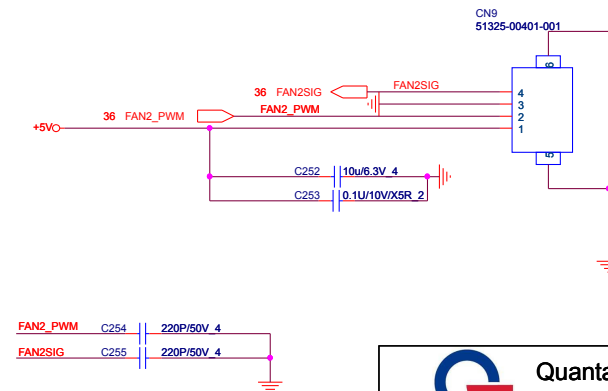



Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

FAN1 for GPU(New)



FAN2 for CPU

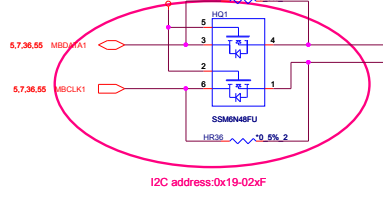



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 PROJECT : FX506/706

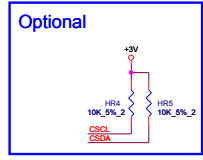
Size	Document Number	Rev
	FAN	1A

Date: Thursday, December 05, 2019 Sheet 38 of 59

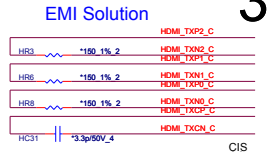
HDMI 2.0 Re-Driver



I2C address: 0x19-024F



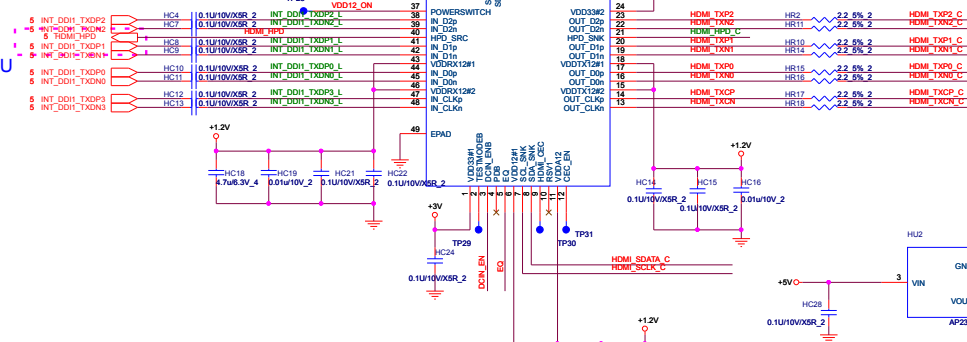
Optional



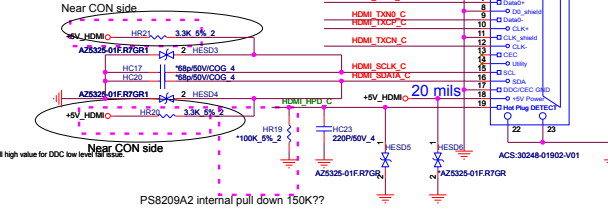
EMI Solution

HDMI_HPD to APU and Level shift to NV

From APU



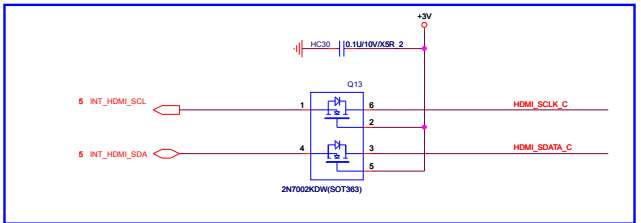
PR_08 Change HDMI pull high value for DDC low level fail issue.



PR_08 Change HDMI pull high value for DDC low level fail issue.

PS8209A2 internal pull down f50K??

3.3V and 5V Level shifter

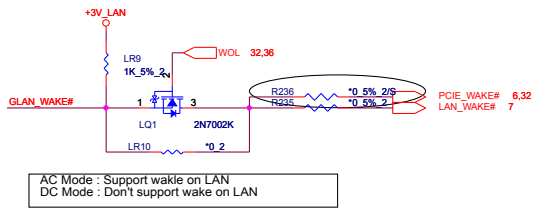
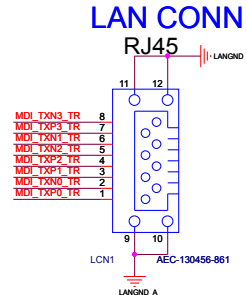
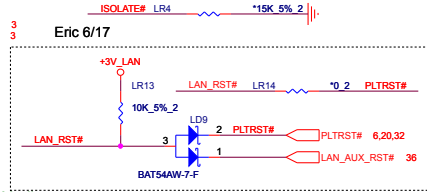
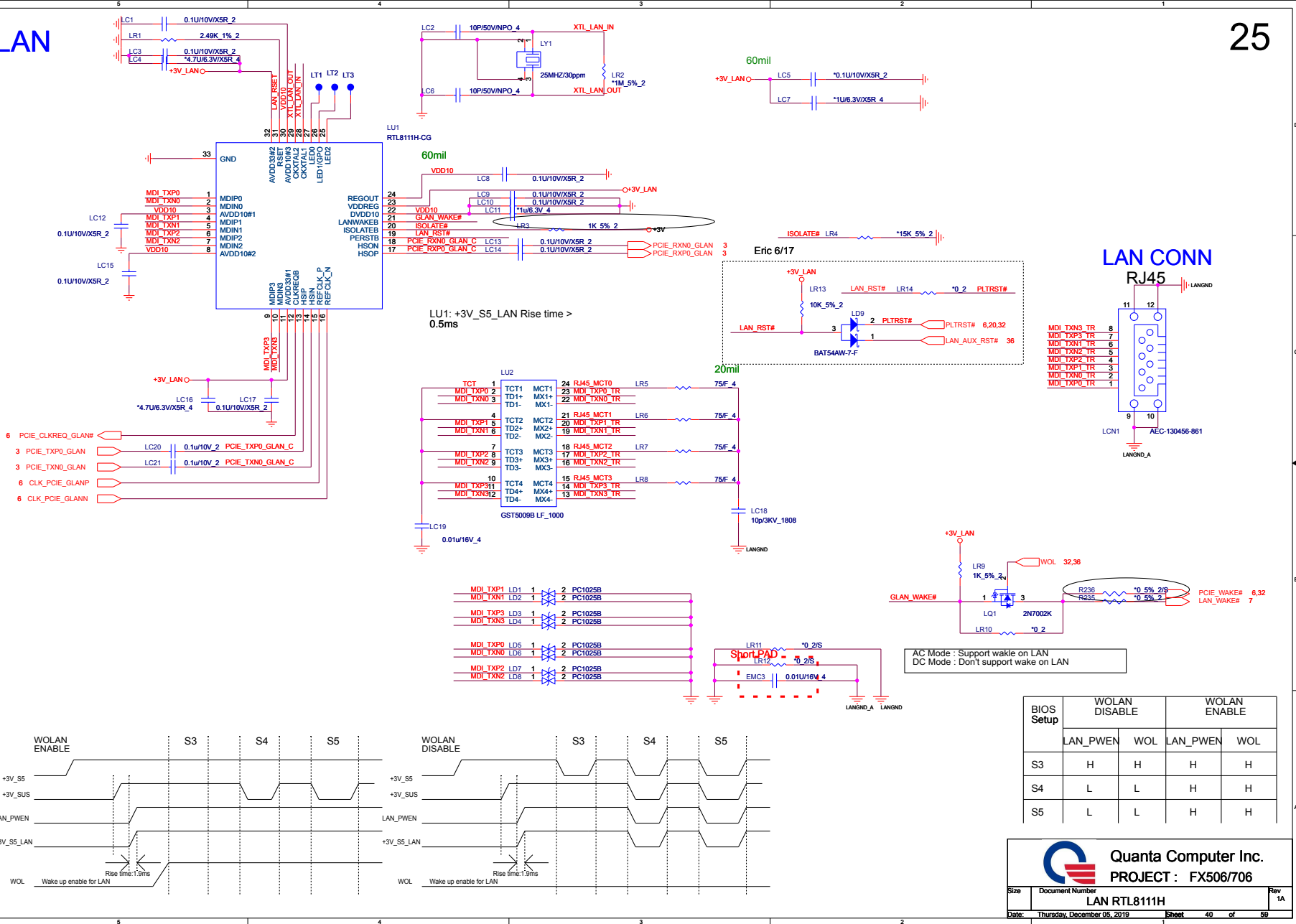


<p>DCEN_EN HR31 4.7K 5% 2</p>	<p>DC coupling enable; Internal pull up, 3.3V I/O. L: DC coupling input H: Default, AC coupling input</p>
<p>EQ HR24 4.7K 5% 2 HR32 4.7K 5% 2</p>	<p>Receiver equalization setting; Internal pull up, 3.3V I/O. L: Compensation for channel loss up to 13dB H: Default, Compensation for channel loss up to 17dB M: Compensation for channel loss up to 11dB</p>
<p>PRE HR30 4.7K 5% 2</p>	<p>Output pre-emphasis setting; Internal pull up, 3.3V I/O. L: Pre-emphasis = 2.5dB H: Default, No Pre-emphasis</p>
<p>I2C_ADDR HR23 4.7K 5% 2</p>	<p>I2C Slave Address selection; Internal pull down, 3.3V I/O: L: Default, Slave address 0x10-0x2F. H: Alternative slave address 0x50-0x5F, 0x60-0x6F.</p>
<p>HDMI_ID HR25 4.7K 5% 2</p>	<p>HDMI ID enable; Internal pull down, 3.3V I/O. L: Default, HDMI ID enable H: HDMI ID disable</p>

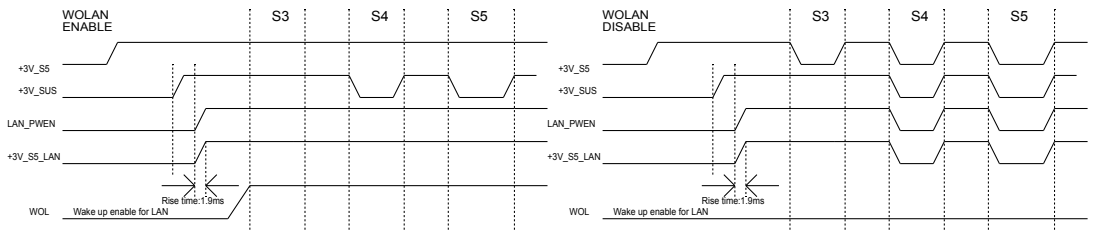
ESD73034D-10TR	6	NGM4	GHM4	5	HDMI_TXP2_C
	7	NGM5	GHM5	3	HDMI_TXN2_C
	8	ONGM6	GOM6	2	HDMI_TXP1_C
	10	NGM2	GHM2	2	HDMI_TXN1_C
	10	NGM1	GHM1	2	HDMI_TXCP_C
					HESJ2

Quanta Computer Inc.
PROJECT : FX506706
 Size Document Number
HDMI 2.0 Redriver
 Date: Thursday, December 05, 2019 Sheet 39 of 89 Rev 1A

LAN



BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H

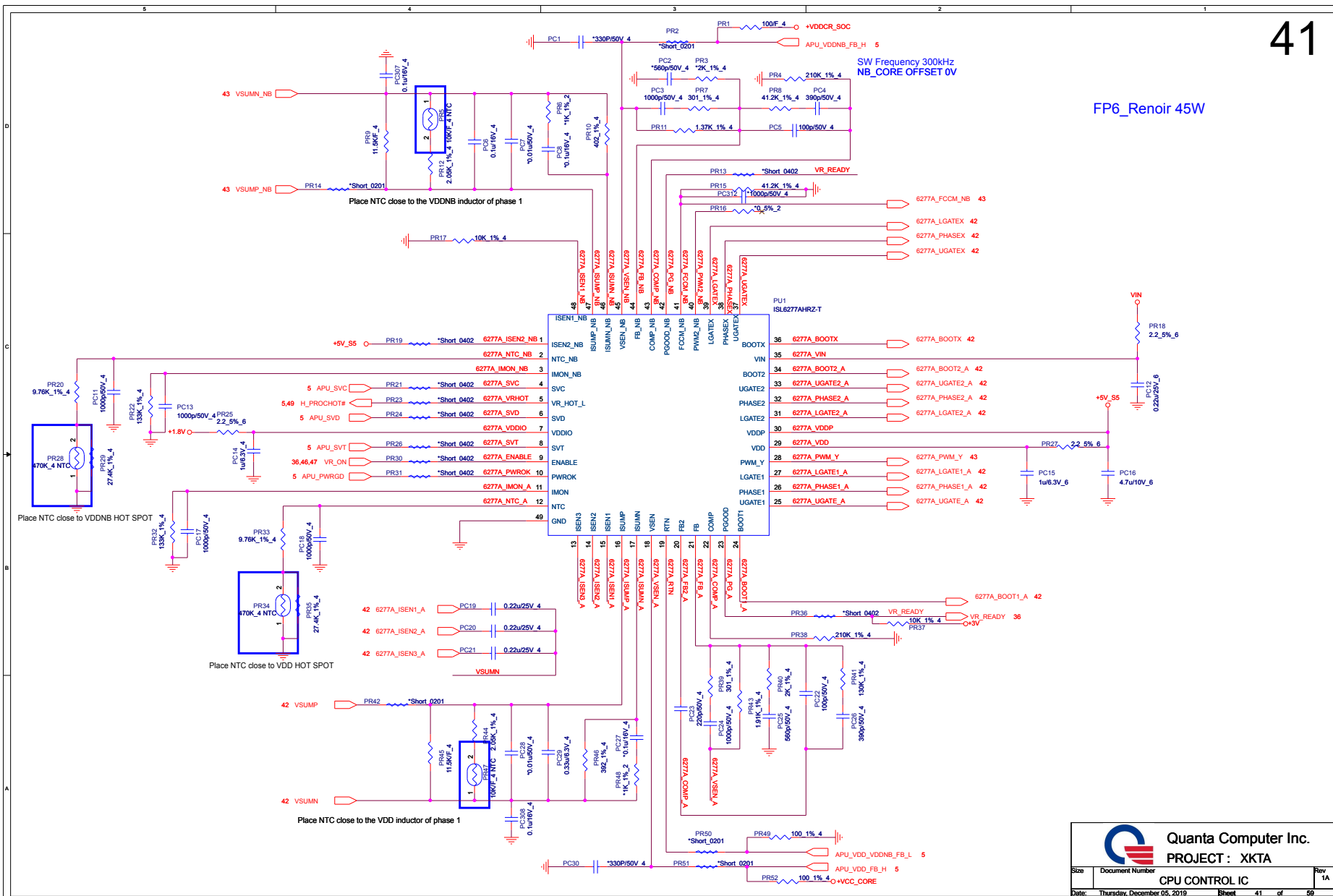



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PROJECT : FX506/706

Size	Document Number	Rev
	LAN RTL8111H	1A

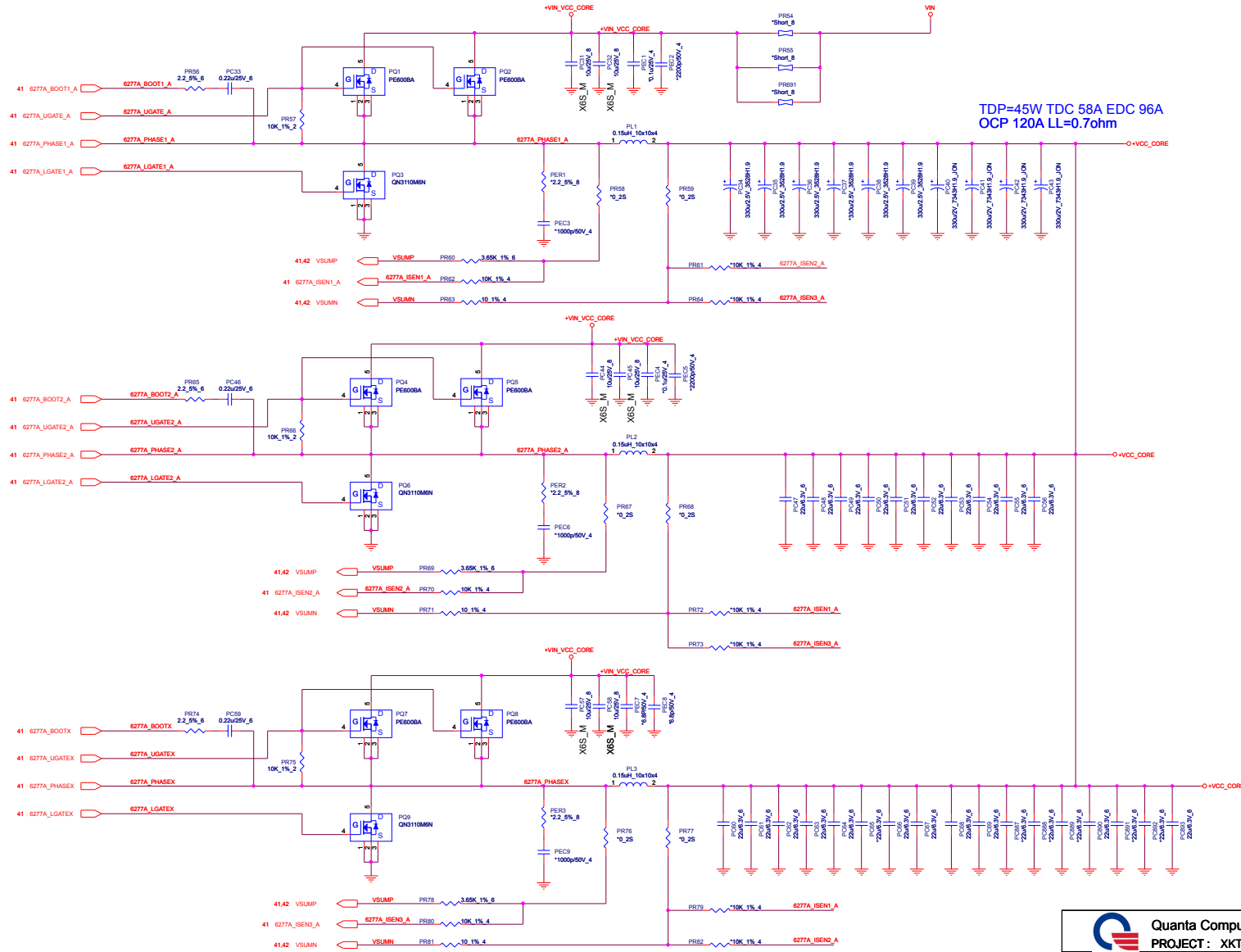
Date: Thursday, December 05, 2019 Sheet 40 of 59


FP6_Renoir 45W



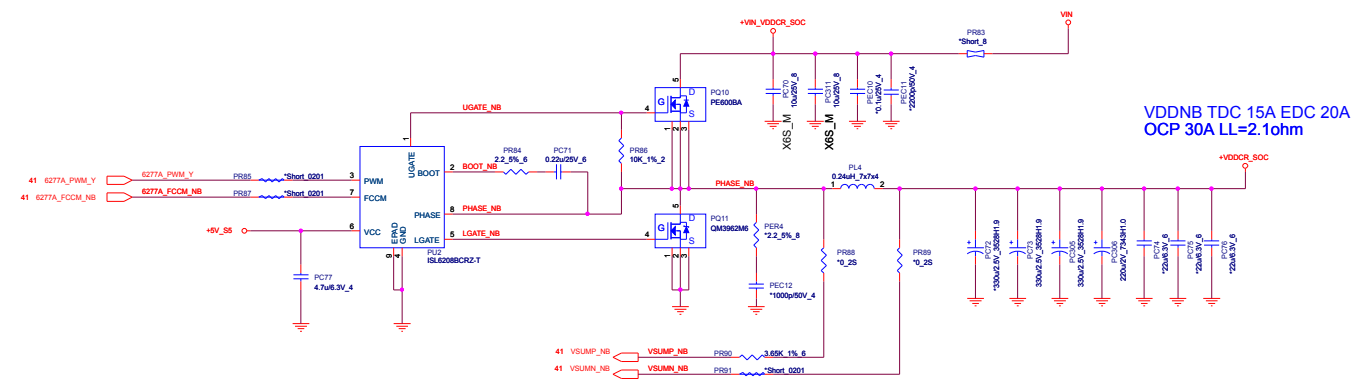

Quanta Computer Inc.
 PROJECT : XKTA
 Size Document Number
CPU CONTROL IC
 Date: Thursday, December 05, 2019 Sheet 41 of 80 Rev 1A

VCORE

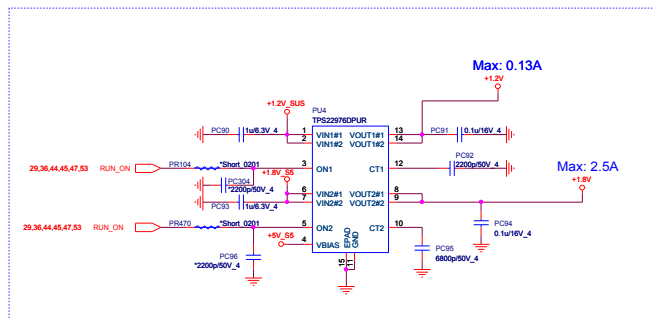
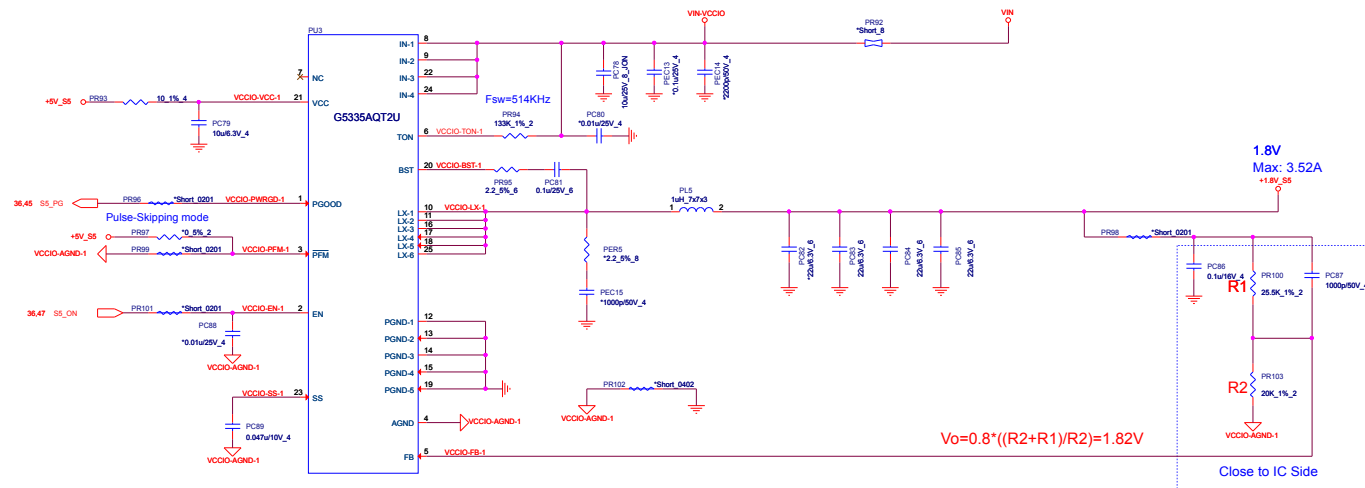


 Quanta Computer Inc. PROJECT : XKTA		
Size	Document Number	Rev
		1A
VCORE POWER		
Date	Thursday, December 05, 2019	Sheet 42 of 80

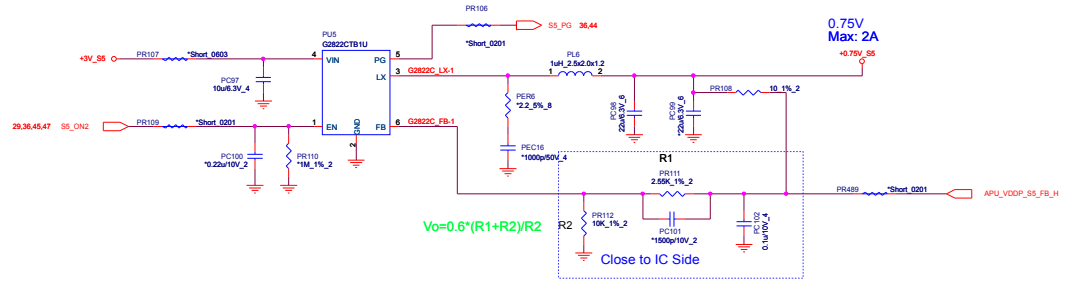
+NB_CORE



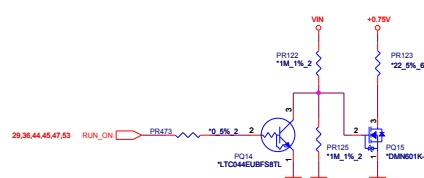
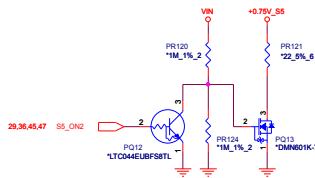
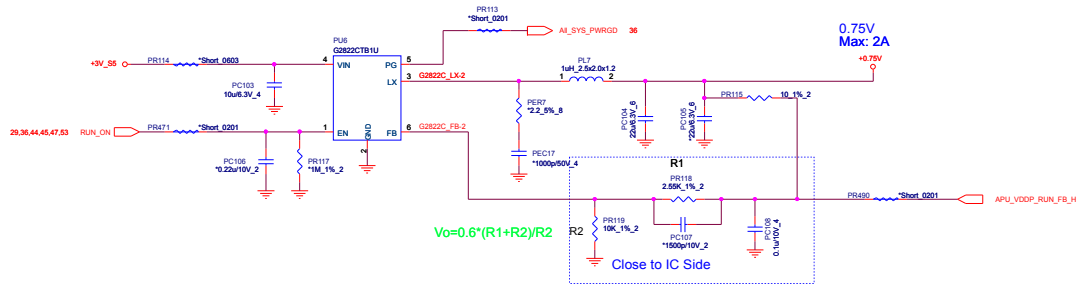
+1.8V_S5



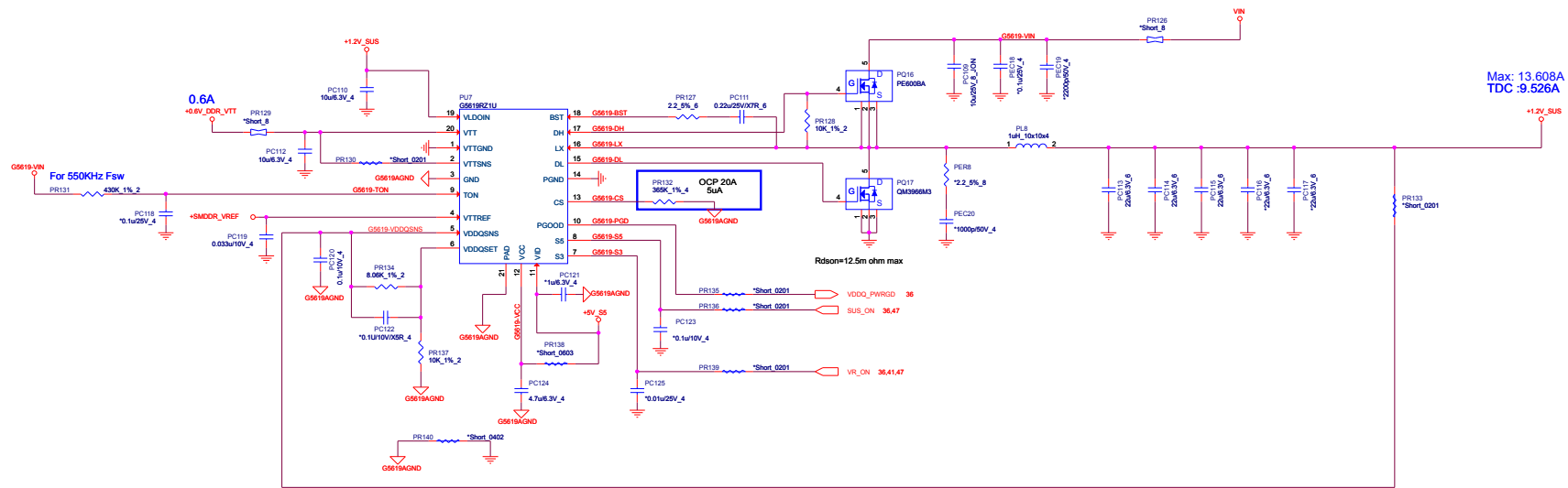
+0.75V_S5



+0.75V

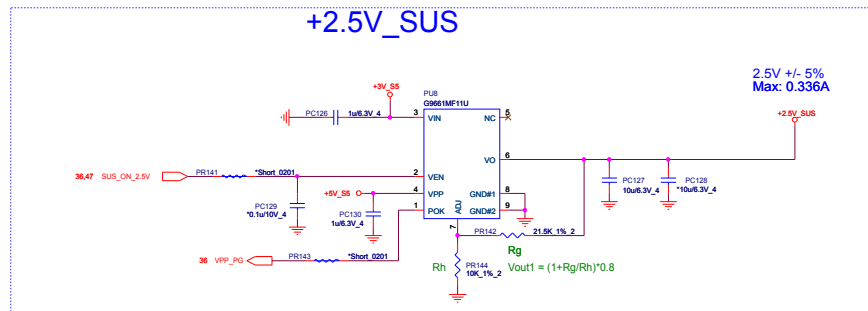


1.2VSUS & VTT_MEM

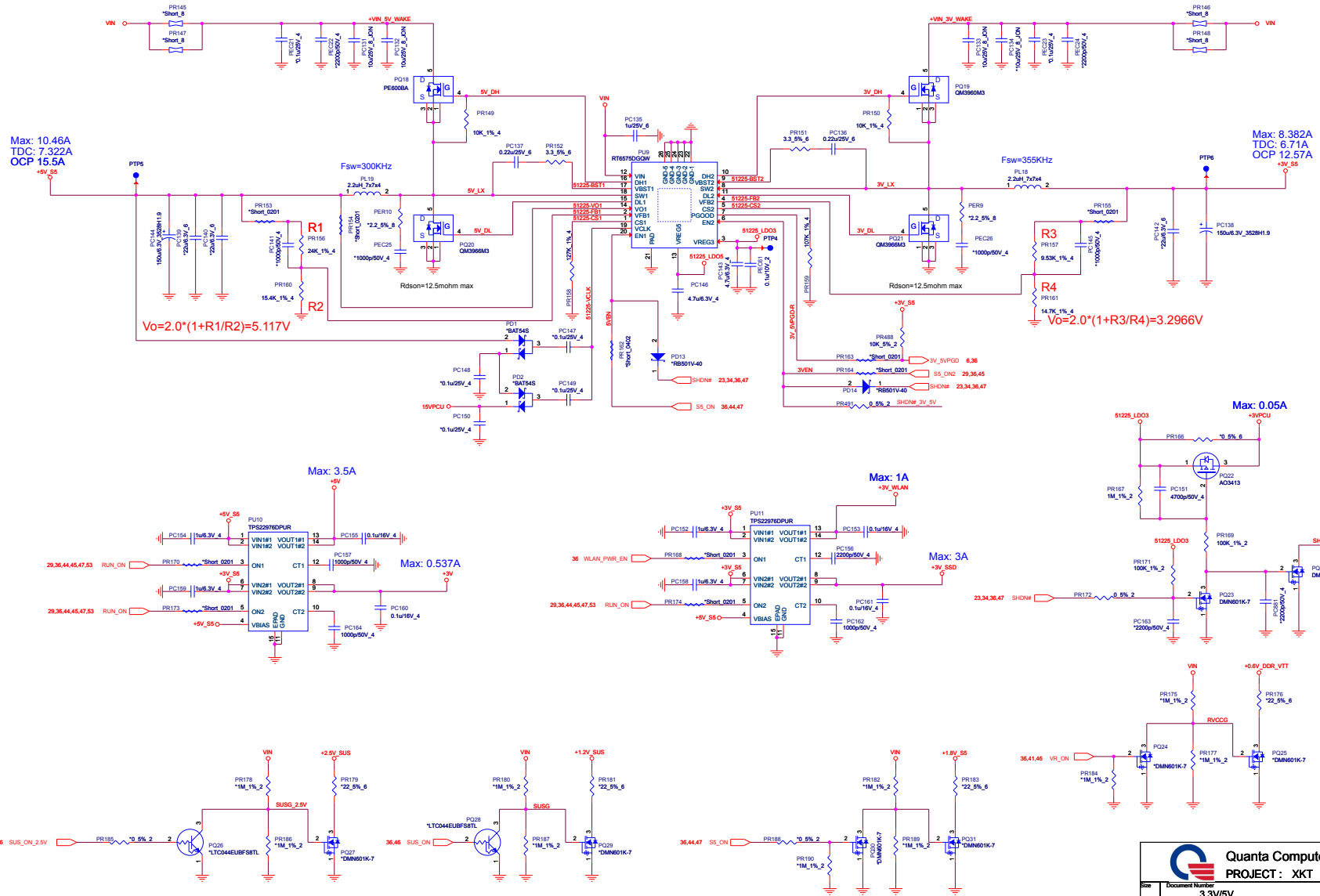


Max: 13.608A
TDC :9.526A

+2.5V_SUS



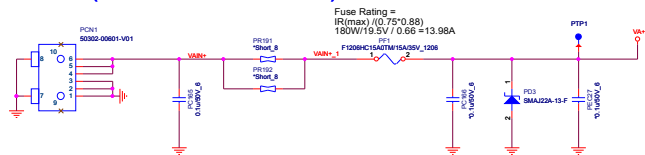
3.3V & 5V



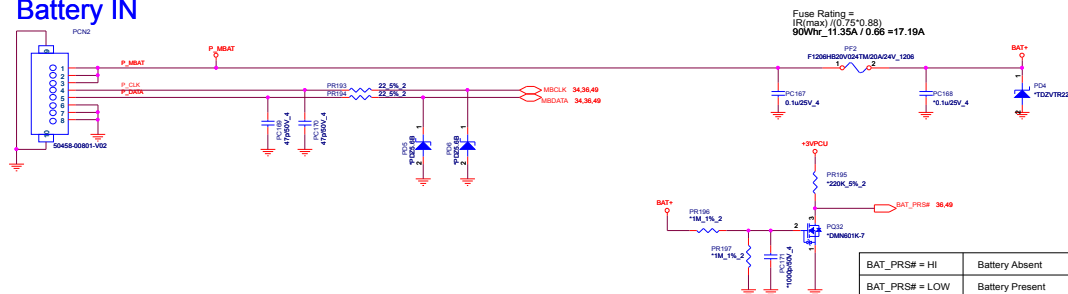
Quanta Computer Inc.
PROJECT: XKT

Doc	Document Number	Rev
	3.3V/5V	3A
Date:	Thursday, December 05, 2019	Sheet 47 of 99

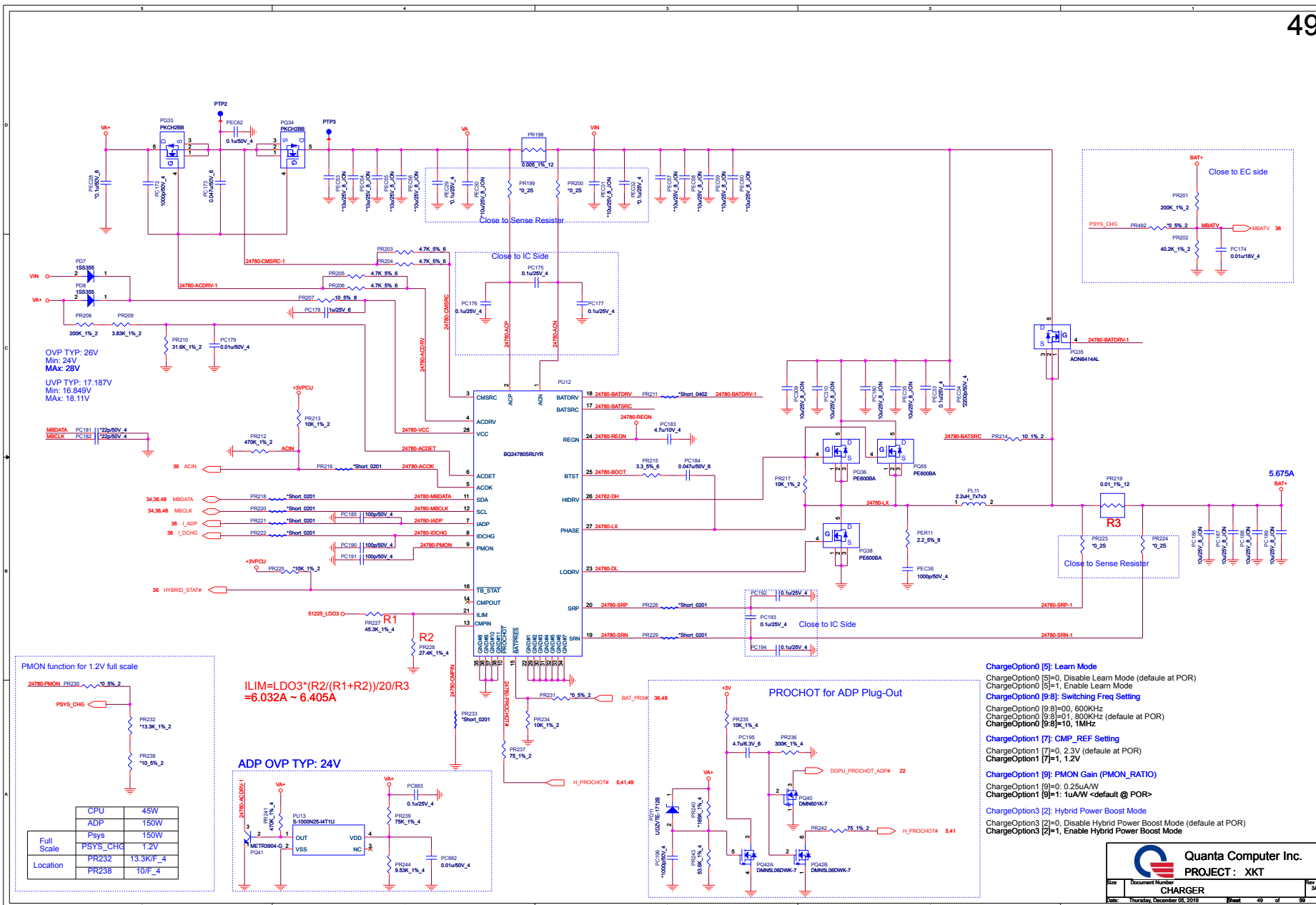
AC IN (On-Board DC-Jack)

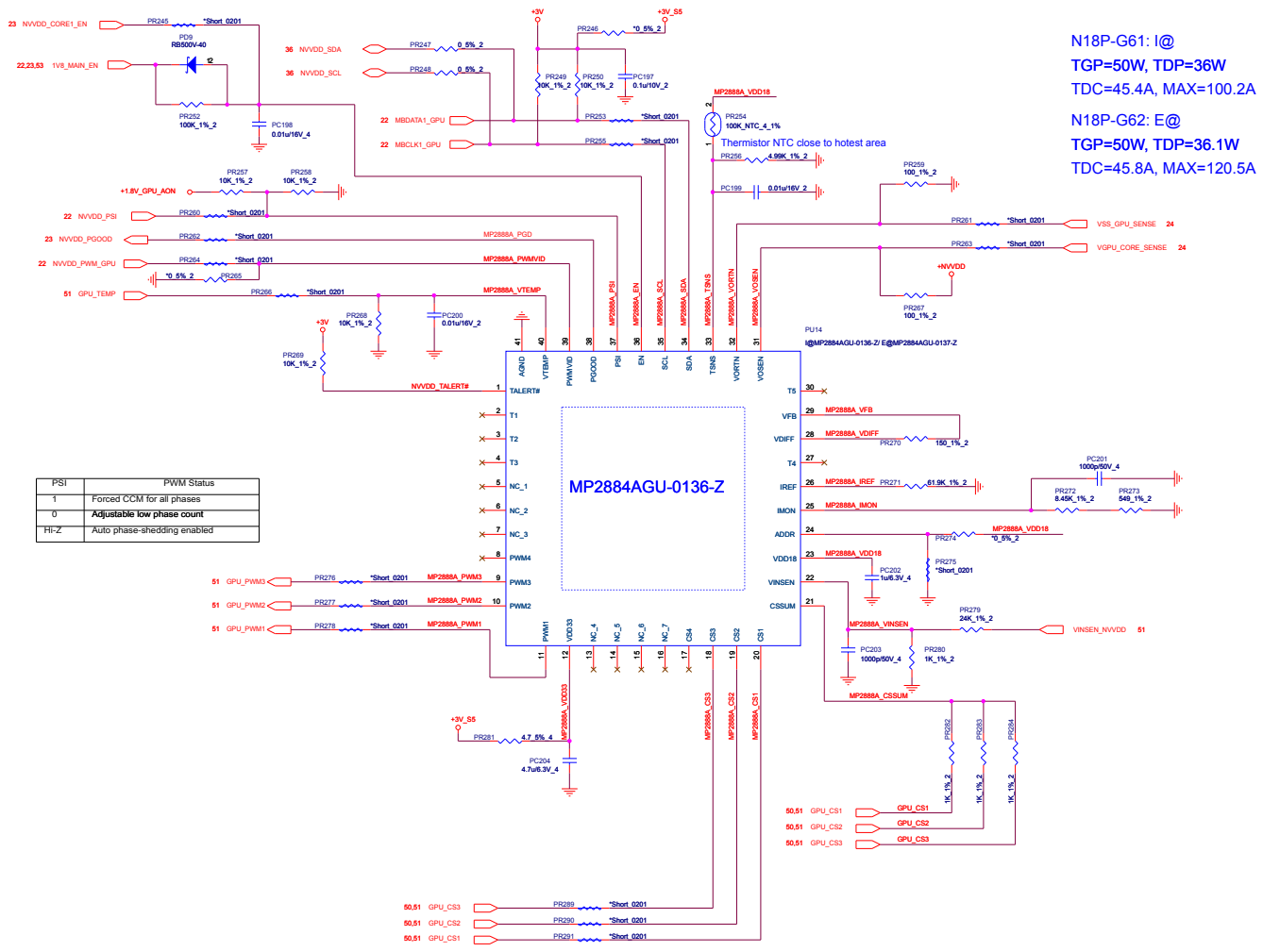


Battery IN



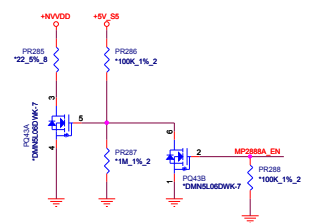
BAT_PRS# = HI	Battery Absent
BAT_PRS# = LOW	Battery Present



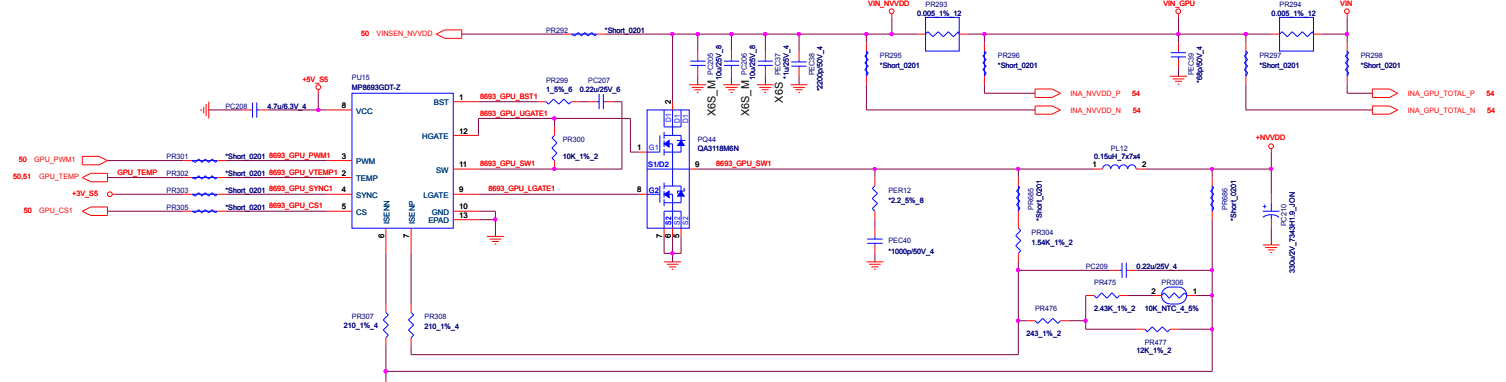


N18P-G61: I@
 TGP=50W, TDP=36W
 TDC=45.4A, MAX=100.2A
 N18P-G62: E@
 TGP=50W, TDP=36.1W
 TDC=45.8A, MAX=120.5A

PSI	PWM Status
1	Forced CCM for all phases
0	Adjustable low phase count
Hi-Z	Auto phase-shedding enabled

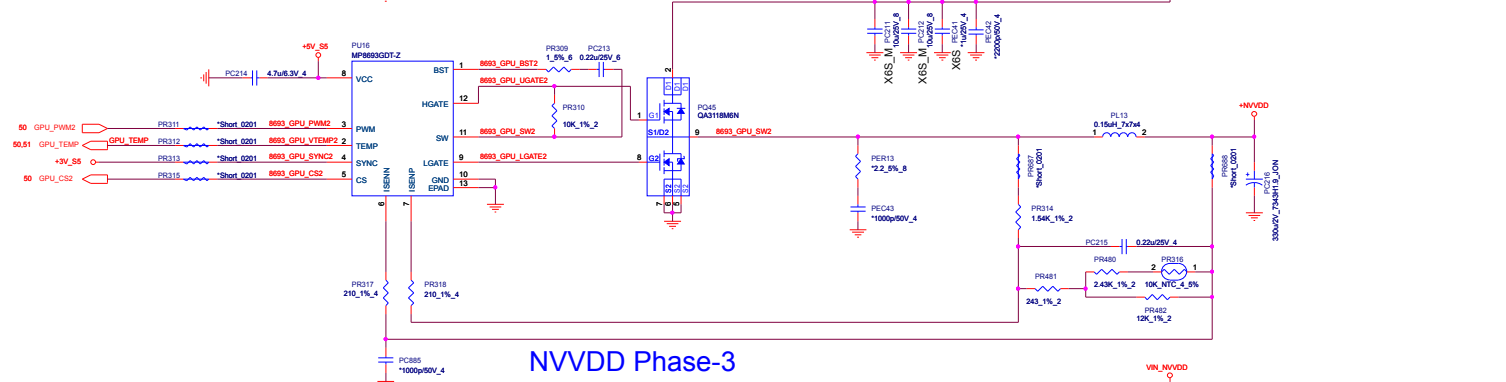


NVDD Phase-1

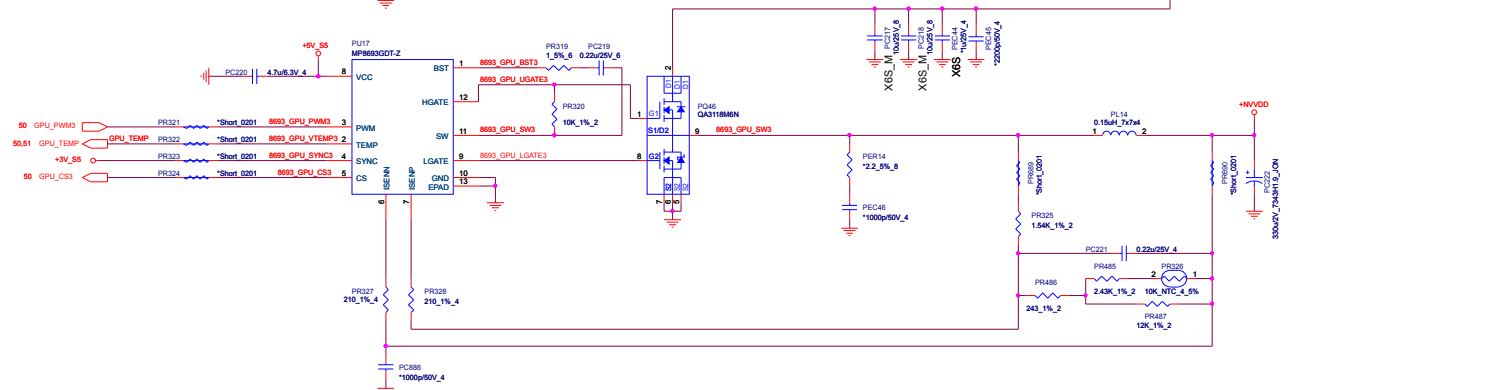



N18P-G61
 TGP=50W, TDP=36W
 TDC=45.4A, MAX=100.2A
 N18P-G62
 TGP=50W, TDP=36.1W
 TDC=45.8A, MAX=120.5A

NVDD Phase-2



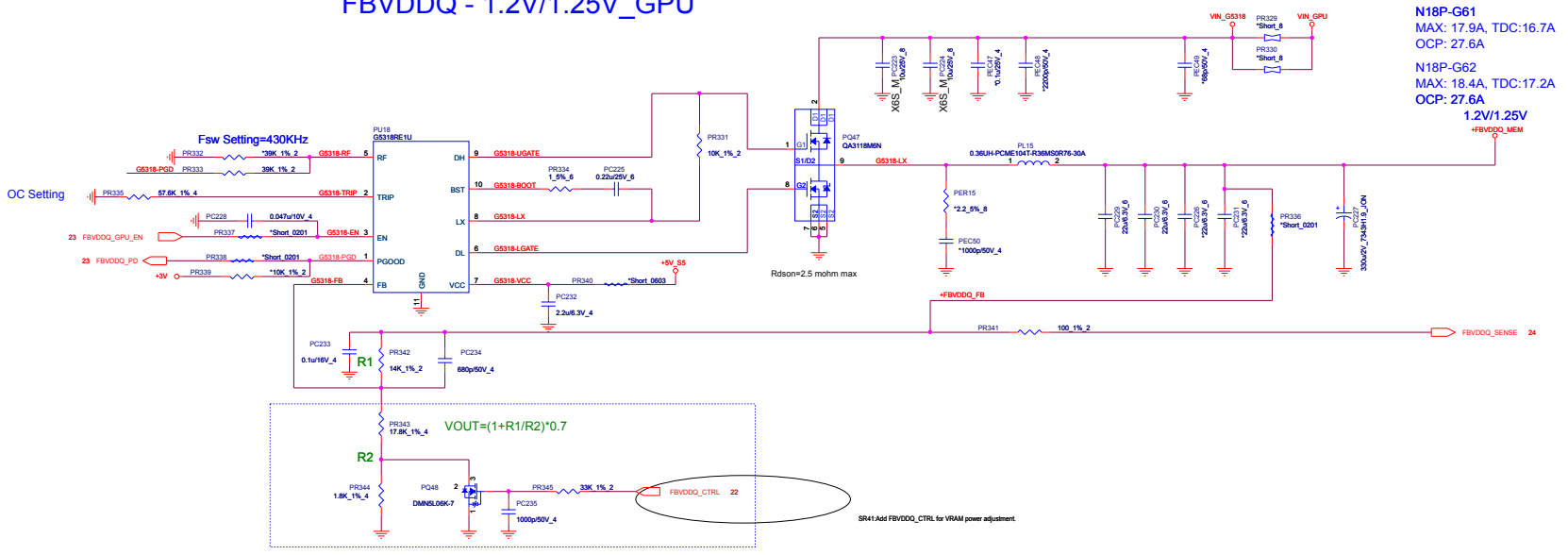
NVDD Phase-3



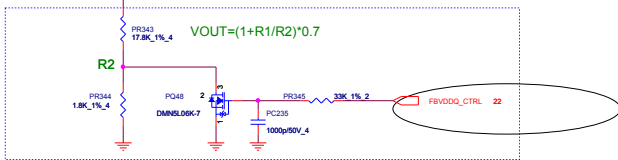
 **Quanta Computer Inc.**
 PROJECT : XKT

Site	Document Number	Rev
	dGPU CORE MP2886A)	1A
Date	Thursday, December 05, 2019	Sheet 51 of 69

FBVDDQ - 1.2V/1.25V_GPU

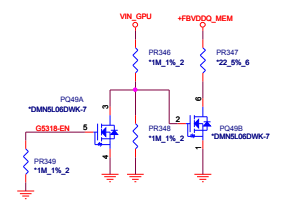


N18P-G61
 MAX: 17.9A, TDC:16.7A
 OCP: 27.6A
 N18P-G62
 MAX: 18.4A, TDC:17.2A
 OCP: 27.6A
 1.2V/1.25V
 +FBVDDQ_MEM

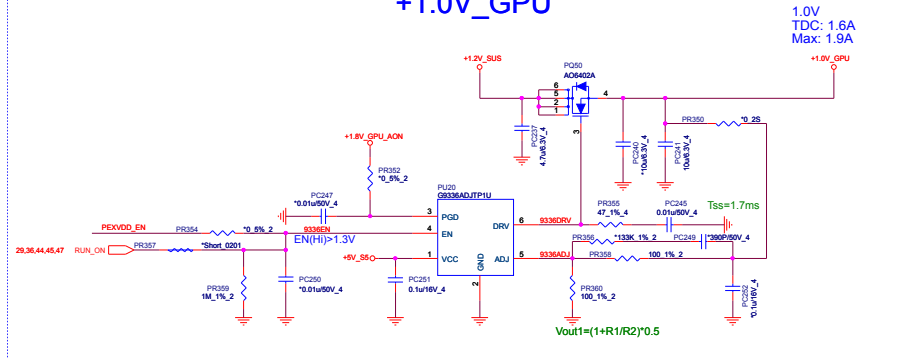


FBVDDQ Voltage Setting: 1.20V / 1.25V for MICRON & SAMSUNG VRAM

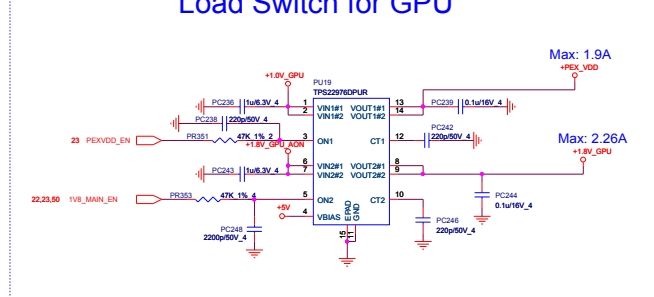
FBVDDQ_CTRL	PR343	PR344	FBVDDQ
1	17.8K(CS31782FB10)	1.8K(CS21802FB10)	1.25V
0	17.8K(CS31782FB10)	1.8K(CS21802FB10)	1.2V



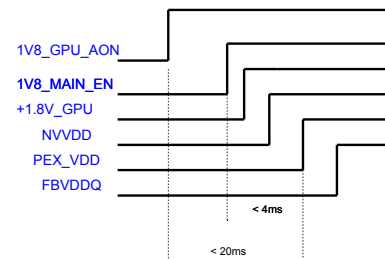
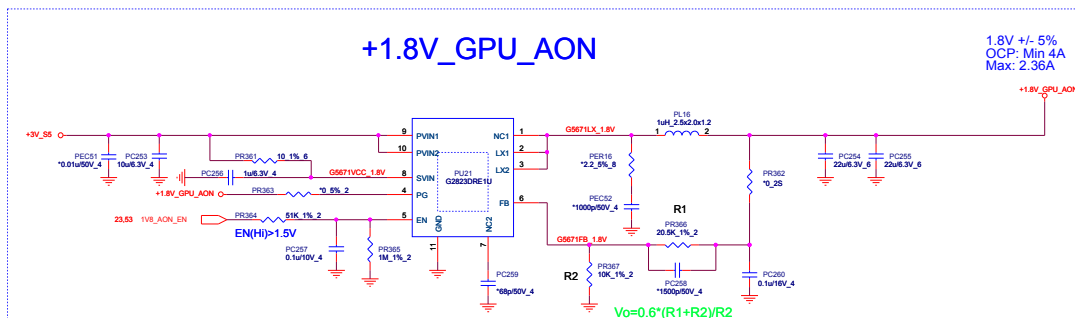
+1.0V_GPU



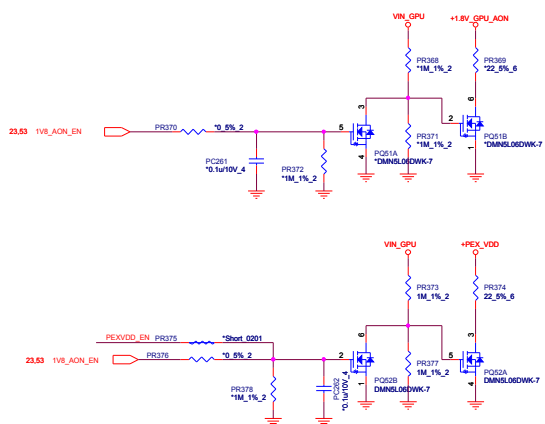
Load Switch for GPU



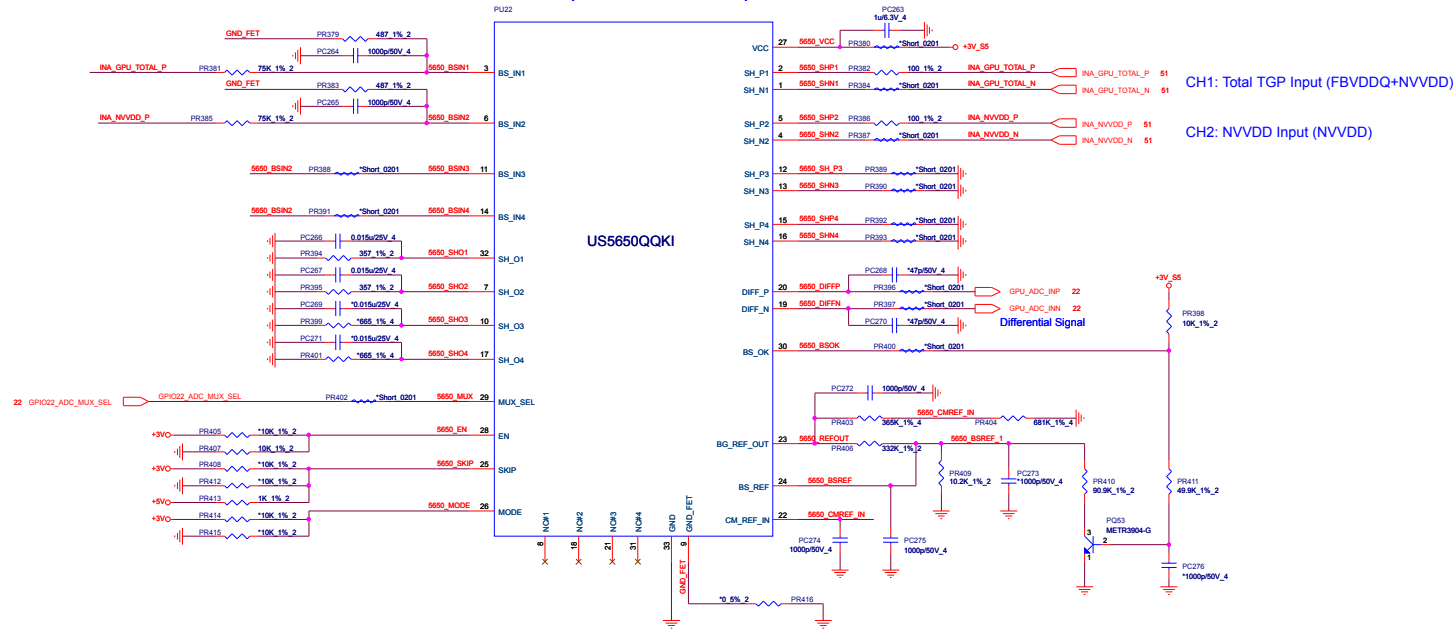
+1.8V_GPU_AON

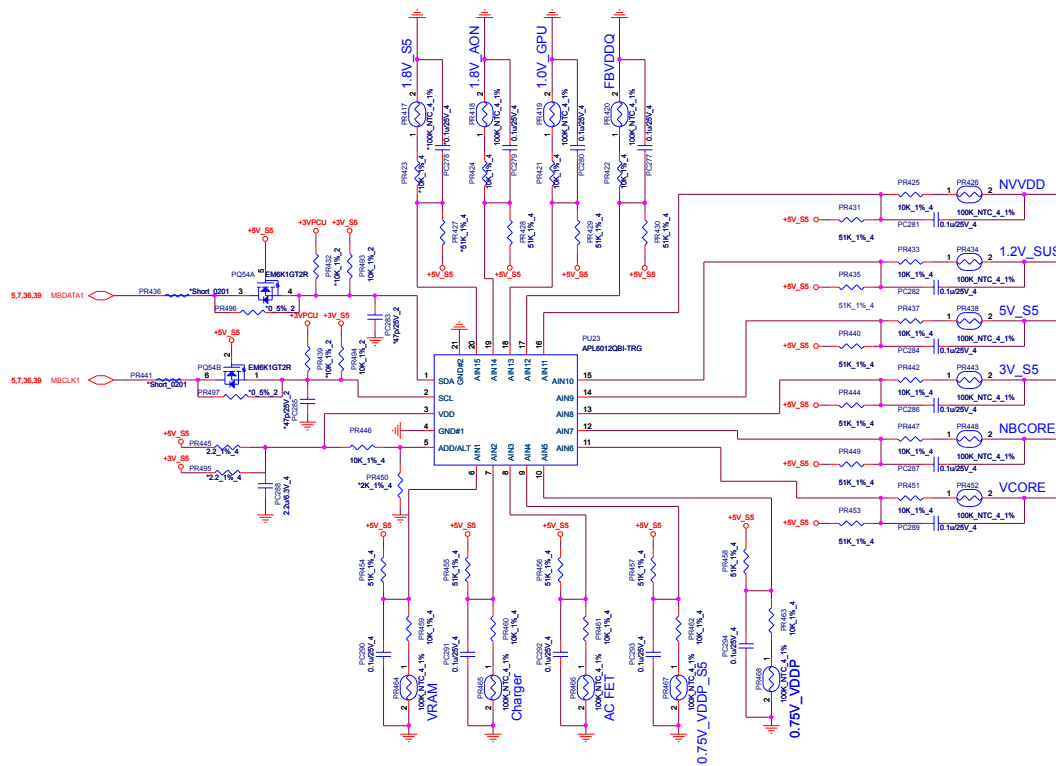


Discharge

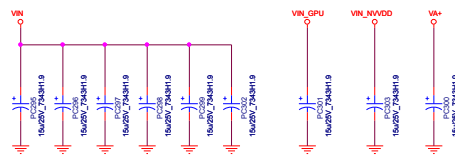


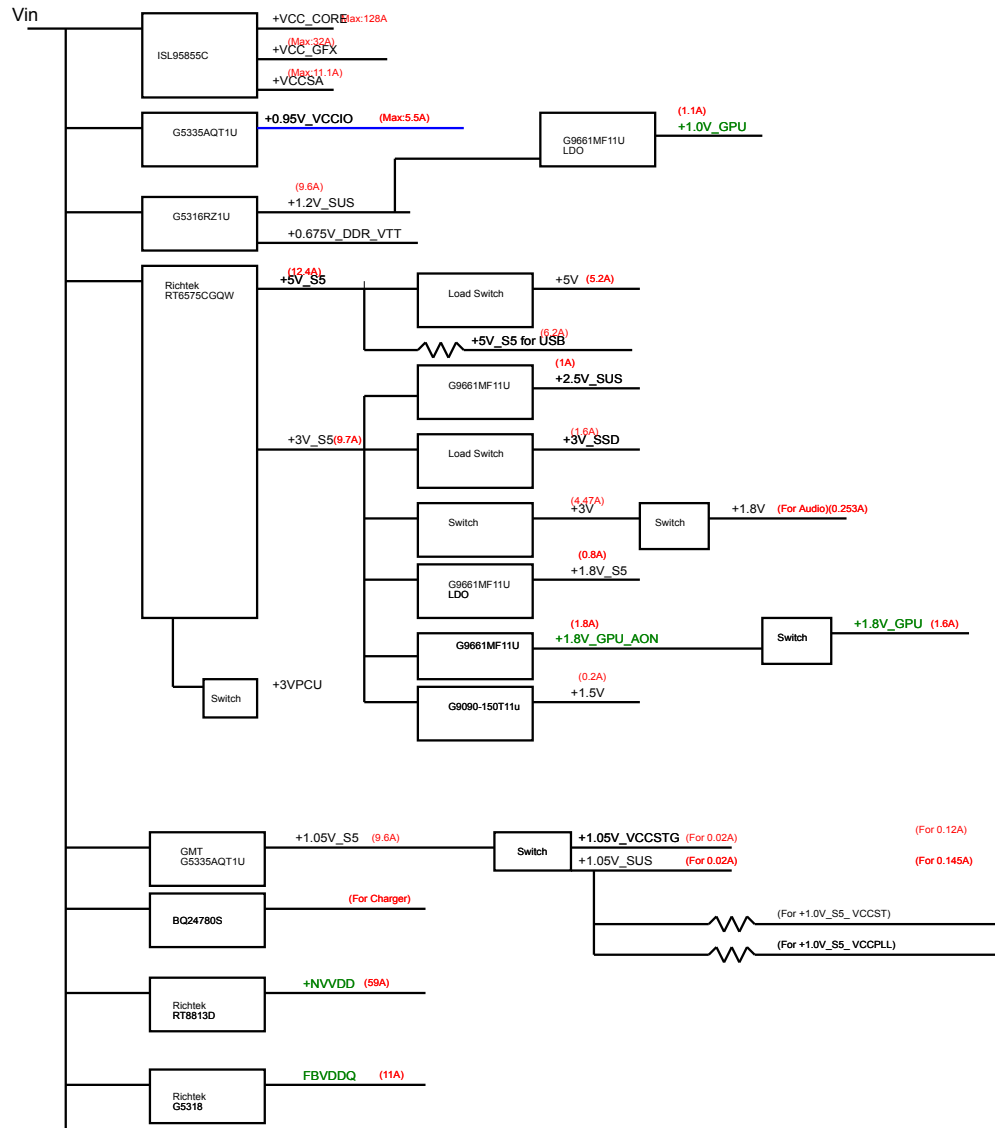
OVR-M(N18P-G61/G62)



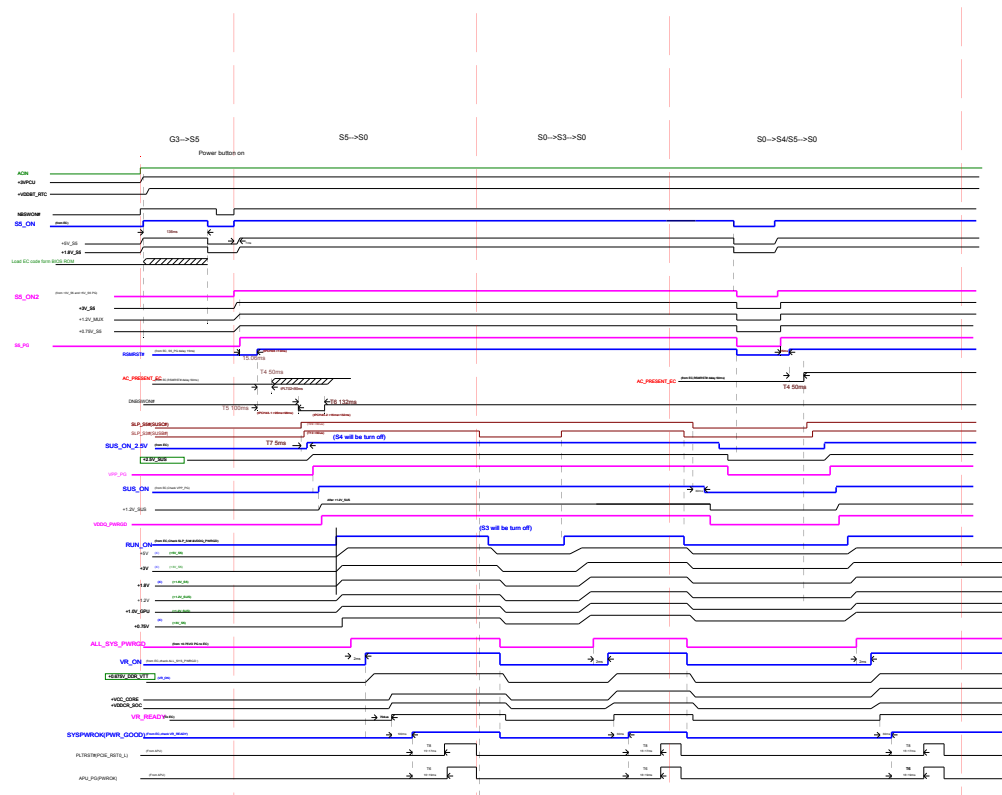


For ADP 180W



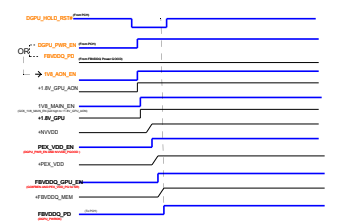


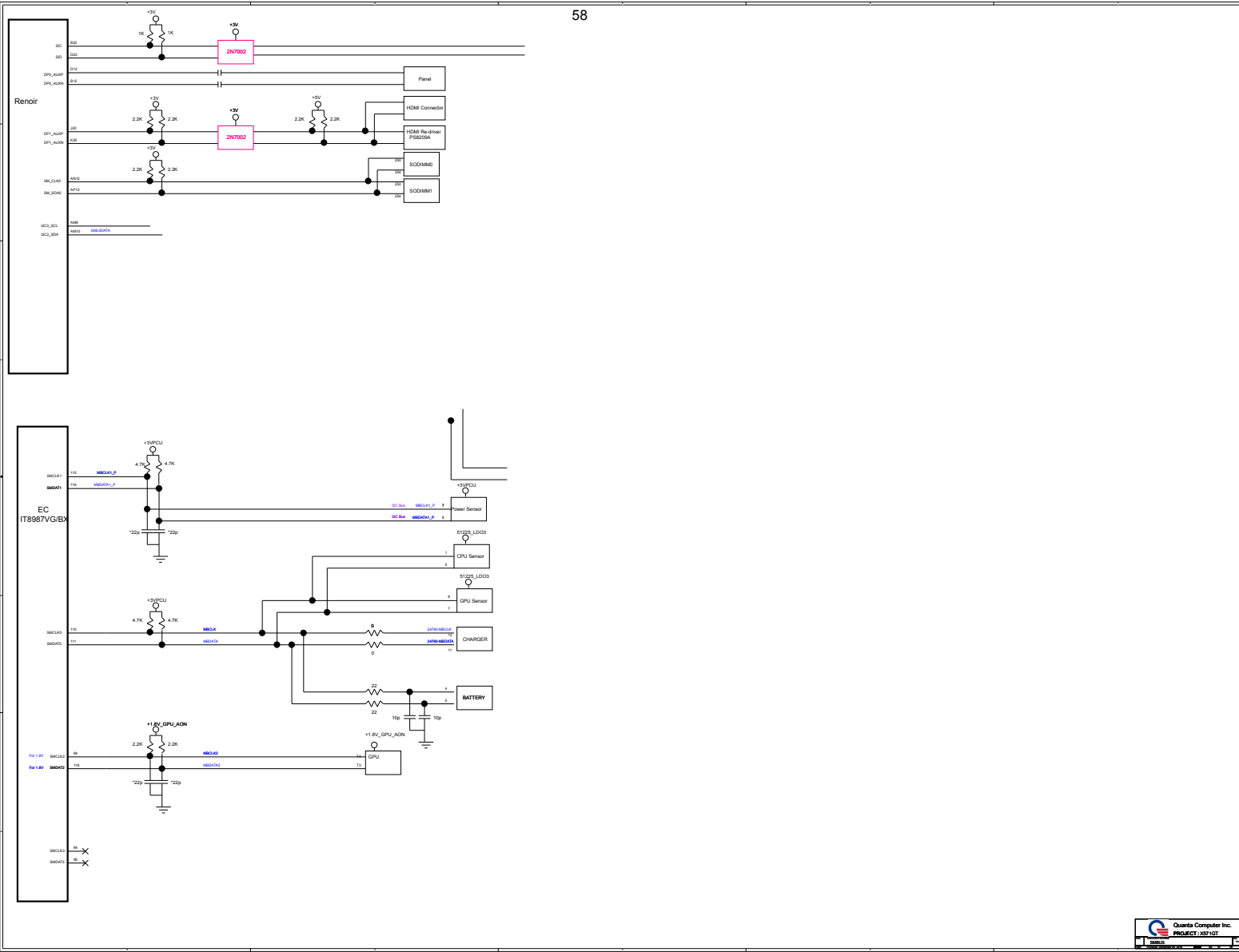
Renoir FP6 Power-Up/OFF Sequencing




N18P-G61/G62 Power-Up Sequencing

N18P-G61/G62 Power-Down Sequencing (GC-OFF)





OS status	S0	S3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "v")	S5 (Fast Startup "x")
RUN_ON	H	L	L	L	L	L
+3V	H	L	L	L	L	L
+5V	H	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L
+12V	H	L	L	L	L	L
+3V_SSD/+3V_PCH_CARD/+1.5V	H	L	L	L	L	L
+1.05V_VCCSTG	H	L	L	L	L	L
+VCCSA	H	L	L	L	L	L
+VCC_GFX	H	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L
+0.95V_VCCIO	H	L	L	L	L	L
SUS_ON	H	H	L	L	L	L
+1.05V_VCCPLL/+1.05V_VCCST	H	H	L	L	L	L
+1.05V_SUS	H	H	L	L	L	L
+1.2V_SUS	H	H	L	L	L	L
SUS_ON_2.5V	H	H	L	L	L	L
+2.5V_SUS	H	H	L	L	L	L
S5_ON	H	H	H	L	L	L
+1.8V_S5	H	H	H	L	L	L
+1.05V_S5	H	H	H	L	L	L
S5_ON	H	H	H	L	H	L
+3V_S5	H	H	H	L	H	L
+5V_S5	H	H	H	L	H	L



Quanta Computer Inc.
PROJECT : X571GT

Size	Document Number	Rev
	POWER MAP	1A
Date: Thursday, December 05, 2019		Sheet 59 of 59