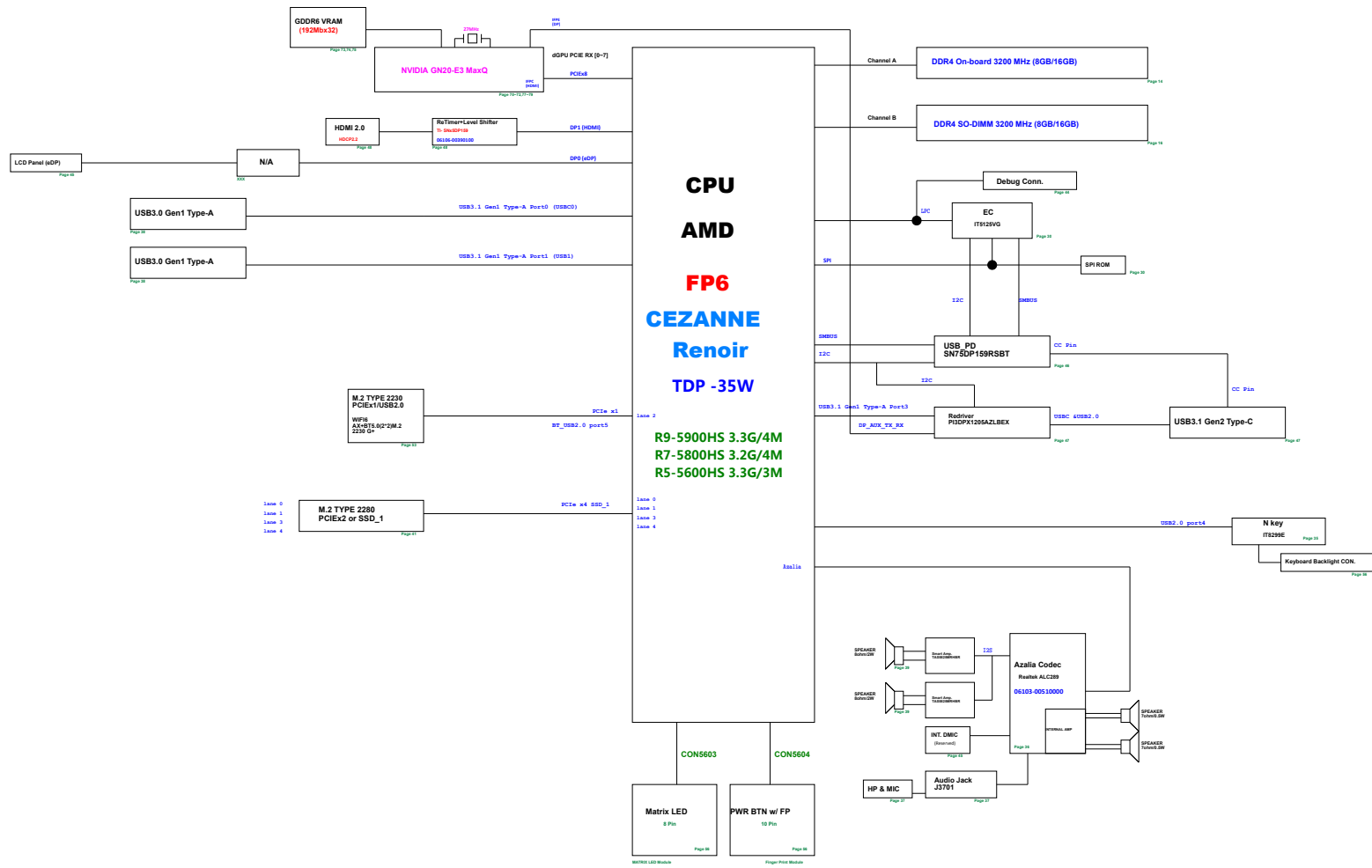


GA401QM AMD+NVIDIA Block Diagram



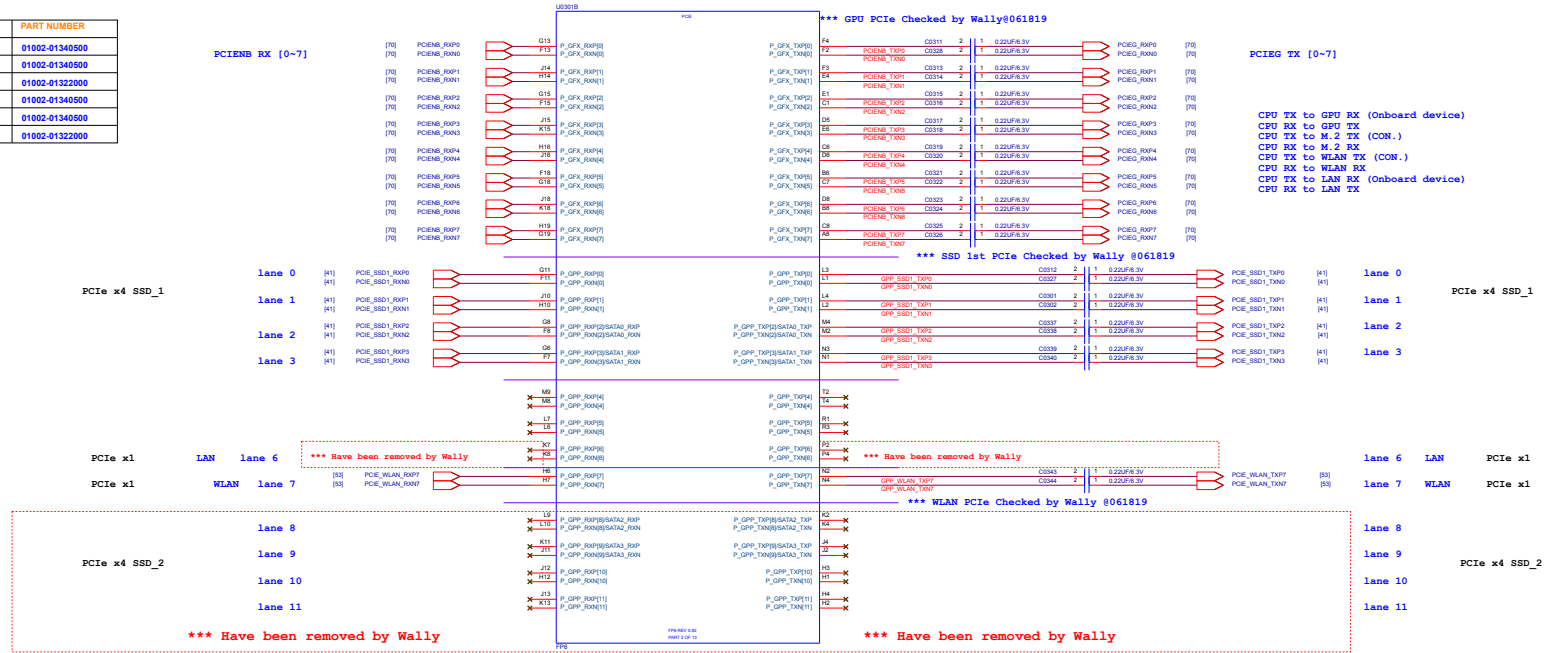
PCIE/WLAN/LAN/SSD

Main Board

RX Side

TX Side

CPU SKU	PART NUMBER
SKU6 R9	01002-01340500
SKU6_SAMSUNG_R9	01002-01340500
SKU7 R7	01002-01322000
SKU6-1 R9	01002-01340500
SKU6-1_SAMSUNG_R9	01002-01340500
SKU7-1 R7	01002-01322000



Memory Channel A

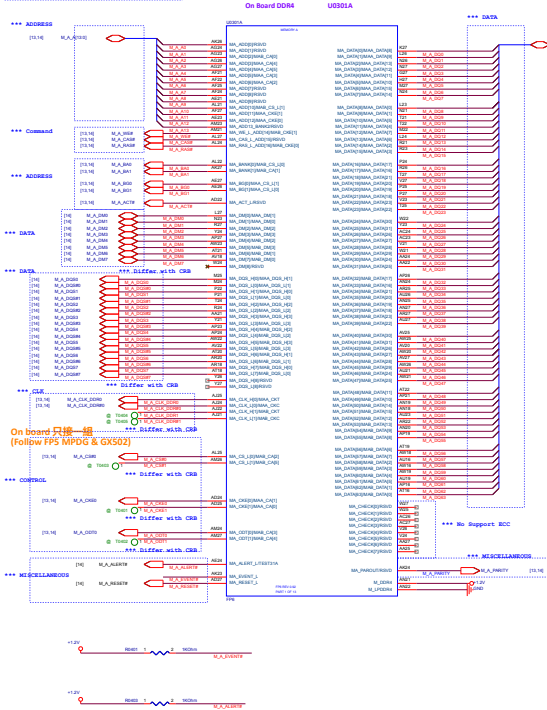


Table 12. DDR4 Signal Descriptions

Signal Group	Processor Signal Name	Description	Processor Pin Type
Data	MA_DATA[0:15]	Memory Data	Bidirectional
	MA_DQS[0:7] (H)	Data Strobes (non-Dram Strobe compliant)	Bidirectional
	MA_DM[7:0]	Data Mask	Bidirectional
Clocks	MA_CLK[0] (H)	Differential Clock (non)	Output
	MA_CLK[1] (H)	Differential Clock (complement)	Output
Address	MA_ADDR[15:0]	Memory Address	Output
	MA_ADDR[16:31] (H)	Memory Address / Bank Address	Output
	MA_BANK[0] (H)	Bank Address	Output
Command	MA_BKE[1] (H)	Bank Group	Output
	MA_ACT[1]	Activation Command	Output
	MA_RAS_L_ADDR[0]	Multi-Bank Command Address, Row Address Strobe or Address 16, depending on the state of the Activation command signal.	Output
	MA_CAS_L_ADDR[0]	Multi-Bank Command Address, Column Address Strobe or Address 15, depending on the state of the Activation command signal.	Output

Table 12. DDR4 Signal Descriptions (continued)

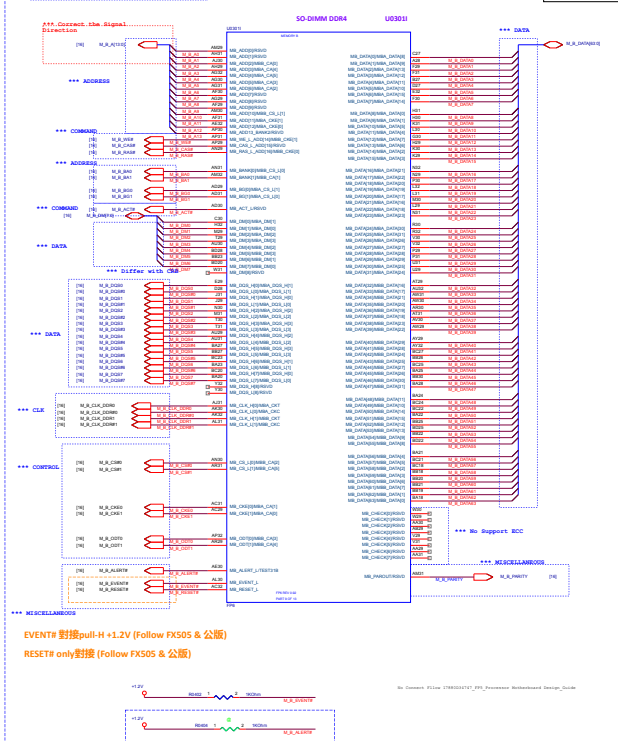
Signal Group	Processor Signal Name	Description	Processor Pin Type
Command	MA_WL_ADDR[0]	Multi-Bank Command Address, Write Enable or Address 04, depending on the state of the Activation command signal.	Output
Control	MA_CKE[0] (H)	Clock Enable	Output
	MA_ODT[0]	DRAM On Die Termination	Output
	MA_CS_L[0] (H)	Chip Select	Output
Miscellaneous	MA_EVENT_1	Memory Thermal Event	Input
	MA_RESET_1	Memory Reset	Output
	MA_ALERT_1	Write Inaction / CRC error (Eg and Command and Address parity error)	Input/Output
	MA_PABOUT	Command and Address Parity Output: DDR4 supports Error Parity check in DRAM with M1 setting.	Output

M_DDR4	Enabled DDR4	Stag II	platforms dependent	0	1
				Disable DDR4 (used to force LPDDR4 to enable) HZ (1.7V) pull-down resistor or direct connect to VSS	Enable DDR4 memory controller HZ (1.7V) pull-up resistor or direct connect to VDDO (MEM_S)
M_LPDDR4	Enabled LPDDR4	Stag II	platforms dependent	0	1
				Disable LPDDR4 (used to force DDR4 to enable) HZ (1.7V) pull-down resistor or direct connect to VSS	Enable LPDDR4 memory controller HZ (1.7V) pull-up resistor or direct connect to VDDO (MEM_S)

Note: • Enable M_DDR4 or M_LPDDR4 can be used for pull-up or use as the other. M1SE is only on other DDR4 mode or LPDDR4 mode.

Note: All settings must be configured with either minimal pull-up or pull-down resistors or direct connections as listed in table.

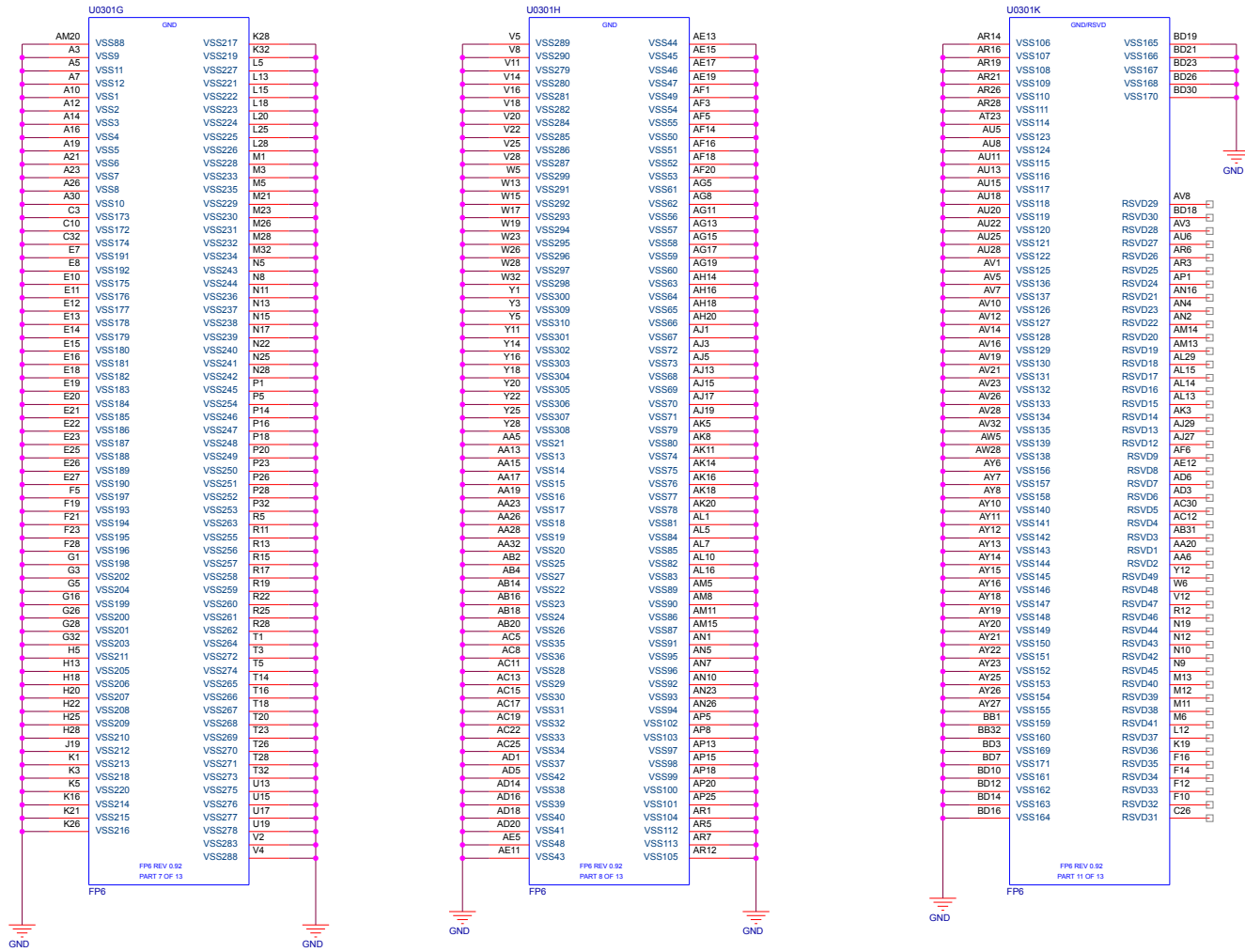
Memory Channel B



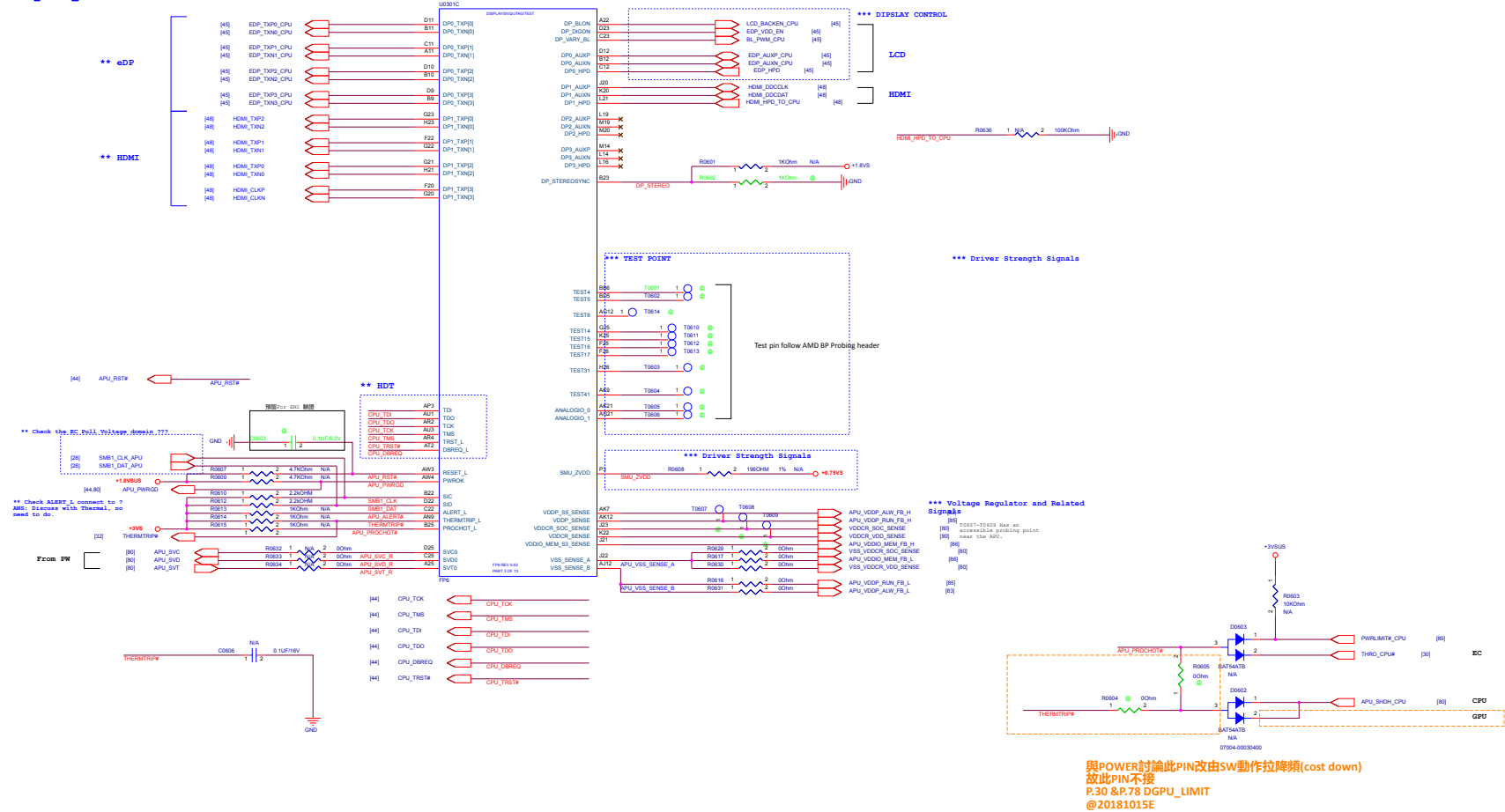
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CPU_GND

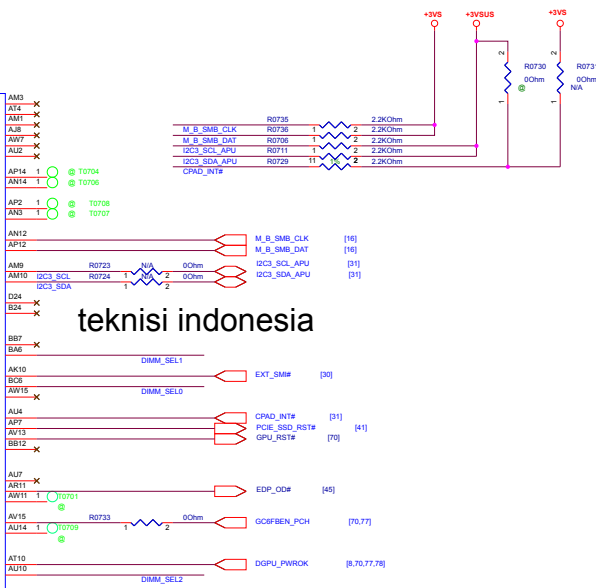
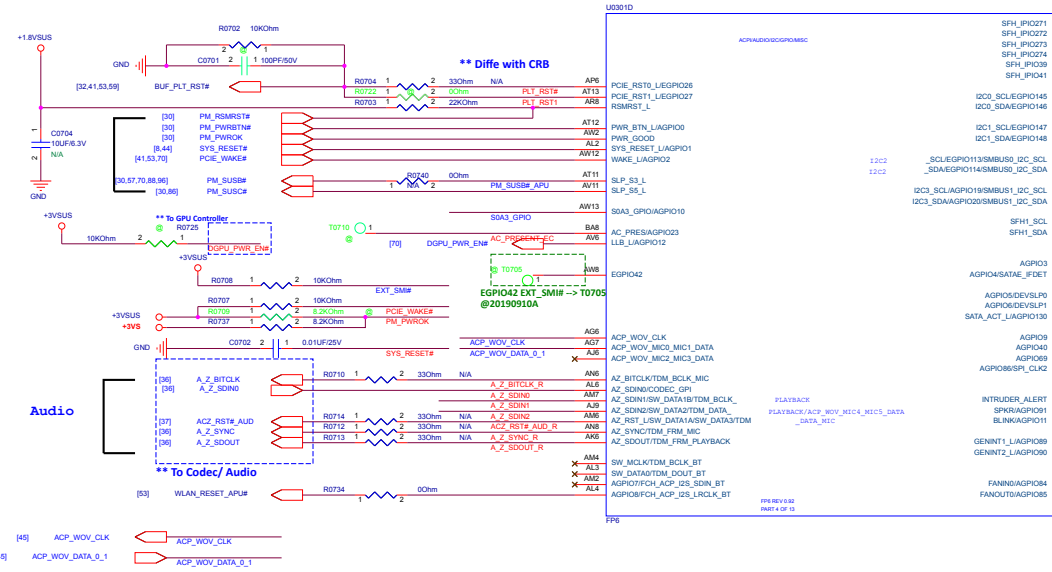
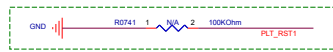


Display



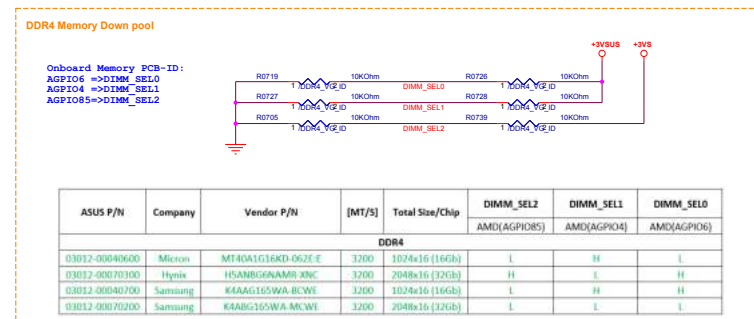
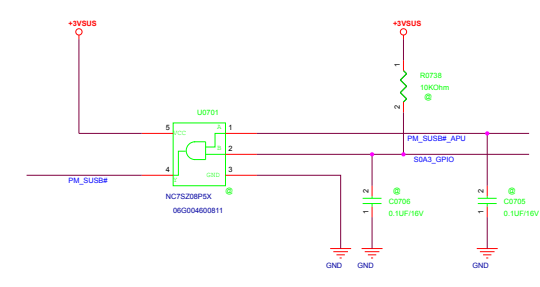
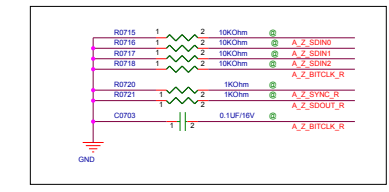
I2C/RST/GPIO/AZ

Add R0741 @20190904A following VC



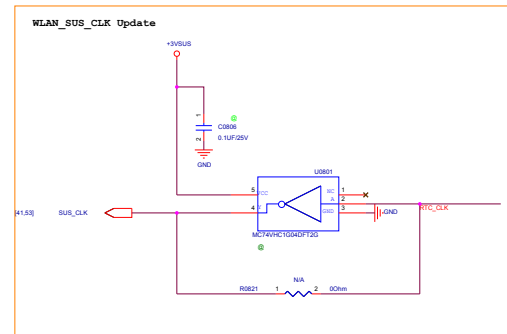
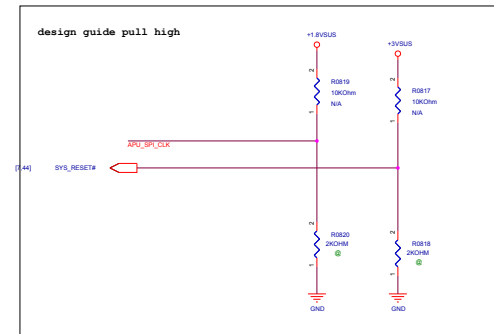
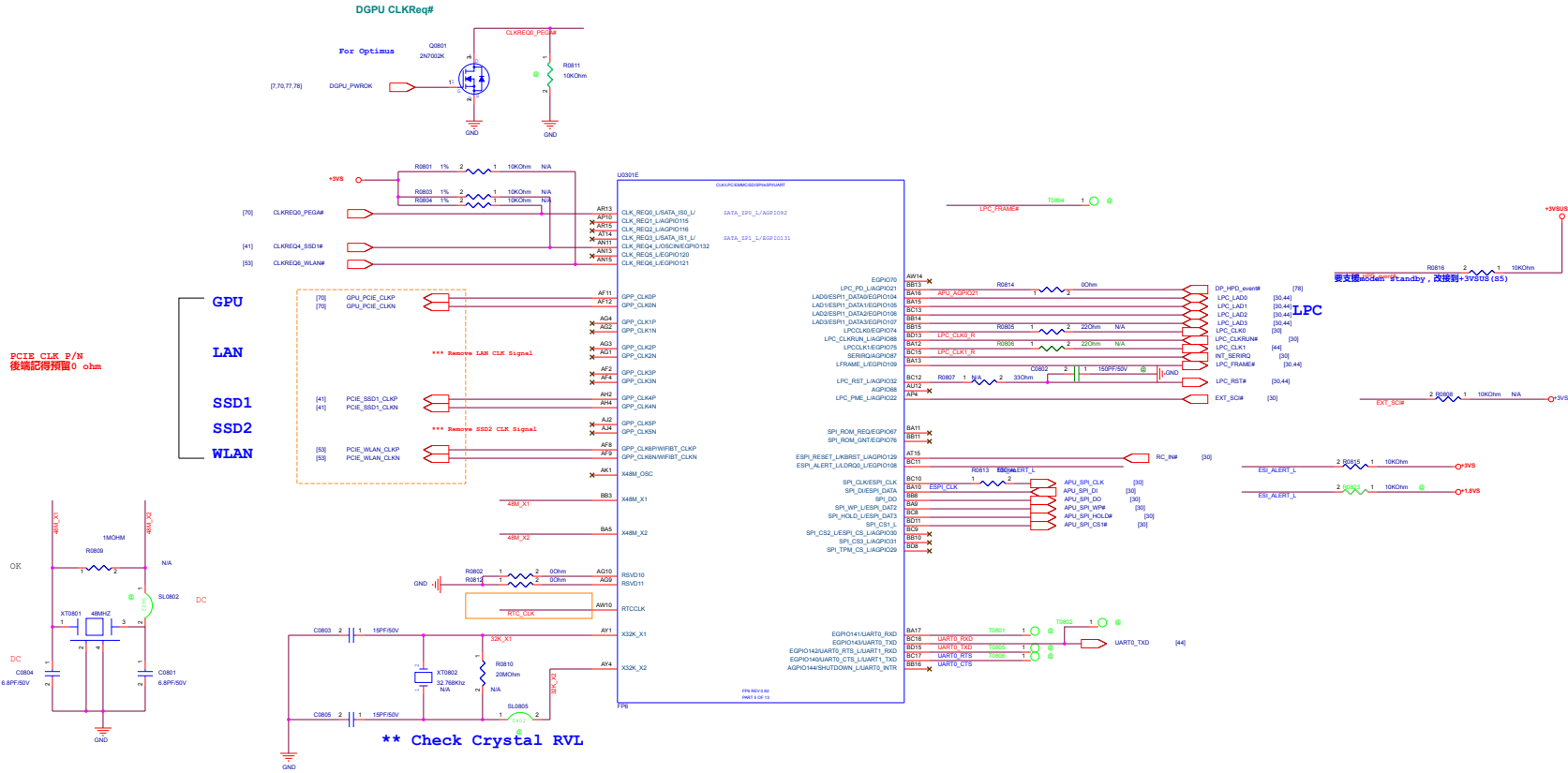
tekni indonesia

@20181013B

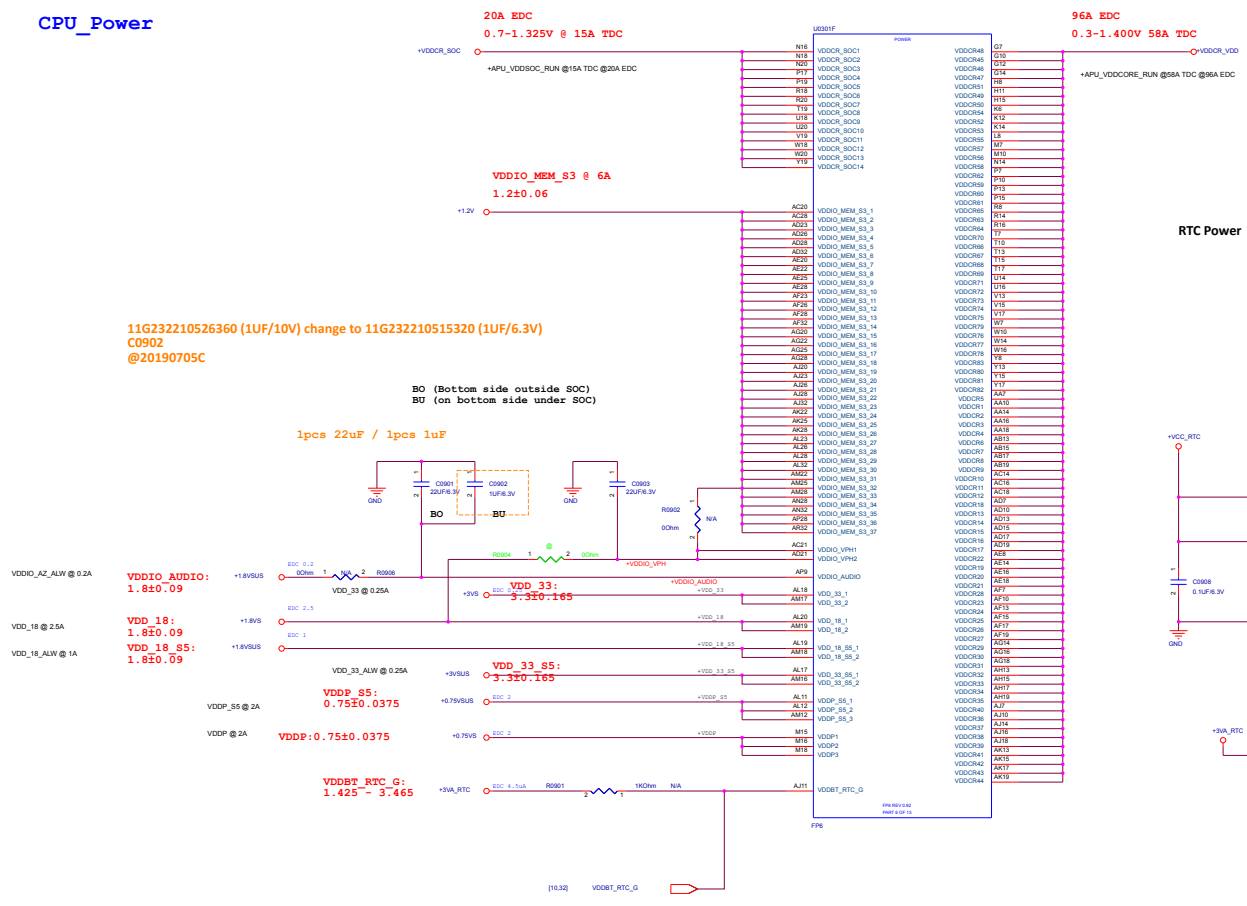


ASUS P/N	Company	Vendor P/N	[MT/S]	Total Size/Chip	DIMM_SEL2	DIMM_SEL1	DIMM_SELO
					AMD(AGP108)	AMD(AGP104)	AMD(AGP106)
DDR4							
03012-00040600	Micron	MT40A1G16KD-0G2E-E	3200	1624x16 (16Gb)	L	H	L
03012-00070300	Hynix	H5AN8G6NAMR-XNC	3200	2048x16 (32Gb)	H	L	H
03012-00040700	Samsung	K4AAG1659A-BCWE	3200	1624x16 (16Gb)	L	H	H
03012-00070200	Samsung	K4A8G165W-A-MCW	3200	2048x16 (32Gb)	L	L	L

CPU CLK

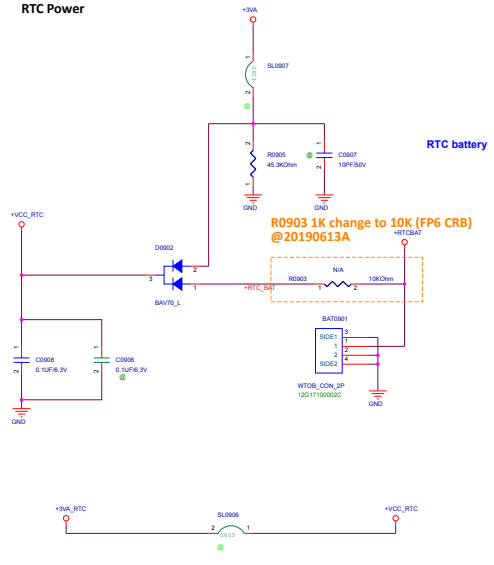


CPU_Power

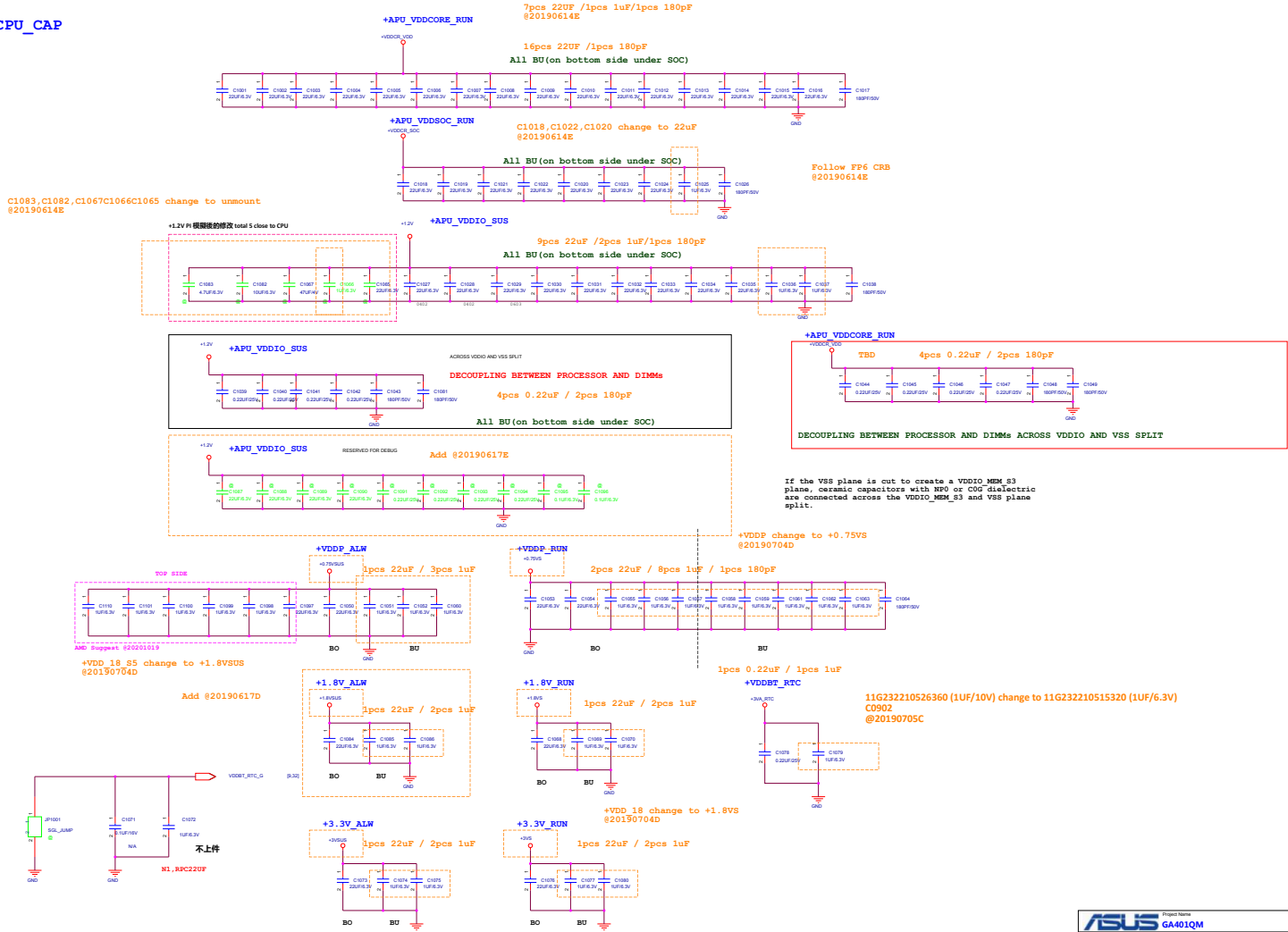


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RTC Power



CPU_CAP



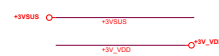
C1083, C1082, C1067, C1066, C1065 change to unmount @20190614E

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or COG dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

*** POWER

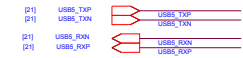
** [P.88]

** [P.87]

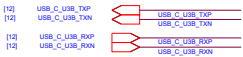
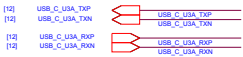


*** SINGAL

** To APU-USB Interface



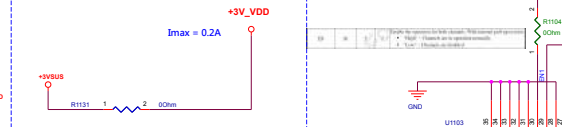
** To Type C Choke TVS/ CONN.



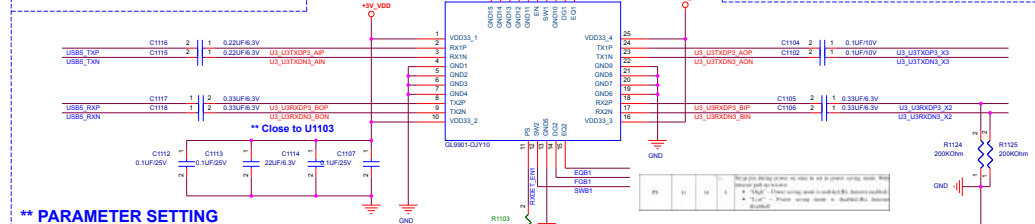
** From PD to MUX Control



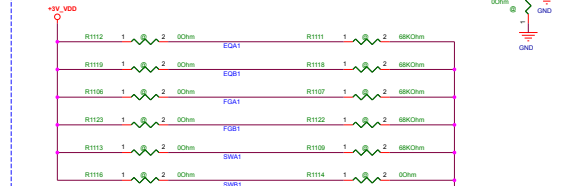
** PWR DISTRIBUTION



** SubSystem Block Diagram



** PARAMETER SETTING



** TP for Tuning

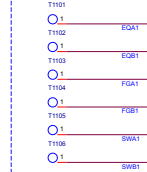


Table 4.1 - 4-Level Control Pin Settings

Setting Level	Connecting Condition
0	Tie to GND
R	Tie to VDD, R to GND
F	Float (Leave open)
1	Tie to VDD

Table 4.2 - Receiver Equalization Settings

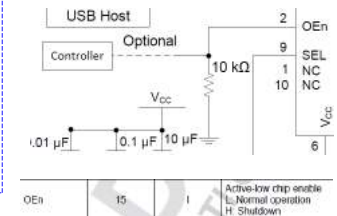
EQx Setting	EQ @ 2.5 GHz	EQ @ 9 GHz
0	-6.7 dB	0.1 dB
R	2.2 dB	4.4 dB
F	4.1 dB	7.1 dB
1	7.6 dB	11.6 dB

Table 4.3 - DC Gain Settings

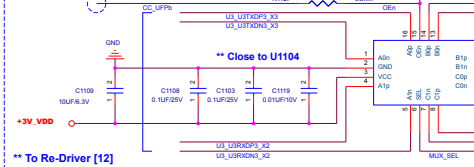
DCx Setting	Gain Level
0	-2.0 dB
R	-1.5 dB
F	0.5 dB
1	2.0 dB

Table 4.4 - Output Swing Settings

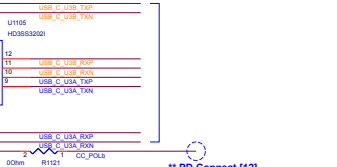
SWx Setting	Output Swing Level
0	300 mV
R	1200 mV
F	1000 mV
1	1100 mV



** PD Connect [12]



** From TypeC CONN. [12]



** To Re-Driver [12]

Table 1. Port Select Control Logic⁽¹⁾

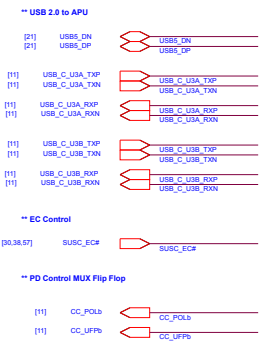
PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

ASUS Project Name		Rev
GA401QM		R1.0
Title : TypeC_U3SSP_repeater		
Size	Dept: ASUS/PC COMPUTER INC.	Engineer: ROG EE
Custom	Date: Wednesday, December 02, 2020	
Page: 11		of 104

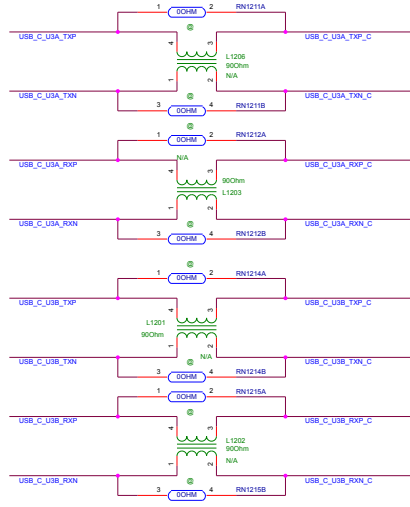
*** POWER



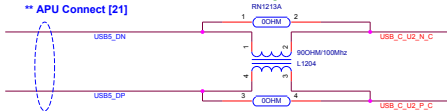
*** SINGAL



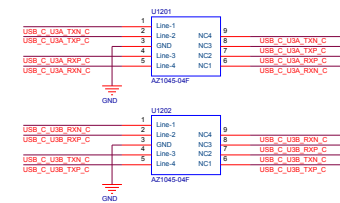
** USB 3.0 Gen2 to Re-Driver



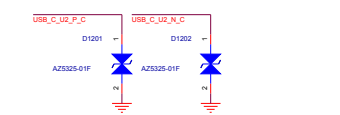
** USB 2.0 to APU



** USB3.0 ESD-Protection

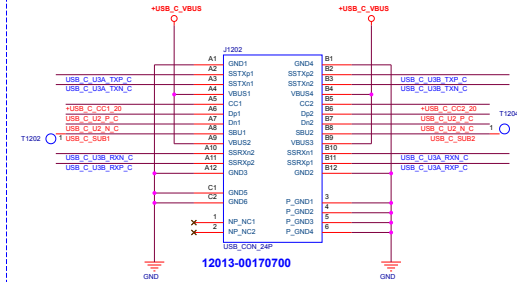


** USB2.0 ESD-Protection



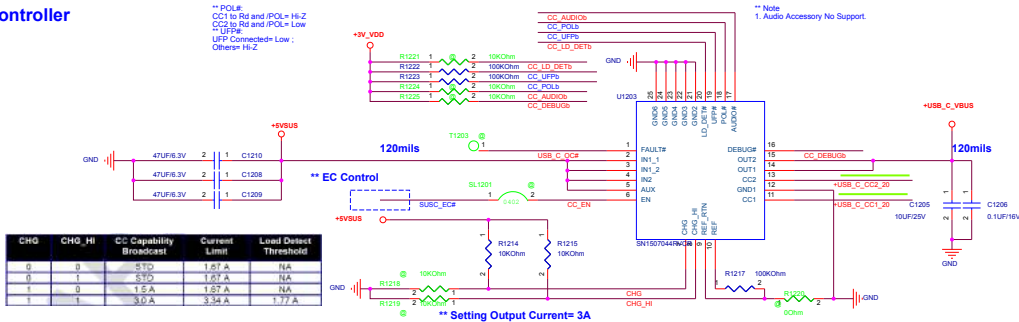
Main Board

TYPE-C Connector



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** TI PD Controller



SN1507044RVC Type C Port	CC1	CC2	OUT	SN1507044RVC Response			
				VCONN On CC1 or CC2	/POL	/UFP	/AUDIO
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z
Powered Cable/No UFP Connected	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Re	OPEN	NO	Hi-Z	Hi-Z	Hi-Z

Project Name: **GA401QM**

Title: **TypeC&SN1507044**

Dept.: **ASUSTEK COMPUTER INC.** Engineer: **ROG EE**

Date: Wednesday, December 02, 2020

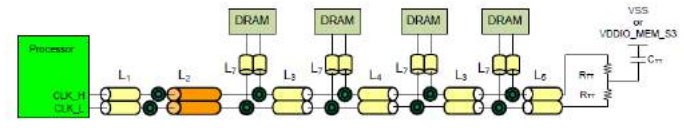
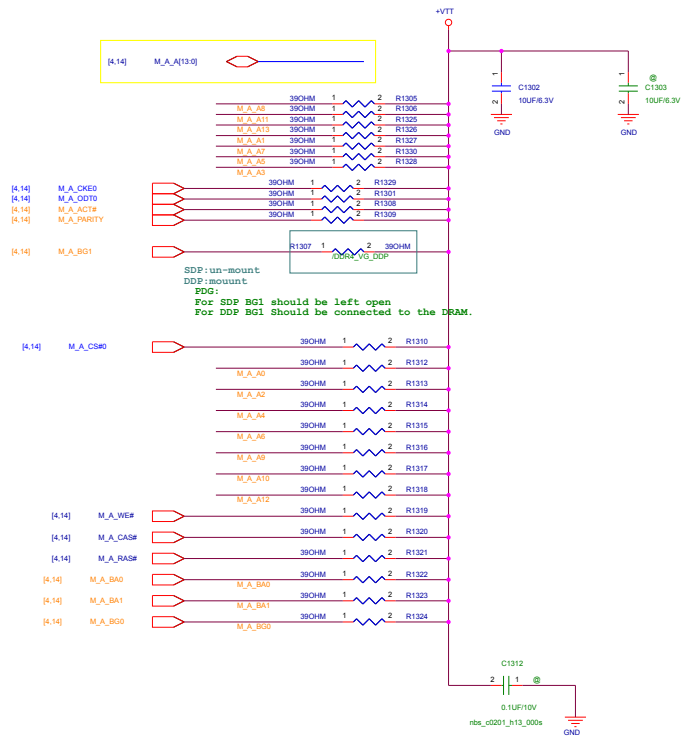
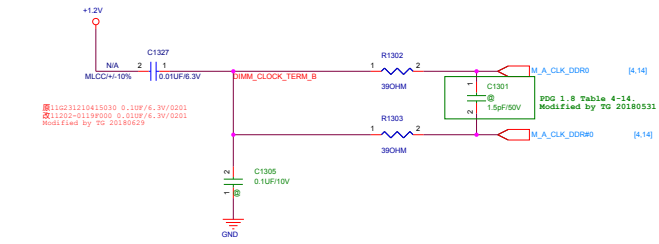


Figure 57. CLK Routing Model (DDR4 x16 DRAM Down)

The termination component values for MA_CLK are listed in Table 40.

Table 40. Component Table—DDR4 x16 CLK Termination

Ref	Value	Tolerance	Package	Comments
R _{TT}	39Ω	5%	0402	CLK termination
C _{TT}	0.1 μF	5%	0402	CLK termination to VSS or VDDIO_MEM_S3. CLK termination must match the CLK reference plane.



Clock Full up power change from +0.6V to +1.2V (CPL PDG) 20820601

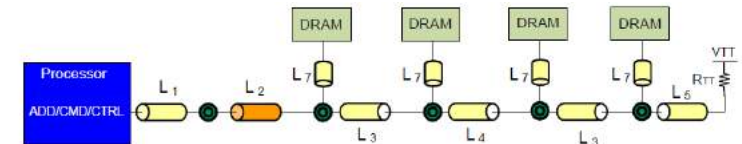
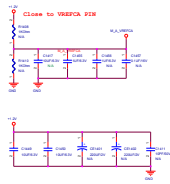
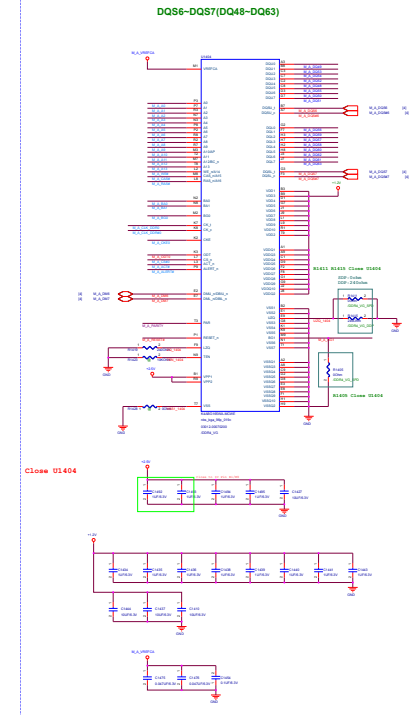
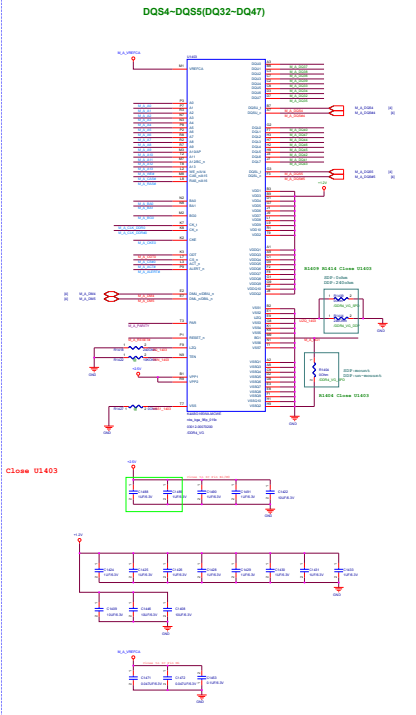
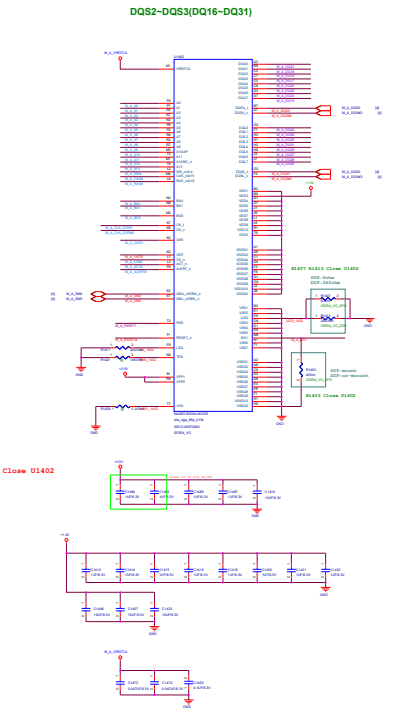
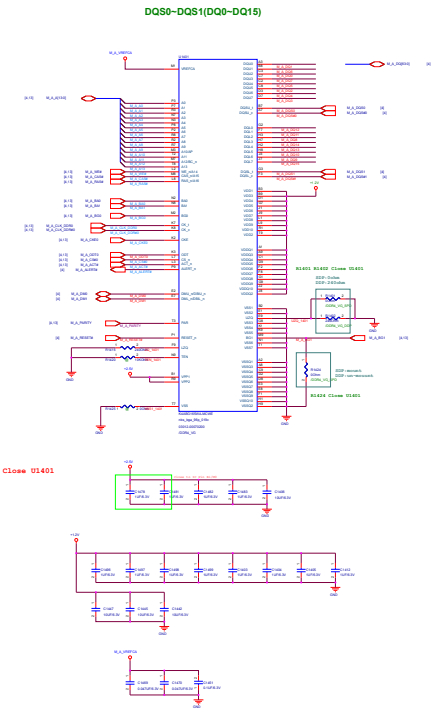


Figure 58. ADD/CMD/CTL Routing Model (DDR4 x16 DRAM Down)

The termination component values for ADD/CMD/CTL are listed in Table 42.

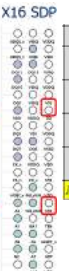
Table 42. Component Table—DDR4 x16 ADD/CMD/CTL Termination

Ref	Value	Tolerance	Package	Comments
R _{TT}	39Ω	5%	0402	ADD/CMD/CTL termination to VTT



X16 DDP

7	8	9
UDQS_c	VSSQ	VDDQ
UDQS_i	UDQ1	VDD
UDQ3	UDQ5	VSSQ
UDQ7	VSSQ	VDDQ
LDM_n/DBI_e	VSSQ	UDQ
LDQ1	VDDQ	LDQ
VDD	VSS	VDDQ
LDQ3	LDQ5	VSSQ
LDQ7	VDDQ	VDD
CK_1	CK_c	VSS
CS_n	RAS_n/A16	VDD
A12BC_n	CAS_n/A15	BG1
A3	BA1	TEN
A1	A6	ALERT_n
A9	A7	VSP
VSS	A13	VDD

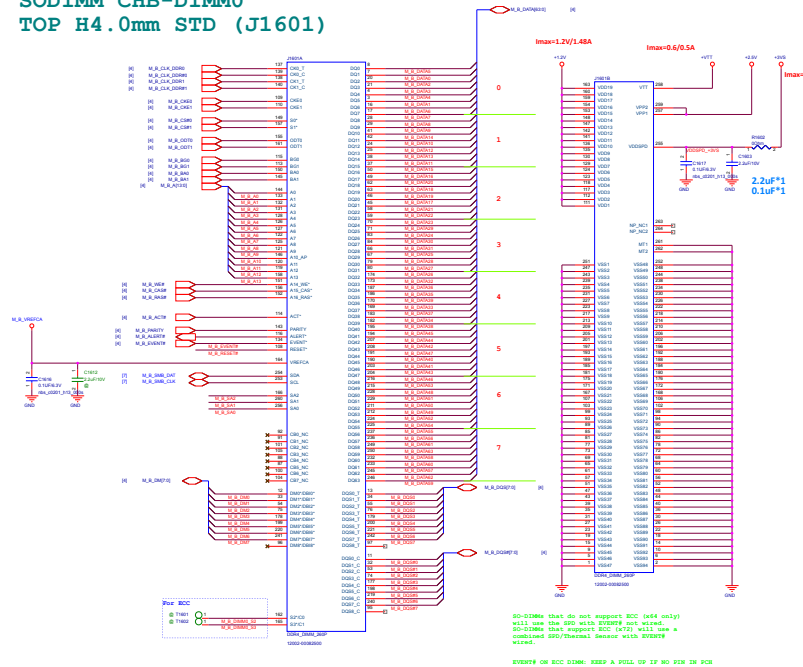


CHANNEL A and B						
MEM VREFCA	Vref Source	Connected to the center of a 50% VDDIO voltage divider network, comprised of:	2	1 k	Ω	1%
VDDIO ¹	Channel A and B Decoupling	Ceramic capacitors connected to VSS.	36	0.22	μF	0402
VTT ¹		Ceramic capacitors connected to VSS and VDDIO.	20	0.22	μF	0402
VREF_CA ¹		Ceramic capacitors connected to VDDIO.	4	0.1	μF	0402

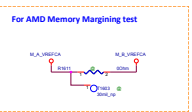
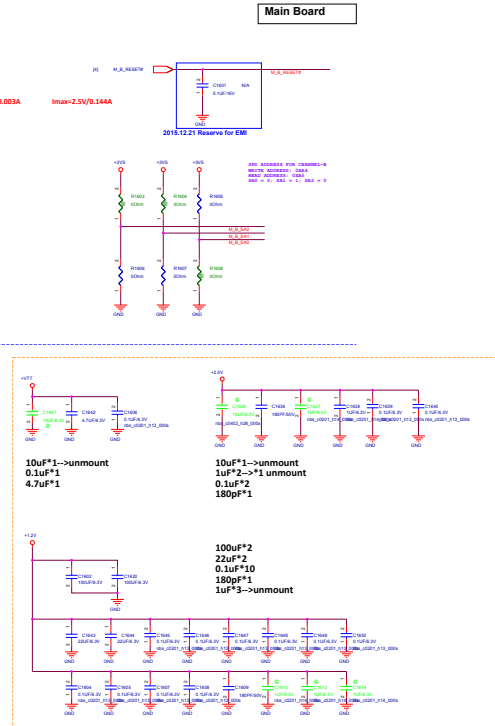
Note: 1. Double the capacitor quantity for DRx16 configuration.



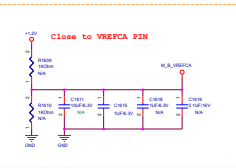
**SODIMM CHB-DIMMO
TOP H4.0mm STD (J1601)**



Main Board



新增M_B_VRECA (Follow FX505) and remove page18



Follow FP6 CRB CAP number @20190701A

Table 4-24. DDR4 SODIMM Power Plane Decoupling

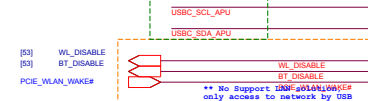
Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)	
		1 placeholder	1x 330 μ F (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10 μ F (0603)	
		Placed on VTT plane close to DIMM	4x 1 μ F (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10 μ F (0603)	
VDDSPD	Place close to DIMM	2x 0.1 μ F (0402)		
	Place close to DIMM	2x 2.2 μ F (0402)		

CPU_USB

- USB Port0
- USB Port1
- USB 2.0 Port2
- USB 2.0 Port3
- USB Port4
- USB Port5

- USB3.1 Gen1 Type-A Port0
- USB3.1 Gen1 Type-A Port1
- N-KEY
- ** USB3.1 Gen2 Type-C Port4 w/ Full Function
- ** USB3.1 Gen2 Type-C Port5 Only USB

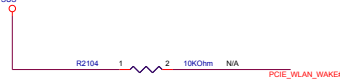
** USB 2.0 Port6 to FP



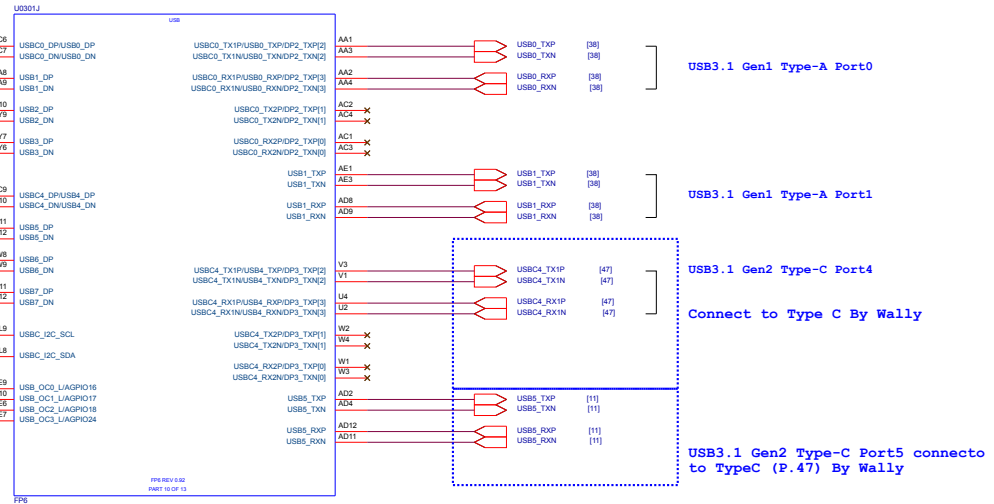
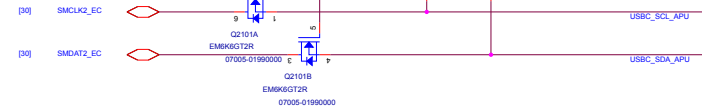
** Modified the Pin Connection@0701A

AMD Design check

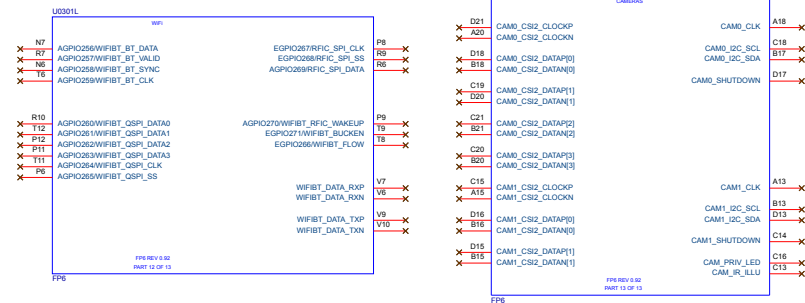
AGPIO13. If unused, enable internal pull down by software.

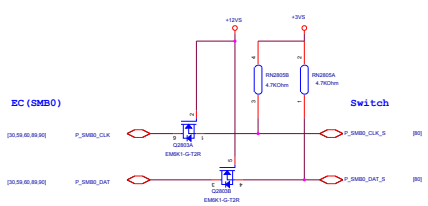
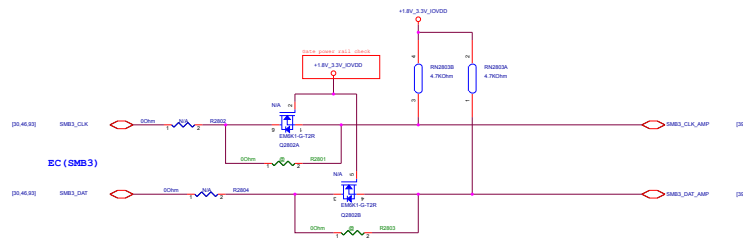
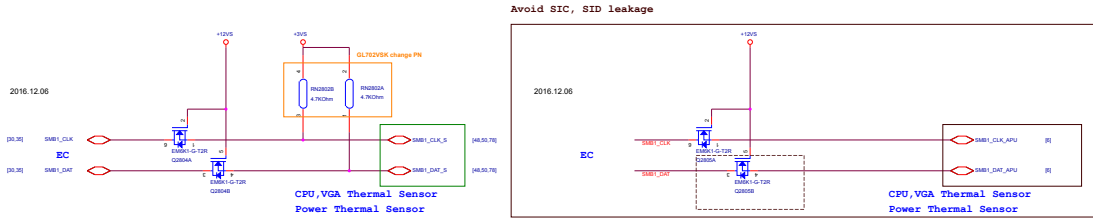


** EC

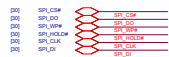
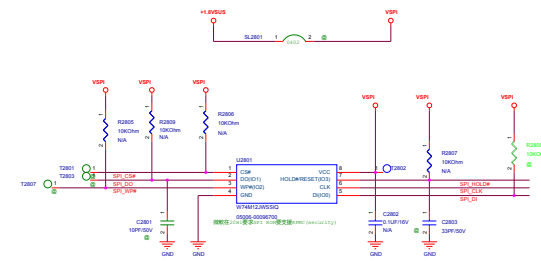


- USB Port 0,1,4,5
- USB-A USB3.2 Gen1(5Gbps): 304.8mm (12000mil)
- USB-C USB3.2 Gen1(5Gbps): 177.8mm (7000mil)
- USB-A & USB-C USB3.2 Gen2(10Gbps): 152.4mm (6000mil)





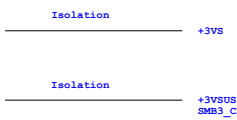
SPI ROM



- NKEY_預留0 OHM對接
- APU_PU +3VS
- EC_PU +3VA
- APU I2C3_PU +3VSUS
- DDR4 SO-DIMM_對接
- EC (SMB3)
- Type-C PD
- Slave charger

EC (SMB1)

EC (SMB3)
M_B_SMB_DAT

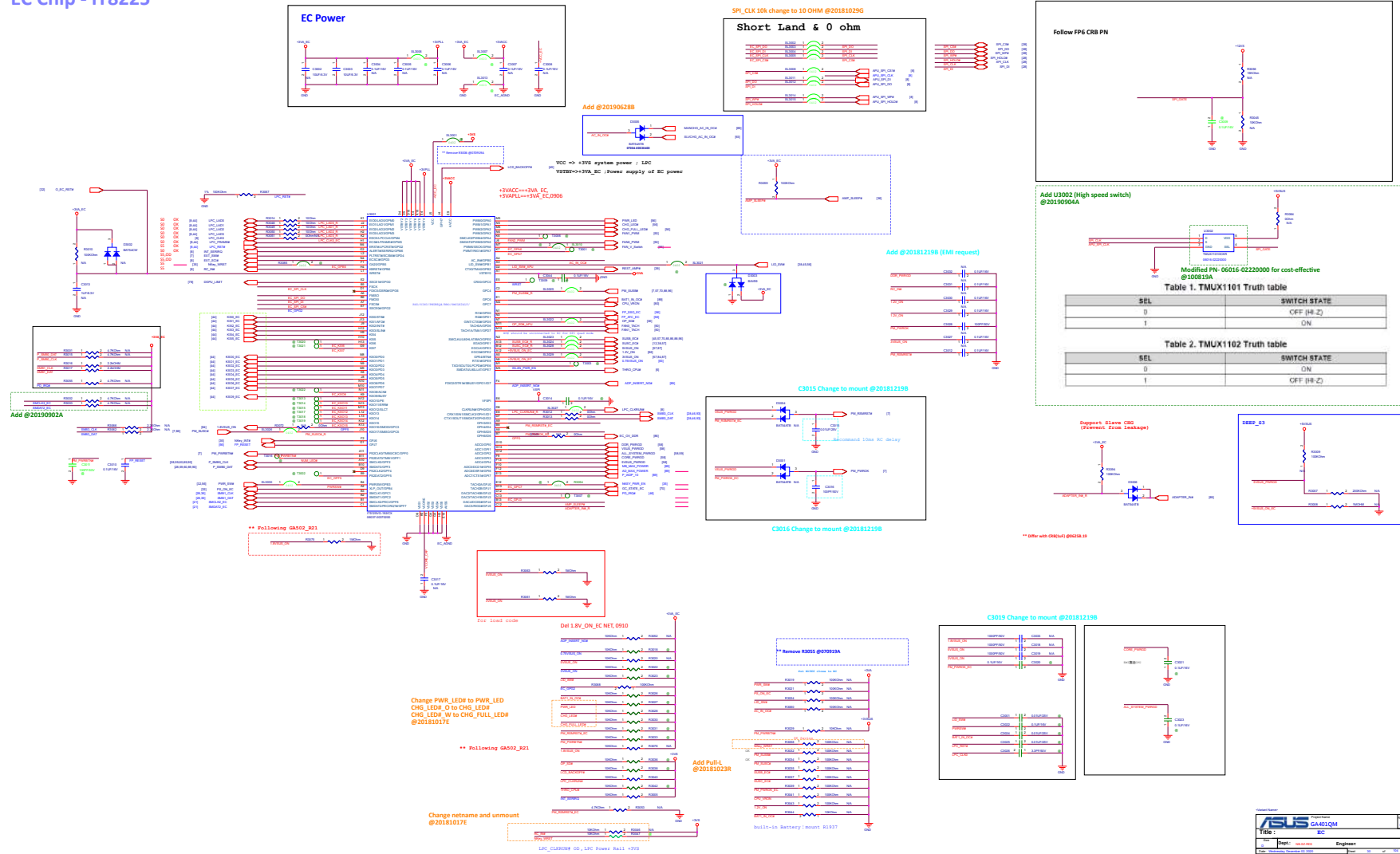


- GPU sensor
- VRAM sensor
- CPU sensor
- HDMI_預留
- Audio AMP

Project Name		Rev.
ASUS GA401QM		1.0
Title: PCH-SPI ROM.OTH		
Dept:	ASUS/TK COMPUTER	Engineer: ROG EE
Date: Wednesday, December 02, 2020	Sheet	28 of 104

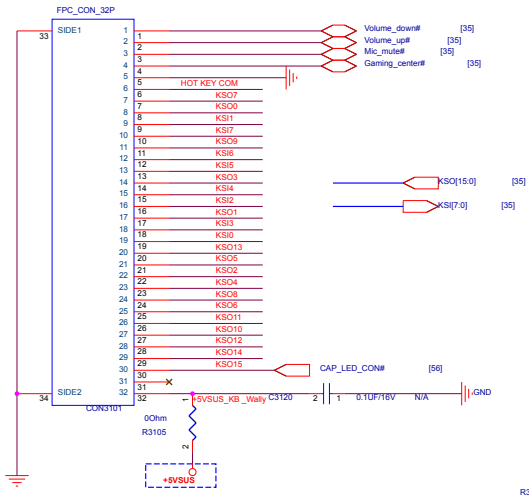


EC Chip - IT8225



12018-00620100

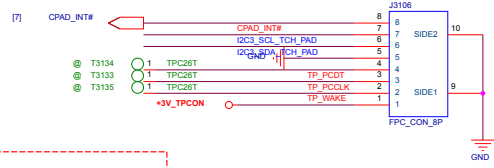
Keyboard Connector
** Mirror with Pin Define



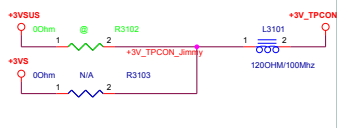
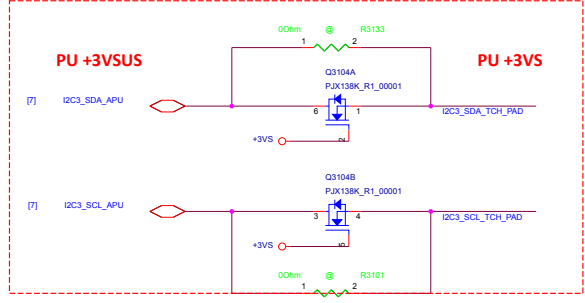
Pin	IO	VEL
Pin 1	IO	VEL
Pin 2	IO	NC
Pin 3	IO	Caplock_LED
Pin 4	IO	KS015
Pin 5	IO	KS014
Pin 6	IO	KS012
Pin 7	IO	KS010
Pin 8	IO	KS011
Pin 9	IO	KS008
Pin 10	IO	KS008
Pin 11	IO	KS013
Pin 12	IO	KS013
Pin 13	IO	KS014
Pin 14	IO	KS013
Pin 15	IO	KS014
Pin 16	IO	KS012
Pin 17	IO	KS010
Pin 18	IO	KS011
Pin 19	IO	KS013
Pin 20	IO	KS005
Pin 21	IO	KS011
Pin 22	IO	KS02
Pin 23	IO	KS04
Pin 24	IO	KS08
Pin 25	IO	KS08
Pin 26	IO	KS010
Pin 27	IO	KS012
Pin 28	IO	KS014
Pin 29	IO	KS015
Pin 30	IO	KS015
Pin 31	IO	NC
Pin 32	IO	NC

Pin#	Signal	I/O	Description
1	VCC	VCC	VCC, 3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	WAKE	O	Just pin reserved in the connector for system wake-up
3	PS2_CLK	I	Not connected (Just pin reserved)
4	PS2_DATA	I	Not connected (Just reserve pin in the connector)
5	GND	GND	Ground
6	I2C_SDA	I/O	I2C data.
7	I2C_SCL	I/O	I2C clock
8	/INT	O	Indicates touchpad likes to send data to system (heat)

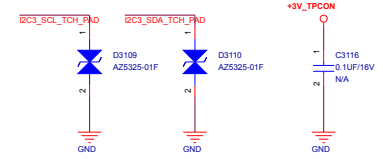
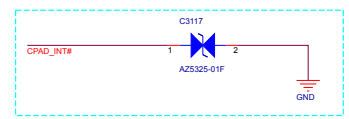
TP Conn.



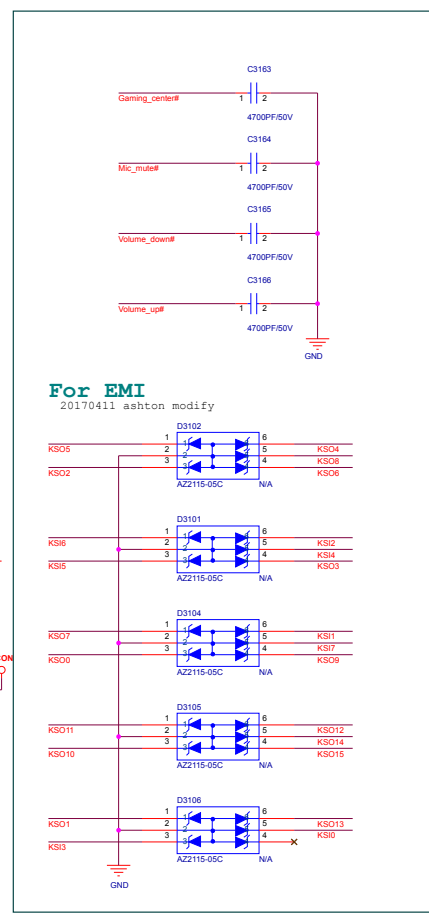
**** Following GA502_R21**



Add @20181219B (EMI request)

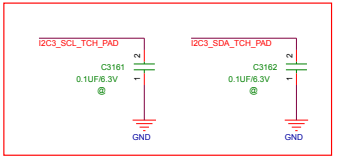


Main Board

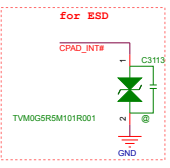


For EMI
20170411 ashton modify

EMI Reserve
如要上件請確認容值 (選擇Pico等級)



D3110 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

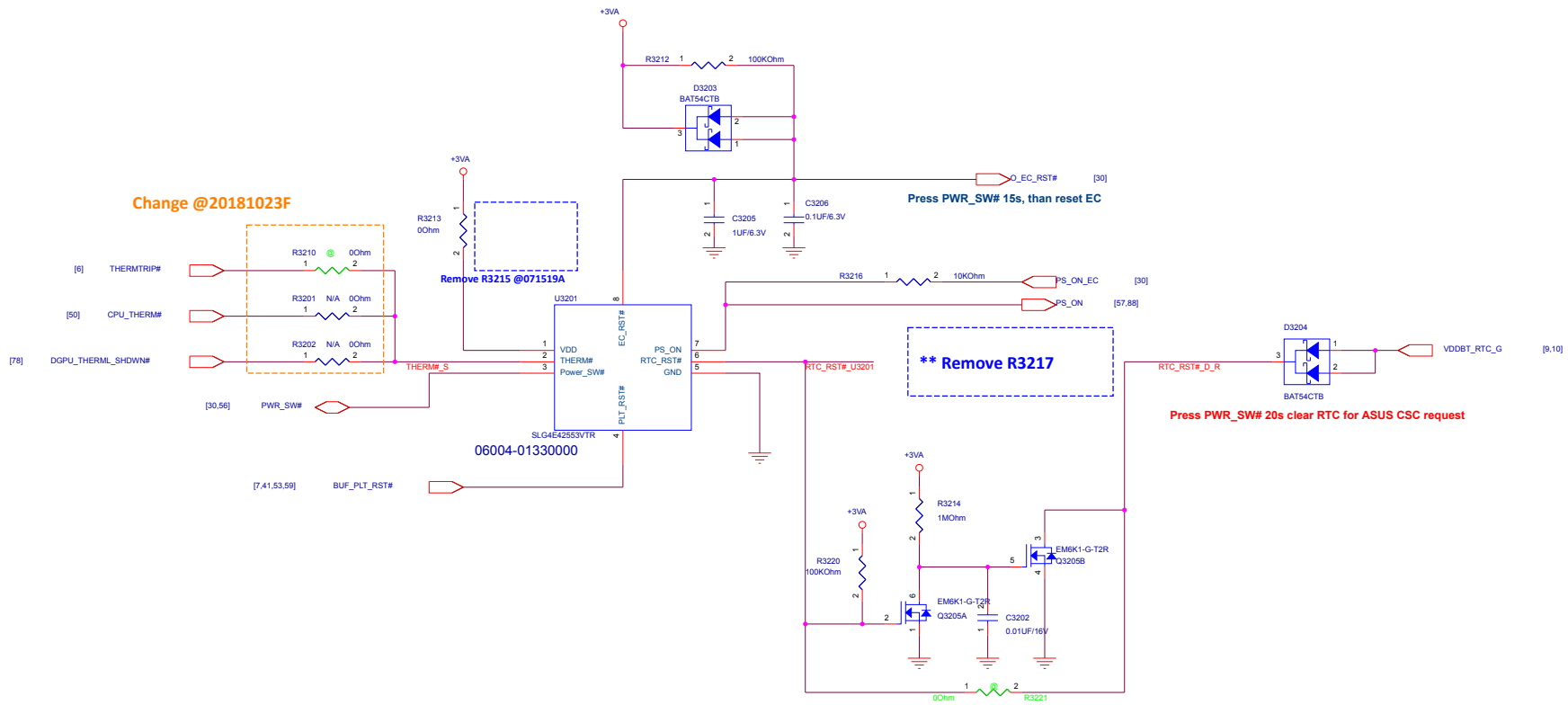


ASUS		Title : KBC_KB & TP
ASUSTek COMPUTER		Engineer: ROG EE
Size	Project Name	Rev
B	GA401QM	R1.0
Date: Wednesday, December 02, 2020	Sheet	31 of 104

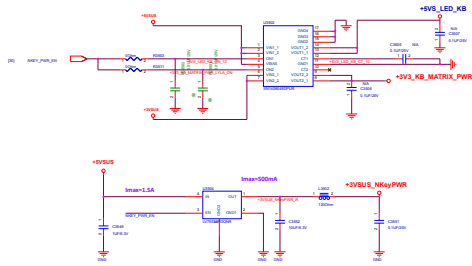
Modern standby project should use Siligo solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

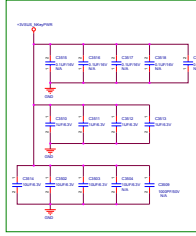
<https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60--shared-minimum-hardware-requirements-for-components>
UX362FA R1.3 board will verify this circuit 7/E



N_KEY_IT8299E



Nkey_Power



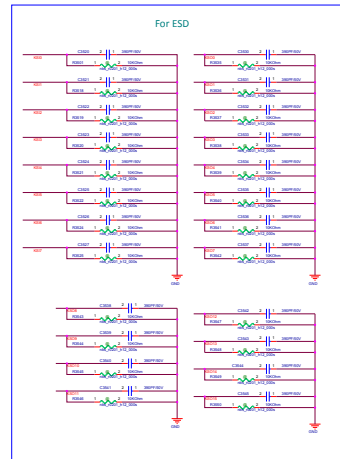
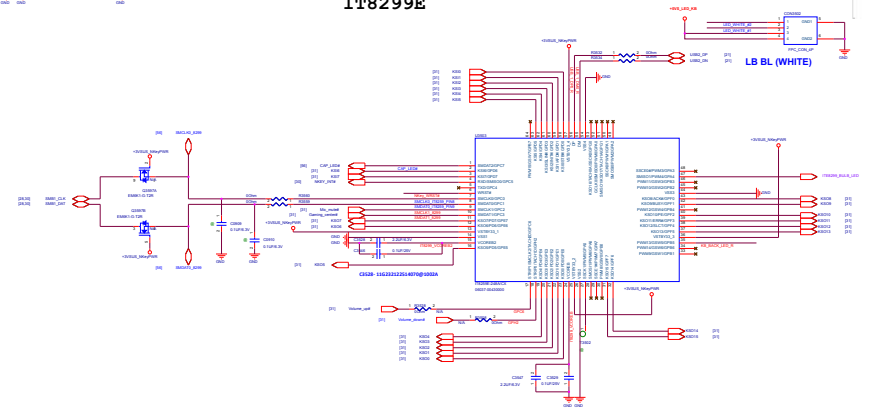
For EC Reset N_key



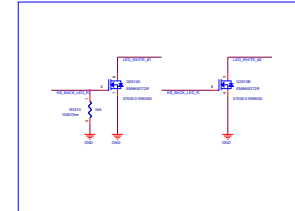
Pull up



IT8299E

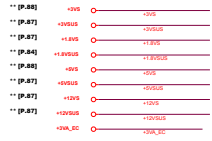


KB WHITE LED



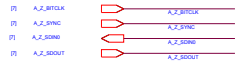
www.teknisi-indonesia.com

*** POWER



*** SINGAL

** PCH Control



** EC Control



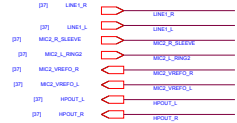
** Jack Control



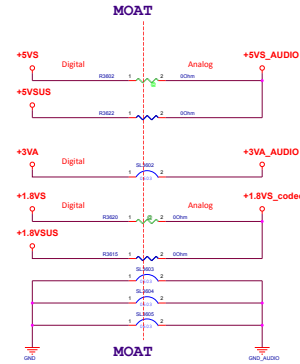
** To EXT. Amp.



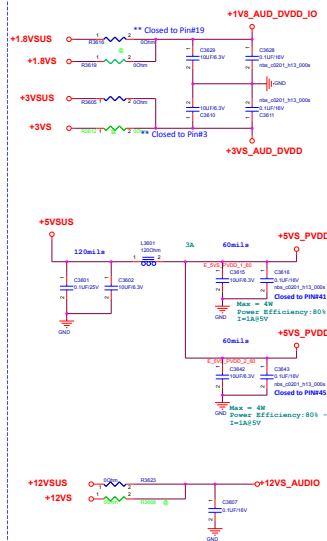
** Headset Connection



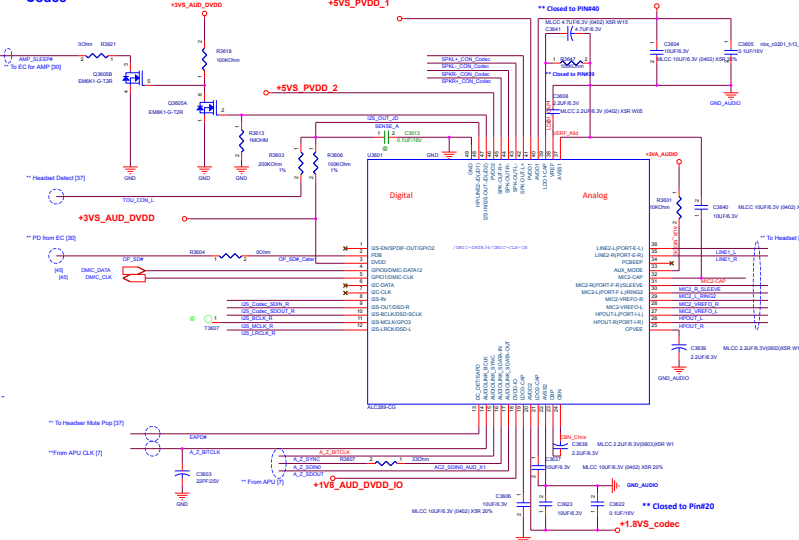
** PWR DISTRIBUTION (ANALOG)



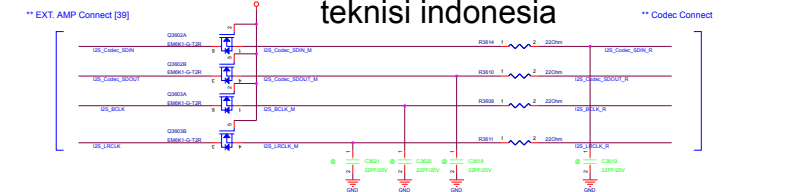
** PWR DISTRIBUTION (DIGITAL)



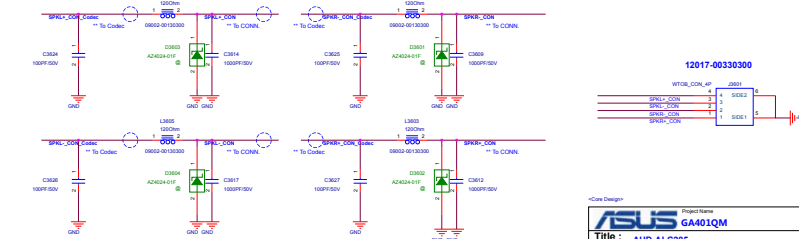
** Codec



** EXT. AMP Connection



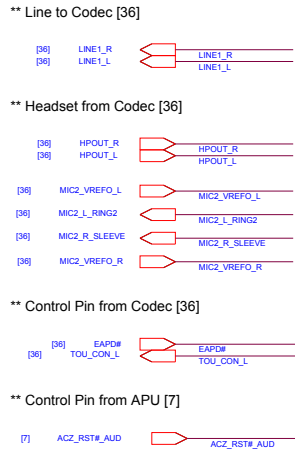
** Tweeter AMP CONN.



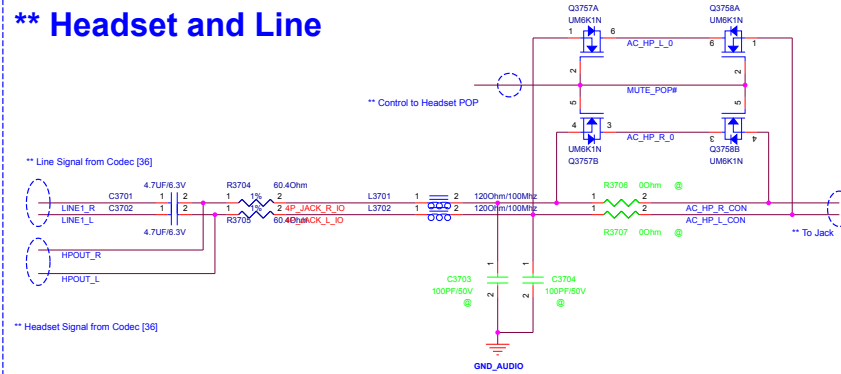
*** POWER



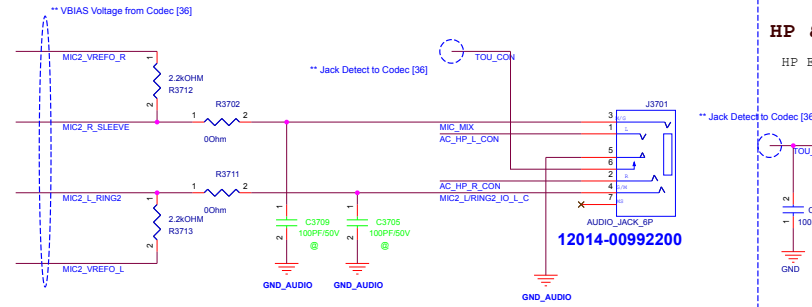
*** SINGAL



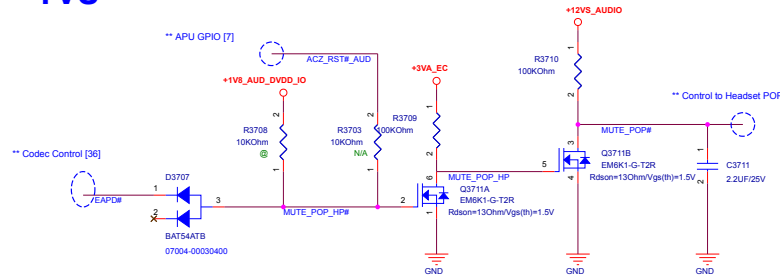
** Headset and Line



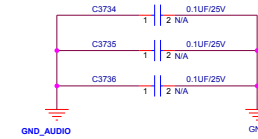
** Jack and MIC



** TVS



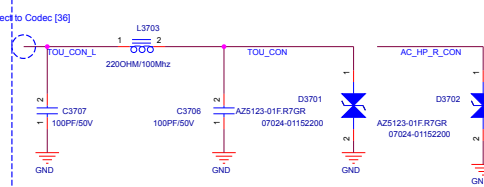
** A_GND / GND



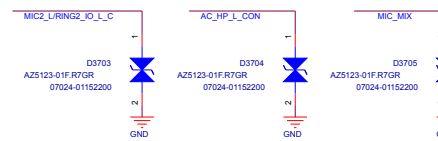
** TVS

HP & MIC Connector

HP ESD Protect

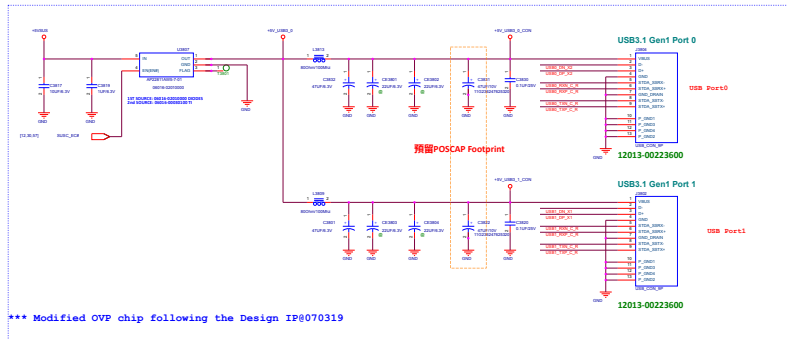


EXTERNAL MICROPHONE



Project Name GA401QM		Rev R1.2
Title : AUD_EXT Jack		
Size B	Dept.: ASUSTek COMPUTER INC. Engineer: ROG EE	
Date: Wednesday, December 02, 2020	Sheet 37	of 104

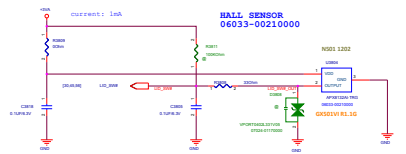
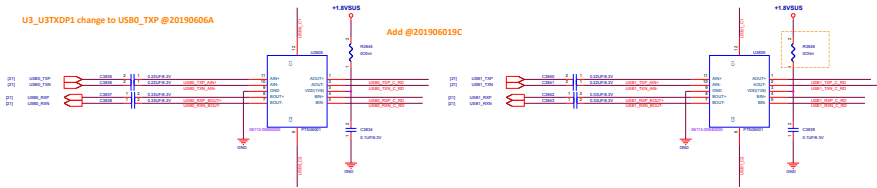
*** Remove all Charger Plus070319A



USB3.1 Gen1 Port0

USB3.1 Gen1 Port1

U3_U3TXDP1 change to USB0_TXP @20190606A



Hub/driver Control strap pin

	USB1_C1	USB1_C2	USB2_C1	USB2_C2	USB3_C1	USB3_C2
PULL UP/DN	DNI unmount	DNI unmount	DNI unmount	DNI unmount	DNI unmount	DNI unmount
OPEN MODE						
PULL DOWN	DNI unmount	DNI unmount	DNI unmount	DNI unmount	DNI unmount	DNI unmount

DNI unmount
NI mount

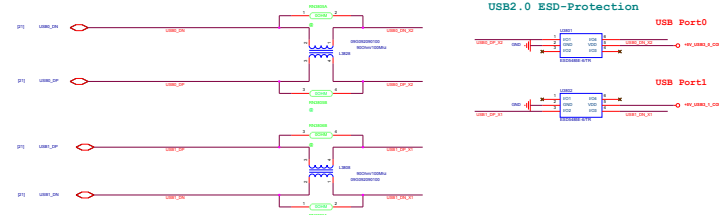
CPU 到 USB-hub/river 長度 11 inch -> 請優先使用Medium (長度141 再改140)
Vendor layout 建議 每一段等長要141 以內, 建議等長僅能差2次;

USB3.0 EMI-Protection

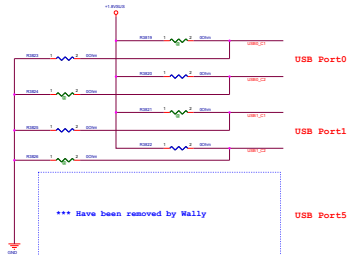
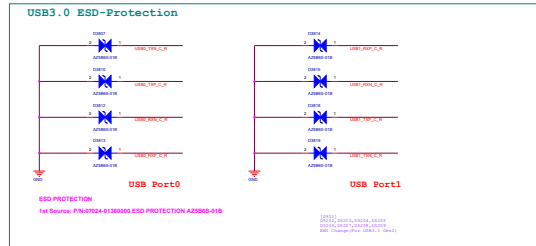
Close to Connector side



USB2.0 ESD-Protection

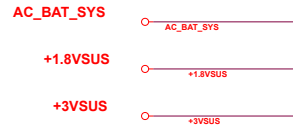


USB3.0 ESD-Protection



ASUS Title: Asus_HP Jack_MIC
Engineer: POOL EE
Date: 2019/06/06
Drawn: GA401QM

*** POWER

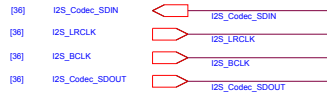


*** SINGAL

** from EC [36]



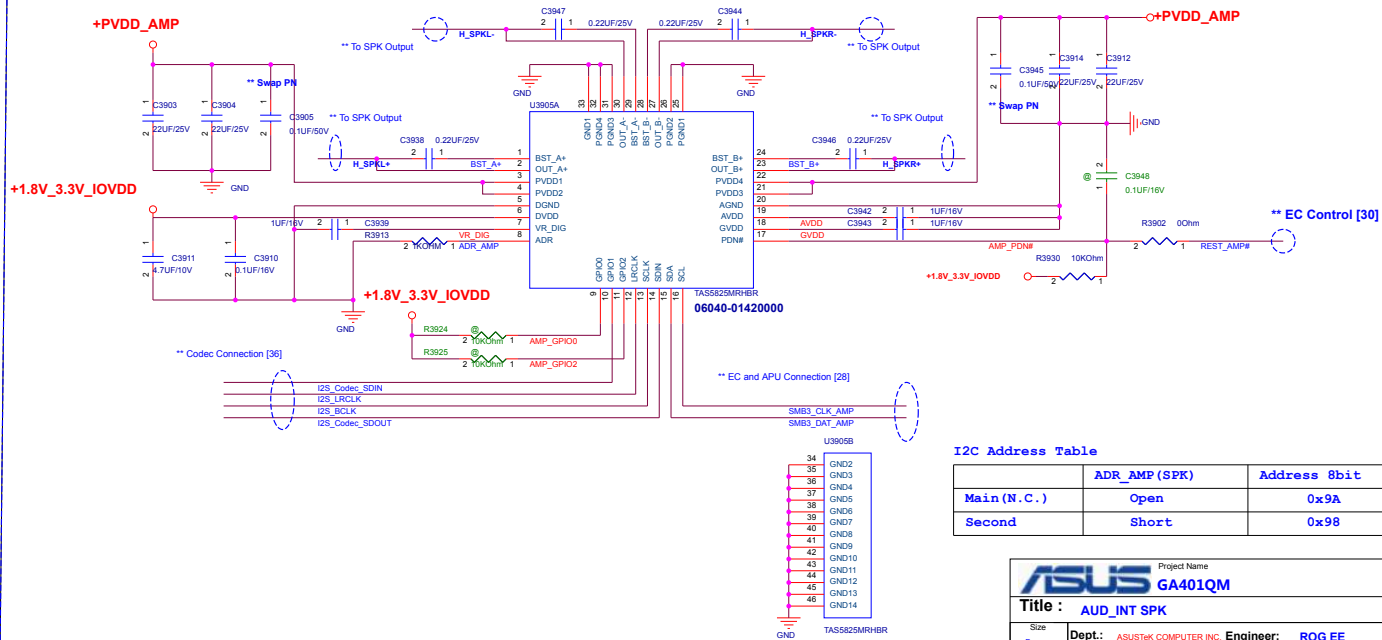
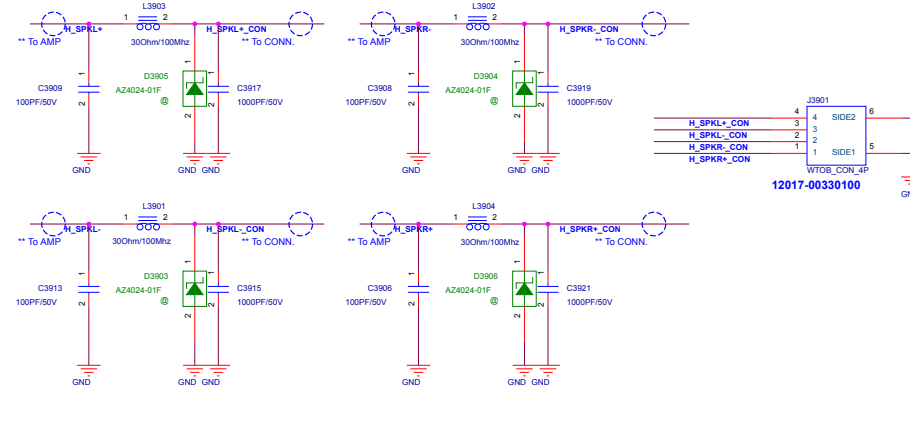
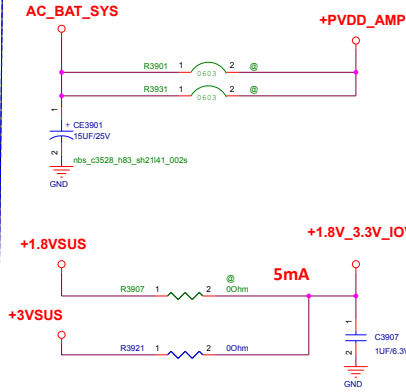
** from Codec [36]



** from EC and APU [28]



** PWR DISTRIBUTION



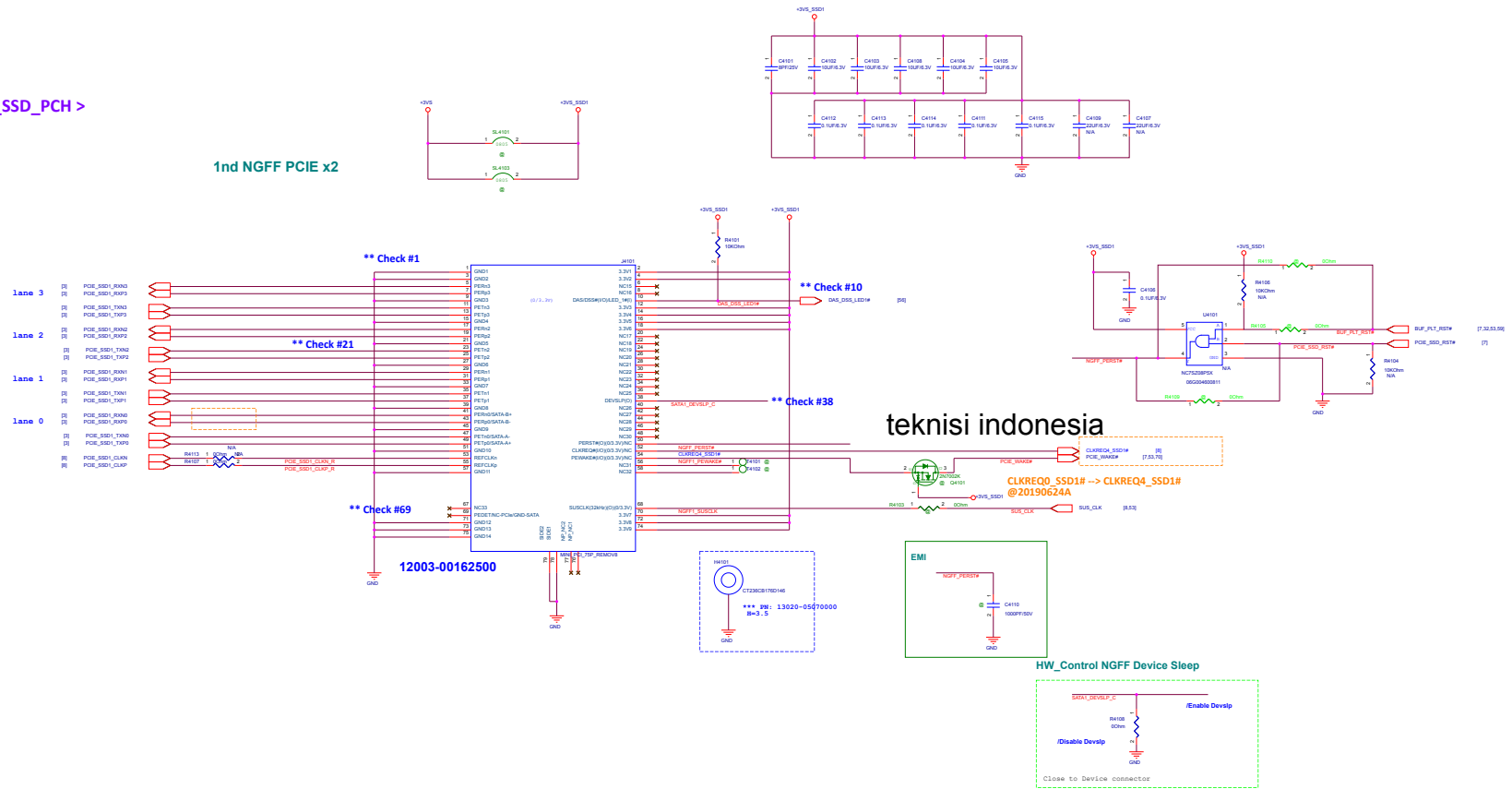
I2C Address Table

	ADR_AMP (SPK)	Address 8bit
Main (N.C.)	Open	0x9A
Second	Short	0x98

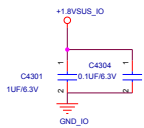
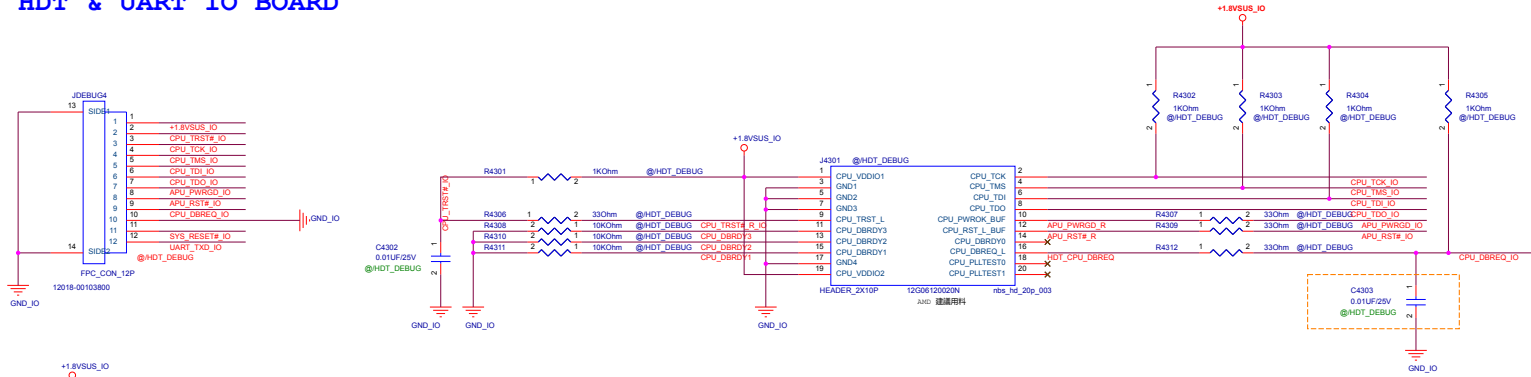
ASUS Project Name		Rev
GA401QM		R1.2
Title: AUD_INT SPK		
Size	Dept.: ASUSTek COMPUTER INC	Engineer: ROG EE
B	Date: Wednesday, December 02, 2020	Sheet 39 of 104

< KEY-M NGFF_SSD_PCH >

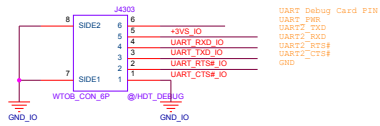
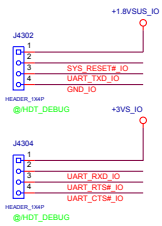
1nd NGFF PCIE x2



HDT & UART IO BOARD



UART Debug

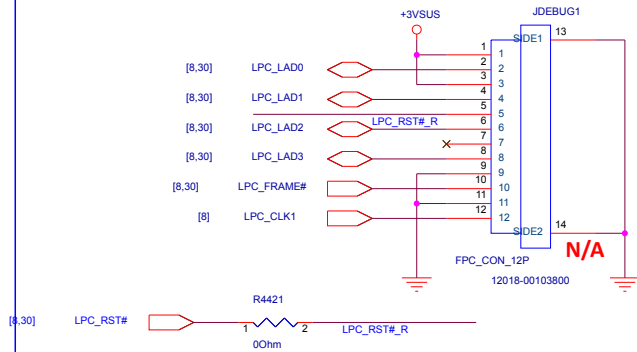


12G171230062

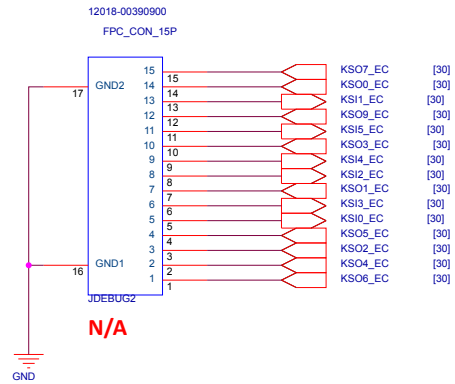
UART Debug card 上的RX = MB的TX

ASUS		Project Name	Rev
		GA401QM	1.0
Title : IO Board			
Size	Dept.:	ASUSTek COMPUTER	Engineer: ROG EE
Date: Wednesday, December 02, 2020	Sheet	43	of 130

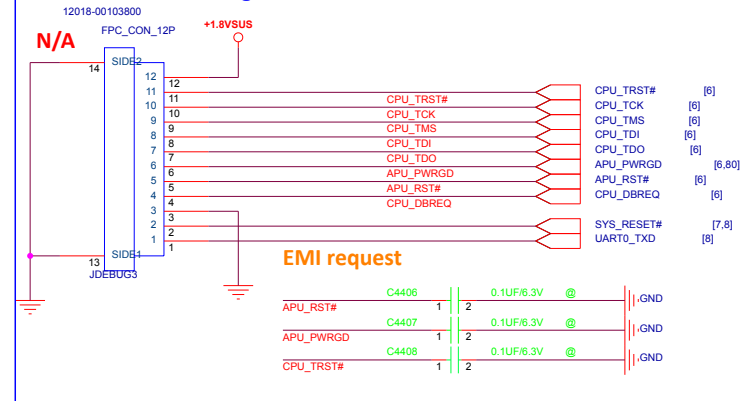
LPC Debug Port



Jia Board

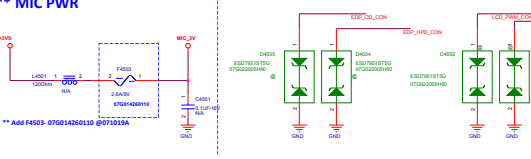
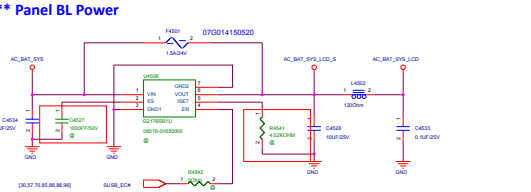
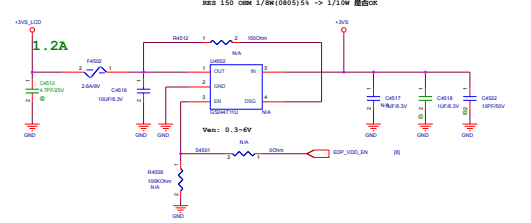
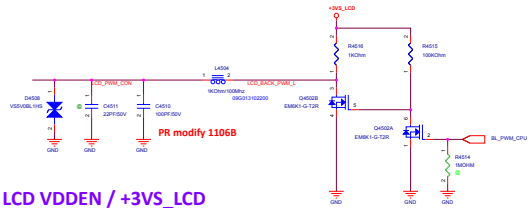
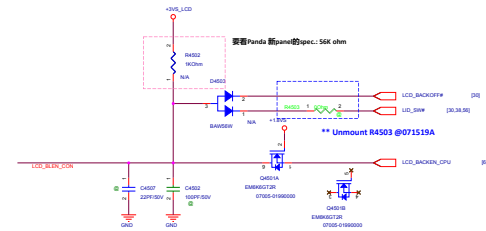


HDT + UART Debug



***** POWER**

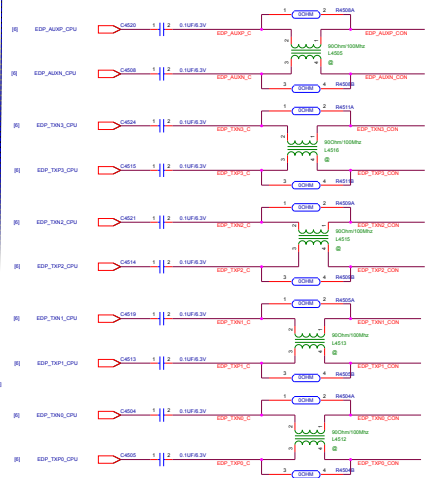
Controll Signal (LCD/BL)



***** SINGAL**

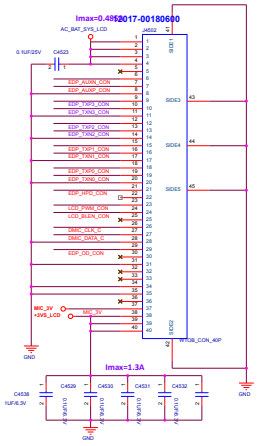
eDP from CPU

For EMI



**** Modified the LCM CONN@07002219**

eDP Panel Conn.



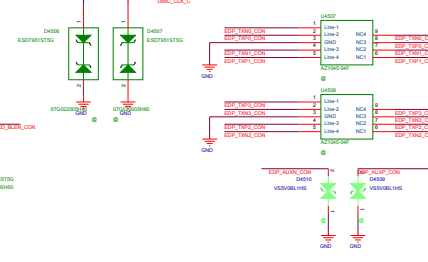
**** eDP_HPDC (CPU)**



MIC



**** For ESD**

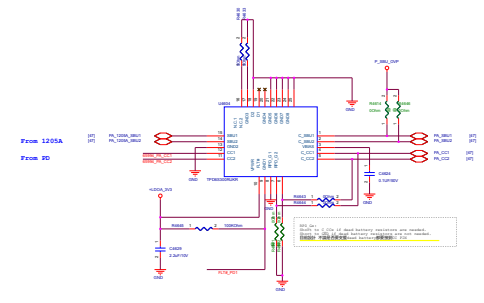
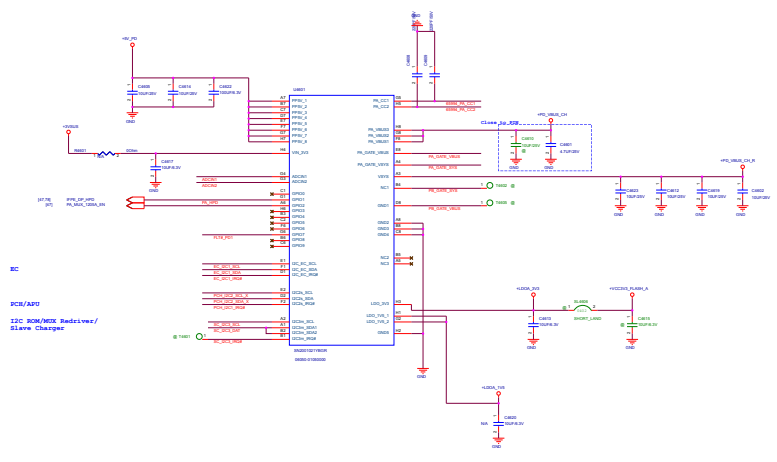
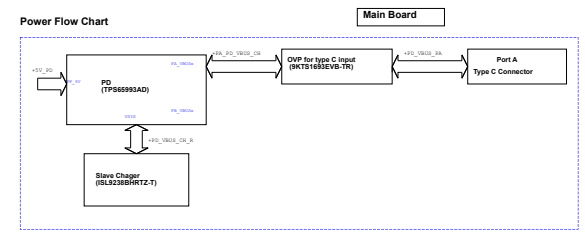
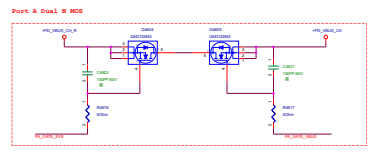
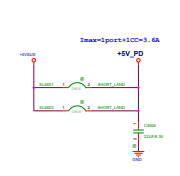
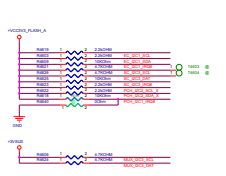


M/B side [CN1]			
Pin	Pin Defn	Pin Defn	Impedance
1	NC		
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	NC		
10	NC		
11	NC		
12	NC		
13	NC		
14	DMIC_DATA_E		<100m ohm
15	DMIC_CLK_E		50 ohm
16	NC		
17	BL_Sense		
18	BL_PWM_PWM		
19	NC		
20	HPD		
21	NC		
22	LcmA0_N		Cosial
23	LcmA0_P		30 ohm
24	NC		
25	LcmA1_N		Cosial
26	LcmA1_P		30 ohm
27	NC		
28	LcmA2_N		Cosial
29	LcmA2_P		30 ohm
30	NC		
31	LcmA3_N		Cosial
32	LcmA3_P		30 ohm
33	NC		
34	AUX_CH_P		Cosial
35	AUX_CH_N		30 ohm
36	NC		
37	NC		
38	NC		
39	NC		
40	NC		

**** Note 1. DMIC Add FUSE**

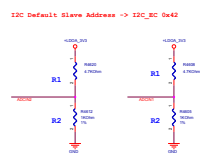
ASUS Logo
 Title: CRT_eDP
 Engineer: ROG_EE
 Project Name: GA401QM
 Rev: 1.0



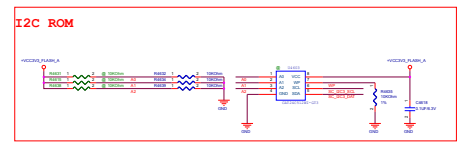
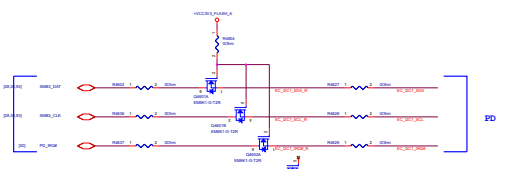


Supported Slave Charger

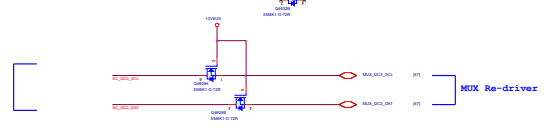
	N/O I2C ROM	W/ I2C ROM
R4620	4.7K ohm	unmount
R4612	1K ohm	1K ohm
R4608	4.7K ohm	unmount
R4605	1K ohm	1K ohm



EC & Slave Charger



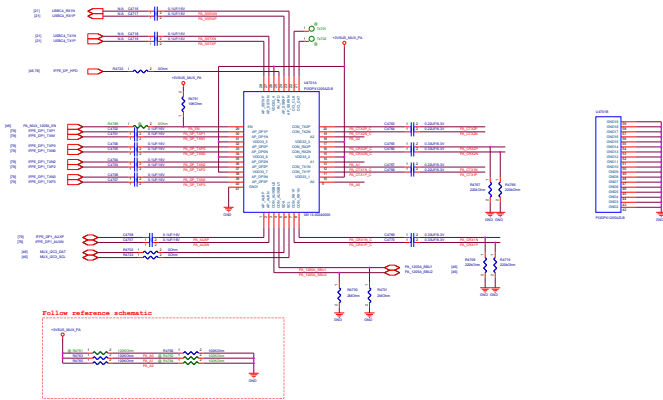
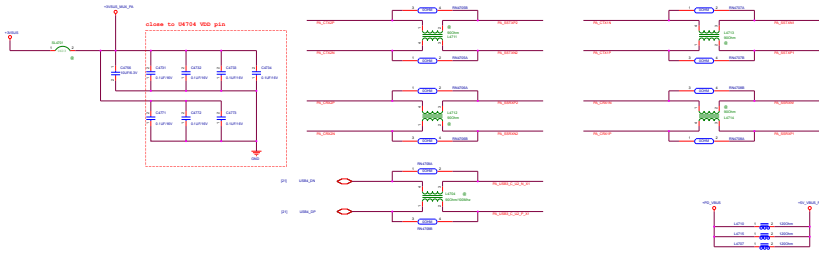
PD I2C ROM



MUX Re-driver

www.teknisi-indonesia.com

USB EMI-Protection

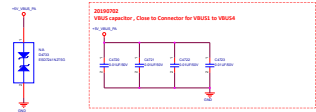


NOTE 4: PIN ASSIGNMENT: 10001110001

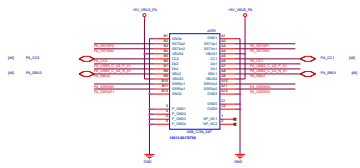
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	ATE	A11	A12
	GND	RX1+	RX1-	V _{DD}	CC1	D+	D-	SBUS1	V _{DD}	RX2+	RX2-	GND

Pin No.	B11	B11	B11	B5	B3	B7	D5	D5	D4	D3	D2	B1

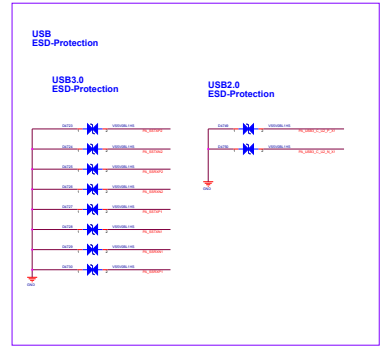
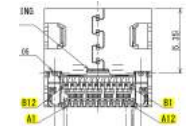
NOTE 4: LAND-NEED POINTS MAY BE 810/000/000



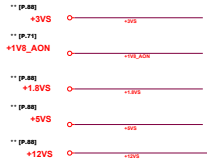
TYPE-C Connector



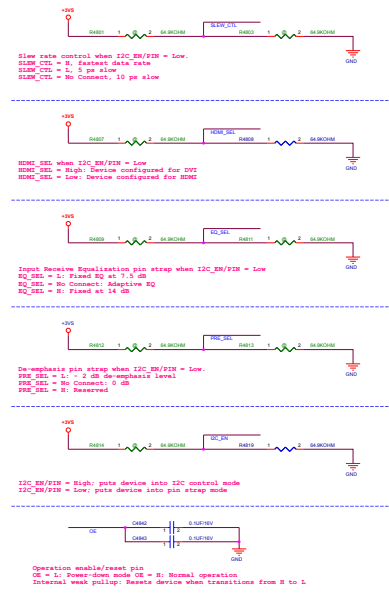
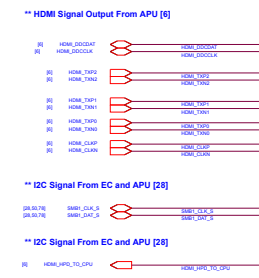
TYPE-C USB3.1



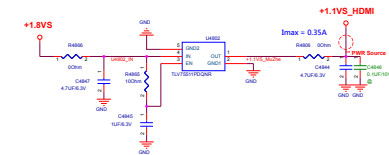
*** POWER



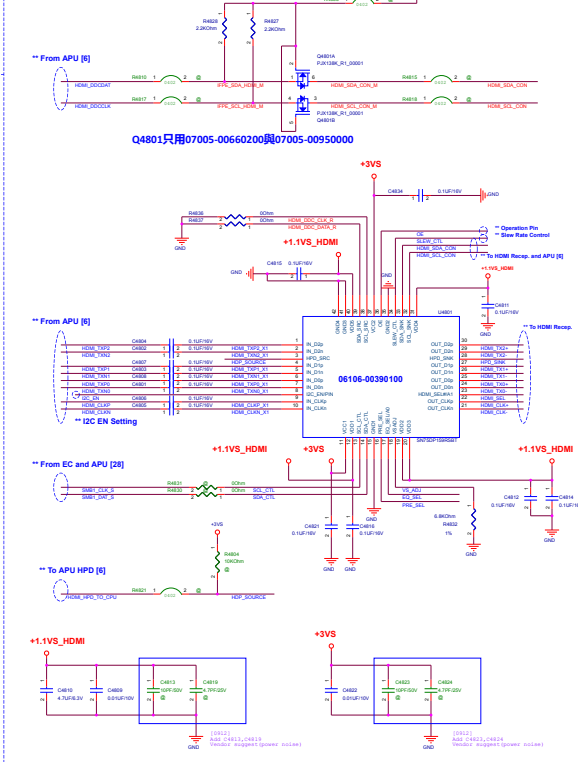
*** SINGAL



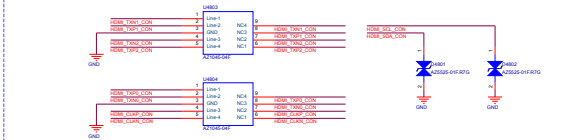
** HDMI LDO 1.1VS



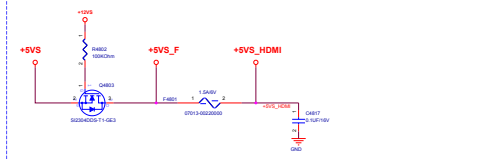
** HDMI Active-Level Shift



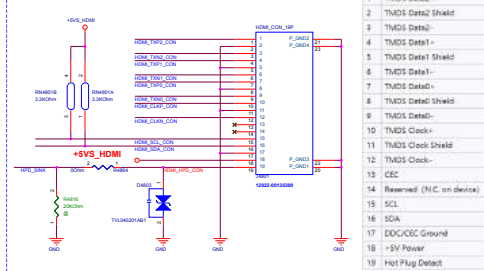
** TVS



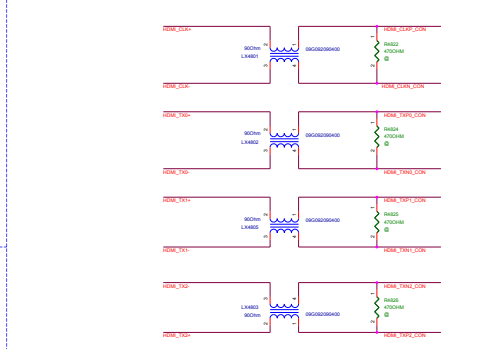
** HDMI PWR_+5VS_HDMI



** HDMI Receptacle



** HDMI EMI



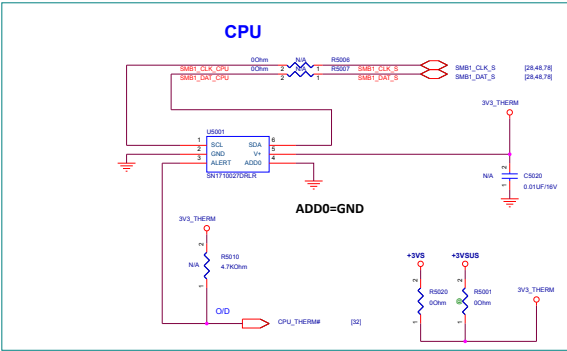
Thermal Sensor : SN170027

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

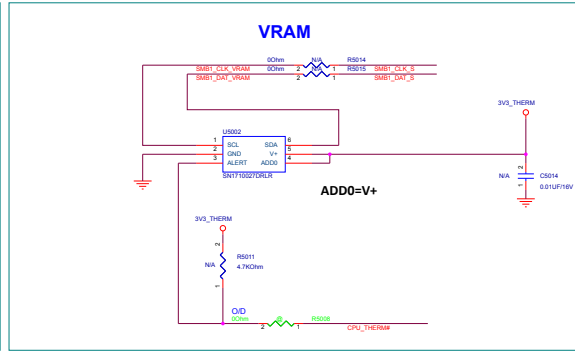
Pin function Supply voltage : 1.62 V to 3.6 V

power rail : 3.3V

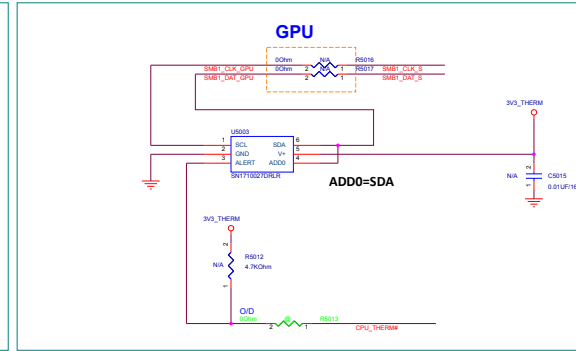
SMBUS1 to EC



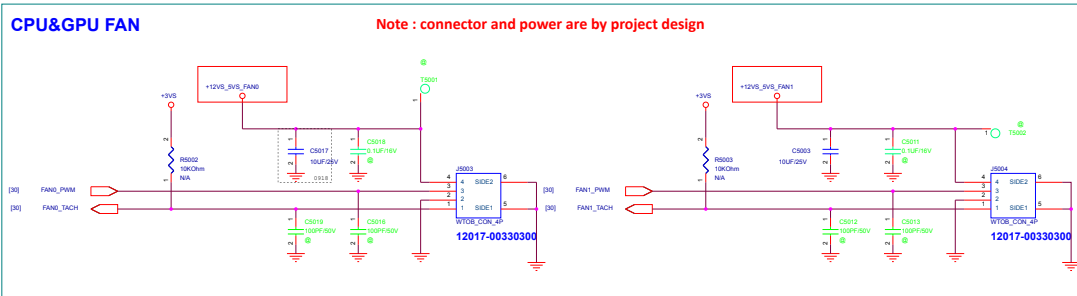
Near CPU
SMBUS addr=10010000 (90)



Near VRAM
SMBUS addr=10010010(92)

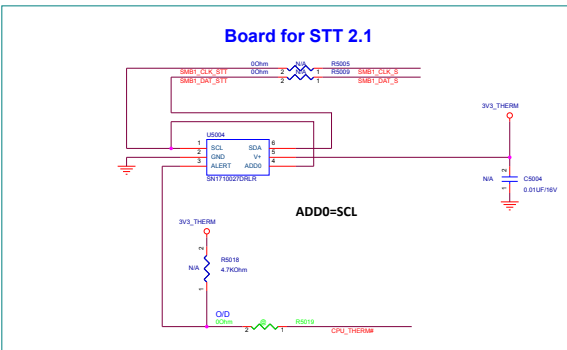


Near GPU
SMBUS addr=11001010(94)



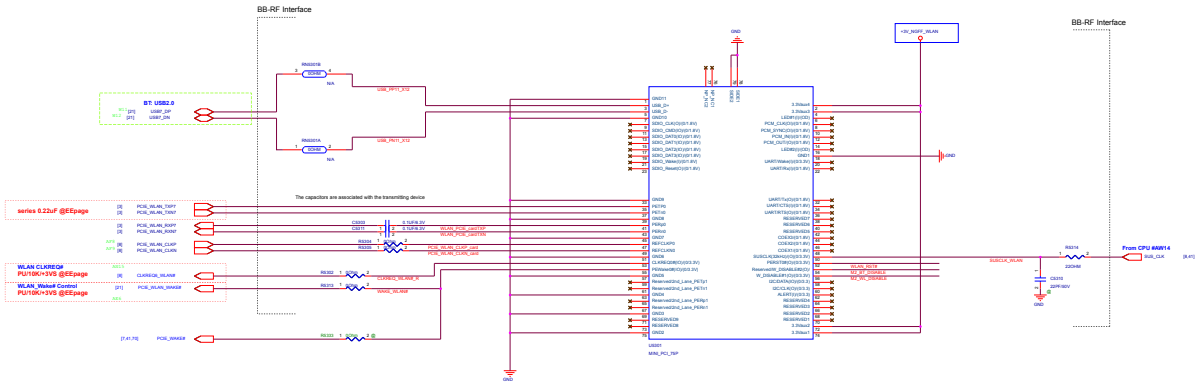
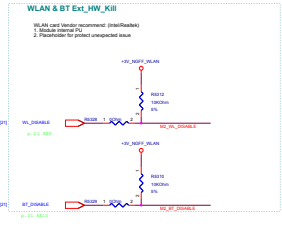
ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
1001000	90	Ground
1001001	91	V+
1001010	92	SDA
1001011	93	SCL
		Board

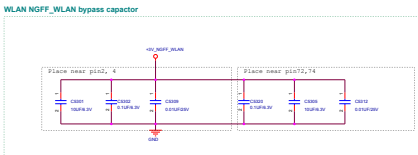
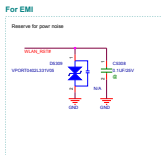
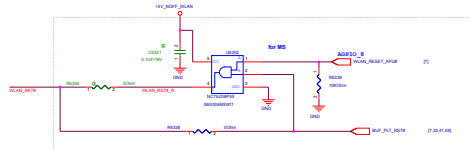


NGFF M.2 TYPE_E-KEY WIFI

Main Board

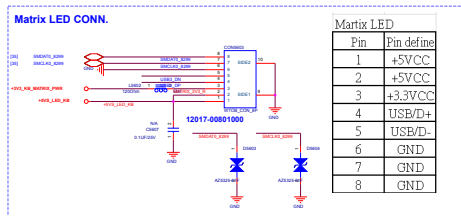
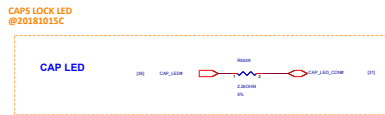
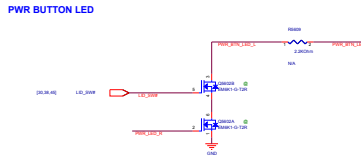
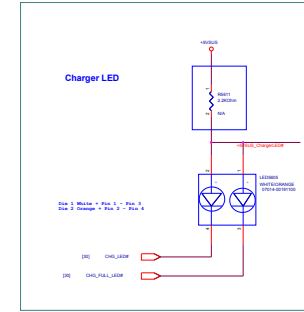
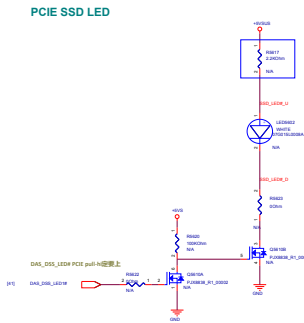
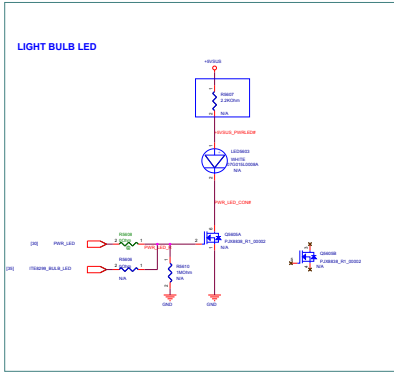


COMESBY NGFF E-KEY WLAN Connector
Do 4 pins, upper WLAN card = 2.4 mm
AGBZC04AGS02T11544
PIN: 1200-00160100

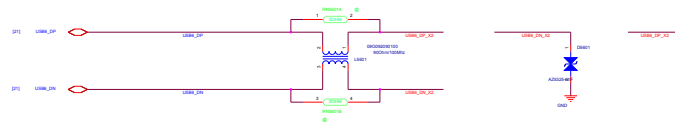
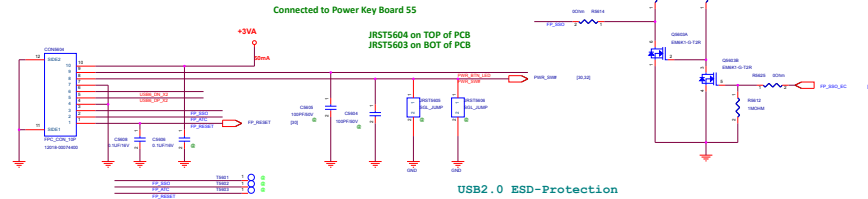


*** POWER

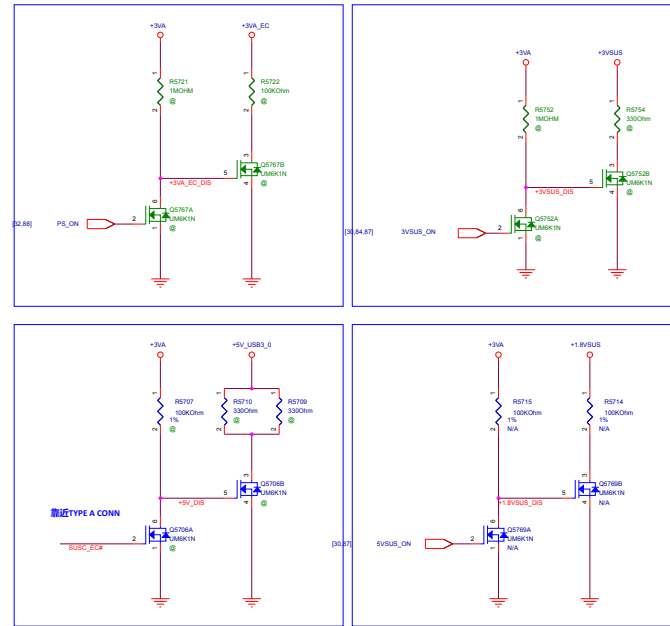
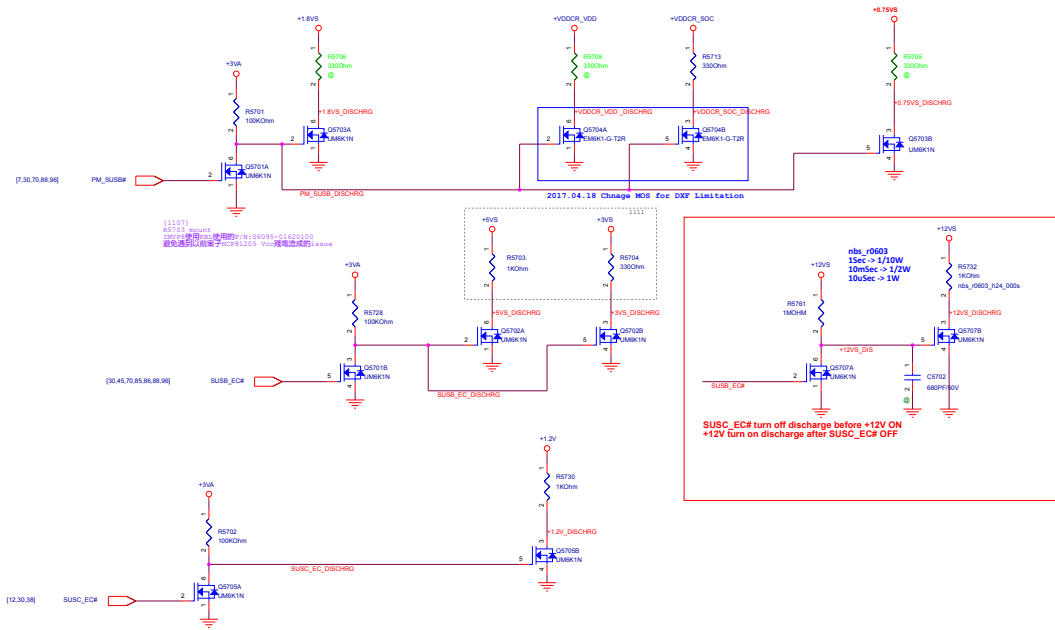
*** SINGAL



MB_PWR BUTTON CONN_10pin



NOTE:
1. PERKEY CHIP PWR ADD !!!!

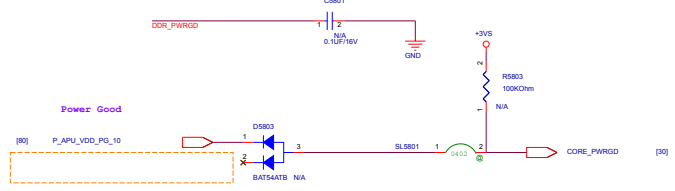
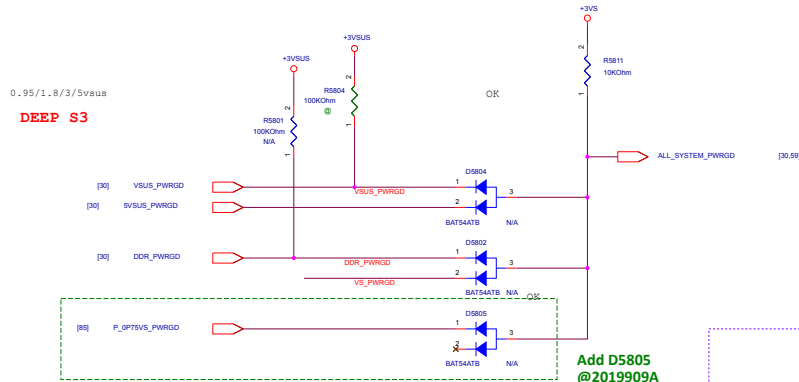


©Core Design

ASUS		Title : DSG_Discharge
ASUSTEK COMPUTER		Engineer: ROG EE
Size	Project Name	Rev
Custom	GA401QM	1.0
Date: Wednesday, December 03, 2020	Sheet	57 of 104

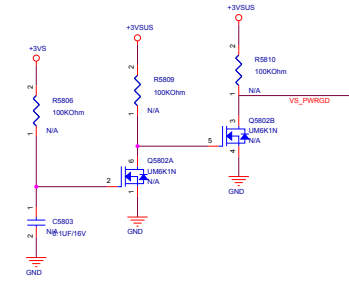
POWER GOOD DETECTOR

0.95/1.8/3/5vbus
DEEP S3

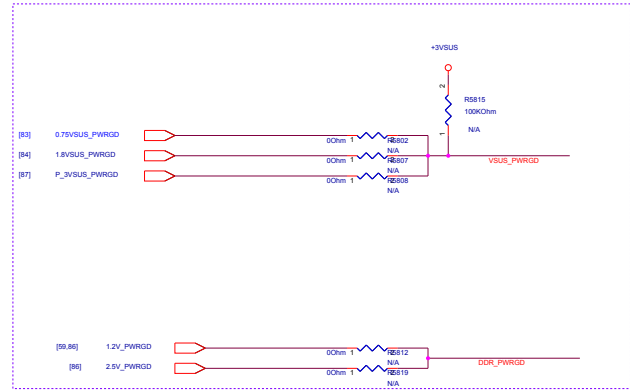


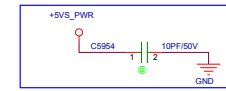
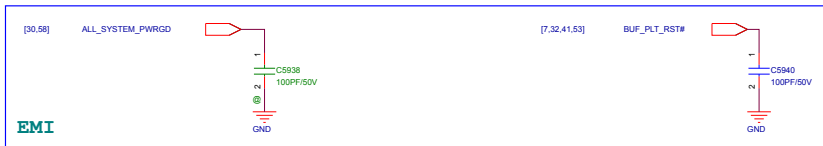
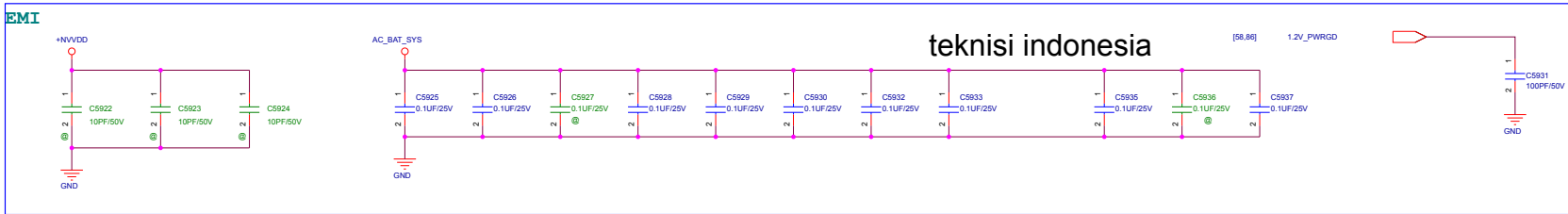
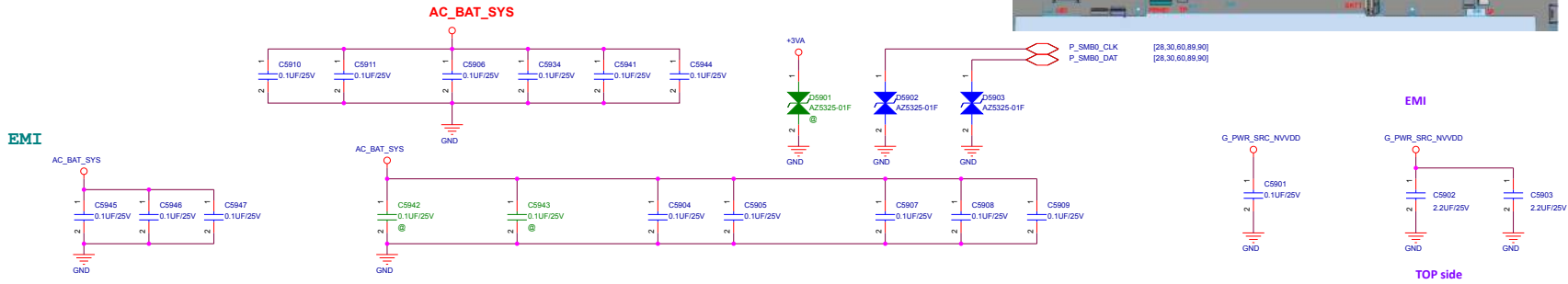
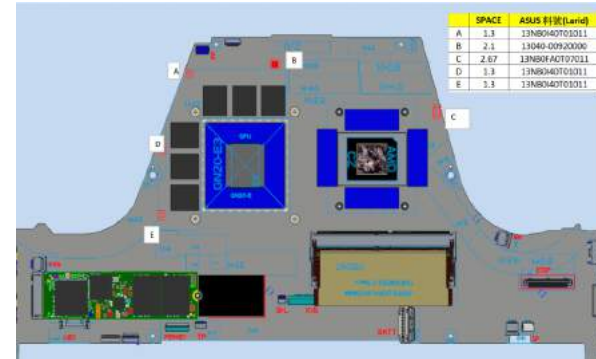
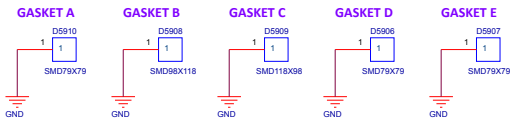
Delete P_APU_VDD_PGA_10
@ 20190626A

Remove AMD GPU PWRGD
@ 20181009K



Power Good





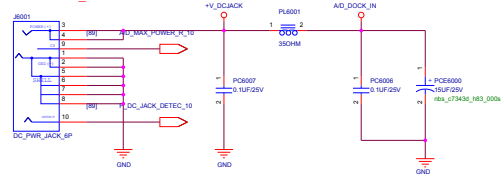
<Core Design> 2017.05.02 EMI Reserve

ASUS		Title : OTH_EMI
ASUSTEK COMPUTER		Engineer: ROG EE
Size B	Project Name GA401QM	Rev 1.0
Date: Wednesday, December 02, 2020	Sheet 59	of 104

DC-IN Connector

DC Jack使用請詢用River_Hsu

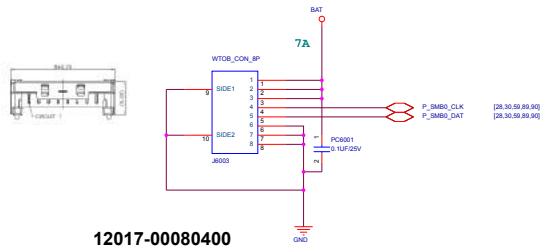
New 6 Phi 4 Pin DC_Jack



	3.4CH	1.55CH
J6001	12033-00020200	12033-00020300

CHIP Cap (H=2.1)

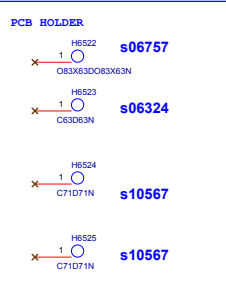
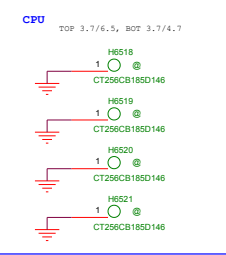
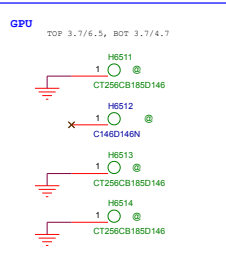
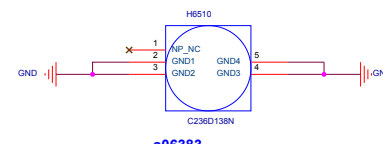
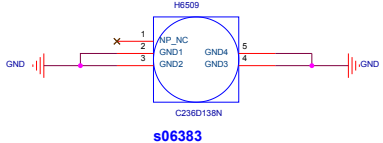
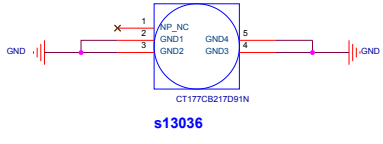
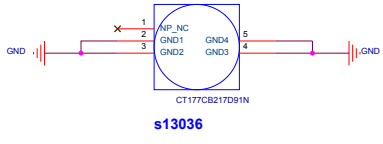
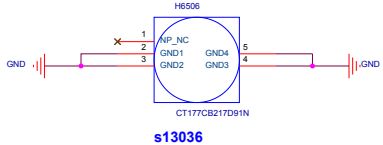
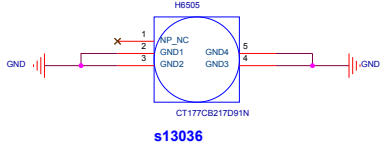
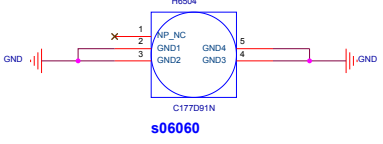
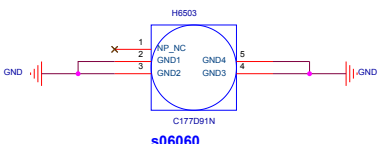
Battery Connector

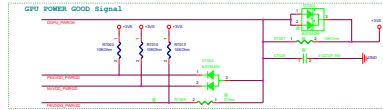


12017-00080400

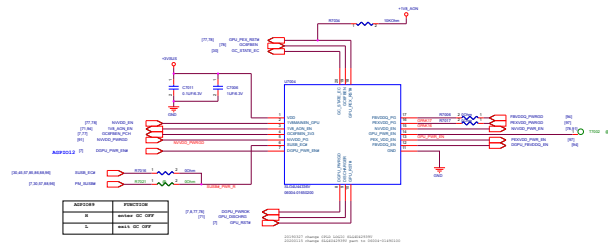
Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS		Project Name	Rev
		GA502IV	R1.0
Title : DC & BAT IN			
Size	Dept:	Engineer:	Power RD
A3	MS_Power team		
Date	Wednesday, December 02, 2020	Sheet	65 of 104

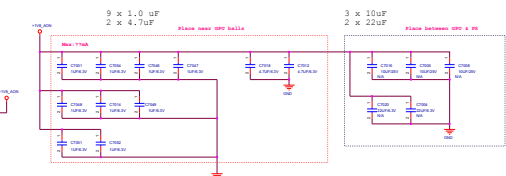
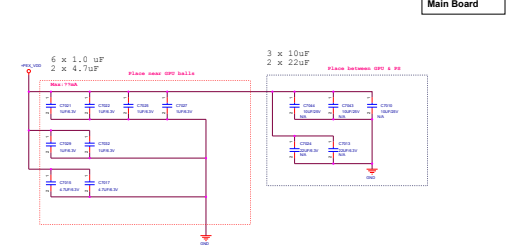
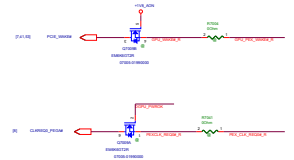
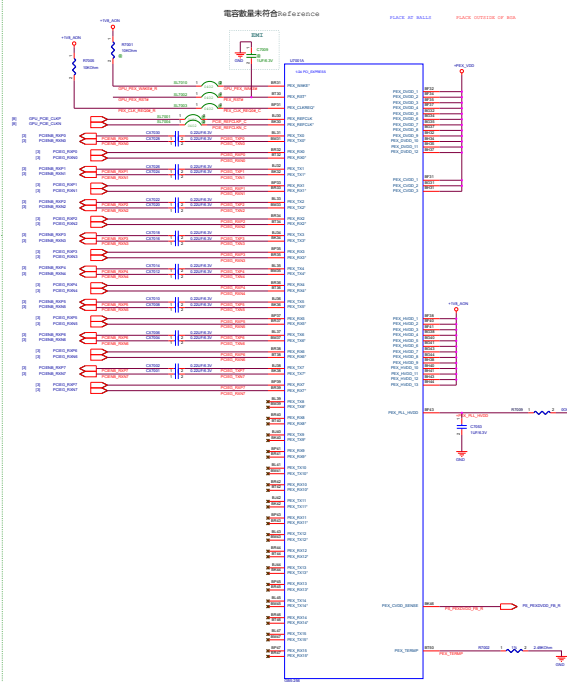




GPU POWER SEQUENCE CONTROL

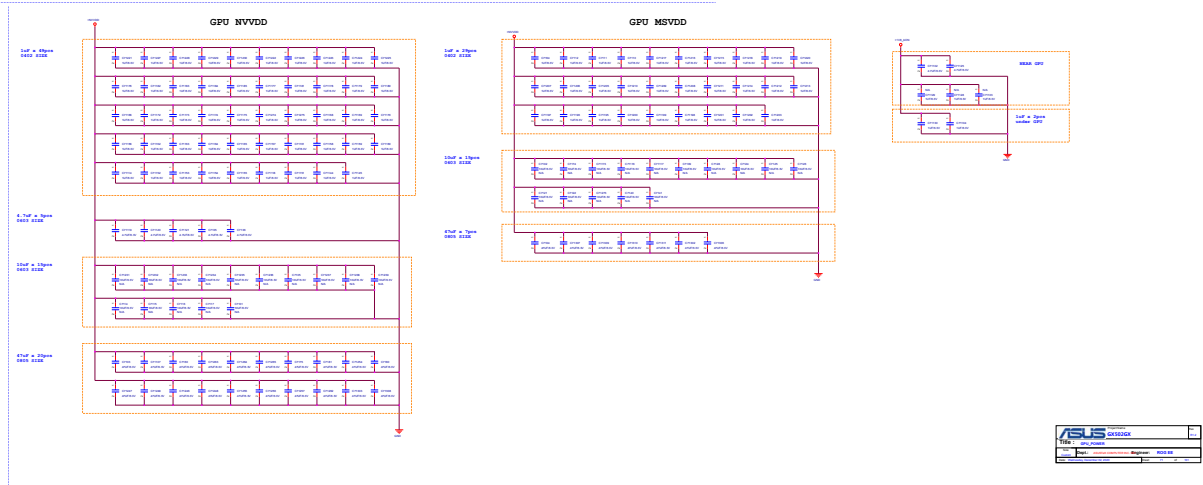
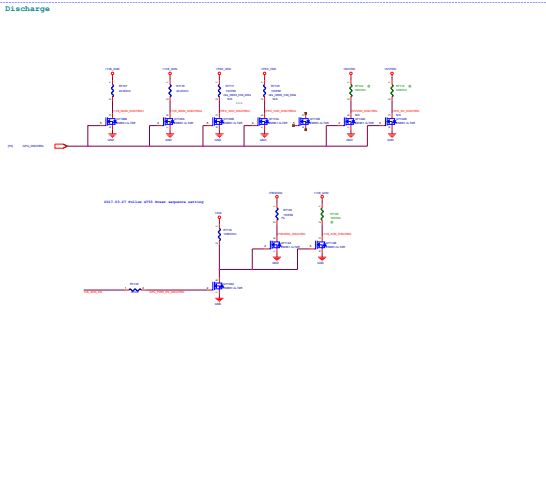
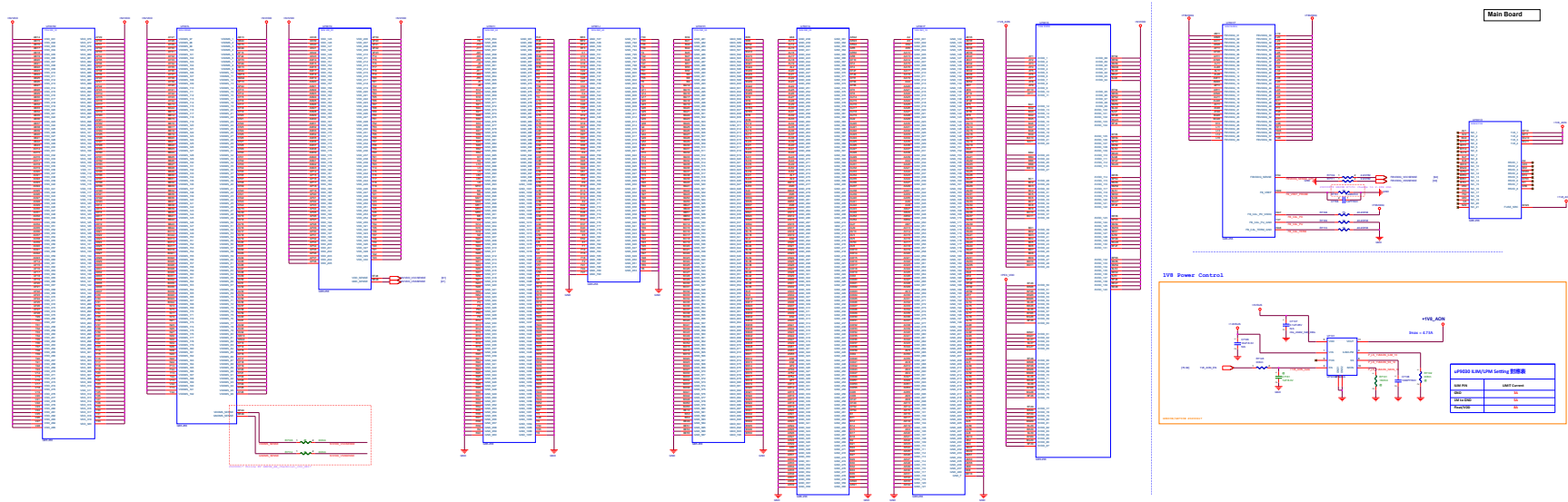


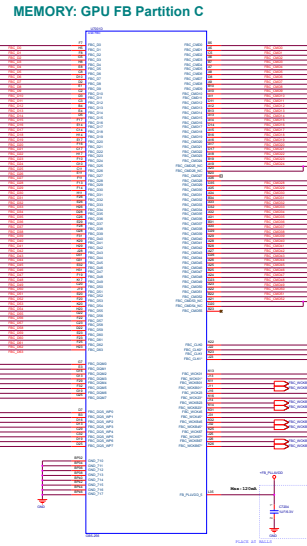
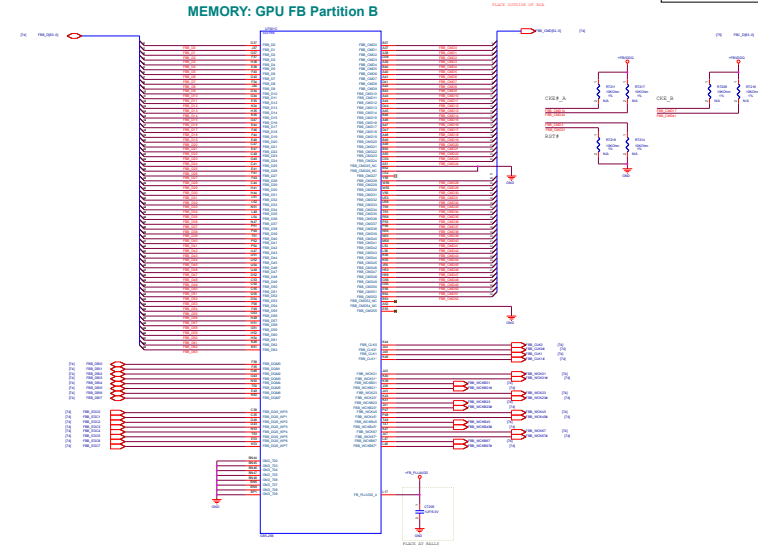
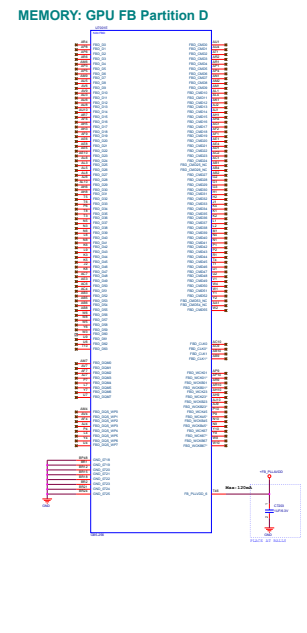
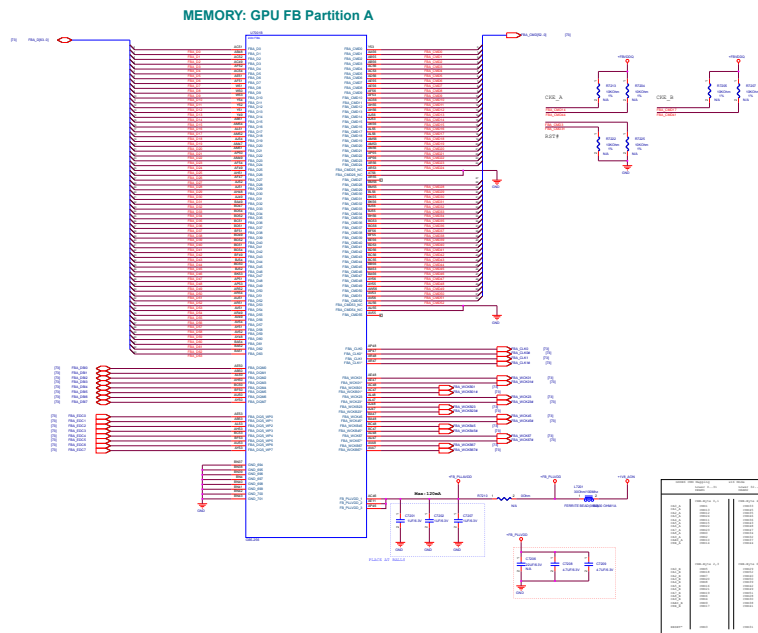
ADAPTER	FUNCTION
A	MAXX OC OFF
B	MAXX OC OFF



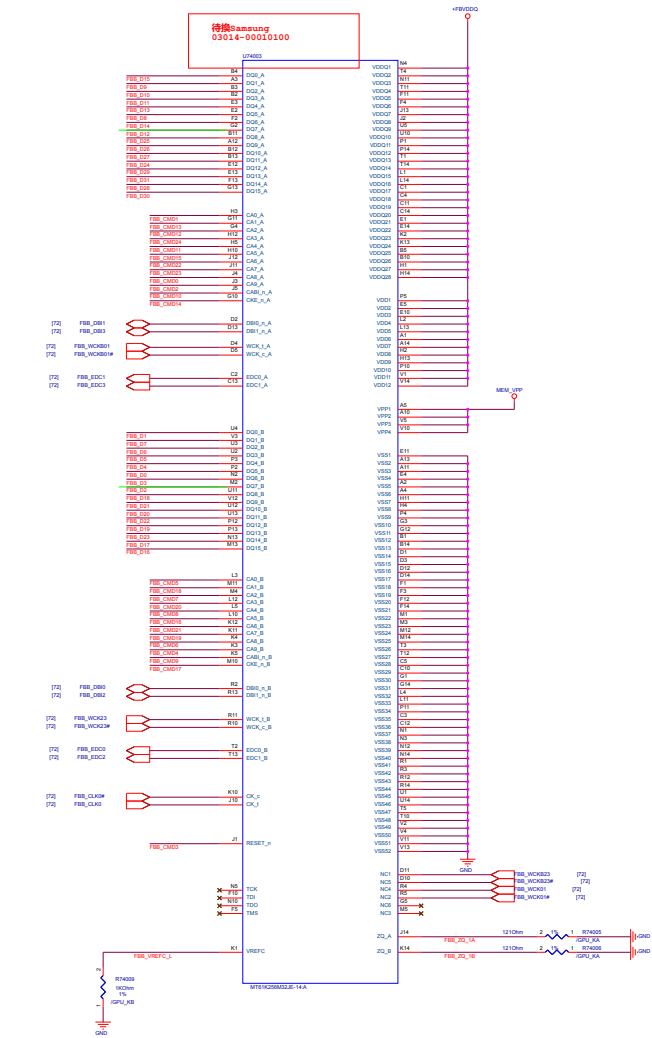
ASUS
Title: GPU_PCIE_W
Date: 2024-01-10
Author: ASUS



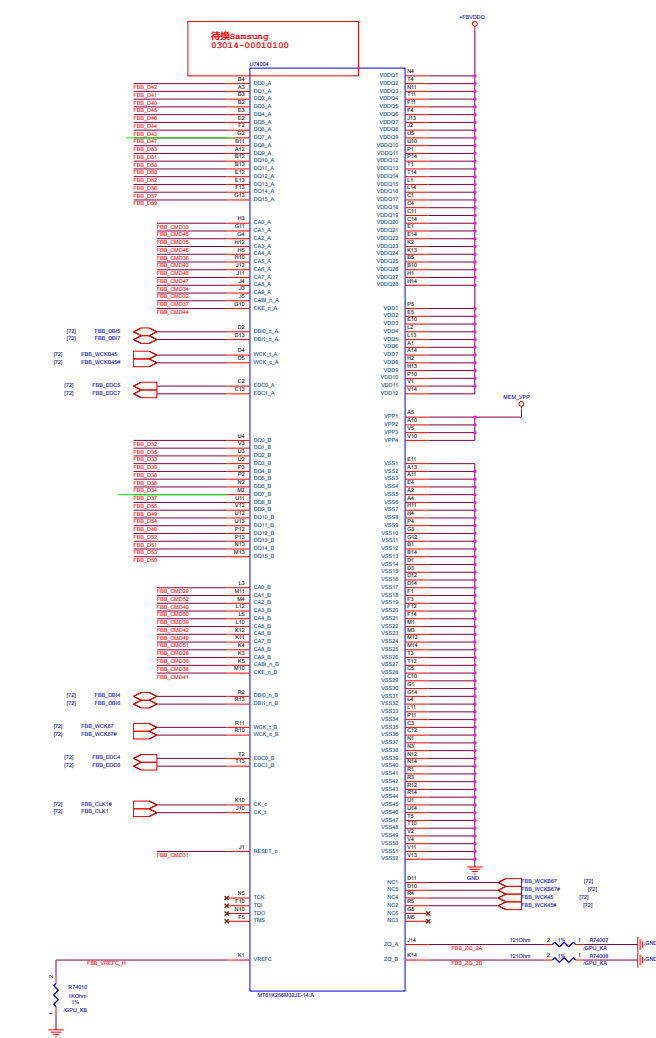




40 Ohm NET
 FBB Partition 31..0
 MF=1 Mirror

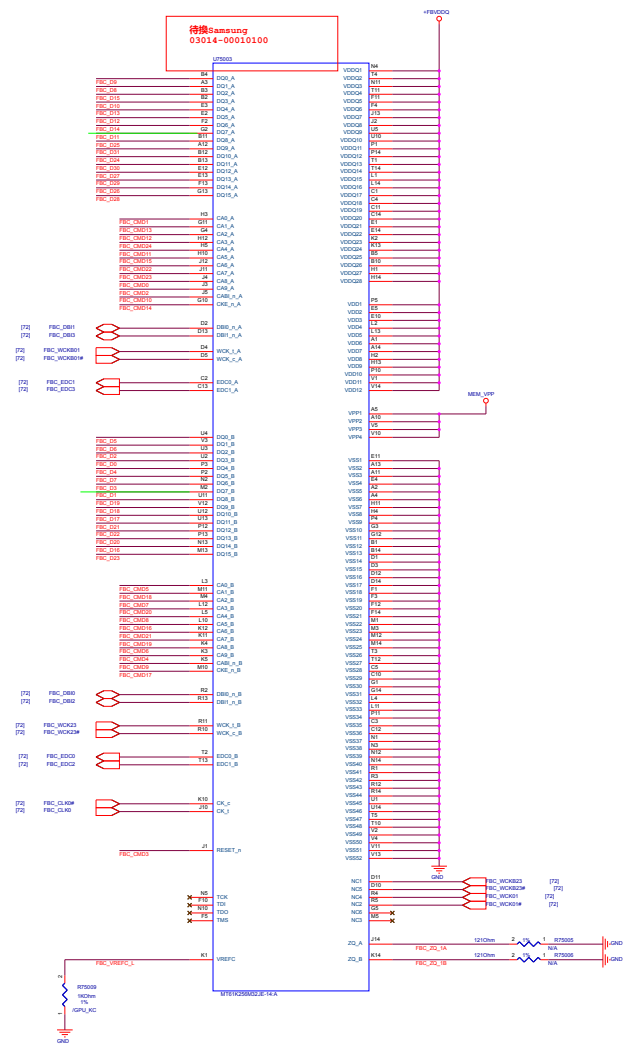


40 Ohm NET
 FBB Partition 64..32
 MF=0 Normal

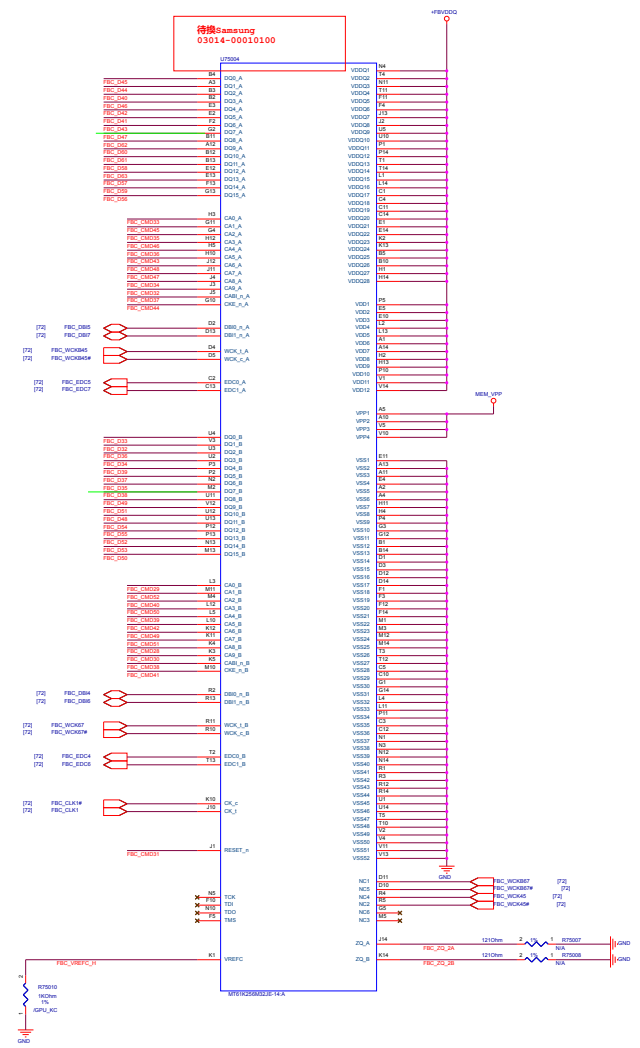




40 Ohm NET
FBC Partition 31..0
MF=1 Mirror

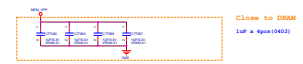
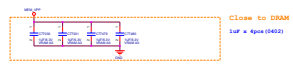
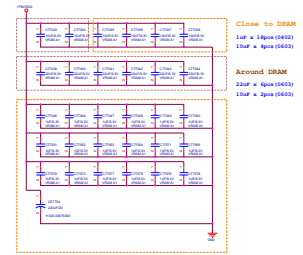
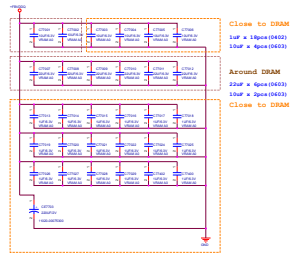


40 Ohm NET
FBC Partition 64..32
MF=0 Normal

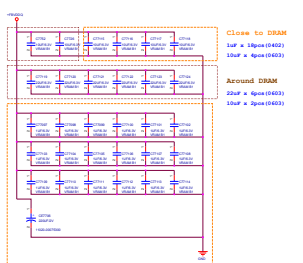
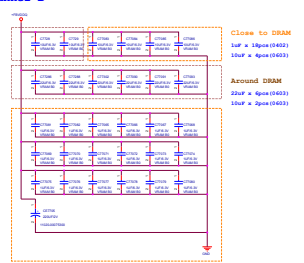


FBVDDQ
VRAM side

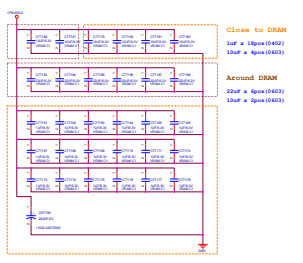
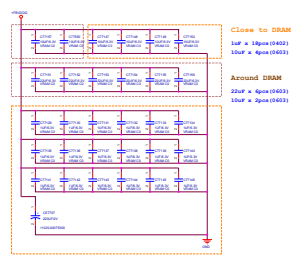
Channel A



Channel B

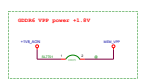
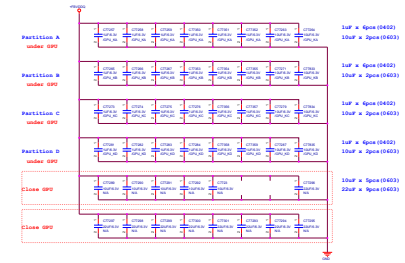


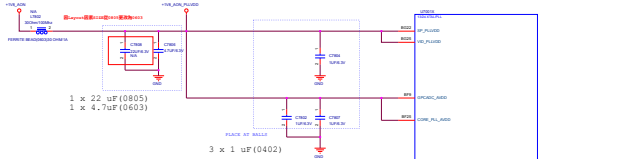
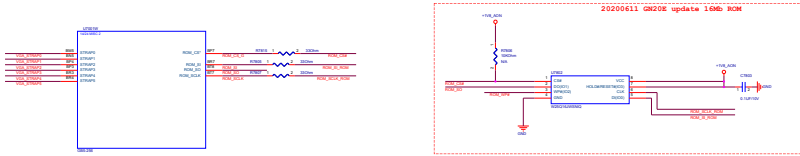
Channel C



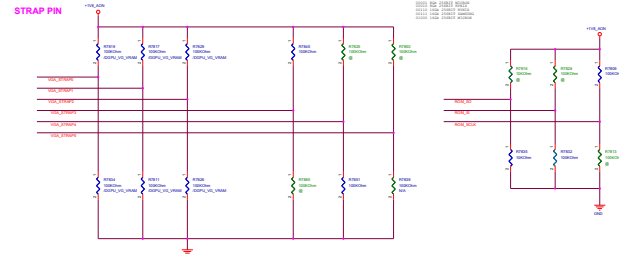
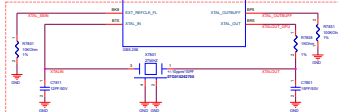
FBVDDQ
GPU side

VRAM_FWR_FBVDDQ





X7691 278M2 (1-Regulator) (2225)
 for: PIN#GTG1602765 TAD2VZ000690
 for: PIN#GTG1602761 HOSGN0CE3P827 20M11011



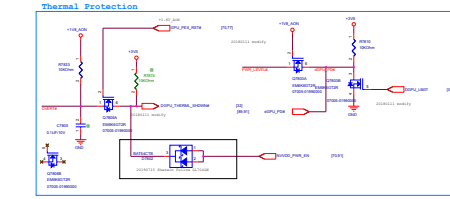
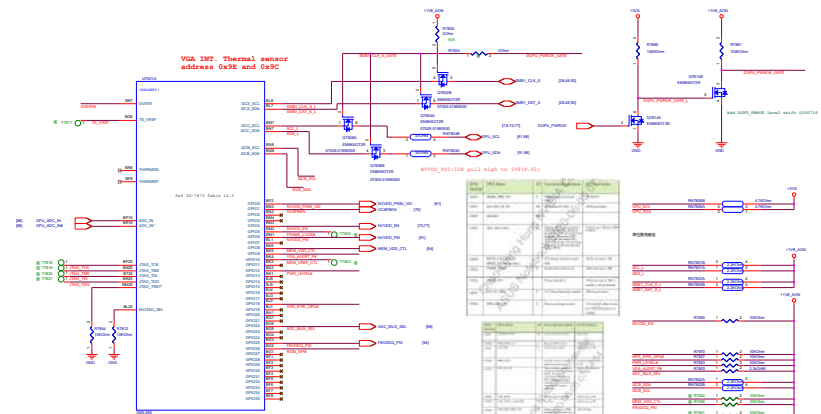
ASUS P/N	Company	Vendor P/N	[MT/s]	Density	Strap	STRAP2	STRAP1	STRAP0
VRAM								
09014-00010600	Samsung	K4Z80325BC-HC14	14.0Gb/s	8Gb	0x0	L	L	L
09014-00010900	Hynix	H56C8H24AIR-S2C	14.0Gb/s	8Gb	0x2	L	H	L
09014-00010500	Micron	MT61K256M32JE-14-A	14.0Gb/s	8Gb	0x1	L	L	H

Strap Pin	Recommended Pull-Up Resistor		Strap	Strap Pin	Recommended Pull-Up Resistor	
	Value	Part No.			Value	Part No.
STRAP0	10k	0402	0x0	STRAP1	10k	0402
STRAP1	10k	0402	0x2	STRAP2	10k	0402
STRAP2	10k	0402	0x1	STRAP3	10k	0402
STRAP3	10k	0402	0x3	STRAP4	10k	0402
STRAP4	10k	0402	0x4	STRAP5	10k	0402
STRAP5	10k	0402	0x5	STRAP6	10k	0402
STRAP6	10k	0402	0x6	STRAP7	10k	0402
STRAP7	10k	0402	0x7			

Level	Part No.	Value	Part No.	Value
Level 1	10k	0402	10k	0402
Level 2	10k	0402	10k	0402
Level 3	10k	0402	10k	0402
Level 4	10k	0402	10k	0402
Level 5	10k	0402	10k	0402
Level 6	10k	0402	10k	0402
Level 7	10k	0402	10k	0402
Level 8	10k	0402	10k	0402
Level 9	10k	0402	10k	0402
Level 10	10k	0402	10k	0402

Strap Pin	Value	Part No.
STRAP0	10k	0402
STRAP1	10k	0402
STRAP2	10k	0402
STRAP3	10k	0402
STRAP4	10k	0402
STRAP5	10k	0402
STRAP6	10k	0402
STRAP7	10k	0402

Recommended Configuration: STRAP0=0, STRAP1=0, STRAP2=0, STRAP3=0, STRAP4=0, STRAP5=0, STRAP6=0, STRAP7=0.



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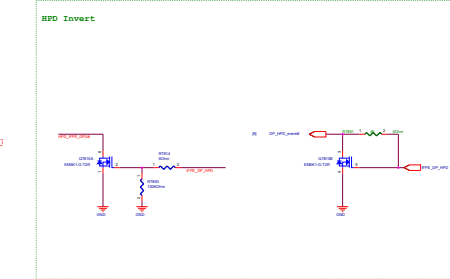
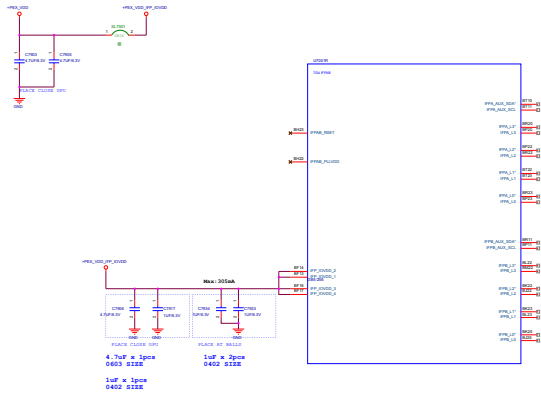


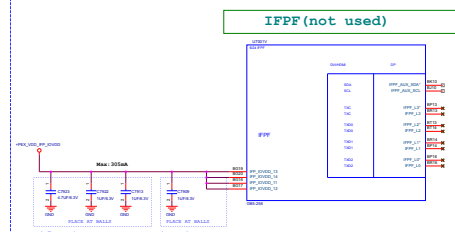
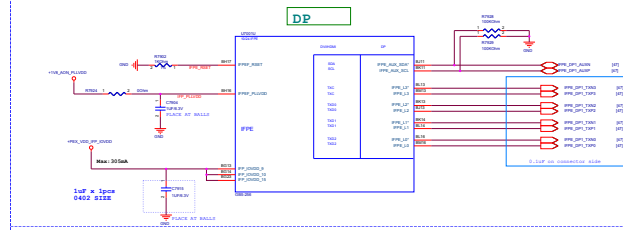
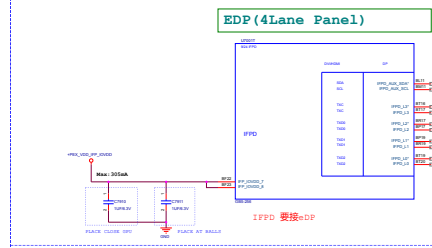
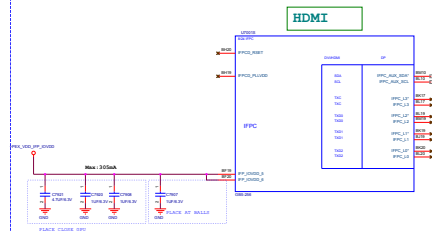
Table 3. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Aleft	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	20200611	Full	Production candidate
		1.25V	Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.2V ¹	Micron	MT61K256M32JE-14-A	A-die	0x1	14 Gbps	1940 ²	Full	Production candidate

Notes:
 1 Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
 2 Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SP1" letters inserted before the seven digits in its lot ID.
 3 Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "RPDR6 1.2V @ 11 Gbps" words in the label.
 4 For GN20-E3, the maximum allowable memory case temperature is 75 °C.



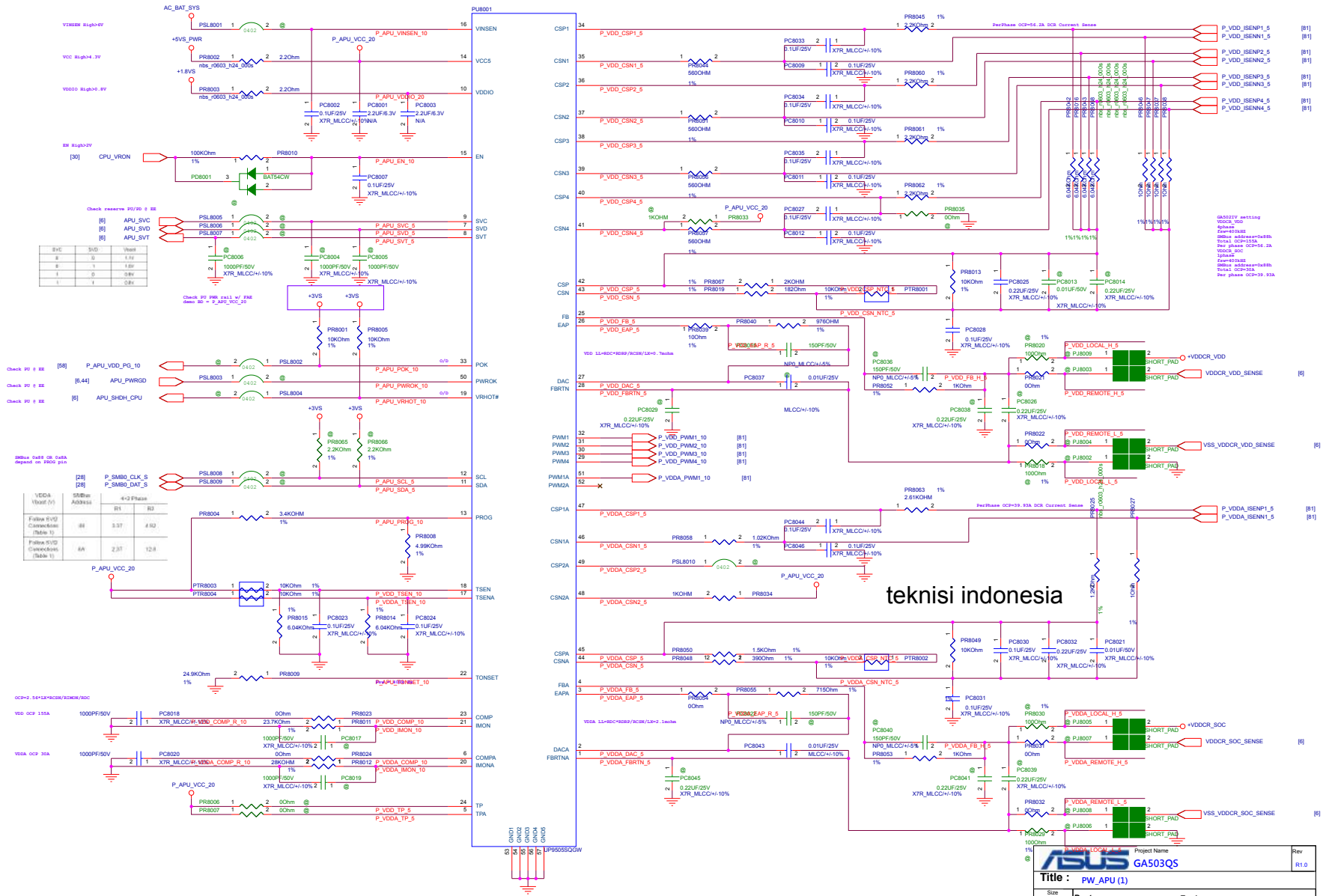
Main Board



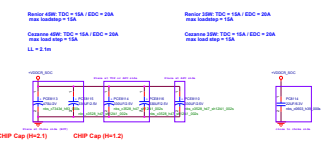
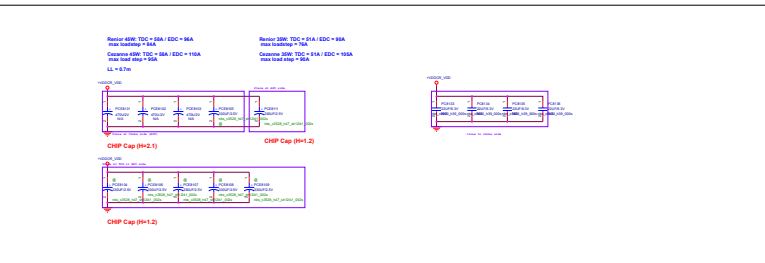
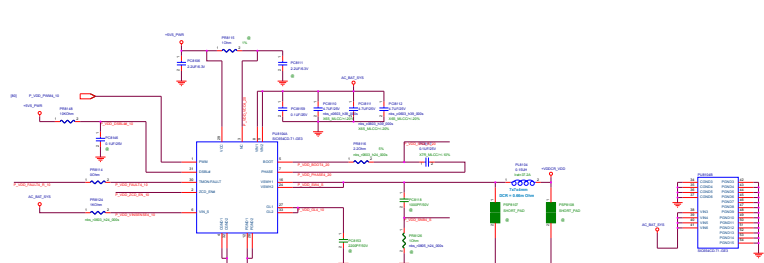
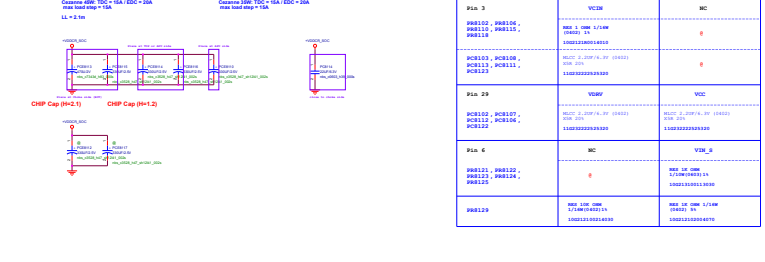
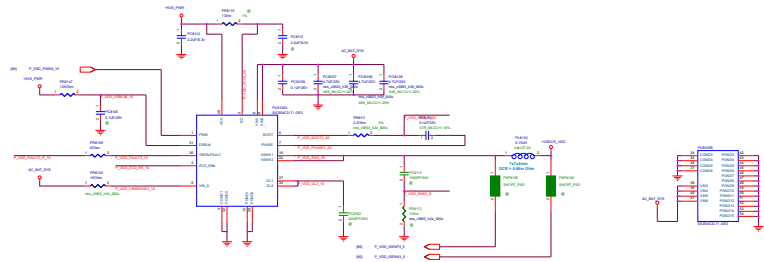
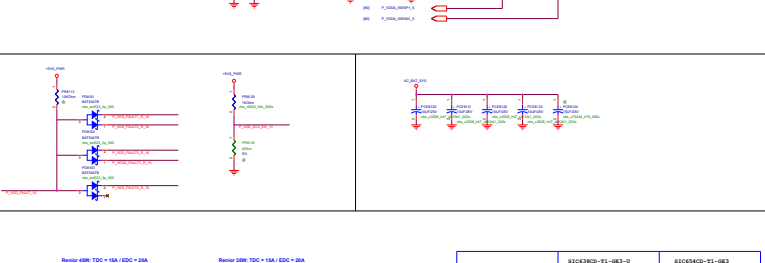
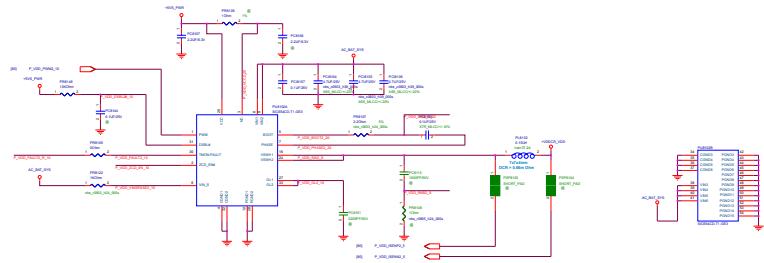
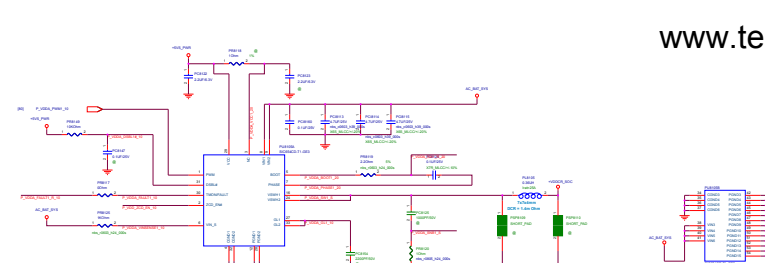
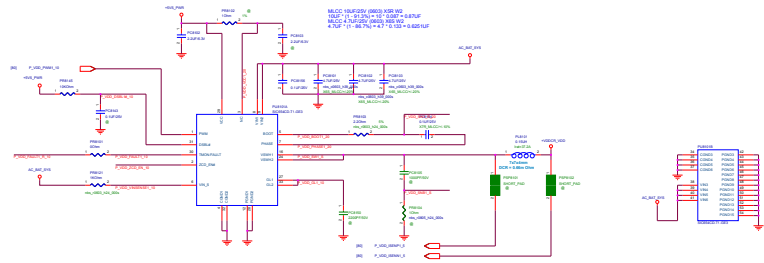
7.2 Unused pins

If an IEP link is unused, in general, it should be left unconnected. This includes Mst and Aux links. IEP0, IEP1 and IEP2, PLLVD0 (by a AB, C, D, E) can be left unconnected if neither of IEP0/ IEP1 is in use. For example, if neither link of the IEP0/ IEP1 link is to be used, then IEP0, PLLVD0 and IEP0, IEP1, IEP2 should be left unconnected. IEP0, IEP1, IEP2, IEP3, IEP4, IEP5, IEP6, IEP7, IEP8, IEP9, IEP10, IEP11, IEP12, IEP13, IEP14, IEP15, IEP16, IEP17, IEP18, IEP19, IEP20, IEP21, IEP22, IEP23, IEP24, IEP25, IEP26, IEP27, IEP28, IEP29, IEP30, IEP31, IEP32, IEP33, IEP34, IEP35, IEP36, IEP37, IEP38, IEP39, IEP40, IEP41, IEP42, IEP43, IEP44, IEP45, IEP46, IEP47, IEP48, IEP49, IEP50, IEP51, IEP52, IEP53, IEP54, IEP55, IEP56, IEP57, IEP58, IEP59, IEP60, IEP61, IEP62, IEP63, IEP64, IEP65, IEP66, IEP67, IEP68, IEP69, IEP70, IEP71, IEP72, IEP73, IEP74, IEP75, IEP76, IEP77, IEP78, IEP79, IEP80, IEP81, IEP82, IEP83, IEP84, IEP85, IEP86, IEP87, IEP88, IEP89, IEP90, IEP91, IEP92, IEP93, IEP94, IEP95, IEP96, IEP97, IEP98, IEP99, IEP100.

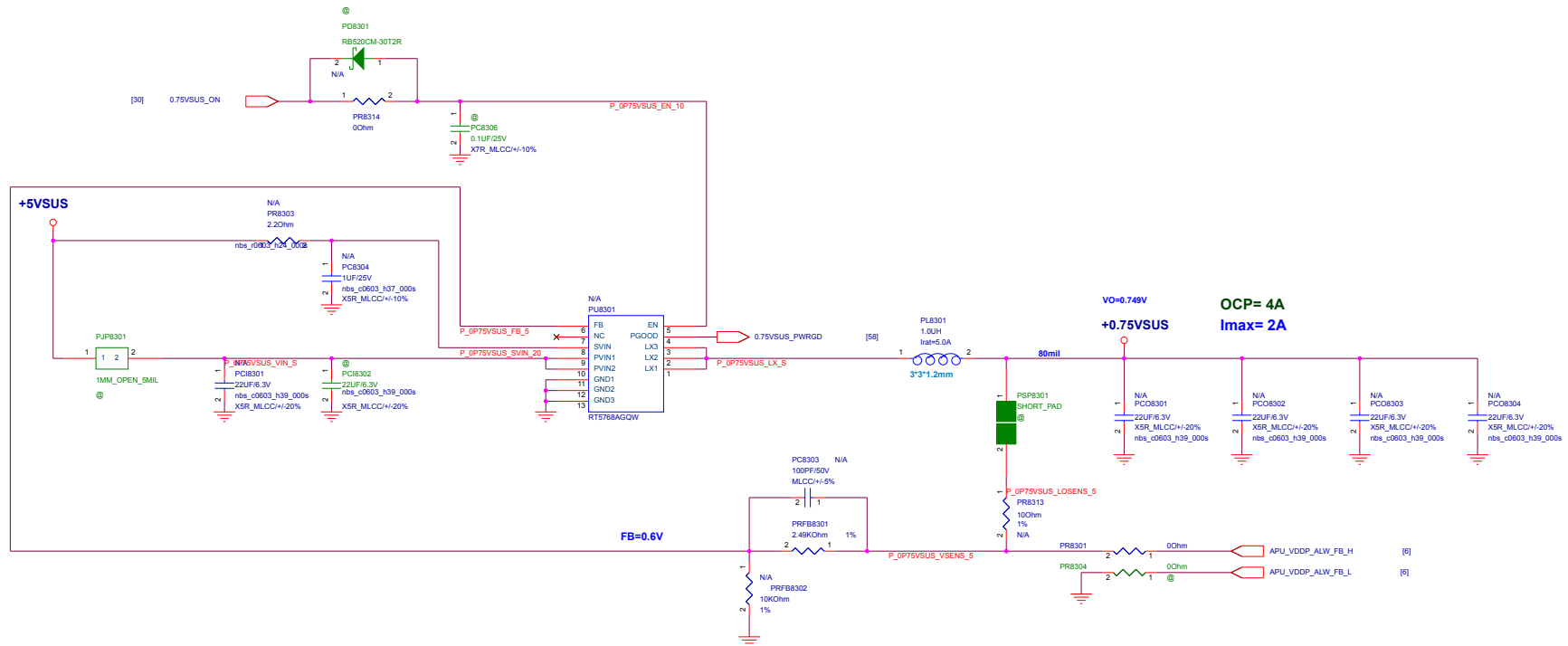




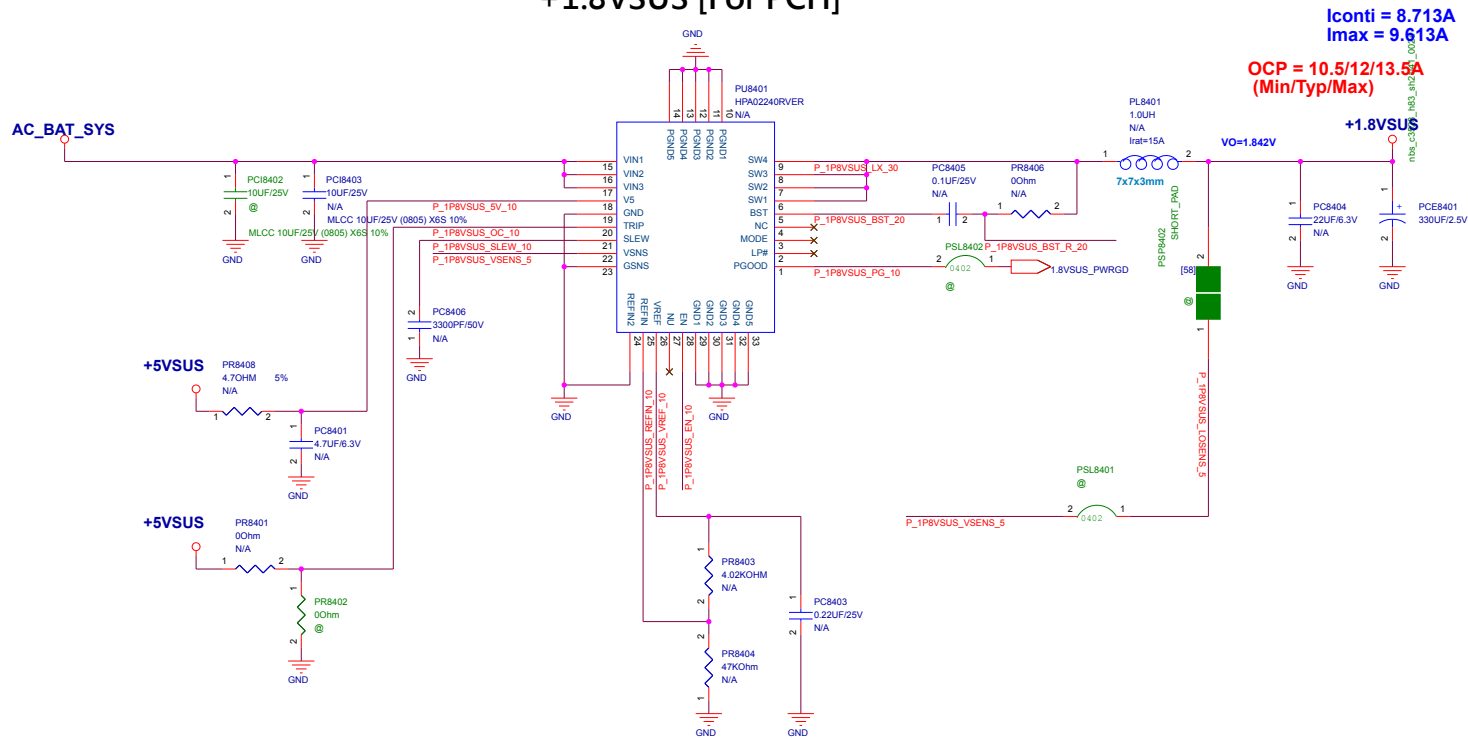
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	81063403-T1-0B3-D 07028-02020000	81063403-T1-0B3 07028-02020100
Pin 3	R86102, R86104, R86110, R86111, R86112 VCCB REF, 0V, 1/2W 10000000000000 R86103, R86106, R86113, R86114, R86115 REF, 2.20074, 1W (00001) 10000000000000 10000000000000	NC 0 0 0 0 0
Pin 20	VCCB	VCC
R86100, R86107, R86112, R86114, R86115	REF, 2.20074, 1W (00001) 10000000000000 10000000000000	REF, 2.20074, 1W (00001) 10000000000000 10000000000000
Pin 4	NC	VCC_0
R86110, R86111, R86112	0	REF, 0V, 0W 10000000000000
R86119	REF, 0V, 0W 10000000000000 10000000000000	REF, 0V, 0W 10000000000000 10000000000000



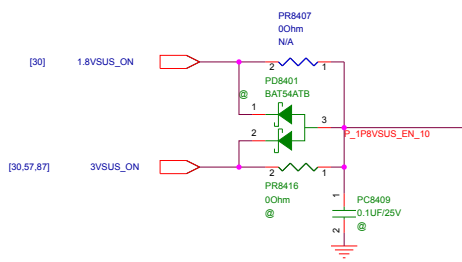
+1.8VSUS [For PCH]



Icont = 8.713A
I_{max} = 9.613A

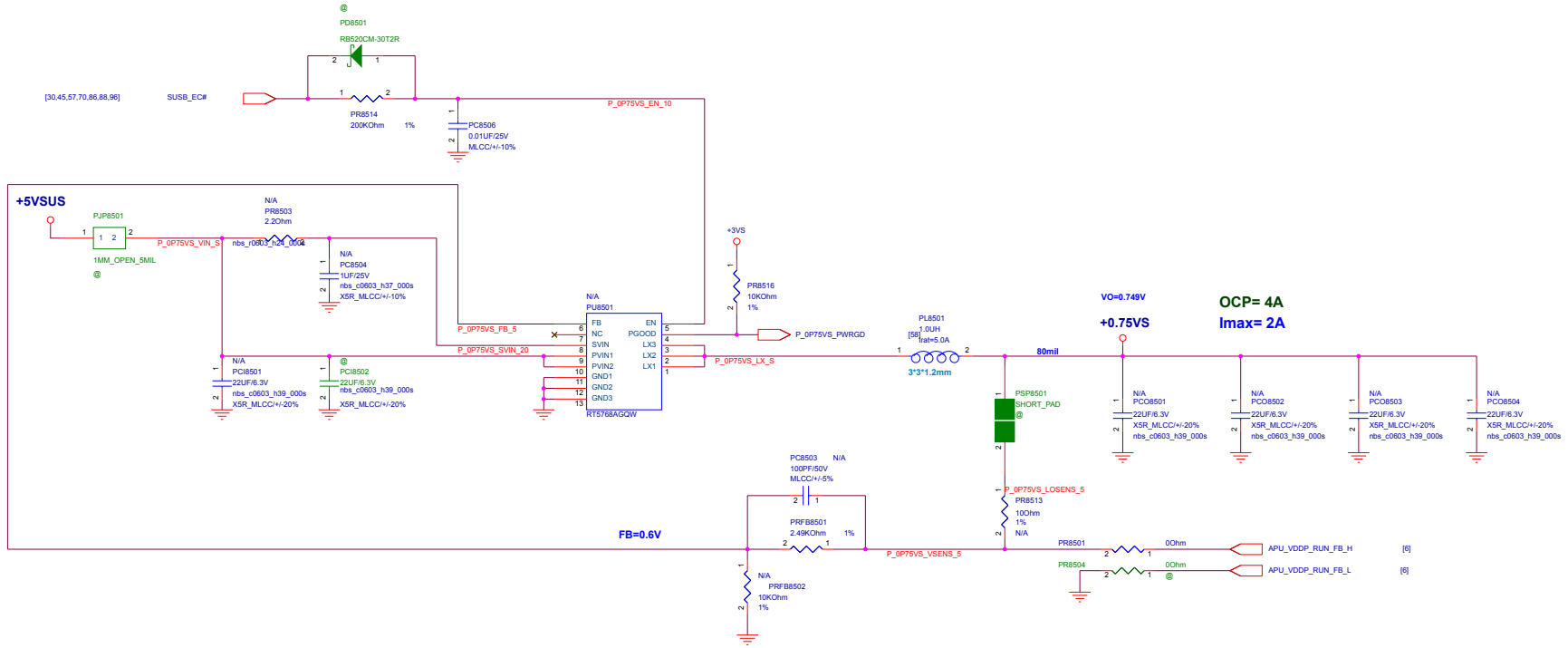
OCP = 10.5/12/13.5A
(Min/Typ/Max)

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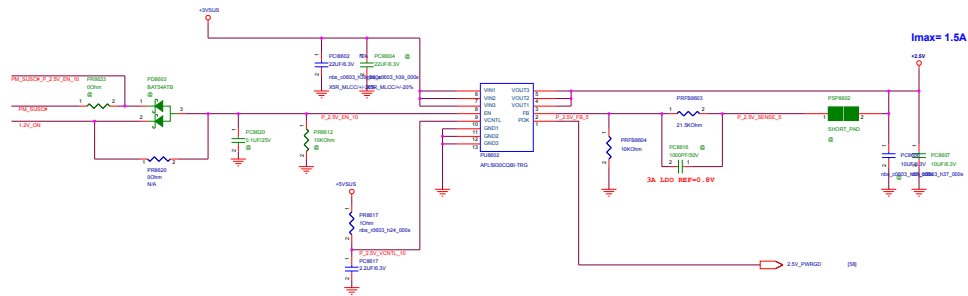
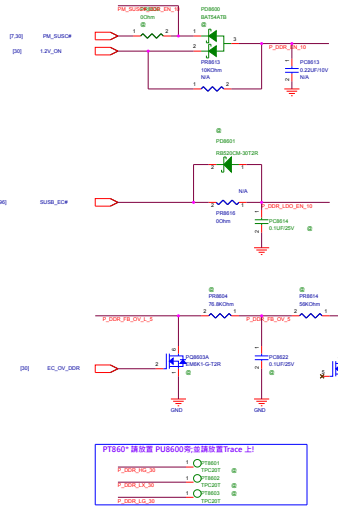
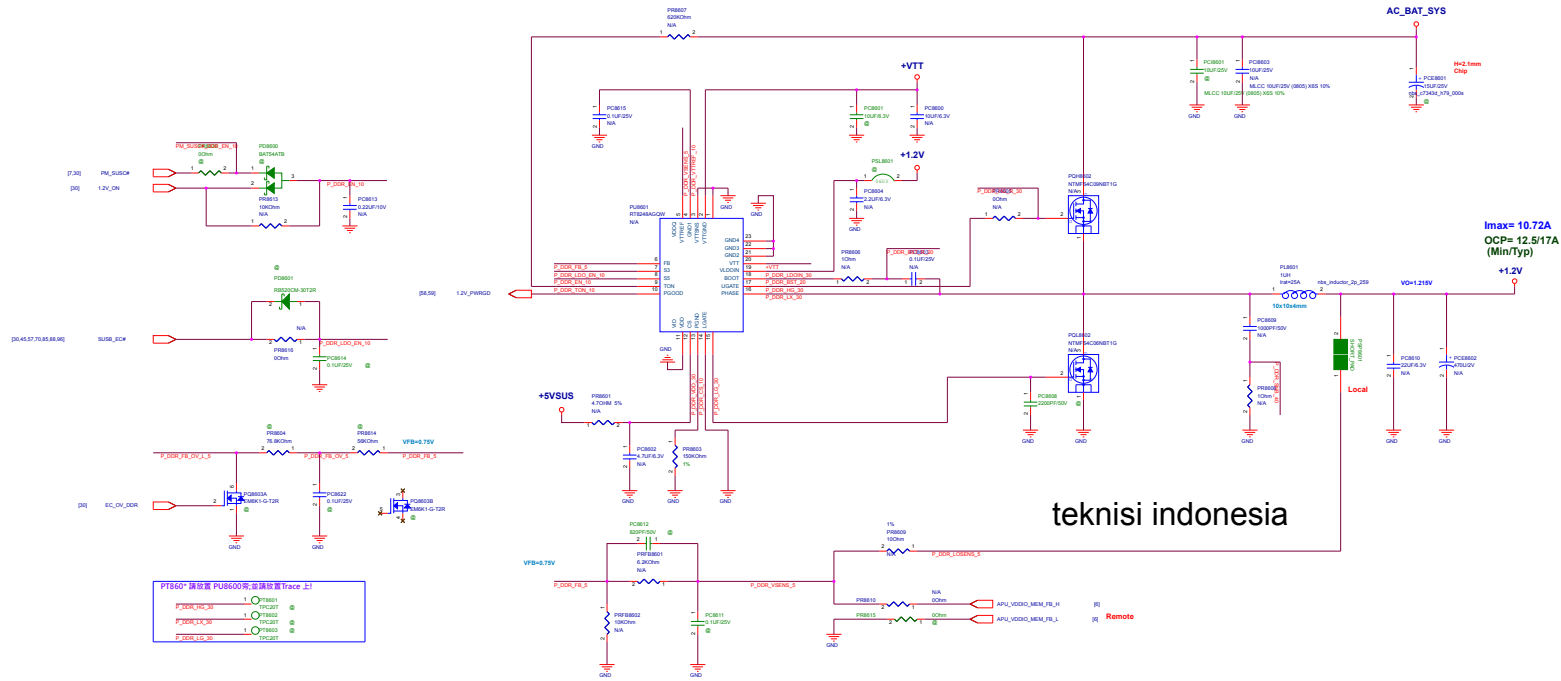


PT840* 請放置 PU8401旁;並請放置Trace 上!

<Variant Name>		Project Name	Rev
ASUS		GA401QM	R1.0
Title : PW_+1.8VSUS			
Size	Dept.: NB Power team	Engineer: Power RD	
A4	Date: Wednesday, December 02, 2020	Sheet 84 of 103	

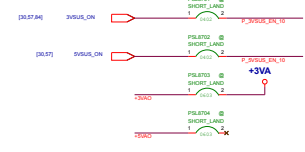
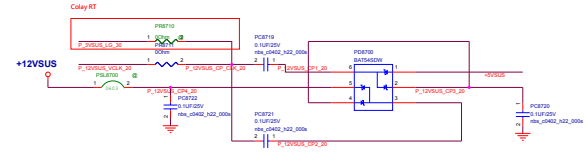
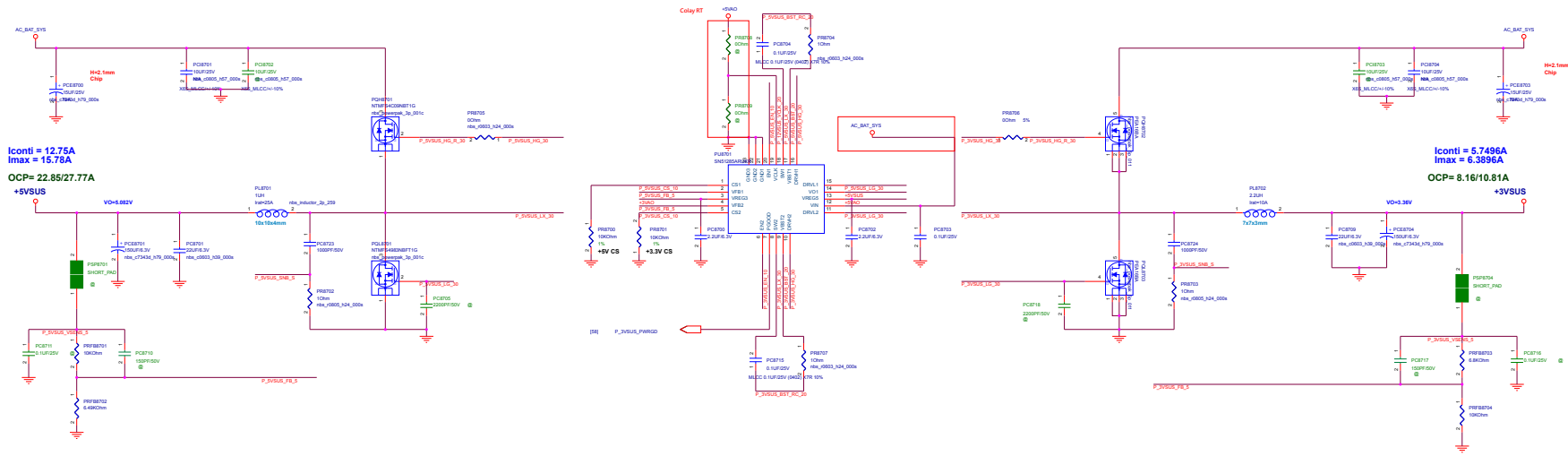


+1.2V / +VTT / +2.5V[For Memory]



ASUS		Project Name	REV
GA503QS			1.0
Title	PW_+1.2V/+VTT/+2.5V		
Size	Dept.: MS Power team	Engineer: Power RD	
Date	Thursday, December 10, 2020	Sheet	68 of 100

+3VA_DSW / +5VSUS [System Power]



Adaptor Mode (MVP6)

	S0	CS	S3	S3	S4	S5	S5 with USB Charger*
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	1	-	1
SUBS_ECH	1	-	1	-	0	-	0
SUBS_ECH	1	-	0	-	0	-	0

Battery Mode (MVP6)

	S0	CS	S3	S3	S4	S5	S5 with USB Charger*
PS_ON	1	-	-	1	0	0	0
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUBS_ECH	1	-	-	0	0	0	0
SUBS_ECH	1	-	-	0	0	0	0



ASUS GAS03QS

Title: PW_+3VSUS/+5VSUS

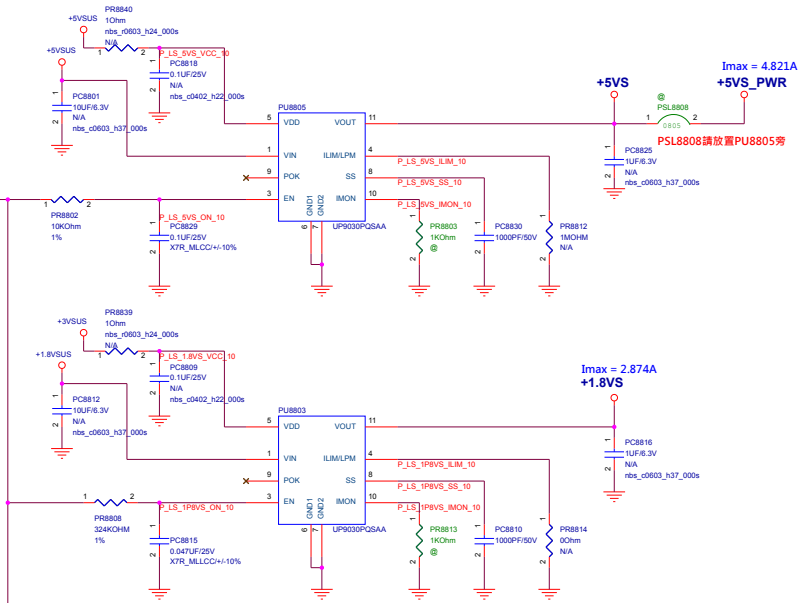
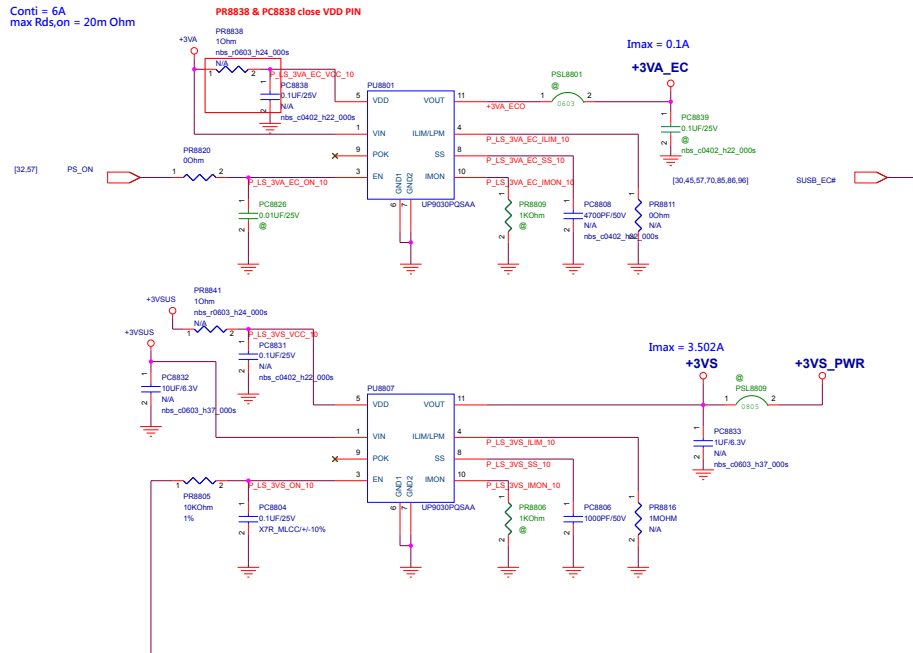
Dept: 168 Power team Engineer: Power RD

Date: Wednesday, December 22, 2021



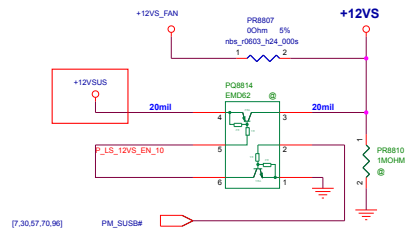
uP9030 ILIM/LPM Setting 對應表		
ILIM PIN	LPM	LIMIT Current
GND	Off	3A
1M to GND	Off	5A
Float/VDD	On	8A

Conti = 6A
max Rds, on = 20m Ohm

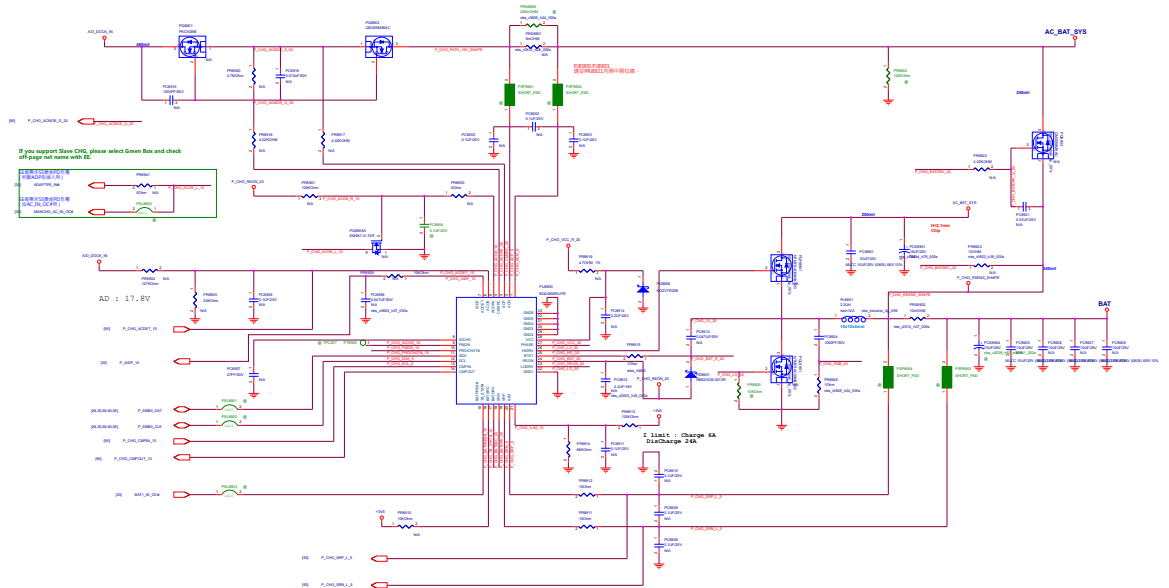


+12VS 的 Vin 對應 BOM 表

	+12VS_FAN	+12VSUS
PR8807	N/A	@
PR8810	@	N/A
PQ8814	@	N/A



PR8901	ADP1120W	ADP1130W	ADP1135W	ADP1135W
	5m	5m	5m	2m
	1000000000	1000000000	1000000000	1000000000

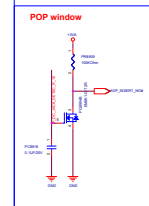
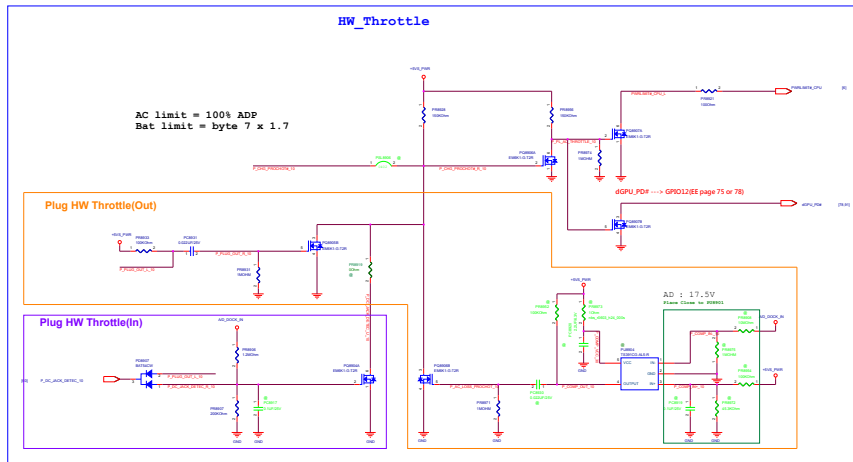


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Adaptor select total power = 90% ADP

Adaptor select			
VIN	VOUT	Power	Efficiency
PR8901	1.0m	5m	
PR8906	0.4V	30W	12.0%
	0.8V	40W	15.0%
	1.2V	45W	18.0%
	1.6V	45W	23.0%
	2.0V	75W	30.0%
	2.4V	90W	33.0%
	2.8V	120W	40.0%



ASUS	Power
TYPE :	PMU CHARGER
Model :	Engineer: Power RD

P90_PROTECTION

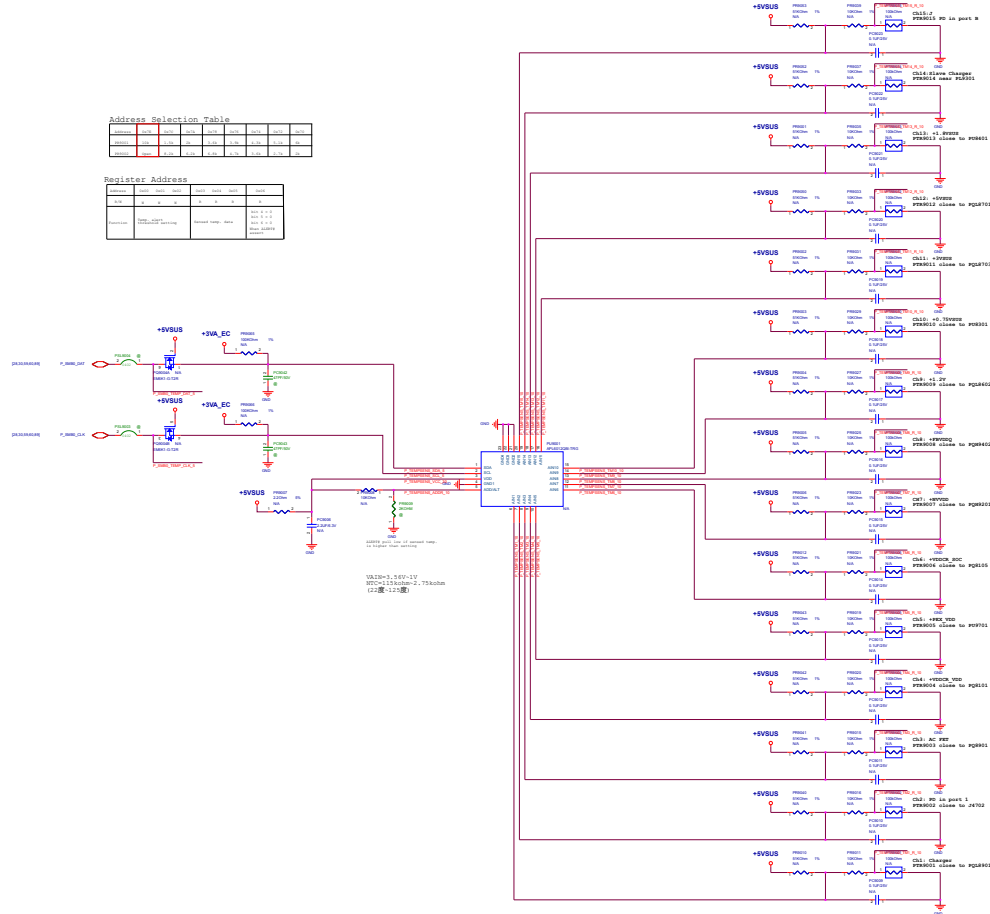
+0.7900 uem 0811 17

Address Selection Table

Chipset	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	

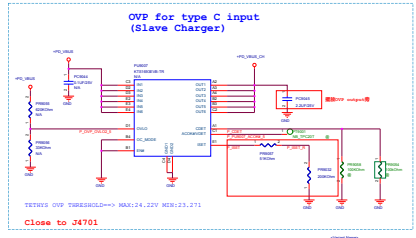
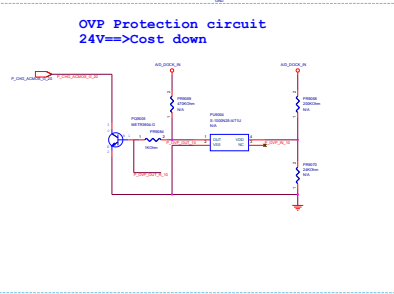
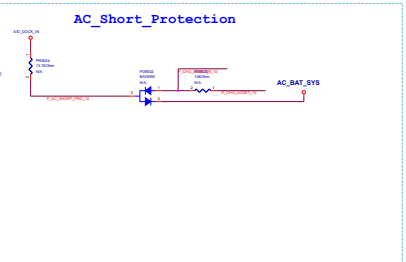
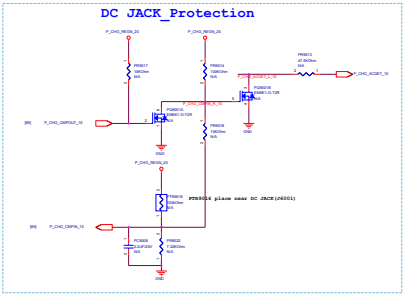
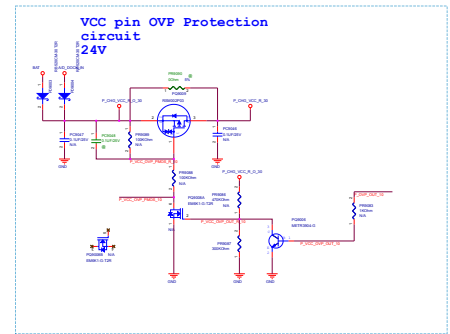
Register Address

Chipset	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	

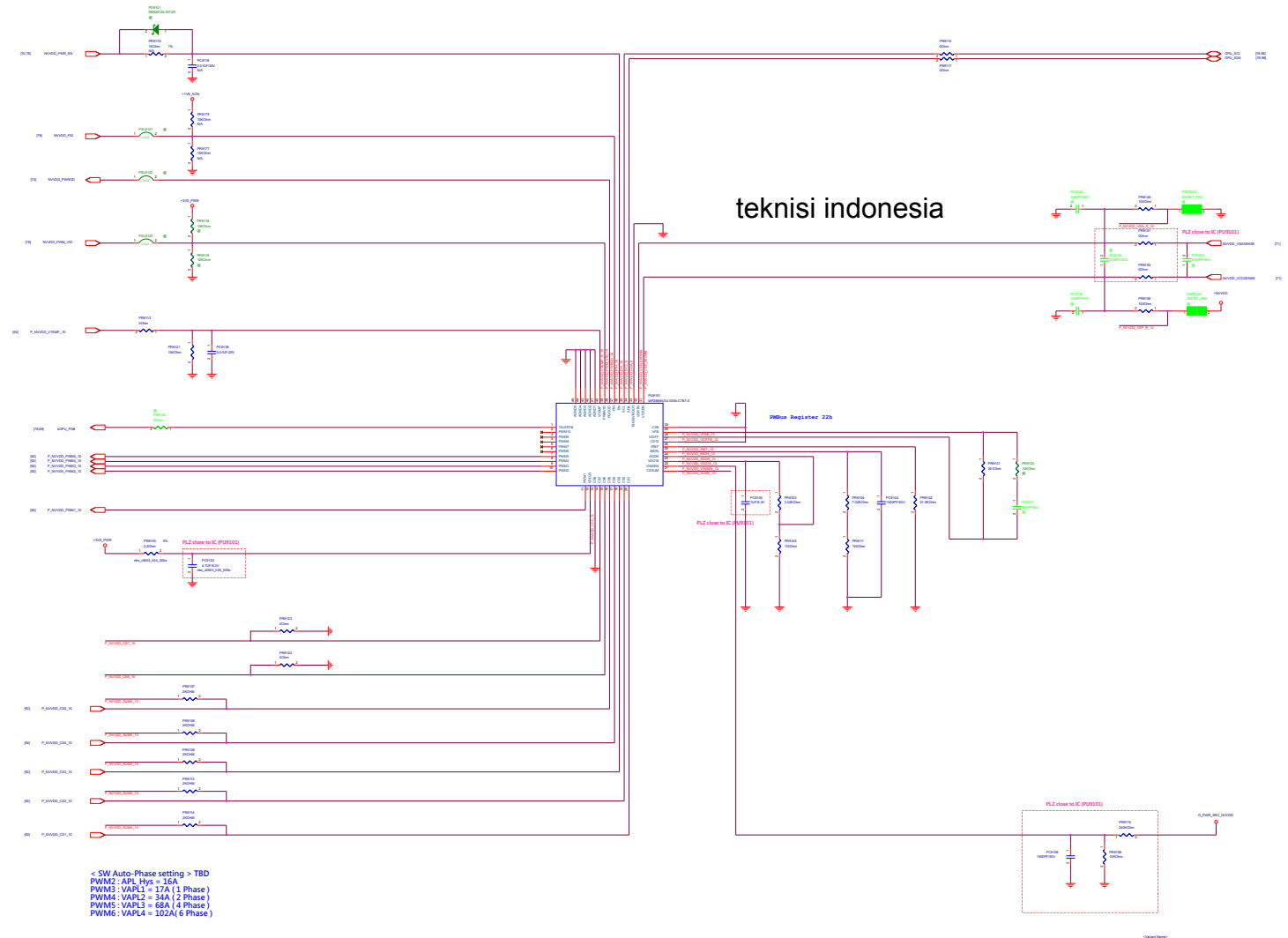


SWC	SWC	SWC
CB15	ZD in port B	ZD in port B
CB14	Slave Charger	Slave Charger
CB13	1.8VSW	1.8VSW
CB12	TVS	TVS
CB11	TVS_CSW	TVS_CSW
CB10	1.8VSW	PREL_WD
CB09	1.2V	1.2V
CB08	FWVDQ	FWVDQ
CB07	SWVDQ	SWVDQ
CB06	YOC	YOC
CB05	YOC	YOC
CB04	YOC	YOC
CB03	AC_PSE	AC_PSE
CB02	ZD in port A	ZD in port A
CB01	Charger Max	Charger Max

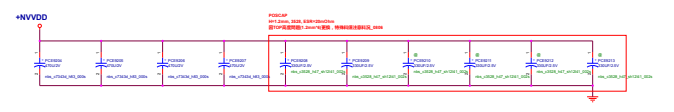
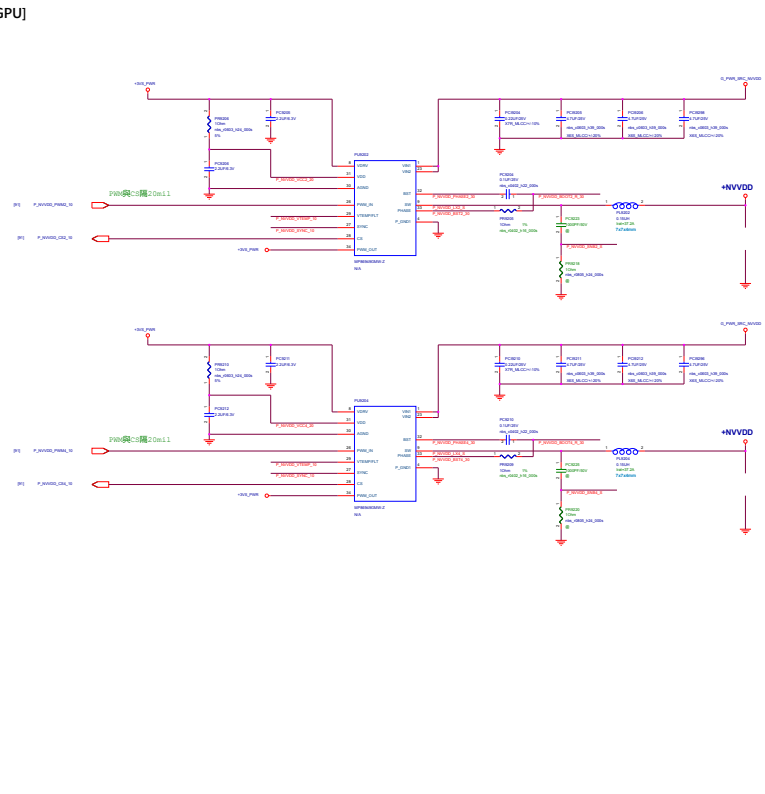
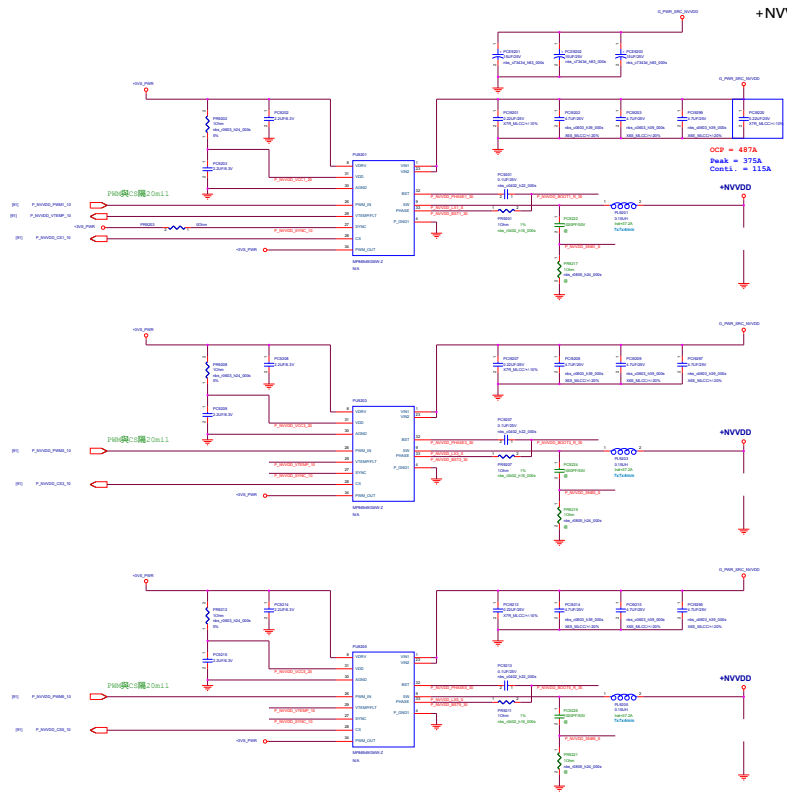
SWC	SWC
CB15	ZD in port B
CB14	Slave Charger
CB13	1.8VSW
CB12	TVS
CB11	TVS_CSW
CB10	1.8VSW
CB09	1.2V
CB08	FWVDQ
CB07	FWVDQ
CB06	YOC_CSD
CB05	YOC
CB04	YOC
CB03	AC_PSE
CB02	ZD in port A
CB01	Charger Max



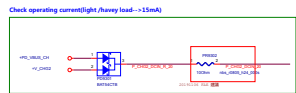
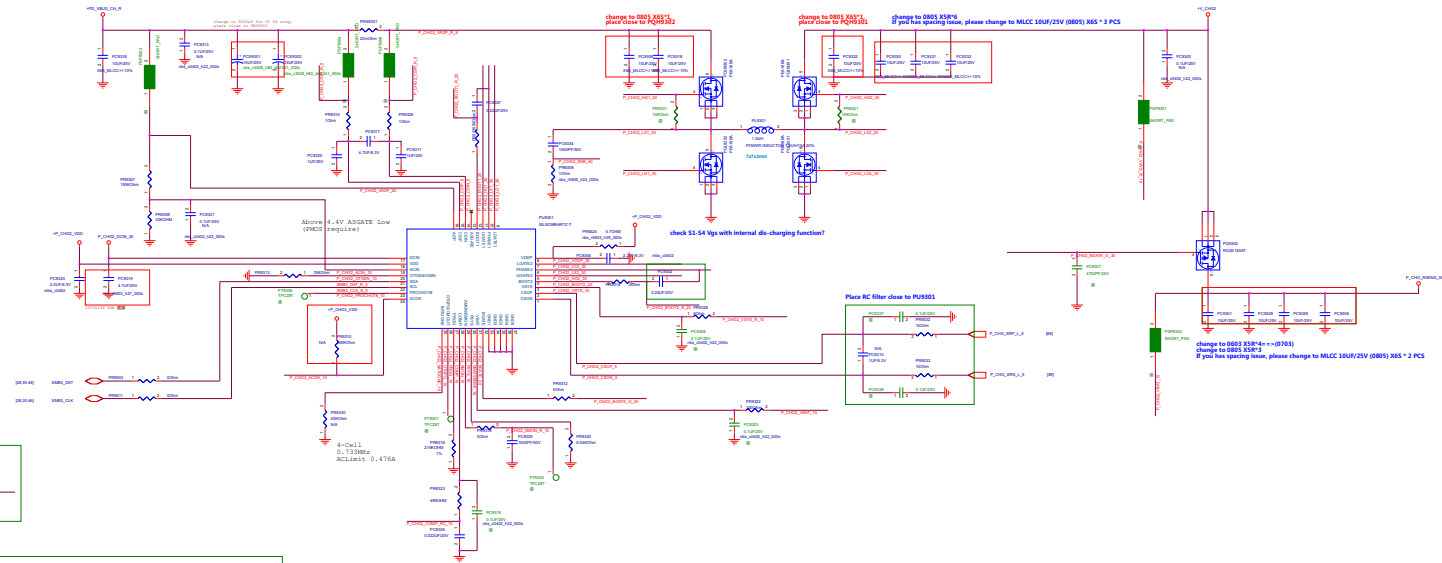
+NVVDD [For DGPU]



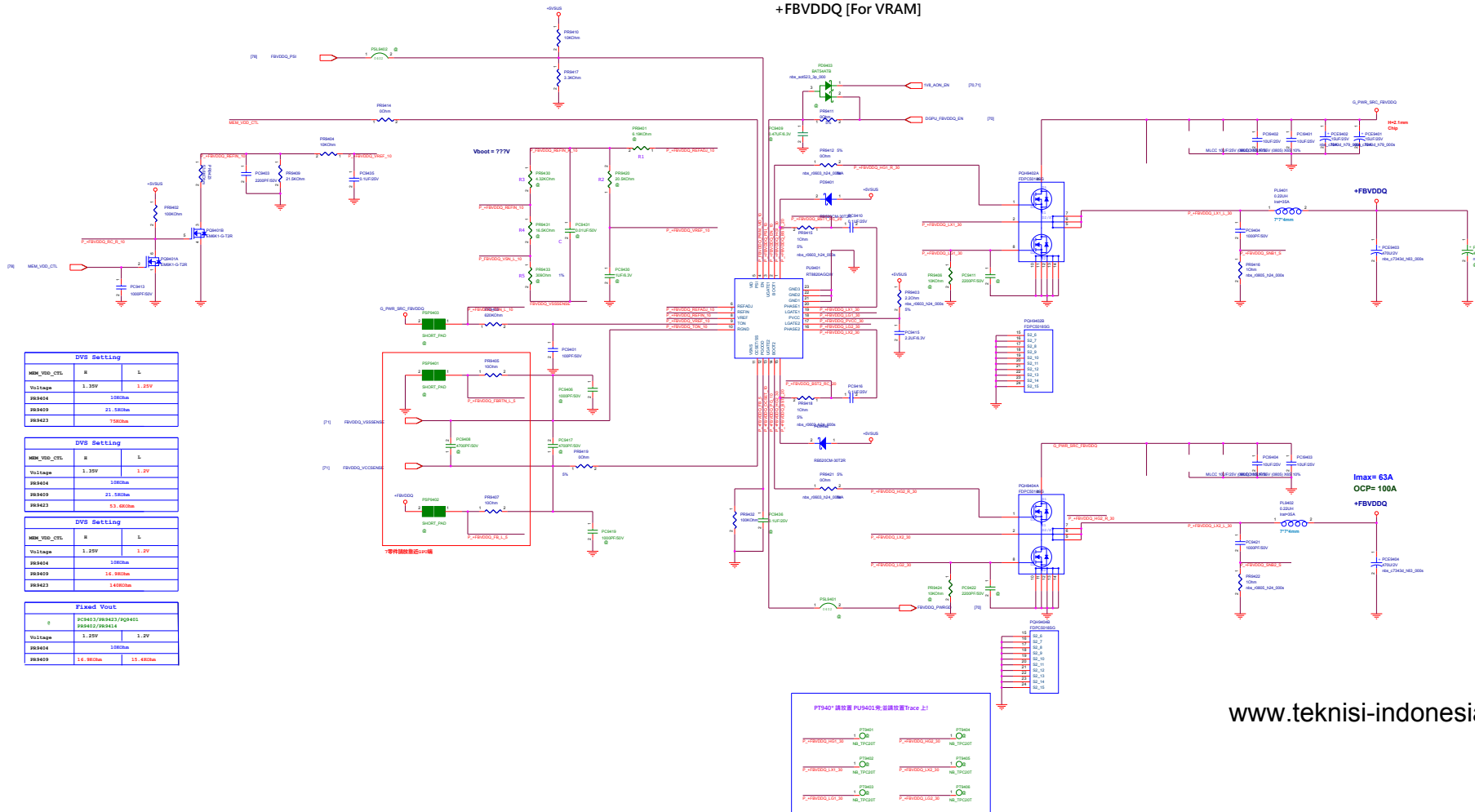
+NVVDD [For DGPU]



Charger ISL9238 (NVDC)



+FBVDDQ [For VRAM]



DVS Setting

MDM_VDD_CTL	H	L
Volstage	1.25V	1.25V
PS9404	10000uA	
PS9409	21.5000uA	
PS9423	75000uA	

DVS Setting

MDM_VDD_CTL	H	L
Volstage	1.25V	1.2V
PS9404	10000uA	
PS9409	21.5000uA	
PS9423	53.0000uA	

DVS Setting

MDM_VDD_CTL	H	L
Volstage	1.25V	1.2V
PS9404	10000uA	
PS9409	14.0000uA	
PS9423	1.0000uA	

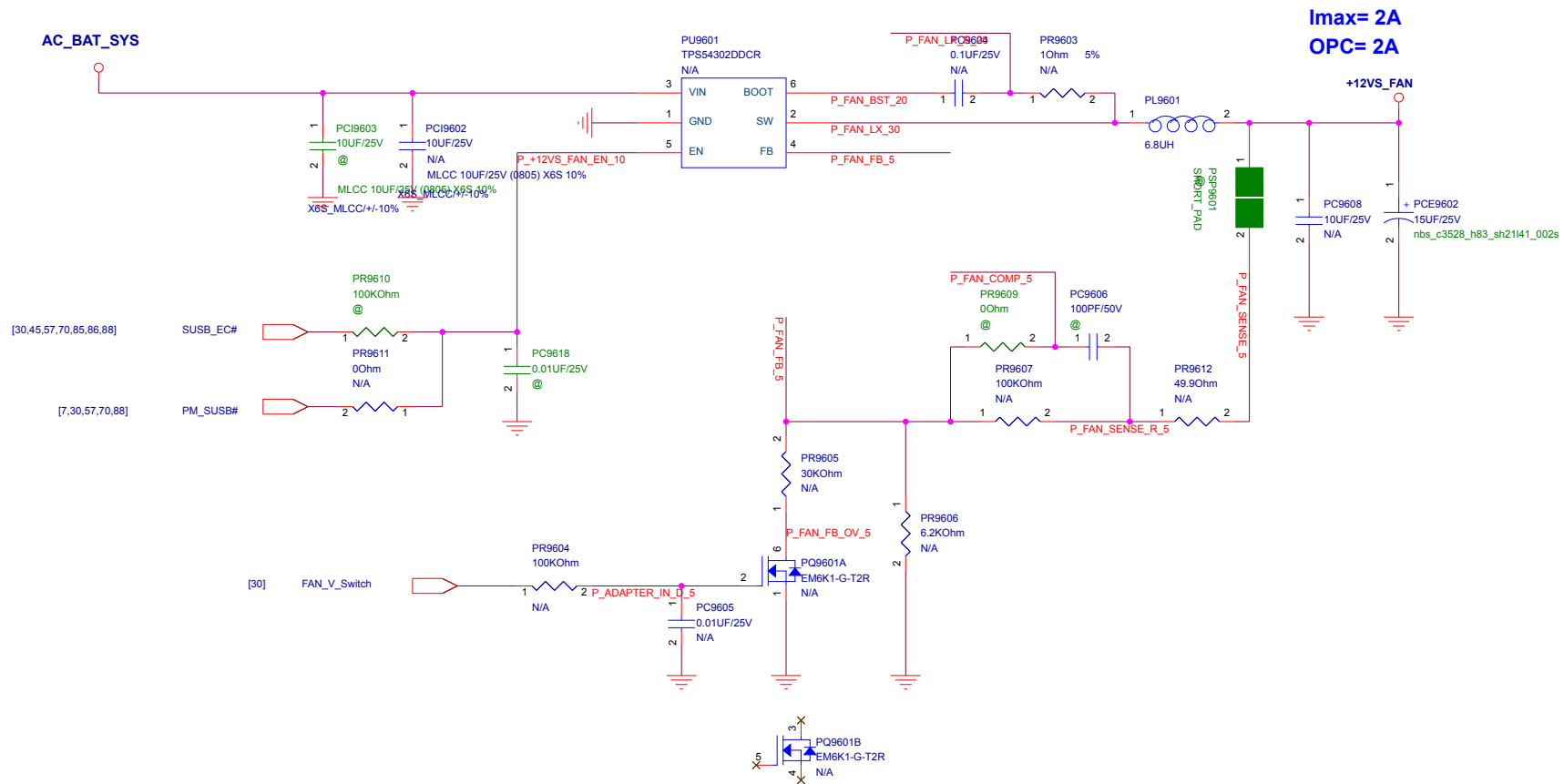
Fixed Volt

#	PC9423/PS9423/PS9401	PS9422/PS9414
Volstage	1.25V	1.2V
PS9404	10000uA	
PS9409	14.0000uA	15.4000uA

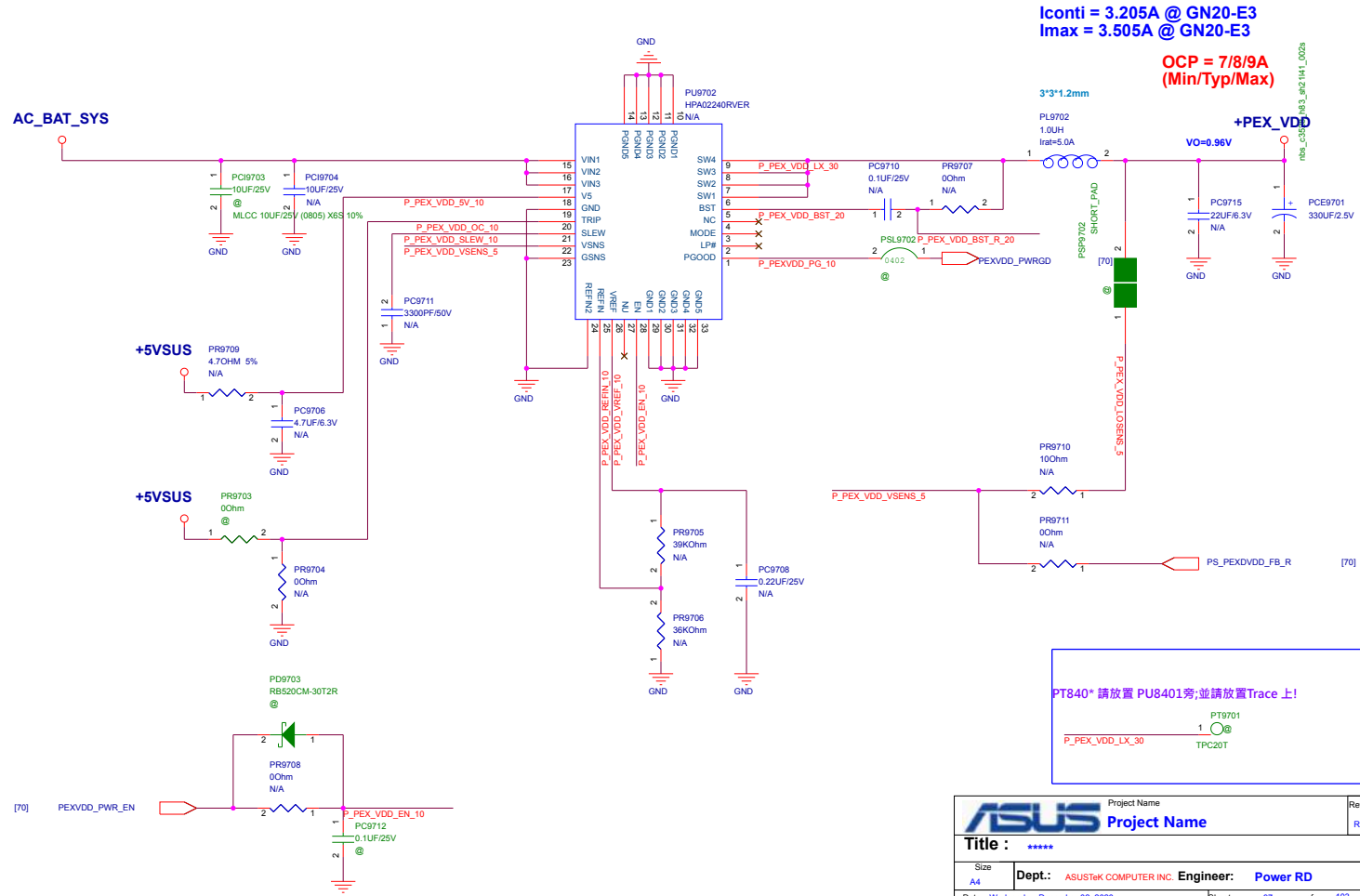


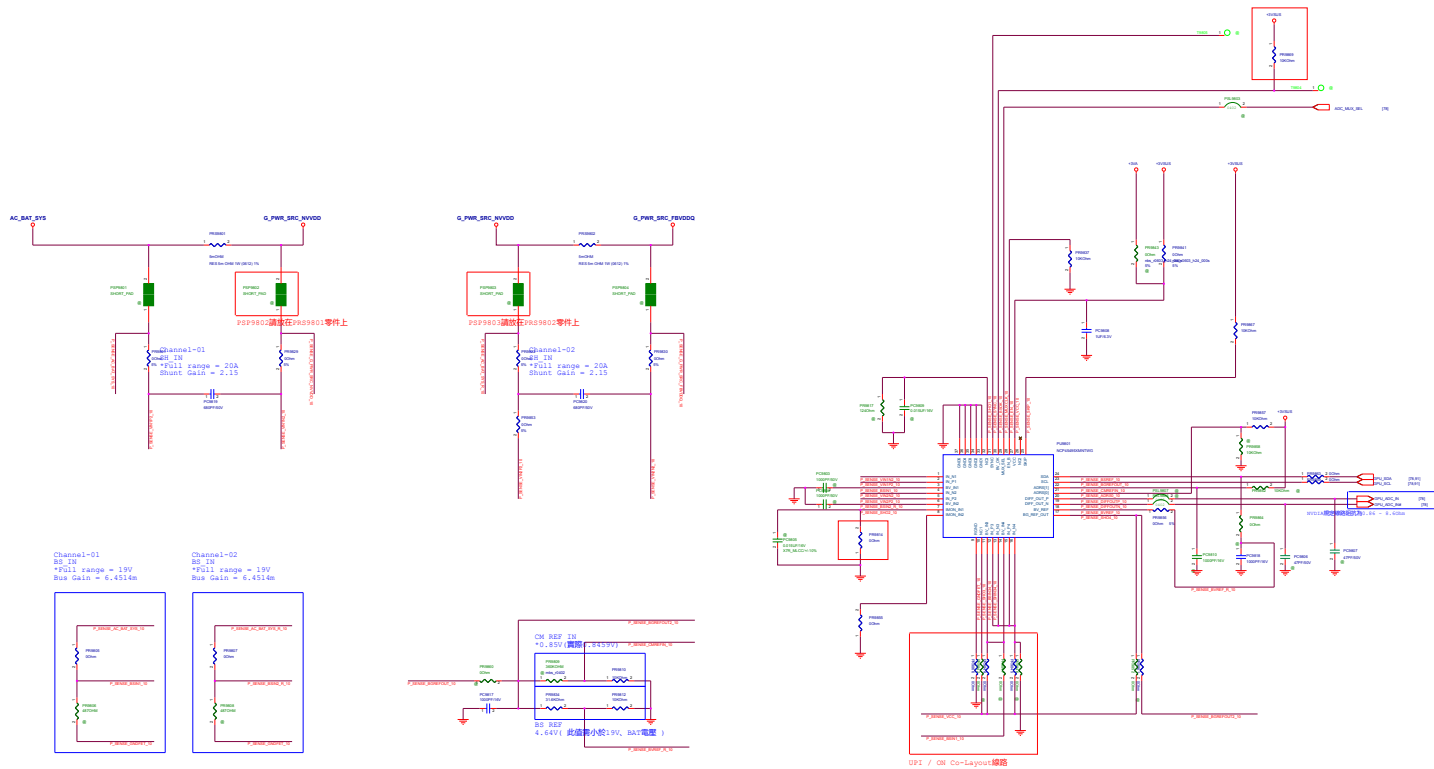
I_{max} = 63A
OCP = 100A

+12VS_FAN [For FAN]



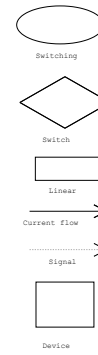
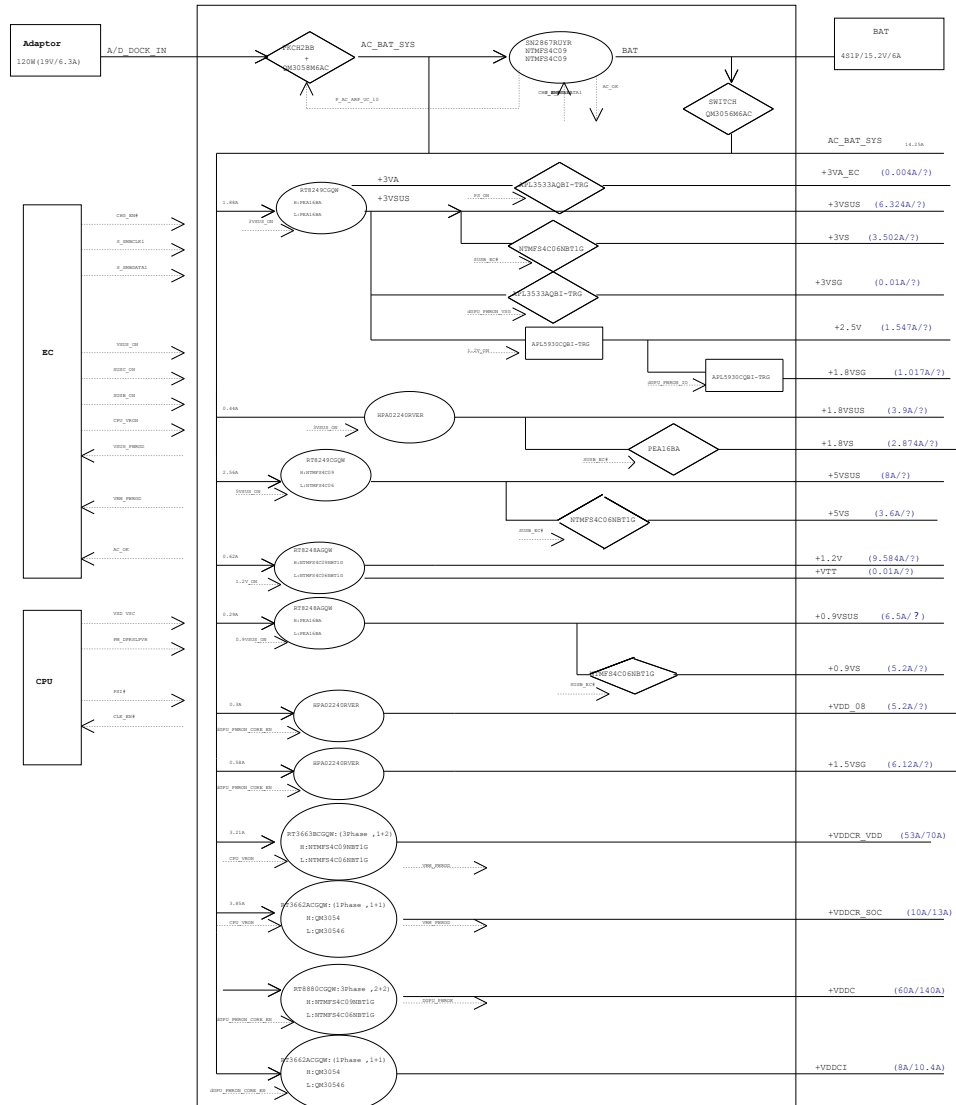
PEX_VDD [For GPU]





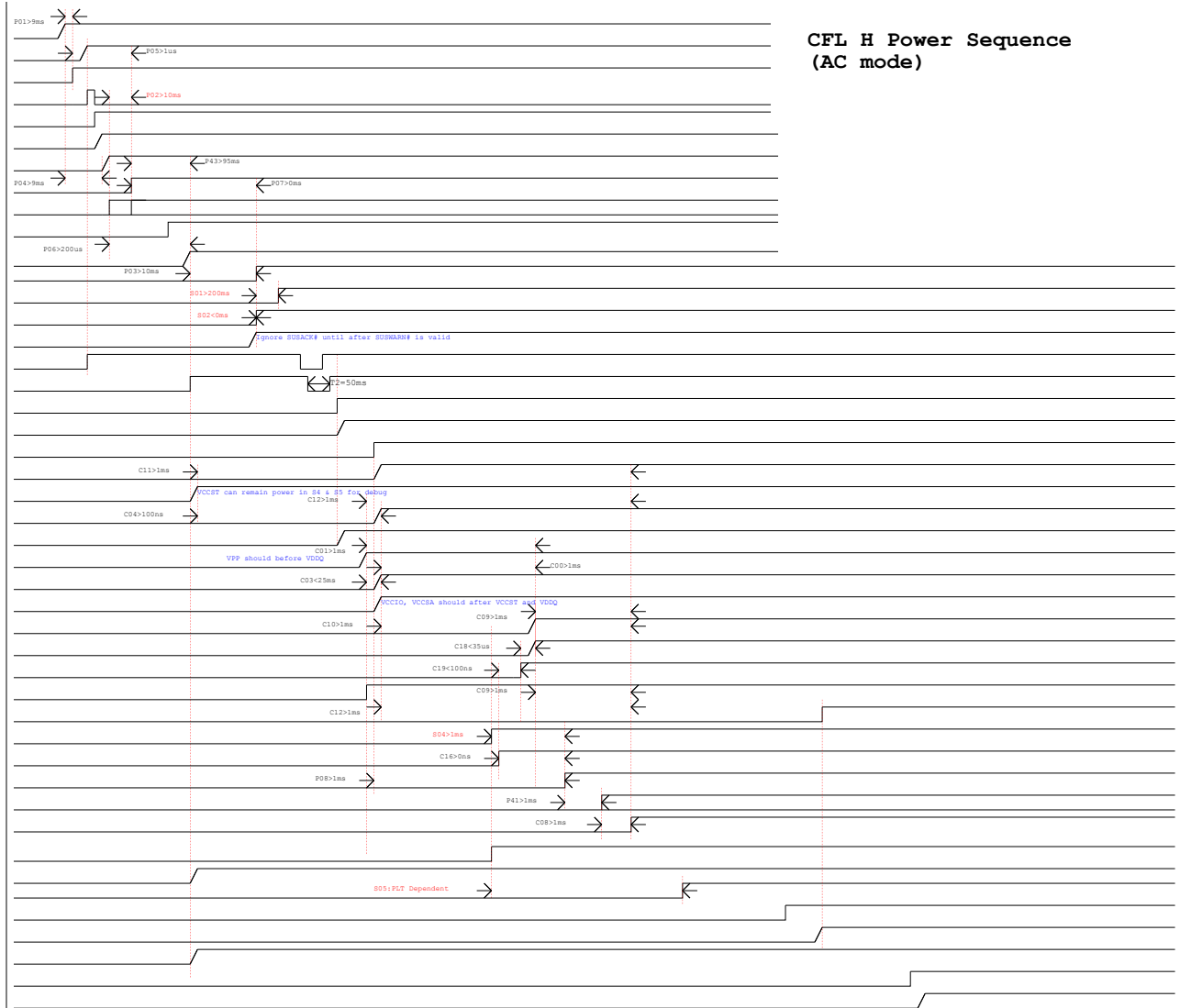
	PU9801	PR9805	PR9807	PC9803	PC9804	PC9805	PR9814	PR9855	PR9822
GN20	NCP44530MTWG 06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0	0	0	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
NI18P-G1	UPP905QGR1 06129-00110100	750KOhm 10G212750214010	750KOhm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.0150PF/16V 11G232115311360	3570Ohm 10G212357014010	0	49.30Ohm 10G212498914010
	PC9810	PR9860	PR9809	PR9810	PR9834	PR9863	PR9859	PC9809	PR9808
GN20	0	0	0	10K0Ohm 10G212100214010	31.6K0Ohm 10G212316214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0	0
NI18P-G1	1000PF/16V 11G232110211030	0 Ohm 10G212000004030	360K0Ohm 10G212364004010	680K0Ohm 10G212680314010	324K0Ohm 10G212324314010	0	0	0.0150PF/16V 11G232115311360	4870Ohm 10G212487014010
	PR9806	PR9861	PR9864	PR9857	PR9801	PR9853	PR9817	PR9844/PR9845/PR9846	PR9846/PR9847
GN20	0	0 Ohm 10G212000004030	0	10K0Ohm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0	0 Ohm 10G212000004030	0
NI18P-G1	4870Ohm 10G212487014010	0	0Ohm 10G212000004030	0	1000Ohm 10G212300014010	49.90Ohm 10G212498914010	3070Ohm 10G212357014010	0	0 Ohm 10G212000004030

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AC-IN Mode

- C:CPU
 - P:PCH
 - S:PLT
 - Power
 - Signal
- (+RTCBAT)+3VA_RTC
 - (AC_BAT_SYS)+3VA/+5VA
 - (+3VA_RTC)RTCRST#(PCH)
 - (Power)AC_IN_OC#(EC)
 - (EC)PS_ON(+3VA_EC)
 - (PS_ON)+3VA_EC(EC)
 - (3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
 - (EC)DPWRK_EC(PCH)
 - (+3VA_DSW)PM_BATLOW#(PCH)
 - (PCH)PM_SLP_SUS#(EC)
 - (VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
 - (EC)PM_RSMRST#_PCH(PCH)
 - (PCH)SUSWARN#(EC)
 - (EC)ME_AC_PRESENT_PCH(PCH)
 - (EC)PCH_SUSACK#(PCH)
 - (PWR Switch)PWR_SW#(EC)
 - (EC)PM_PWRBTN#(PCH)
 - (EC)SUSC_EC#(Power)
 - (SUSC_EC#)+12V/+5V/+3V
 - (EC)SUSB_EC#(Power)
 - (SUSB_EC#)+12VS/+5VS/+3VS
 - (SUSB_EC#)+1.0V_VCCST,VCCPLL
 - (SUSB_EC#)+VCCIO,(+12VS)+VCCSTG
 - (1.2V_ON)+2.5V(2.5V_PWRGD)
 - (1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
 - (+12VS)+VCCPLL_OC
 - (SUSB_EC#)+VCCIO(VCCIO_PWRGD)
 - (ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
 - (DDR_VTT_CTRL)+0.6V
 - (CPU)DDR_VTT_CTRL(Power)
 - (Power)1.2V_PWRGD(AND)
 - (Power)IMVP8_PWRGD
 - (AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
 - (ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
 - (EC)PM_PWROK_PCH(PCH)
 - (PCH)CLK_PCH_BCLK(CPU)
 - (PCH)H_CPUPWRGD(CPU)
 - (CPU)P_SVID_DATA_X2(Power)
 - (EC)PM_SYSPWROK_PCH(PCH)
 - (PCH)PLT_RST#(CPU/EC/Device)
 - (P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
 - (CPU)H_THERMTRIP#(PCH)
 - (PCH)DDR4_DRAMRST#(Memory)
 - +VCCGT



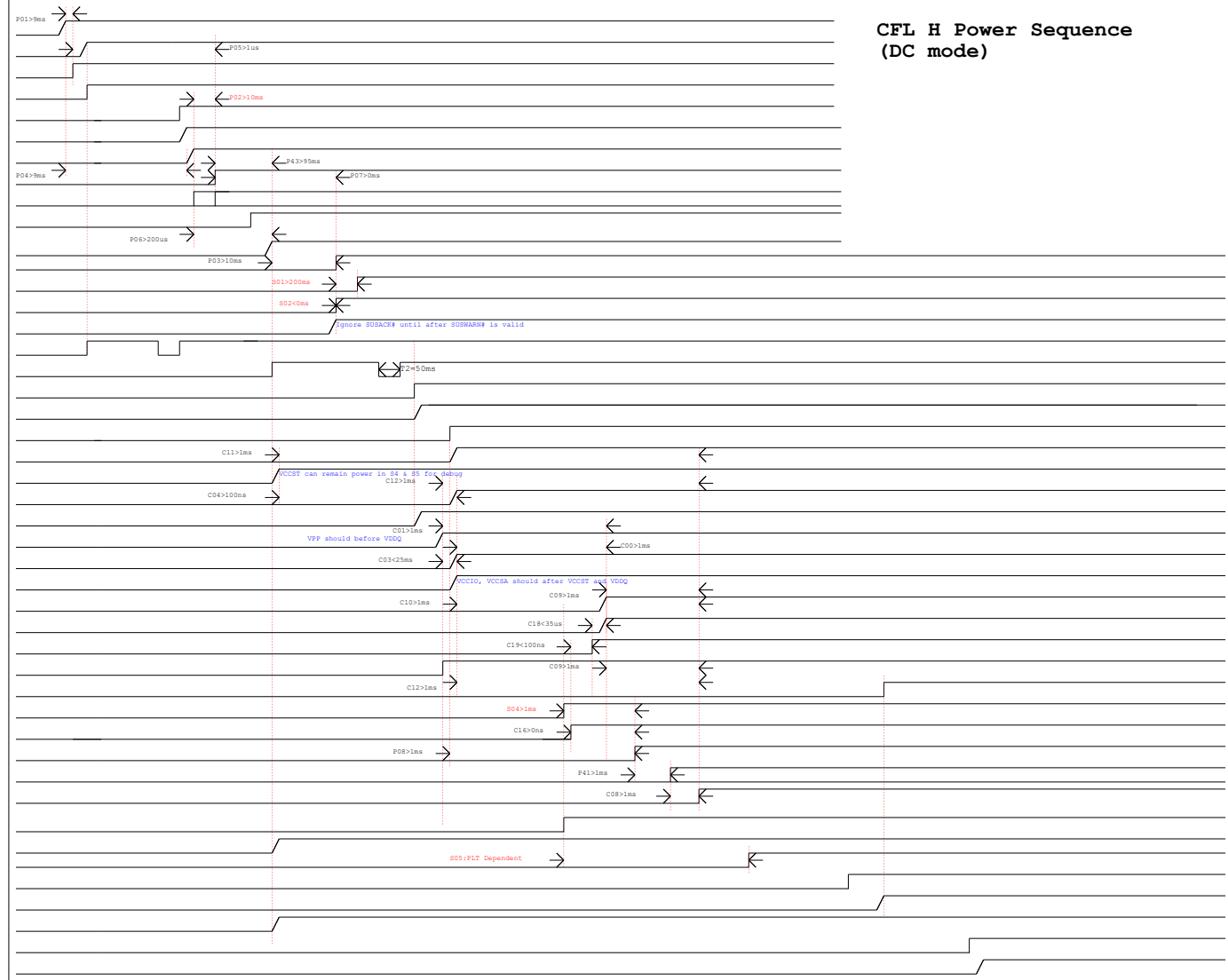
CFL H Power Sequence (AC mode)

ASUS		Project Name		Rev	
GA401QM				1.0	
Title : Power On Timing-AC mode					
Size	Dept.: ASUS/PC COMPUTER INC.		Engineer:	ROG EE	
Date:	Wednesday, December 02, 2020	Sheet	100	of 104	

DC-IN Mode

- C: CPU (+RTCBAT)+3VA_RTC
- P: PCH (AC_BAT_SYS)+3VA/+5VA
- S: PLT (+3VA_RTC)RTCRST# (PCH)
- Power (Power) AC_IN_OC# (EC)
- Signal (EC) PS_ON (+3VA_EC)
- (PS_ON)+3VA_EC (EC)
- (3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
- (EC) DFWROK_EC (PCH)
- (+3VA_DSW) PM_BATLOW# (PCH)
- (PCH) PM_SLP_SUS# (EC)
- (VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
- (EC) PM_RSMRST#_PCH (PCH)
- (PCH) SUSWARN# (EC)
- (EC) ME_AC_PRESENT_PCH (PCH)
- (EC) PCH_SUSACK# (PCH)
- (PWR Switch) PWR_SW# (EC)
- (EC) PM_PWRBTN# (PCH)
- (EC) SUSC_EC# (Power)
- (SUSC_EC#)+12V/+5V/+3V
- (EC) SUSB_EC# (Power)
- (SUSB_EC#)+12VS/+5VS/+3VS
- (VSUS_ON)+1.0V_VCCST, VCCPLL (VCCST_PWRGD)
- (+VCCIO)+VCCSTG
- (1.2V_ON)+2.5V (2.5V_PWRGD)
- (1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
- (+12VS)+VCCPLL_OC
- (SUSB_EC#)+VCCIO (VCCIO_PWRGD)
- (ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
- (DDR_VTT_CTRL)+0.6V
- (CPU) DDR_VTT_CTRL (Power)
- (Power) 1.2V_PWRGD (AND)
- (Power) IMVP8_PWRGD
- (AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
- (ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
- (EC) PM_PWRROK_PCH (PCH)
- (PCH) CLK_PCH_BCLK (CPU)
- (PCH) H_CPUPWRGD (CPU)
- (ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
- (CPU) P_SVID_DATA_X2 (Power)
- (EC) PM_SYSPWRROK_PCH (PCH)
- (PCH) PLT_RST# (CPU/EC/Device)
- (P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
- (CPU) H_THERMTRIP# (PCH)
- (PCH) DDR4_DRAMRST# (Memory)

+VCCGT



CFL H Power Sequence (DC mode)

ASUS		Project Name	Rev
GA401QM			1.0
Title : Power On Timing-DC mode			
Size	Dept:	ASUSTek COMPUTER INC.	Engineer: ROG EE
Created	Date:	Wednesday, December 02, 2020	Sheet 101 of 104