

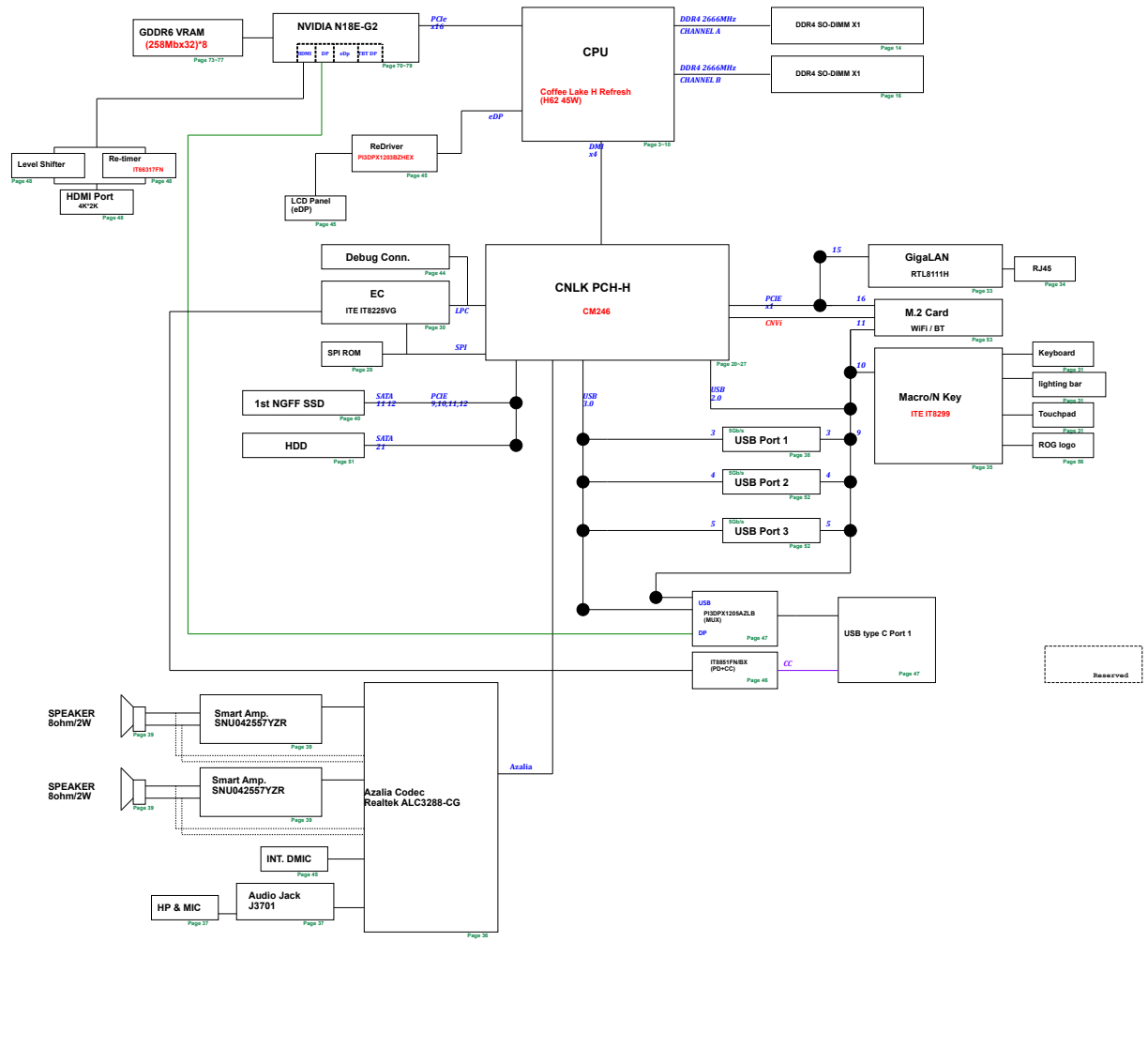
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002_System Setting
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005_CPU_GND
006_CPU_CFG,RSVD
007_
008_CPU_PWR
009_CPU_PWR
010_CPU_POWER_CAP
011_TBT_Alpine-Ridge
012_TBT_TPS65982&Type C
013_TBT_PWR
014_DIM_DDR4 SO-DIMM A(0)
015_DIM_DDR4 SO-DIMM B(0)
016_DIM_DDR4 SO-DIMM A(1)
017_DIM_DDR4 SO-DIMM B(1)
018_DIM_CA/DQ Voltage
020_PCH_HDA,SMB,SEC,RTC,JTAG
021_PCH_PCIE,SATA,USB2,MISC
022_PCH_CLK,LPC,USB3
023_PCH_LVDS,eDP,DP
024_PCH_SPI,CNV
025_PCH_GPIO
026_PCH_POWER,GND
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028_PCH_SPI ROM,OTH
029_TEST_POINT
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031_KBC_KB & TP
032_RST_Reset Circuit
033_LAN_RTL8111H-CG
034_LAN_RJ45_CON
035_MacroN_KEY_IT8291
036_AUD_ALC295
037_AUD_EXT Jack
039_AUD_INT SPK
040_NGFF_SSD_PCIE_CON
041_NGFF_SSD_PCIE_CON_3
042_CR_GL3215
043_
044_BUG_LPC
045_eDP_CON & Tobii IS4_CON
046_
047_Display Port
048_HDMI
049_
050_FAN_Thermal Sensor & Fan
051_HDD
052_USB3.0 Port
053_NGFF_WLAN & BT & XBBOX
055_USB3.0 Port
056_LED & Switch
057_DSG_Discharge
058_Power Protect
059_EMI
060_DC & BAT IN
063_>>>Power Button_JO_BD
064_>>>LED_IO_BD
065_ME_W2B conn. & NUT
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067_
068_
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070_GPU_PCIE I/F
071_GPU_POWER
072_GPU_FRAME BUFFER
073_VRAM-CHANNEL A
074_VRAM-CHANNEL B
075_VRAM-CHANNEL C
076_VRAM-CHANNEL D
077_VRAM_CAP

080_PW_COFFEE LAKE (1)
081_PW_COFFEE LAKE (2)
082_PW_VCCIO
083_PW_+1.05VSUS
084_PW_+1.8VSUS
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+SVSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD (1)
092_PW_+NVVDD (2)
093_PW_+NVVDD5
094_PW_+FBVDQ
096_PW_+12VS_FAN
097_PW_PEX_VDD
098_PW_IPC

100_Power On Timing-AC mode
101_Power On Timing-DC mode

G531GW Block Diagram

Coffee Lake H Refresh Platform



Power

- +VCCORE/HVCCSA/HVCCGT (Page 85.41)
- +VCCIO (Page 82)
- +1.05VSUS (Page 83)
- +1.8VSUS (Page 84)
- 1.2V/+VTT/2.5V (Page 85)
- +3VADSW/+SVSUS (Page 87)
- Load Switch (Page 88)
- Charger (Page 89)
- Protection (Page 90)
- VGA CORE (+NVVDD) (Page 91.32)
- +NVVDD5 (Page 93)
- +FBVDQ (+1.55V) (Page 94)
- +12VS (Page 96)
- IPC (Page 98)

	Default	Use As	Signal Name	EXT PWRD	Power
GP00	A11	GP0	IO0_020		
GP01	00	GP0	IO0_020A	P0 100 (18)	+150, 30
GP02	00	GP0	IO0_020B_020C	P0 100 (18)	+150, 30
GP03	A11	GP0	PA0_000		
GP04	0	GP0	SC_000A		
GP05	A11	GP0	FAN0_000		
GP06	A11	GP0	PG_040_000		
GP07	0	GP0	IG_000A		
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	Default	Use As	Signal Name	EXT PWRD	Power
GP08	A11	GP1	AC_10_00A	P0 100B	+150
GP09	0	GP1	LT0_000	P0 100B	+150
GP10	0	GP1	IO0_020A_020B		
GP11	A11	GP0	SC_000A/FAN0_000A	P0 100B	+150
GP12	0	GP0	IG_000_000		
GP13	0	GP1	IO0A_000A	P0 10A	+150
GP14	0	GP0	SC_000A	P0 10B	+150
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	Default	Use As	Signal Name	EXT PWRD	Power
GP15	0	GP0	IO0_020A	P0 10 (18)	+150, 30
GP16	A11	IO000A	IO00_000A	P0 1 (8)	+150, 30
GP17	A11	IO000A	IO00_000B	P0 1 (8)	+150, 30

Object	Default	Use As	Signal Name	EXT PUPP	Power
0001	1	0001	SC_000101_0001_0001	00	10000
0002	0	0001	SC_000101_0001_0002	00	10000
0003	0	0001	SC_000101_0001_0003	00	10000
0004	0	0001	SC_000101_0001_0004	00	10000
0005	0	0001	SC_000101_0001_0005	00	10000
0006	0	0001	SC_000101_0001_0006	00	10000
0007	0	0001	SC_000101_0001_0007	00	10000
0008	0	0001	SC_000101_0001_0008	00	10000
0009	0	0001	SC_000101_0001_0009	00	10000
0010	0	0001	SC_000101_0001_0010	00	10000
0011	0	0001	SC_000101_0001_0011	00	10000
0012	0	0001	SC_000101_0001_0012	00	10000
0013	0	0001	SC_000101_0001_0013	00	10000
0014	0	0001	SC_000101_0001_0014	00	10000
0015	0	0001	SC_000101_0001_0015	00	10000
0016	0	0001	SC_000101_0001_0016	00	10000
0017	0	0001	SC_000101_0001_0017	00	10000
0018	0	0001	SC_000101_0001_0018	00	10000
0019	0	0001	SC_000101_0001_0019	00	10000
0020	0	0001	SC_000101_0001_0020	00	10000
0021	0	0001	SC_000101_0001_0021	00	10000
0022	0	0001	SC_000101_0001_0022	00	10000
0023	0	0001	SC_000101_0001_0023	00	10000
0024	0	0001	SC_000101_0001_0024	00	10000
0025	0	0001	SC_000101_0001_0025	00	10000
0026	0	0001	SC_000101_0001_0026	00	10000
0027	0	0001	SC_000101_0001_0027	00	10000
0028	0	0001	SC_000101_0001_0028	00	10000
0029	0	0001	SC_000101_0001_0029	00	10000
0030	0	0001	SC_000101_0001_0030	00	10000
0031	0	0001	SC_000101_0001_0031	00	10000
0032	0	0001	SC_000101_0001_0032	00	10000
0033	0	0001	SC_000101_0001_0033	00	10000
0034	0	0001	SC_000101_0001_0034	00	10000
0035	0	0001	SC_000101_0001_0035	00	10000
0036	0	0001	SC_000101_0001_0036	00	10000
0037	0	0001	SC_000101_0001_0037	00	10000
0038	0	0001	SC_000101_0001_0038	00	10000
0039	0	0001	SC_000101_0001_0039	00	10000
0040	0	0001	SC_000101_0001_0040	00	10000
0041	0	0001	SC_000101_0001_0041	00	10000
0042	0	0001	SC_000101_0001_0042	00	10000
0043	0	0001	SC_000101_0001_0043	00	10000
0044	0	0001	SC_000101_0001_0044	00	10000
0045	0	0001	SC_000101_0001_0045	00	10000
0046	0	0001	SC_000101_0001_0046	00	10000
0047	0	0001	SC_000101_0001_0047	00	10000
0048	0	0001	SC_000101_0001_0048	00	10000
0049	0	0001	SC_000101_0001_0049	00	10000
0050	0	0001	SC_000101_0001_0050	00	10000
0051	0	0001	SC_000101_0001_0051	00	10000
0052	0	0001	SC_000101_0001_0052	00	10000
0053	0	0001	SC_000101_0001_0053	00	10000
0054	0	0001	SC_000101_0001_0054	00	10000
0055	0	0001	SC_000101_0001_0055	00	10000
0056	0	0001	SC_000101_0001_0056	00	10000
0057	0	0001	SC_000101_0001_0057	00	10000
0058	0	0001	SC_000101_0001_0058	00	10000
0059	0	0001	SC_000101_0001_0059	00	10000
0060	0	0001	SC_000101_0001_0060	00	10000
0061	0	0001	SC_000101_0001_0061	00	10000
0062	0	0001	SC_000101_0001_0062	00	10000
0063	0	0001	SC_000101_0001_0063	00	10000
0064	0	0001	SC_000101_0001_0064	00	10000
0065	0	0001	SC_000101_0001_0065	00	10000
0066	0	0001	SC_000101_0001_0066	00	10000
0067	0	0001	SC_000101_0001_0067	00	10000
0068	0	0001	SC_000101_0001_0068	00	10000
0069	0	0001	SC_000101_0001_0069	00	10000
0070	0	0001	SC_000101_0001_0070	00	10000
0071	0	0001	SC_000101_0001_0071	00	10000
0072	0	0001	SC_000101_0001_0072	00	10000
0073	0	0001	SC_000101_0001_0073	00	10000
0074	0	0001	SC_000101_0001_0074	00	10000
0075	0	0001	SC_000101_0001_0075	00	10000
0076	0	0001	SC_000101_0001_0076	00	10000
0077	0	0001	SC_000101_0001_0077	00	10000
0078	0	0001	SC_000101_0001_0078	00	10000
0079	0	0001	SC_000101_0001_0079	00	10000
0080	0	0001	SC_000101_0001_0080	00	10000
0081	0	0001	SC_000101_0001_0081	00	10000
0082	0	0001	SC_000101_0001_0082	00	10000
0083	0	0001	SC_000101_0001_0083	00	10000
0084	0	0001	SC_000101_0001_0084	00	10000
0085	0	0001	SC_000101_0001_0085	00	10000
0086	0	0001	SC_000101_0001_0086	00	10000
0087	0	0001	SC_000101_0001_0087	00	10000
0088	0	0001	SC_000101_0001_0088	00	10000
0089	0	0001	SC_000101_0001_0089	00	10000
0090	0	0001	SC_000101_0001_0090	00	10000
0091	0	0001	SC_000101_0001_0091	00	10000
0092	0	0001	SC_000101_0001_0092	00	10000
0093	0	0001	SC_000101_0001_0093	00	10000
0094	0	0001	SC_000101_0001_0094	00	10000
0095	0	0001	SC_000101_0001_0095	00	10000
0096	0	0001	SC_000101_0001_0096	00	10000
0097	0	0001	SC_000101_0001_0097	00	10000
0098	0	0001	SC_000101_0001_0098	00	10000
0099	0	0001	SC_000101_0001_0099	00	10000
0100	0	0001	SC_000101_0001_0100	00	10000
0101	0	0001	SC_000101_0001_0101	00	10000
0102	0	0001	SC_000101_0001_0102	00	10000
0103	0	0001	SC_000101_0001_0103	00	10000
0104	0	0001	SC_000101_0001_0104	00	10000
0105	0	0001	SC_000101_0001_0105	00	10000
0106	0	0001	SC_000101_0001_0106	00	10000
0107	0	0001	SC_000101_0001_0107	00	10000
0108	0	0001	SC_000101_0001_0108	00	10000
0109	0	0001	SC_000101_0001_0109	00	10000
0110	0	0001	SC_000101_0001_0110	00	10000
0111	0	0001	SC_000101_0001_0111	00	10000
0112	0	0001	SC_000101_0001_0112	00	10000
0113	0	0001	SC_000101_0001_0113	00	10000
0114	0	0001	SC_000101_0001_0114	00	10000
0115	0	0001	SC_000101_0001_0115	00	10000
0116	0	0001	SC_000101_0001_0116	00	10000
0117	0	0001	SC_000101_0001_0117	00	10000
0118	0	0001	SC_000101_0001_0118	00	10000
0119	0	0001	SC_000101_0001_0119	00	10000
0120	0	0001	SC_000101_0001_0120	00	10000
0121	0	0001	SC_000101_0001_0121	00	10000
0122	0	0001	SC_000101_0001_0122	00	10000
0123	0	0001	SC_000101_0001_0123	00	10000
0124	0	0001	SC_000101_0001_0124	00	10000
0125	0	0001	SC_000101_0001_0125	00	10000
0126	0	0001	SC_000101_0001_0126	00	10000
0127	0	0001	SC_000101_0001_0127	00	10000
0128	0	0001	SC_000101_0001_0128	00	10000
0129	0	0001	SC_000101_0001_0129	00	10000
0130	0	0001	SC_000101_0001_0130	00	10000
0131	0	0001	SC_000101_0001_0131	00	10000
0132	0	0001	SC_000101_0001_0132	00	10000
0133	0	0001	SC_000101_0001_0133	00	10000
0134	0	0001	SC_000101_0001_0134	00	10000
0135	0	0001	SC_000101_0001_0135	00	10000
0136	0	0001	SC_000101_0001_0136	00	10000
0137	0	0001	SC_000101_0001_0137	00	10000
0138	0	0001	SC_000101_0001_0138	00	10000
0139	0	0001	SC_000101_0001_0139	00	10000
0140	0	0001	SC_000101_0001_0140	00	10000
0141	0	0001	SC_000101_0001_0141	00	10000
0142	0	0001	SC_000101_0001_0142	00	10000
0143	0	0001	SC_000101_0001_0143	00	10000
0144	0	0001	SC_000101_0001_0144	00	10000
0145	0	0001	SC_000101_0001_0145	00	10000
0146	0	0001	SC_000101_0001_0146	00	10000
0147	0	0001	SC_000101_0001_0147	00	10000
0148	0	0001	SC_000101_0001_0148	00	10000
0149	0	0001	SC_000101_0001_0149	00	10000
0150	0	0001	SC_000101_0001_0150	00	10000
0151	0	0001	SC_000101_0001_0151	00	10000
0152	0	0001	SC_000101_0001_0152	00	10000
0153	0	0001	SC_000101_0001_0153	00	10000
0154	0	0001	SC_000101_0001_0154	00	10000
0155	0	0001	SC_000101_0001_0155	00	10000
0156	0	0001	SC_000101_0001_0156	00	10000
0157	0	0001	SC_000101_0001_0157	00	10000
0158	0	0001	SC_000101_0001_0158	00	10000
0159	0	0001	SC_000101_0001_0159	00	10000
0160	0	0001	SC_000101_0001_0160	00	10000
0161	0	0001	SC_000101_0001_0161	00	10000
0162	0	0001	SC_000101_0001_0162	00	10000
0163	0	0001	SC_000101_0001_0163	00	10000
0164	0	0001	SC_000101_0001_0164	00	10000
0165	0	0001	SC_000101_0001_0165	00	10000
0166	0	0001	SC_000101_0001_0166	00	10000
0167	0	0001	SC_000101_0001_0167	00	10000
0168	0	0001	SC_000101_0001_0168	00	10000
0169	0	0001	SC_000101_0001_0169	00	10000
0170	0	0001	SC_000101_0001_0170	00	10000
0171	0	0001	SC_000101_0001_0171	00	10000
0172	0	0001	SC_000101_0001_0172	00	10000
0173	0	0001	SC_000101_0001_0173	00	10000
0174	0	0001	SC_000101_0001_0174	00	10000
0175	0	0001	SC_000101_0001_0175	00	10000
0176	0	0001	SC_000101_0001_0176	00	10000
0177	0	0001	SC_000101_0001_0177	00	10000
0178	0	0001	SC_000101_0001_0178	00	10000
0179	0	0001	SC_000101_0001_0179	00	10000
0180	0	0001	SC_000101_0001_0180	00	10000
0181	0	0001	SC_000101_0001_0181	00	10000
0182	0	0001	SC		

	Default	Use As	Signal Name	EXT PWRP	Power
0000		0	SWD0_000		
0001		0	SWD0_001		
0002	A15	0	SWD0_002	A15 00000000_000	A15A_000
0003	A15	0	SWD00_000	A15 00000000_000	A15A_000
0004		0	SWD00_001	A15 00000000_000	
0005		0	SWD00_002	A15 00000000_000	
0006		0	SWD00_003	A15 00000000_000	
0007		0	SWD00_004	A15 00000000_000	
0008		0	SWD00_005	A15 00000000_000	
0009		0	SWD00_006	A15 00000000_000	
0010		0	SWD00_007	A15 00000000_000	
0011		0	SWD00_008	A15 00000000_000	
0012		0	SWD00_009	A15 00000000_000	
0013		0	SWD00_010	A15 00000000_000	
0014		0	SWD00_011	A15 00000000_000	
0015		0	SWD00_012	A15 00000000_000	
0016		0	SWD00_013	A15 00000000_000	
0017		0	SWD00_014	A15 00000000_000	
0018		0	SWD00_015	A15 00000000_000	
0019		0	SWD00_016	A15 00000000_000	
0020		0	SWD00_017	A15 00000000_000	
0021		0	SWD00_018	A15 00000000_000	
0022		0	SWD00_019	A15 00000000_000	
0023		0	SWD00_020	A15 00000000_000	
0024		0	SWD00_021	A15 00000000_000	
0025		0	SWD00_022	A15 00000000_000	
0026		0	SWD00_023	A15 00000000_000	
0027		0	SWD00_024	A15 00000000_000	
0028		0	SWD00_025	A15 00000000_000	
0029		0	SWD00_026	A15 00000000_000	
0030		0	SWD00_027	A15 00000000_000	
0031		0	SWD00_028	A15 00000000_000	
0032		0	SWD00_029	A15 00000000_000	
0033		0	SWD00_030	A15 00000000_000	
0034		0	SWD00_031	A15 00000000_000	
0035		0	SWD00_032	A15 00000000_000	
0036		0	SWD00_033	A15 00000000_000	
0037		0	SWD00_034	A15 00000000_000	
0038		0	SWD00_035	A15 00000000_000	
0039		0	SWD00_036	A15 00000000_000	
0040		0	SWD00_037	A15 00000000_000	
0041		0	SWD00_038	A15 00000000_000	
0042		0	SWD00_039	A15 00000000_000	
0043		0	SWD00_040	A15 00000000_000	
0044		0	SWD00_041	A15 00000000_000	
0045		0	SWD00_042	A15 00000000_000	
0046		0	SWD00_043	A15 00000000_000	
0047		0	SWD00_044	A15 00000000_000	
0048		0	SWD00_045	A15 00000000_000	
0049		0	SWD00_046	A15 00000000_000	
0050		0	SWD00_047	A15 00000000_000	
0051		0	SWD00_048	A15 00000000_000	
0052		0	SWD00_049	A15 00000000_000	
0053		0	SWD00_050	A15 00000000_000	
0054		0	SWD00_051	A15 00000000_000	
0055		0	SWD00_052	A15 00000000_000	
0056		0	SWD00_053	A15 00000000_000	
0057		0	SWD00_054	A15 00000000_000	
0058		0	SWD00_055	A15 00000000_000	
0059		0	SWD00_056	A15 00000000_000	
0060		0	SWD00_057	A15 00000000_000	
0061		0	SWD00_058	A15 00000000_000	
0062		0	SWD00_059	A15 00000000_000	
0063		0	SWD00_060	A15 00000000_000	
0064		0	SWD00_061	A15 00000000_000	
0065					

Device	Port	Speed	Interface	MDI	Power
SW1	0	100	ETHERNET_0/0	MDI	100 W
SW1	1	100	ETHERNET_0/1	MDI	100 W
SW1	2	100	ETHERNET_0/2	MDI	100 W
SW1	3	100	ETHERNET_0/3	MDI	100 W
SW1	4	100	ETHERNET_0/4	MDI	100 W
SW1	5	100	ETHERNET_0/5	MDI	100 W
SW1	6	100	ETHERNET_0/6	MDI	100 W
SW1	7	100	ETHERNET_0/7	MDI	100 W
SW1	8	100	ETHERNET_0/8	MDI	100 W
SW1	9	100	ETHERNET_0/9	MDI	100 W
SW1	10	100	ETHERNET_0/10	MDI	100 W
SW1	11	100	ETHERNET_0/11	MDI	100 W
SW1	12	100	ETHERNET_0/12	MDI	100 W
SW1	13	100	ETHERNET_0/13	MDI	100 W
SW1	14	100	ETHERNET_0/14	MDI	100 W
SW1	15	100	ETHERNET_0/15	MDI	100 W
SW1	16	100	ETHERNET_0/16	MDI	100 W
SW1	17	100	ETHERNET_0/17	MDI	100 W
SW1	18	100	ETHERNET_0/18	MDI	100 W
SW1	19	100	ETHERNET_0/19	MDI	100 W
SW1	20	100	ETHERNET_0/20	MDI	100 W
SW1	21	100	ETHERNET_0/21	MDI	100 W
SW1	22	100	ETHERNET_0/22	MDI	100 W
SW1	23	100	ETHERNET_0/23	MDI	100 W
SW1	24	100	ETHERNET_0/24	MDI	100 W
SW1	25	100	ETHERNET_0/25	MDI	100 W
SW1	26	100	ETHERNET_0/26	MDI	100 W
SW1	27	100	ETHERNET_0/27	MDI	100 W
SW1	28	100	ETHERNET_0/28	MDI	100 W
SW1	29	100	ETHERNET_0/29	MDI	100 W
SW1	30	100	ETHERNET_0/30	MDI	100 W
SW1	31	100	ETHERNET_0/31	MDI	100 W
SW1	32	100	ETHERNET_0/32	MDI	100 W
SW1	33	100	ETHERNET_0/33	MDI	100 W
SW1	34	100	ETHERNET_0/34	MDI	100 W
SW1	35	100	ETHERNET_0/35	MDI	100 W
SW1	36	100	ETHERNET_0/36	MDI	100 W
SW1	37	100	ETHERNET_0/37	MDI	100 W
SW1	38	100	ETHERNET_0/38	MDI	100 W
SW1	39	100	ETHERNET_0/39	MDI	100 W
SW1	40	100	ETHERNET_0/40	MDI	100 W
SW1	41	100	ETHERNET_0/41	MDI	100 W
SW1	42	100	ETHERNET_0/42	MDI	100 W
SW1	43	100	ETHERNET_0/43	MDI	100 W
SW1	44	100	ETHERNET_0/44	MDI	100 W
SW1	45	100	ETHERNET_0/45	MDI	100 W
SW1	46	100	ETHERNET_0/46	MDI	100 W
SW1	47	100	ETHERNET_0/47	MDI	100 W
SW1	48	100	ETHERNET_0/48	MDI	100 W
SW1	49	100	ETHERNET_0/49	MDI	100 W
SW1	50	100	ETHERNET_0/50	MDI	100 W
SW1	51	100	ETHERNET_0/51	MDI	100 W
SW1	52	100	ETHERNET_0/52	MDI	100 W
SW1	53	100	ETHERNET_0/53	MDI	100 W
SW1	54	100	ETHERNET_0/54	MDI	100 W
SW1	55	100	ETHERNET_0/55	MDI	100 W
SW1	56	100	ETHERNET_0/56	MDI	100 W
SW1	57	100	ETHERNET_0/57	MDI	100 W
SW1	58	100	ETHERNET_0/58	MDI	100 W
SW1	59	100	ETHERNET_0/59	MDI	100 W
SW1	60	100	ETHERNET_0/60	MDI	100 W
SW1	61	100	ETHERNET_0/61	MDI	100 W
SW1	62	100	ETHERNET_0/62	MDI	100 W
SW1	63	100	ETHERNET_0/63	MDI	100 W
SW1	64	100	ETHERNET_0/64	MDI	100 W
SW1	65	100	ETHERNET_0/65	MDI	100 W
SW1	66	100	ETHERNET_0/66	MDI	100 W
SW1	67	100	ETHERNET_0/67	MDI	100 W
SW1	68	100	ETHERNET_0/68	MDI	100 W
SW1	69	100	ETHERNET_0/69	MDI	100 W
SW1	70	100	ETHERNET_0/70	MDI	100 W
SW1	71	100	ETHERNET_0/71	MDI	100 W
SW1	72	100	ETHERNET_0/72	MDI	100 W
SW1	73	100	ETHERNET_0/73	MDI	100 W
SW1	74	100	ETHERNET_0/74	MDI	100 W
SW1	75	100	ETHERNET_0/75	MDI	100 W
SW1	76	100	ETHERNET_0/76	MDI	100 W
SW1	77	100	ETHERNET_0/77	MDI	100 W
SW1	78	100	ETHERNET_0/78	MDI	100 W
SW1	79	100	ETHERNET_0/79	MDI	100 W
SW1	80	100	ETHERNET_0/80	MDI	100 W
SW1	81	100	ETHERNET_0/81	MDI	100 W
SW1	82	100	ETHERNET_0/82	MDI	100 W
SW1	83	100	ETHERNET_0/83	MDI	100 W
SW1	84	100	ETHERNET_0/84	MDI	100 W
SW1	85	100	ETHERNET_0/85	MDI	100 W
SW1	86	100	ETHERNET_0/86	MDI	100 W
SW1	87	100	ETHERNET_0/87	MDI	100 W
SW1	88	100	ETHERNET_0/88	MDI	100 W
SW1	89	100	ETHERNET_0/89	MDI	100 W
SW1	90	100	ETHERNET_0/90	MDI	100 W
SW1	91	100	ETHERNET_0/91	MDI	100 W
SW1	92	100	ETHERNET_0/92	MDI	100 W
SW1	93	100	ETHERNET_0/93	MDI	100 W
SW1	94	100	ETHERNET_0/94	MDI	100 W
SW1	95	100	ETHERNET_0/95	MDI	100 W
SW1	96	100	ETHERNET_0/96	MDI	100 W
SW1	97	100	ETHERNET_0/97	MDI	100 W
SW1	98	100	ETHERNET_0/98	MDI	100 W
SW1	99	100	ETHERNET_0/99	MDI	100 W
SW1	100	100	ETHERNET_0/100	MDI	100 W

	Default	Dev An	SI-grpd: Name	EXT: PUPID	Power
0000	LA001:FE02		LPI_A001_A7100_0001		
0001	LA001:FE03		LPI_A001_A7100_0001		
0002	LA001:FE04		LPI_A001_A7100_0001		
0003	LA001:FE05		LPI_A001_A7100_0001		
0004	LA001:FE06		LPI_A001_A7100_0001		
0005	LA001:FE07		LPI_A001_A7100_0001		
0006	LA001:FE08		LPI_A001_A7100_0001		
0007	LA001:FE09		LPI_A001_A7100_0001		
0008	LA001:FE10		LPI_A001_A7100_0001		
0009	LA001:FE11		LPI_A001_A7100_0001		
0010	LA001:FE12		LPI_A001_A7100_0001		
0011	LA001:FE13		LPI_A001_A7100_0001		
0012	LA001:FE14		LPI_A001_A7100_0001		
0013	LA001:FE15		LPI_A001_A7100_0001		
0014	LA001:FE16		LPI_A001_A7100_0001		
0015	LA001:FE17		LPI_A001_A7100_0001		
0016	LA001:FE18		LPI_A001_A7100_0001		
0017	LA001:FE19		LPI_A001_A7100_0001		
0018	LA001:FE20		LPI_A001_A7100_0001		
0019	LA001:FE21		LPI_A001_A7100_0001		
0020	LA001:FE22		LPI_A001_A7100_0001		
0021	LA001:FE23		LPI_A001_A7100_0001		
0022	LA001:FE24		LPI_A001_A7100_0001		
0023	LA001:FE25		LPI_A001_A7100_0001		
0024	LA001:FE26		LPI_A001_A7100_0001		
0025	LA001:FE27		LPI_A001_A7100_0001		
0026	LA001:FE28		LPI_A001_A7100_0001		
0027	LA001:FE29		LPI_A001_A7100_0001		
0028	LA001:FE30		LPI_A001_A7100_0001		
0029	LA001:FE31		LPI_A001_A7100_0001		
0030	LA001:FE32		LPI_A001_A7100_0001		
0031	LA001:FE33		LPI_A001_A7100_0001		
0032	LA001:FE34		LPI_A001_A7100_0001		
0033	LA001:FE35		LPI_A001_A7100_0001		
0034	LA001:FE36		LPI_A001_A7100_0001		
0035	LA001:FE37		LPI_A001_A7100_0001		
0036	LA001:FE38		LPI_A001_A7100_0001		
0037	LA001:FE39		LPI_A001_A7100_0001		
0038	LA001:FE40		LPI_A001_A7100_0001		
0039	LA001:FE41		LPI_A001_A7100_0001		
0040	LA001:FE42		LPI_A001_A7100_0001		
0041	LA001:FE43		LPI_A001_A7100_0001		
0042	LA001:FE44		LPI_A001_A7100_0001		
0043	LA001:FE45		LPI_A001_A7100_0001		
0044	LA001:FE46		LPI_A001_A7100_0001		
0045	LA001:FE47		LPI_A001_A7100_0001		
0046	LA001:FE48		LPI_A001_A7100_0001		
0047	LA001:FE49		LPI_A001_A7100_0001		
0048	LA001:FE50		LPI_A001_A7100_0001		
0049	LA001:FE51		LPI_A001_A7100_0001		
0050	LA001:FE52		LPI_A001_A7100_0001		
0051	LA001:FE53		LPI_A001_A7100_0001		
0052	LA001:FE54		LPI_A001_A7100_0001		
0053	LA001:FE55		LPI_A001_A7100_0001		
0054	LA001:FE56		LPI_A001_A7100_0001		
0055	LA001:FE57		LPI_A001_A7100_0001		
0056	LA001:FE58		LPI_A001_A7100_0001		
0057	LA001:FE59		LPI_A001_A7100_0001		
0058	LA001:FE60		LPI_A001_A7100_0001		
0059	LA001:FE61		LPI_A001_A7100_0001		
0060	LA001:FE62		LPI_A001_A7100_0001		
0061	LA001:FE63		LPI_A001_A7100_0001		
0062	LA001:FE64		LPI_A001_A7100_0001		
0063	LA001:FE65		LPI_A001_A7100_0001		
0064	LA001:FE66		LPI_A001_A7100_0001		
0065	LA001:FE67		LPI_A001_A7100_0001		
0066	LA001:FE68		LPI_A001_A7100_0001		
0067	LA001:FE69		LPI_A001_A7100_0001		
0068	LA001:FE70		LPI_A001_A7100_0001		
0069	LA001:FE71		LPI_A001_A7100_0001		
0070	LA001:FE72		LPI_A001_A7100_0001		
0071	LA001:FE73		LPI_A001_A7100_0001		
0072	LA001:FE74		LPI_A001_A7100_0001		
0073	LA001:FE75		LPI_A001_A7100_0001		
0074	LA001:FE76		LPI_A001_A7100_0001		
0075	LA001:FE77		LPI_A001_A7100_0001		
0076	LA001:FE78		LPI_A001_A7100_0001		
0077	LA001:FE79		LPI_A001_A7100_0001		
0078	LA001:FE80		LPI_A001_A7100_0001		
0079	LA001:FE81		LPI_A001_A7100_0001		
0080	LA001:FE82		LPI_A001_A7100_0001		
0081	LA001:FE83		LPI_A001_A7100_0001		
0082	LA001:FE84		LPI_A001_A7100_0001		
0083	LA001:FE85		LPI_A001_A7100_0001		
0084	LA001:FE86		LPI_A001_A7100_0001		
0085	LA001:FE87		LPI_A001_A7100_0001		
0086	LA001:FE88		LPI_A001_A7100_0001		
0087	LA001:FE89		LPI_A001_A7100_0001		
0088	LA001:FE90		LPI_A001_A7100_0001		
0089	LA001:FE91		LPI_A001_A7100_0001		
0090	LA001:FE92		LPI_A001_A7100_0001		
0091	LA001:FE93		LPI_A001_A7100_0001		
0092	LA001:FE94		LPI_A001_A7100_0001		
0093	LA001:FE95		LPI_A001_A7100_0001		
0094	LA001:FE96		LPI_A001_A7100_0001		
0095	LA001:FE97		LPI_A001_A7100_0001		
0096	LA001:FE98		LPI_A001_A7100_0001		
0097	LA001:FE99		LPI_A001_A7100_0001		
0098	LA001:FE00		LPI_A001_A7100_0001		
0099	LA001:FE01		LPI_A001_A7100_0001		

SKI-PCH-H Z170-HISIO						SKI-PCH-H Z170-HISIO	
1	USBSB #1 (OTG)					1	USBSB #1 (OTG)
2	USBSB #2	SSICB #1				2	USBSB #2
3	USBSB #3	SSICB #2				3	USBSB #3
4	USBSB #4					4	USBSB #4
5	USBSB #5					5	USBSB #5
6	USBSB #6					6	USBSB #6
7	USBSB #7	PCHB #1	x2	x4	NA	7	USBSB #7
8	USBSB #8	PCHB #2				8	USBSB #8
9	USBSB #9	PCHB #3				9	USBSB #9
10	USBSB #10	PCHB #4	Gen	x4		10	USBSB #10

12	PCIE #5	GBE	X2	NA	15	PCIE #5	
13	PCIE #6		X2		16	PCIE #6	
14	PCIE #7		X2		17	PCIE #7	
15	PCIE #8		X2		18	PCIE #8	
16	PCIE #9	SATA #0	GBE	Intel ITRST PCIe Storage Device #1	19	PCIE #9	
17	PCIE #10	SATA #1	X2		20	PCIE #10	
18	PCIE #11		X2		21	PCIE #11	
19	PCIE #12	GBE	X2		22	PCIE #12	
20	PCIE #13	SATA #0	GBE	Intel ITRST PCIe Storage Device #2	23	PCIE #13	
21	PCIE #14	SATA #1	X2		24	PCIE #14	
22	PCIE #15	SATA #2	X2		25	PCIE #15	
23	PCIE #16	SATA #3	X2		26	PCIE #16	
24	PCIE #17	SATA #4	X2	Intel ITRST PCIe Storage Device #3	27	SATA #4	
25	PCIE #18	SATA #5	X2		28	PCIE #18	
26	PCIE #19	SATA #6	X2		29	PCIE #19	
27	PCIE #20	SATA #7	X2		30	PCIE #20	

EC IT8995 GPIO

Default	Use As	Signal Name	EXT PUMP	Power
0	SPD	100_120	EXT_100	-
0.5	SPD	100_120.5		-0.5A
1	SPD	100_120.5+0.5A	P0 100 100	-0.5A
1.5A	SPD	100_120.5A		-1.5A
2	SPD	100_120.5A+0.5A		-2A
2.5A	SPD	100_120.5A+0.5A		-2.5A
3	SPD	100_120_150		-3A
4	SPD	100_120.5A		-4A

Default	Use As	Signal Name	EXT PUMP	Power
1.5A	SPD	100_120.5A		-1.5A
2	SPD	100_120		-2A
2.5	SPD	100_120.5A		-2.5A
3	SPD	100_120.5A+0.5A	P0 100.5A	-3A
4	SPD	100_120.5A		-4A
5	SPD	100_120.5A		-5A
6	SPD	100_120.5A		-6A
7	SPD	100_120_150		-7A
8	SPD	100_120.5A		-8A
9	SPD	100_120.5A		-9A
10	SPD	100_120.5A		-10A
11	SPD	100_120.5A		-11A
12	SPD	100_120.5A		-12A
13	SPD	100_120.5A		-13A
14	SPD	100_120.5A		-14A
15	SPD	100_120.5A		-15A
16	SPD	100_120.5A		-16A
17	SPD	100_120.5A		-17A
18	SPD	100_120.5A		-18A
19	SPD	100_120.5A		-19A
20	SPD	100_120.5A		-20A
21	SPD	100_120.5A		-21A
22	SPD	100_120.5A		-22A
23	SPD	100_120.5A		-23A
24	SPD	100_120.5A		-24A
25	SPD	100_120.5A		-25A
26	SPD	100_120.5A		-26A
27	SPD	100_120.5A		-27A
28	SPD	100_120.5A		-28A
29	SPD	100_120.5A		-29A
30	SPD	100_120.5A		-30A
31	SPD	100_120.5A		-31A
32	SPD	100_120.5A		-32A
33	SPD	100_120.5A		-33A
34	SPD	100_120.5A		-34A
35	SPD	100_120.5A		-35A
36	SPD	100_120.5A		-36A
37	SPD	100_120.5A		-37A
38	SPD	100_120.5A		-38A
39	SPD	100_120.5A		-39A
40	SPD	100_120.5A		-40A
41	SPD	100_120.5A		-41A
42	SPD	100_120.5A		-42A
43	SPD	100_120.5A		-43A
44	SPD	100_120.5A		-44A
45	SPD	100_120.5A		-45A
46	SPD	100_120.5A		-46A
47	SPD	100_120.5A		-47A
48	SPD	100_120.5A		-48A
49	SPD	100_120.5A		-49A
50	SPD	100_120.5A		-50A
51	SPD	100_120.5A		-51A
52	SPD	100_120.5A		-52A
53	SPD	100_120.5A		-53A
54	SPD	100_120.5A		-54A
55	SPD	100_120.5A		-55A
56	SPD	100_120.5A		-56A
57	SPD	100_120.5A		-57A
58	SPD	100_120.5A		-58A
59	SPD	100_120.5A		-59A
60	SPD	100_120.5A		-60A
61	SPD	100_120.5A		-61A
62	SPD	100_120.5A		-62A
63	SPD	100_120.5A		-63A
64	SPD	100_120.5A		-64A
65	SPD	100_120.5A		-65A
66	SPD	100_120.5A		-66A
67	SPD	100_120.5A		-67A
68	SPD	100_120.5A		-68A
69	SPD	100_120.5A		-69A
70	SPD	100_120.5A		-70A
71	SPD	100_120.5A		-71A
72	SPD	100_120.5A		-72A
73	SPD	100_120.5A		-73A
74	SPD	100_120.5A		-74A
75	SPD	100_120.5A		-75A

Refinit	Est Ao	Signal Name	Est PUPD	Power
0	GPS	ION KATZNER	PD 120 -01	-120dB
A13	GPS	ION KATZNER	PD 120 -01	-120dB
A15	GPS	ION KATZNER	PD 120 -01	-120dB
0	GPS	ION KATZNER	PD 120 -01	-120dB
A13	GPS	ION KATZNER	PD 120 -01	-120dB
A15	GPS	ION KATZNER	PD 120 -01	-120dB
0	GPS	ION KATZNER	PD 120 -01	-120dB
A13	GPS	ION KATZNER	PD 120 -01	-120dB
A15	GPS	ION KATZNER	PD 120 -01	-120dB
0	GPS	ION KATZNER	PD 120 -01	-120dB
A13	GPS	ION KATZNER	PD 120 -01	-120dB
A15	GPS	ION KATZNER	PD 120 -01	-120dB

[illegible][illegible][illegible]

Q	REF	LINK_COMMENT	REF_DATE	REF_SOURCE
Default	Use As	Signal Name	EXT PINS	Power
1	REF1	1_P1_420_420_420_420		
2	REF2	1_P1_420_420_420_420		
3	REF3	1_P1_420_420_420_420		
4	REF4	1_P1_420_420_420_420		
5	REF5	1_P1_420_420_420_420		
6	REF6	1_P1_420_420_420_420		
7	REF7	1_P1_420_420_420_420		
8	REF8	1_P1_420_420_420_420		
9	REF9	1_P1_420_420_420_420		
10	REF10	1_P1_420_420_420_420		
11	REF11	1_P1_420_420_420_420		
12	REF12	1_P1_420_420_420_420		
13	REF13	1_P1_420_420_420_420		
14	REF14	1_P1_420_420_420_420		
15	REF15	1_P1_420_420_420_420		
16	REF16	1_P1_420_420_420_420		
17	REF17	1_P1_420_420_420_420		
18	REF18	1_P1_420_420_420_420		
19	REF19	1_P1_420_420_420_420		
20	REF20	1_P1_420_420_420_420		
21	REF21	1_P1_420_420_420_420		
22	REF22	1_P1_420_420_420_420		
23	REF23	1_P1_420_420_420_420		
24	REF24	1_P1_420_420_420_420		
25	REF25	1_P1_420_420_420_420		
26	REF26	1_P1_420_420_420_420		
27	REF27	1_P1_420_420_420_420		
28	REF28	1_P1_420_420_420_420		
29	REF29	1_P1_420_420_420_420		
30	REF30	1_P1_420_420_420_420		
31	REF31	1_P1_420_420_420_420		
32	REF32	1_P1_420_420_420_420		
33	REF33	1_P1_420_420_420_420		
34	REF34	1_P1_420_420_420_420		
35	REF35	1_P1_420_420_420_420		
36	REF36	1_P1_420_420_420_420		
37	REF37	1_P1_420_420_420_420		
38	REF38	1_P1_420_420_420_420		
39	REF39	1_P1_420_420_420_420		
40	REF40	1_P1_420_420_420_420		
41	REF41	1_P1_420_420_420_420		
42	REF42	1_P1_420_420_420_420		
43	REF43	1_P1_420_420_420_420		
44	REF44	1_P1_420_420_420_420		
45	REF45	1_P1_420_420_420_420		
46	REF46	1_P1_420_420_420_420		
47	REF47	1_P1_420_420_420_420		
48	REF48	1_P1_420_420_420_420		
49	REF49	1_P1_420_420_420_420		
50	REF50	1_P1_420_420_420_420		
51	REF51	1_P1_420_420_420_420		
52	REF52	1_P1_420_420_420_420		
53	REF53	1_P1_420_420_420_420		
54	REF54	1_P1_420_420_420_420		
55	REF55	1_P1_420_420_420_420		
56	REF56	1_P1_420_420_420_420		
57	REF57	1_P1_420_420_420_420		
58	REF58	1_P1_420_420_420_420		
59	REF59	1_P1_420_420_420_420		
60	REF60	1_P1_420_420_420_420		
61	REF61	1_P1_420_420_420_420		
62	REF62	1_P1_420_420_420_420		
63	REF63	1_P1_420_420_420_420		
64	REF64	1_P1_420_420_420_420		
65	REF65	1_P1_420_420_420_420		
66	REF66	1_P1_420_420_420_420		
67	REF67	1_P1_420_420_420_420		
68	REF68	1_P1_420_420_420_420		
69	REF69	1_P1_420_420_420_420		
70	REF70	1_P1_420_420_420_420		
71	REF71	1_P1_420_420_420_420		
72	REF72	1_P1_420_420_420_420		
73	REF73	1_P1_420_420_420_420		
74	REF74	1_P1_420_420_420_420		
75	REF75	1_P1_420_420_420_420		
76	REF76	1_P1_420_420_420_420		
77	REF77	1_P1_420_420_420_420		
78	REF78	1_P1_420_420_420_420		
79	REF79	1_P1_420_420_420_420		
80	REF80	1_P1_420_420_420_420		
81	REF81	1_P1_420_420_420_420		
82	REF82	1_P1_420_420_420_420		
83	REF83	1_P1_420_420_420_420		
84	REF84	1_P1_420_420_420_420		
85	REF85	1_P1_420_420_420_420		
86	REF86	1_P1_420_420_420_420		
87	REF87	1_P1_420_420_420_420		
88	REF88	1_P1_420_420_420_420		
89	REF89	1_P1_420_420_420_420		
90	REF90	1_P1_420_420_420_420		
91	REF91	1_P1_420_420_420_420		
92	REF92	1_P1_420_420_420_420		
93	REF93	1_P1_420_420_420_420		
94	REF94	1_P1_420_420_420_420		
95	REF95	1_P1_420_420_420_420		
96	REF96	1_P1_420_420_420_420		
97	REF97	1_P1_420_420_420_420		
98	REF98	1_P1_420_420_420_420		
99	REF99	1_P1_420_420_420_420		
100	REF100	1_P1_420_420_420_420		

PCIe 00.00				4	USBS0_04
4	USBS0_04				
5	USBS0_05				
6	USBS0_06				
7	USBS0_07	PCIe #1	x2	x4	NA
8	USBS0_08	PCIe #2	x2		
9	USBS0_09	PCIe #3	x2		
10	USBS0_10	PCIe #4	GbE		
11	PCIe #5		x2	x4	NA
12	PCIe #6		x2		
13	PCIe #7		x2		
14	PCIe #8		x2		
15	PCIe #9	SATA #0	GbE		
16	PCIe #10	SATA #1	x2		Intel RST PCI Storage Device #1
17	PCIe #11				
18	PCIe #12		GbE		
19	PCIe #13	SATA #0	x2		Intel RST

21	PCIe #15	SATA#2	x2	x4	PCIe Storage Device #2	21	PCIe #15
22	PCIe #16	SATA#3				22	PCIe #16
23	PCIe #17	SATA#4				23	SATA#4
24	PCIe #18	SATA#5	x2		Intel IRT	24	SATA#5
25	PCIe #19	SATA#6		x4	PCIe Storage Device #3	25	PCIe #19
26	PCIe #20	SATA#7	x2			26	PCIe #20

N501VW Setting	
BM_BUS ADDRESS :	
BM Number	
BM Bus Device	BM Bus Address
BM Slave's memory's LSW	
BM Slave's BUS	BM

IP Address	192.168.1.1	MAC Address	08:00:27:00:00:00
IP Netmask	255.255.255.0	IP Gateway	192.168.1.1
IP Subnet Mask	255.255.255.0	IP Broadcast	192.168.1.255
IP Primary Server	192.168.1.1	IP Secondary Server	192.168.1.2
IP Tertiary Server	192.168.1.3	IP Quaternary Server	192.168.1.4
IP Quinary Server	192.168.1.5	IP Sixth Server	192.168.1.6
IP Seventh Server	192.168.1.7	IP Eighth Server	192.168.1.8
IP Ninth Server	192.168.1.9	IP Tenth Server	192.168.1.10
IP Eleventh Server	192.168.1.11	IP Twelfth Server	192.168.1.12
IP Thirteenth Server	192.168.1.13	IP Fourteenth Server	192.168.1.14
IP Fifteenth Server	192.168.1.15	IP Sixteenth Server	192.168.1.16
IP Seventeenth Server	192.168.1.17	IP Eighteenth Server	192.168.1.18
IP Nineteenth Server	192.168.1.19	IP Twentieth Server	192.168.1.20
IP Twenty-first Server	192.168.1.21	IP Twenty-second Server	192.168.1.22
IP Twenty-third Server	192.168.1.23	IP Twenty-fourth Server	192.168.1.24
IP Twenty-fifth Server	192.168.1.25	IP Twenty-sixth Server	192.168.1.26
IP Twenty-seventh Server	192.168.1.27	IP Twenty-eighth Server	192.168.1.28
IP Twenty-ninth Server	192.168.1.29	IP Thirtieth Server	192.168.1.30
IP Thirty-first Server	192.168.1.31	IP Thirty-second Server	192.168.1.32
IP Thirty-third Server	192.168.1.33	IP Thirty-fourth Server	192.168.1.34
IP Thirty-fifth Server	192.168.1.35	IP Thirty-sixth Server	192.168.1.36
IP Thirty-seventh Server	192.168.1.37	IP Thirty-eighth Server	192.168.1.38
IP Thirty-ninth Server	192.168.1.39	IP Fortieth Server	192.168.1.40
IP Forty-first Server	192.168.1.41	IP Forty-second Server	192.168.1.42
IP Forty-third Server	192.168.1.43	IP Forty-fourth Server	192.168.1.44
IP Forty-fifth Server	192.168.1.45	IP Forty-sixth Server	192.168.1.46
IP Forty-seventh Server	192.168.1.47	IP Forty-eighth Server	192.168.1.48
IP Forty-ninth Server	192.168.1.49	IP Fiftieth Server	192.168.1.50
IP Fifty-first Server	192.168.1.51	IP Fifty-second Server	192.168.1.52
IP Fifty-third Server	192.168.1.53	IP Fifty-fourth Server	192.168.1.54
IP Fifty-fifth Server	192.168.1.55	IP Fifty-sixth Server	192.168.1.56
IP Fifty-seventh Server	192.168.1.57	IP Fifty-eighth Server	192.168.1.58
IP Fifty-ninth Server	192.168.1.59	IP Sixtieth Server	192.168.1.60
IP Sixty-first Server	192.168.1.61	IP Sixty-second Server	192.168.1.62
IP Sixty-third Server	192.168.1.63	IP Sixty-fourth Server	192.168.1.64
IP Sixty-fifth Server	192.168.1.65	IP Sixty-sixth Server	192.168.1.66
IP Sixty-seventh Server	192.168.1.67	IP Sixty-eighth Server	192.168.1.68
IP Sixty-ninth Server	192.168.1.69	IP Seventieth Server	192.168.1.70
IP Seventy-first Server	192.168.1.71	IP Seventy-second Server	192.168.1.72
IP Seventy-third Server	192.168.1.73	IP Seventy-fourth Server	192.168.1.74
IP Seventy-fifth Server	192.168.1.75	IP Seventy-sixth Server	192.168.1.76
IP Seventy-seventh Server	192.168.1.77	IP Seventy-eighth Server	192.168.1.78
IP Seventy-ninth Server	192.168.1.79	IP Eightieth Server	192.168.1.80
IP Eighty-first Server	192.168.1.81	IP Eighty-second Server	192.168.1.82
IP Eighty-third Server	192.168.1.83	IP Eighty-fourth Server	192.168.1.84
IP Eighty-fifth Server	192.168.1.85	IP Eighty-sixth Server	192.168.1.86
IP Eighty-seventh Server	192.168.1.87	IP Eighty-eighth Server	192.168.1.88
IP Eighty-ninth Server	192.168.1.89	IP Ninetieth Server	192.168.1.90
IP Ninety-first Server	192.168.1.91	IP Ninety-second Server	192.168.1.92
IP Ninety-third Server	192.168.1.93	IP Ninety-fourth Server	192.168.1.94
IP Ninety-fifth Server	192.168.1.95	IP Ninety-sixth Server	192.168.1.96
IP Ninety-seventh Server	192.168.1.97	IP Ninety-eighth Server	192.168.1.98
IP Ninety-ninth Server	192.168.1.99	IP One Hundredth Server	192.168.1.100

24	PGM01 / SG002	CEB3 (Perf)	
25	PGM02	CEB3 (Perf)	
26	PGM03	CEB3 (Perf)	
27	PGM07 / PG006	Catapult (CEB005)	
28	PGM08 / PG002		SE2
29	PG003	SL00	SE2
30	PG004 / GB		
31	PG005 / GB		SE3
32	PG006	Thunderbolt	
33	PG007		
34	PG008		
35	PG009 / SG007 / GB	SEA* 100 yards	
36	PG010 / SG008		
37	PG011	SEA* 100	SE3
38	PG012 / GB		
39	PG013 / SG009 / GB		
40	PG014 / SG004		
41	PG015 / SG005		
42	PG016 / SG006		

25			
25			
25			
25			

PCH#1 H170 HS80	
SSIC #1	

SQL PCH-H H1M170 HS80	
1	US803 #1 (OTD)
2	US803 #2
	SSIC #1

Host 1				Host 2			
				4	USPD0 #4		
				5	USPD0 #5		
				6	USPD0 #6		
				7	USPD0 #7	PCIE #1	
				8	USPD0 #8	PCIE #2	
				9	PCIE #3		
				10	PCIE #4		
				11	PCIE #5	QSE	
				12	PCIE #6		
				13	PCIE #7		
				14	PCIE #8		
				15	PCIE #9	SATA #0	
				16	PCIE #10	SATA #1	
				17	PCIE #11		
				18	PCIE #12	QSE	
				19	PCIE #13	SATA #0	

NA#2	x2	x4	PCIe Storage Device #2	21	PCIe #15	SATA#2	x2	x4
NA#3				22	PCIe #16	SATA#3		
				23				
	NA	NA	NA	24			NA	NA
	x2			25			NA	
				26				

N501VW Setting

SIM_Bus ADDRESS :		
PCI Master		
SIM-Bus Device	SIM-Bus Address	
on-chip memory CPU		
SD-CPUW BUS	A40	
EC Master (MPS)	SIM-Bus Address	
SIM-Bus Device		
Vbat Thermal Sensor	700	
CPU Thermal Sensor	701	
Power Thermal Sensor	702	

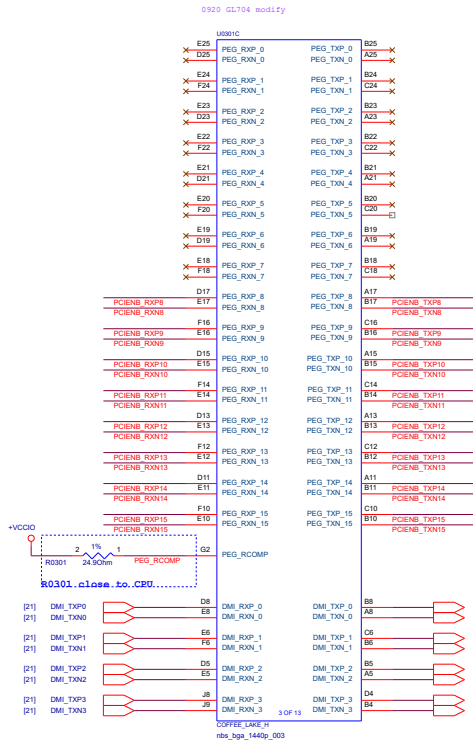
Device Identification

CPU Thermal Sensor		
Id	0000012876	MCT9T0YU
2nd		

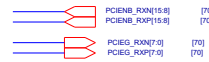
Kabylake HMC17

[illegible]

	Project Name G711GW
Title : System Setting	



```
CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8
```



PCB16B_TX08	CX0317	1	2	0.22uF-5.3V	PC16C_RX08	PC16B_TX08	CX0304	1	2	0.22uF-5.3V
PCB16B_TX09	CX0318	1	2	0.22uF-5.3V	PC16C_RX09	PC16B_TX09	CX0305	1	2	0.22uF-5.3V
PCB16B_TX010	CX0320	1	2	0.22uF-5.3V	PC16C_RX06	PC16B_TXP10	CX0336	1	2	0.22uF-5.3V
PCB16B_TX011	CX0321	1	2	0.22uF-5.3V	PC16C_RX07	PC16B_TXP11	CX0337	1	2	0.22uF-5.3V
PCB16B_TX012	CX0322	1	2	0.22uF-5.3V	PC16C_RX08	PC16B_TXP12	CX0338	1	2	0.22uF-5.3V
PCB16B_TX013	CX0323	1	2	0.22uF-5.3V	PC16C_RX09	PC16B_TXP13	CX0339	1	2	0.22uF-5.3V
PCB16B_TX014	CX0324	1	2	0.22uF-5.3V	PC16C_RX10	PC16B_TXP14	CX0340	1	2	0.22uF-5.3V
PCB16B_TX015	CX0325	1	2	0.22uF-5.3V	PC16C_RX06	PC16B_TXP15				PC16C_RX06

Display

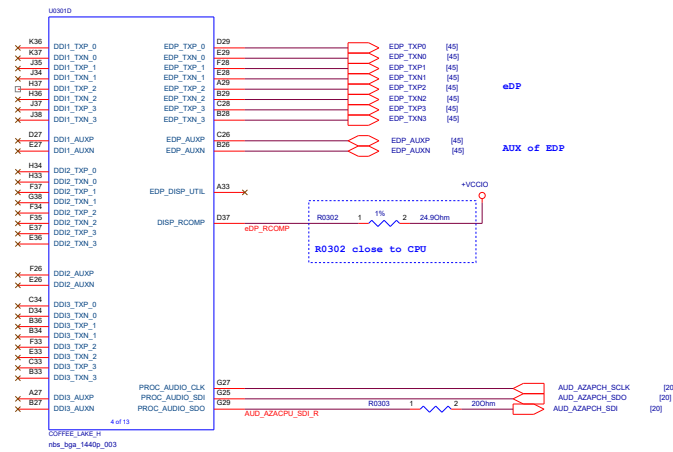


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
 2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.
- For example:
- a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

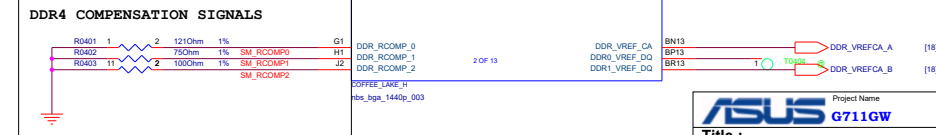
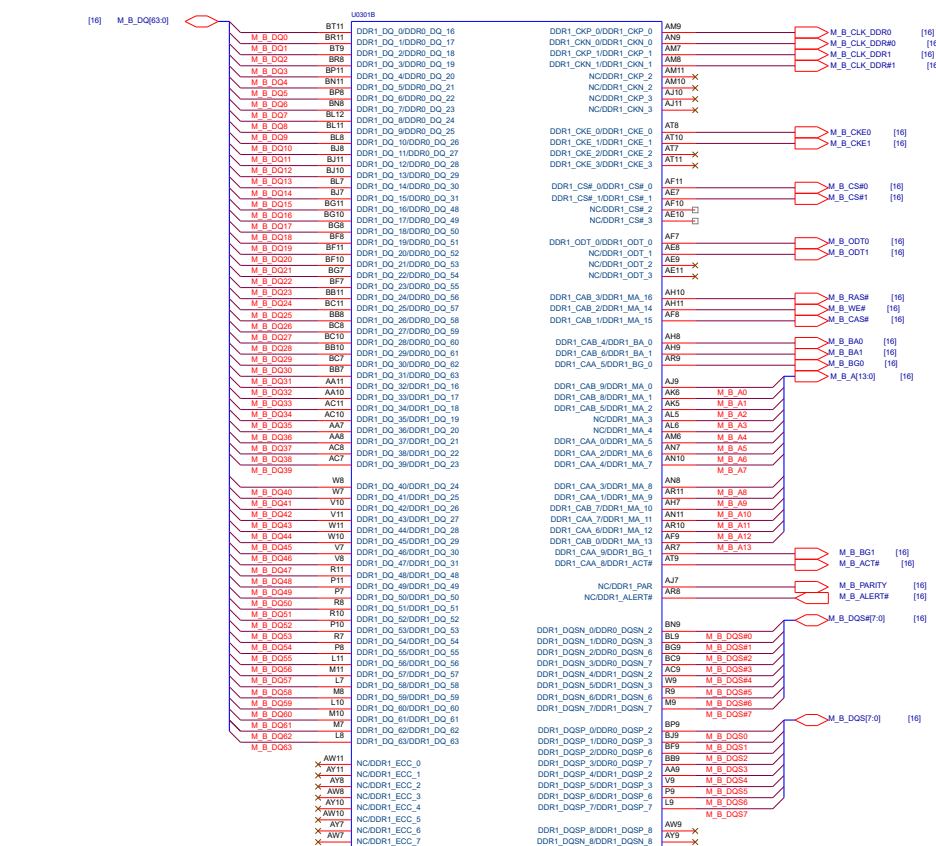
Refer to CFL-H PDG P.363 (Doc.571391)

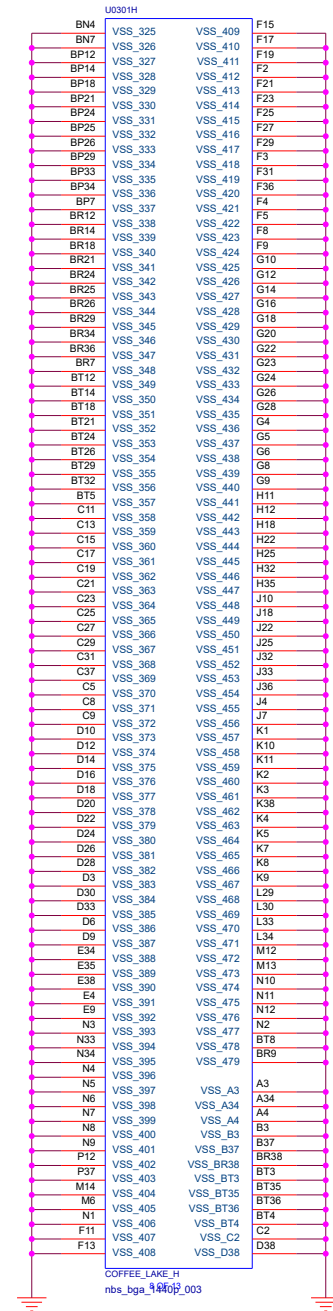
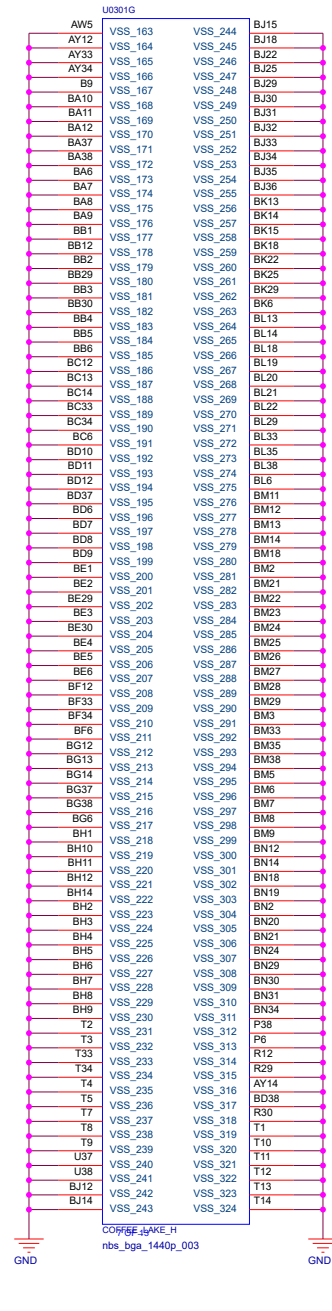
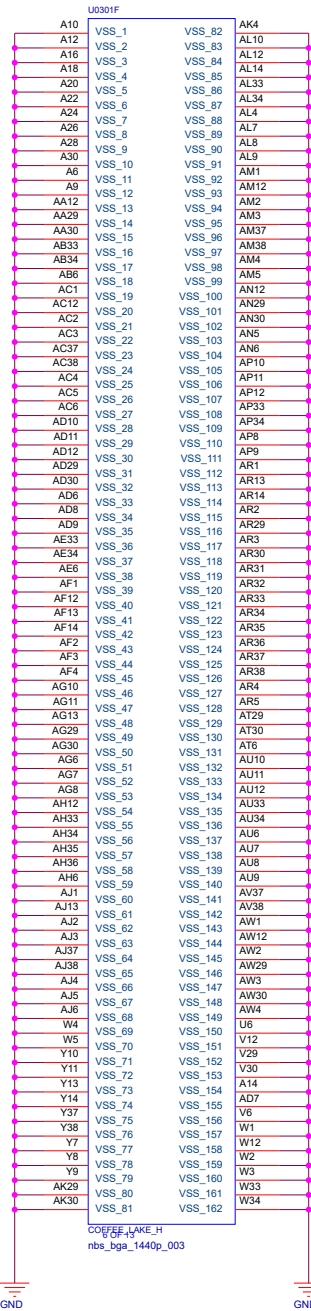
31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

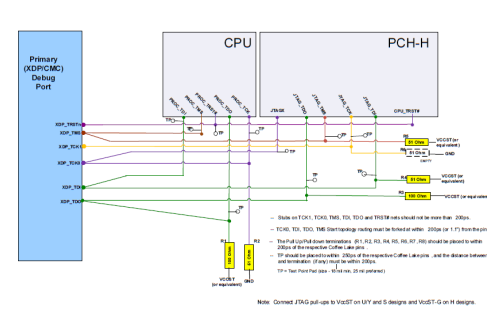
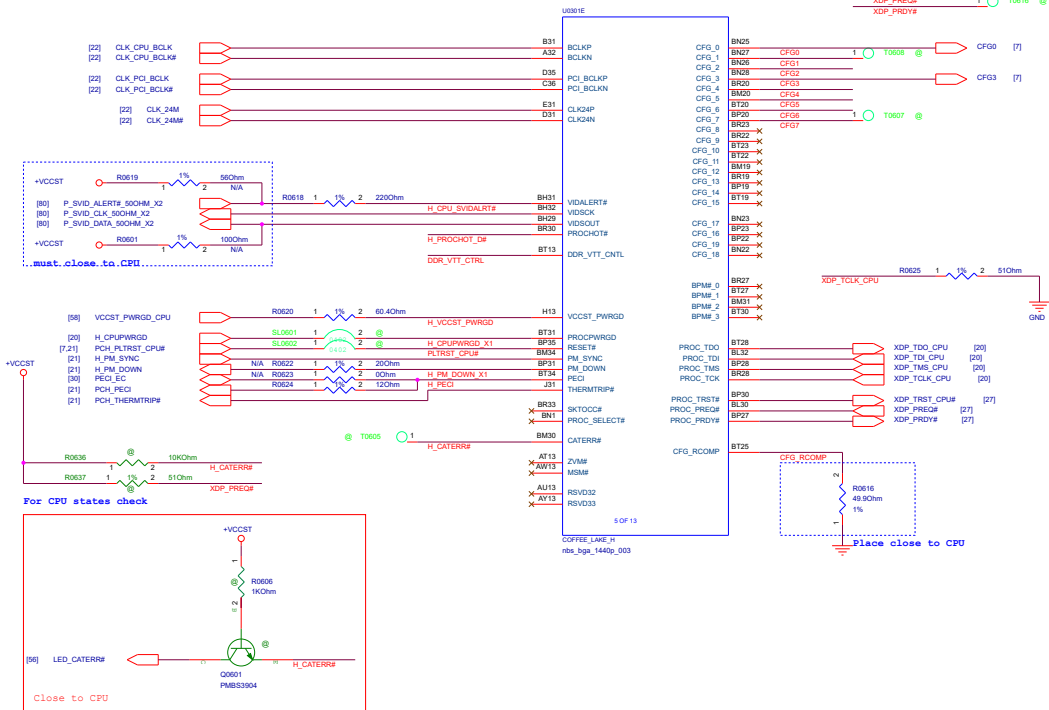
When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. $\sim 2\text{k}\Omega$), PROC_AUDIO_SDO can be left unconnected.

Main Board







Note: Connect JTAG pull-ups to Vcc5T on U/Y and S designs and Vcc5T-G on H designs.

CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express® Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled

CFG[6:5] : PCI Express® Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

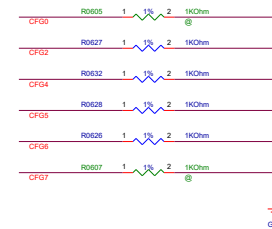
CFG[7] : PEG Training

- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes

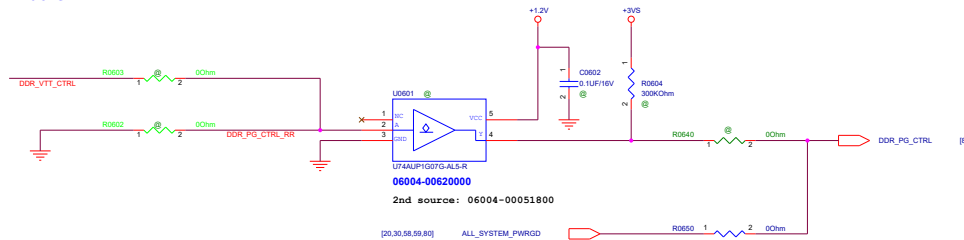
Reserved Configuration Lanes

CFG Straps

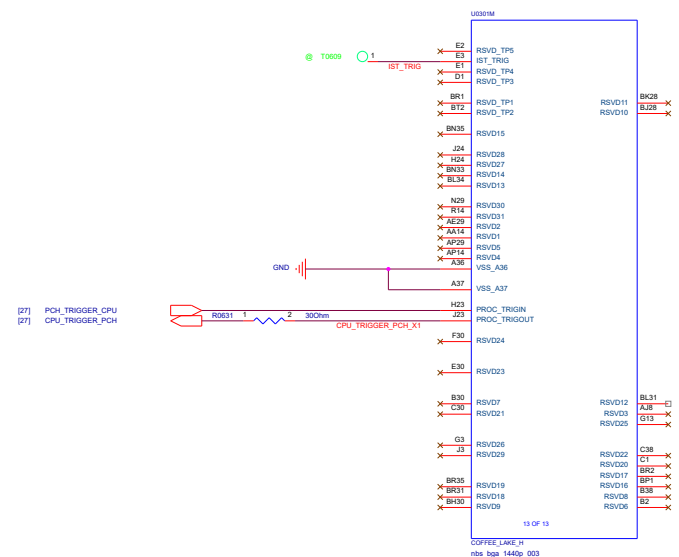
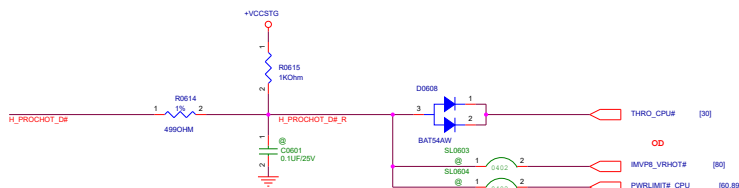


DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

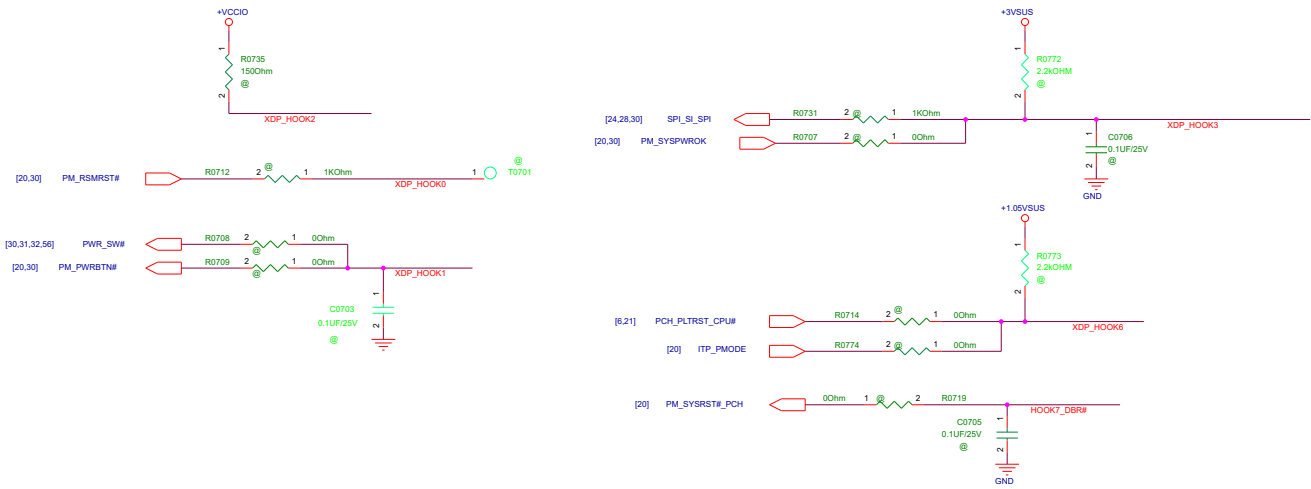
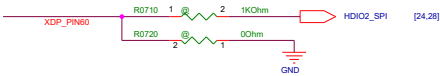
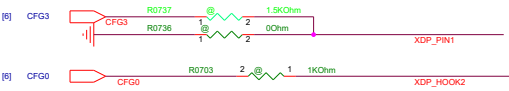
VTT Enable

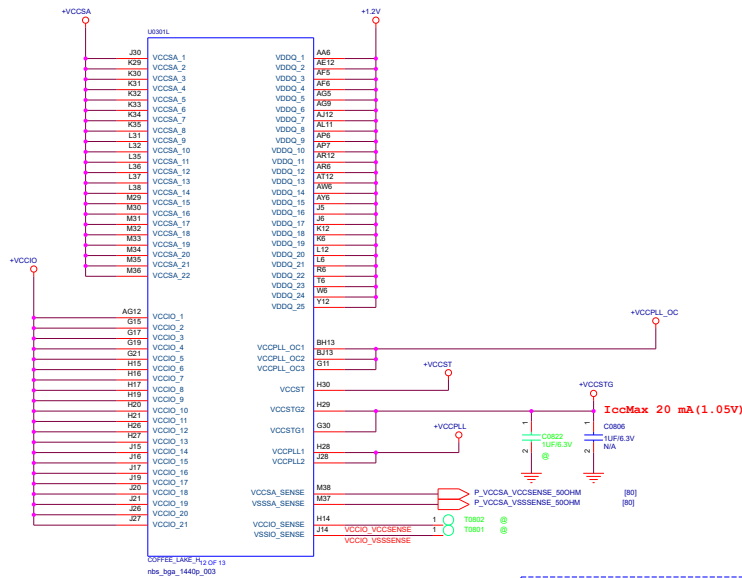


CPU SIDEBAND SIGNALS



CPU XDP





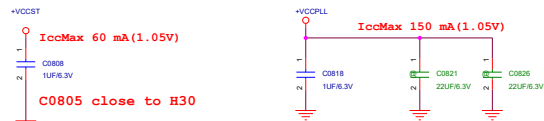
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSDS	+VCCST	
	+1.2V	+VCCSTG	
	+VCCSA	+VTT	
	+VCCIO	+VCCPLL_OC	

Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

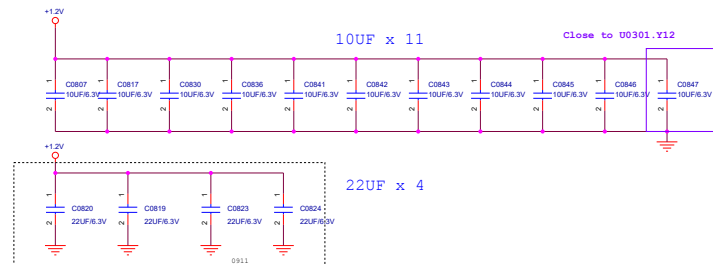
CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCST/+VCCPLL DECAPS Place Back Side (TOP)

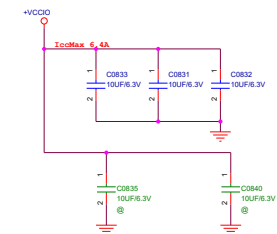


CFL U/H PDG Update for VCCPLL Power Rail Design Guidelines
Due to Display PLL lock issues observed on systems with high noise level on VCCPLL, CFL-H BIP#571391 and CFL-U BIP#571821 Platform design guidelines has been updated with new recommendation for VCCPLL power rail.
An additional capacitor 2005 size placeholder near CPU BGA ball is recommended for better power delivery, this should be stuffed when encountered a noisy VCCPLL power rail.
This new recommendation not required for systems that follows the PDG Power Integrity guidance and kept low noise level on VCCPLL.

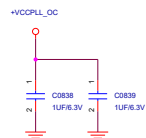
+VDDQ DECAPS Place Back Side (TOP)



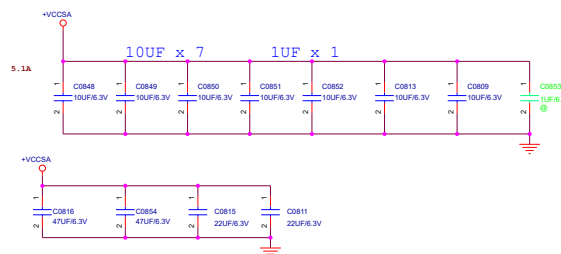
+VCCIO DECAPS Place Back Side (TOP)

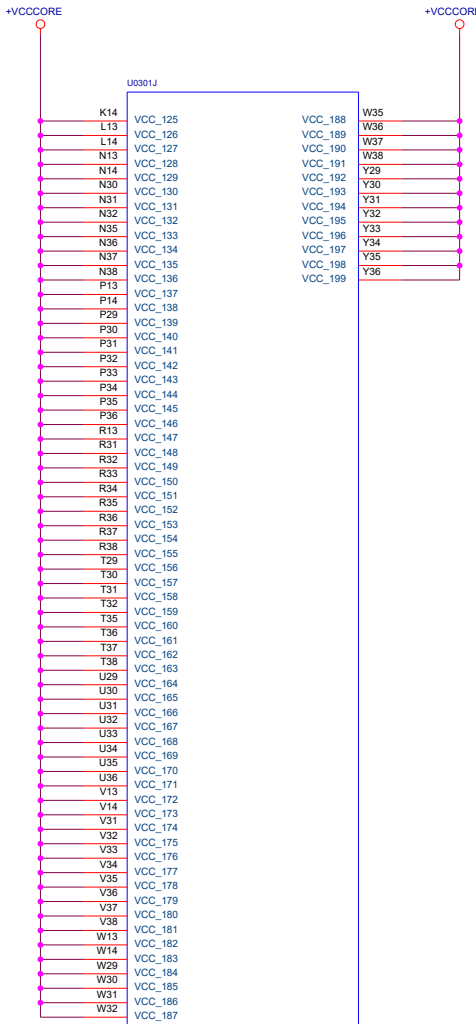
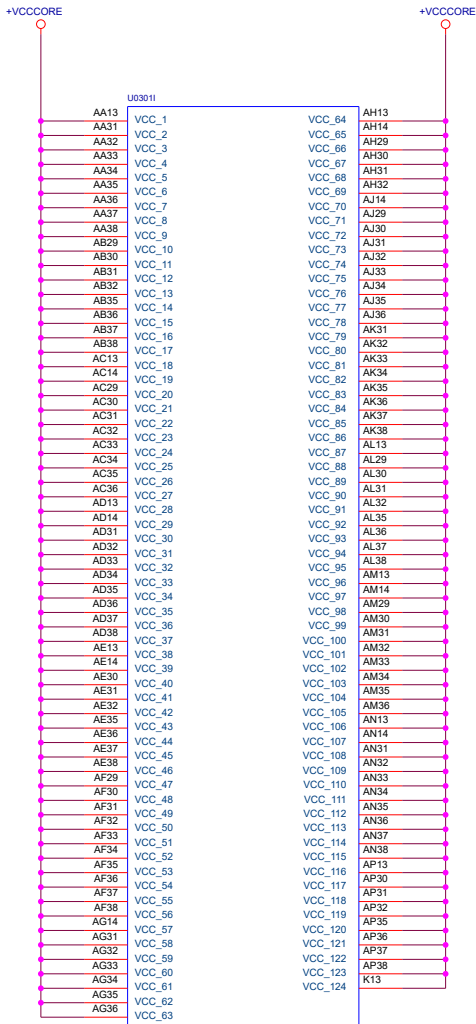
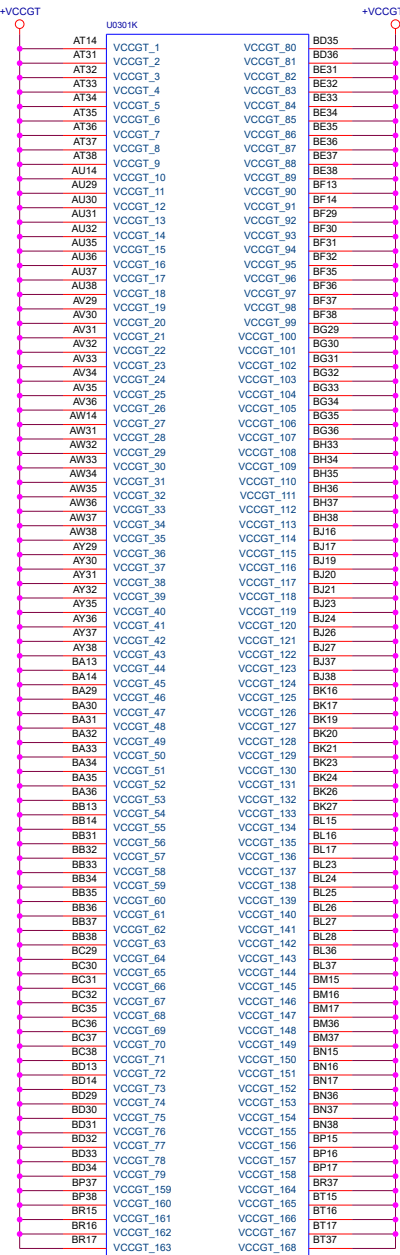


+VCCPLL_OC DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)





COFFEE_LAKE_H 9 OF 13
nbs_bga_1440p_003

VCC_SENSE
VSS_SENSE

AG37 P_VCCCORE_VCCSENSE_500HM
AG38 P_VCCCORE_VSSSENSE_500HM

COFFEE_LAKE_H10 OF 13
nbs_bga_1440p_003

[80]
[80]

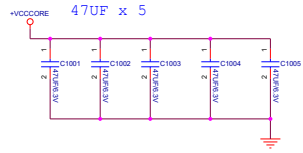
VCCGT_SENSE
VSSGT_SENSE

AH38 P_VCCGT_VCCSENSE_500HM
AH37 P_VCCGT_VSSSENSE_500HM

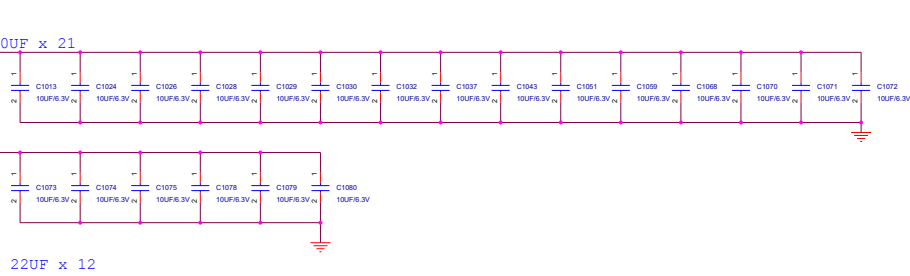
COFFEE_LAKE_H11 OF 13
nbs_bga_1440p_003

[80]
[80]

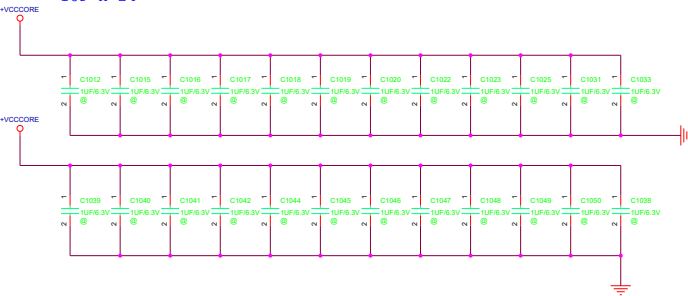
+VCCORE near CPU



+VCCORE DECAPS Place Back Side (TOP)



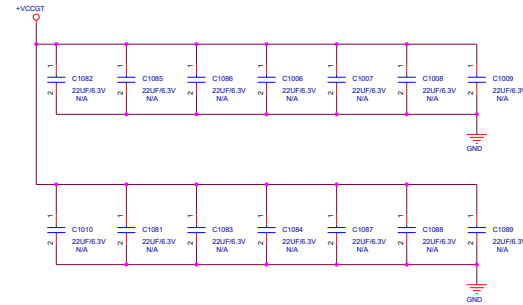
1uF x 24



Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
VCCGT	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

+VCCGT cap near CPU

22uF x14





Project Name

G711GW

Rev

R1.0

Title : **TBT_Alpine-Ridge**

Size

C

Dept.: **ASUSTeK COMPUTER**

Engineer: **Gaming RD**

Date: **Tuesday, April 16, 2019**

Sheet

11

of

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Project Name

G711GW

Rev

R1.3

Title : **CYPRESS CCG4**

Size

D


Dept.: **ASUSTeK COMPUTER**


Engineer: **Gaming RD**

Date: **Tuesday, April 16, 2019**

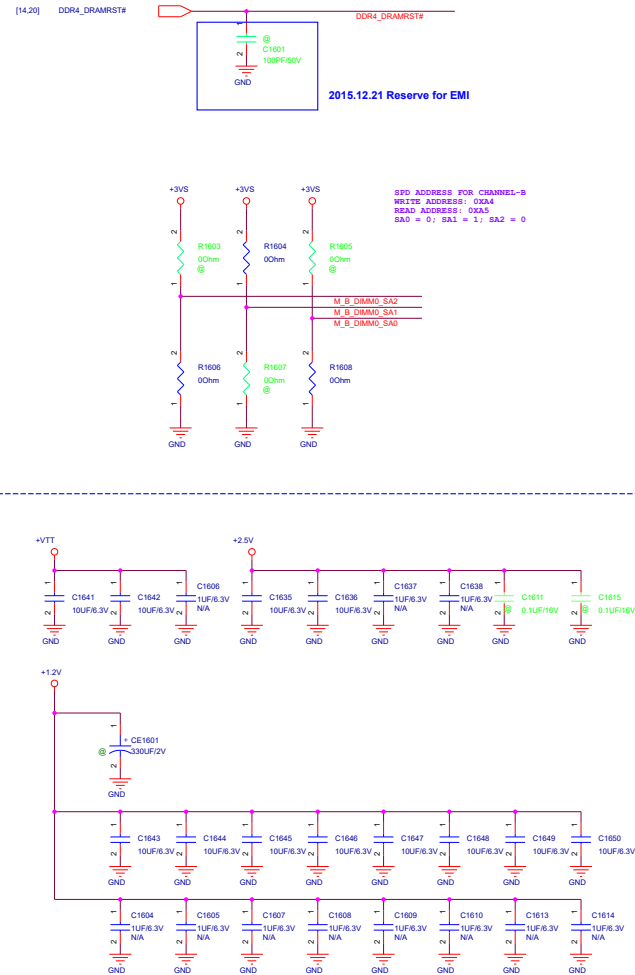
Sheet **12** of **103**

<Variant Name>

		Title : DDR4_TERMINATION	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size Custom	Project Name G711GW		Rev 1.0
Date: Tuesday, April 16, 2019		Sheet 13 of 103	

		Title : DDR4_ON-BOARD_A2	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size	Project Name		Rev
C	G711GW		1.0
Date: Tuesday, April 16, 2019		Sheet 15 of 103	

Main Board



DDR4_DIMM_260P
KEEP_A08_PULL UP IF NO PIN IN PCH

<Variant Name>


		Title : NB_****	
ASUSTeK COMPUTER		Engineer:	Gaming RD
Size A	Project Name G711GW		Rev 1.0
Date: Tuesday, April 16, 2019		Sheet 17	of 103

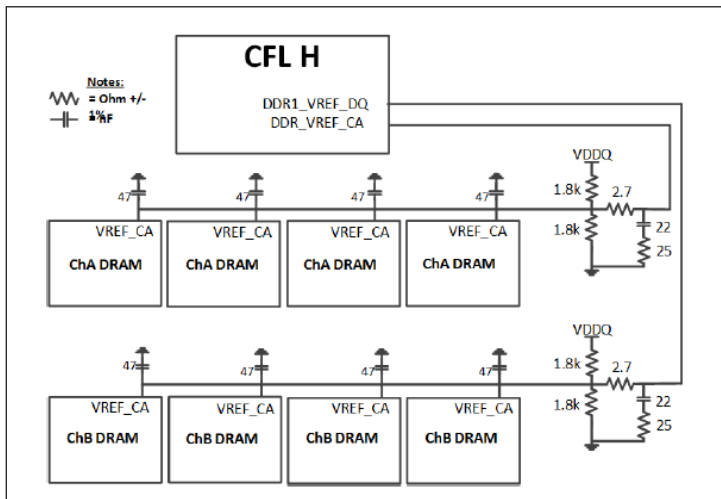
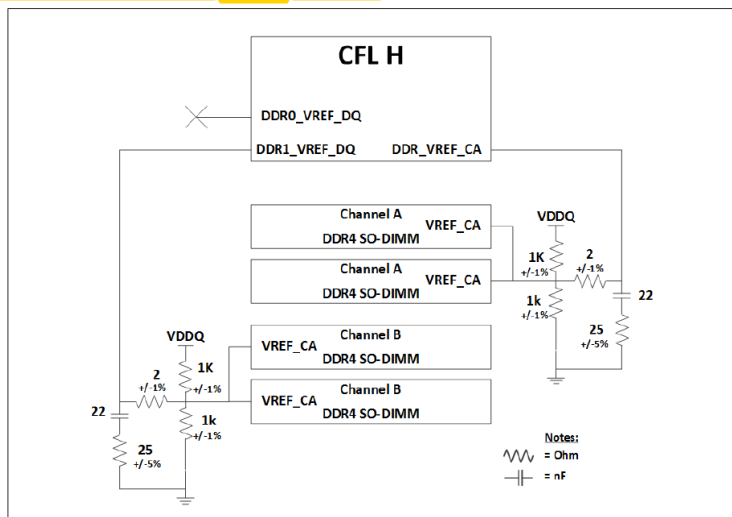
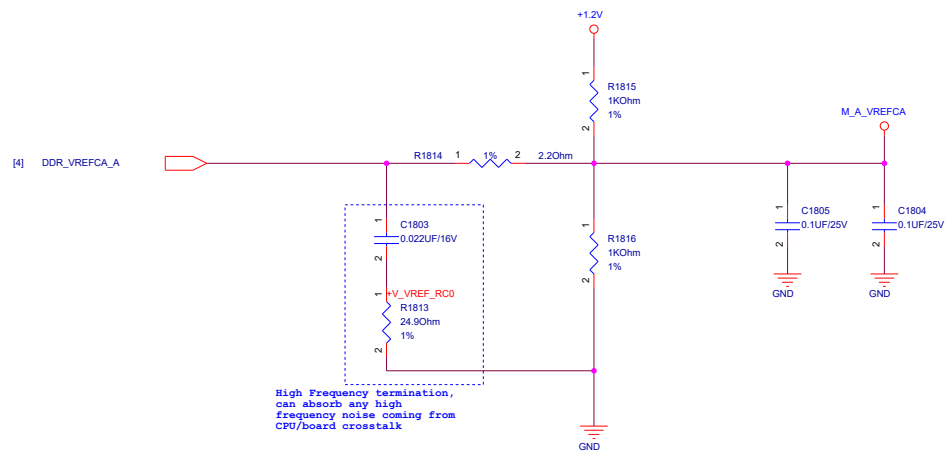
Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview

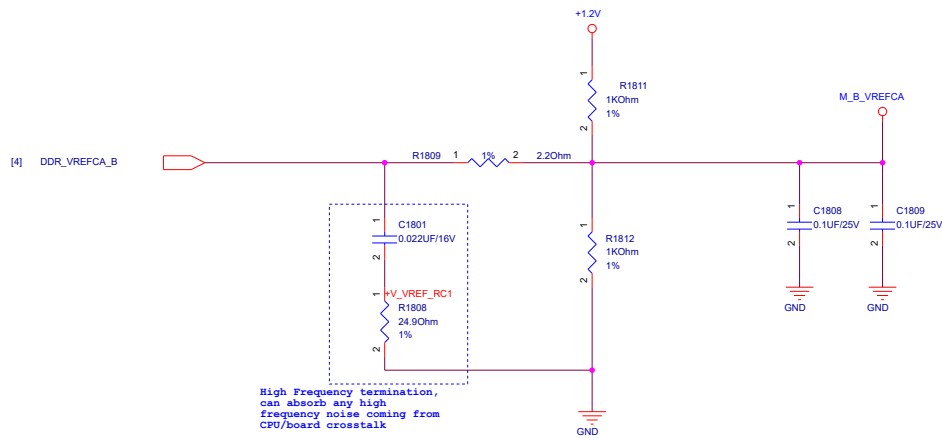
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview




Vref for CHA DIMM0



Vref for CHB_DIMMC



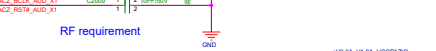
<Variant Name>

		Title : *****	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size	Project Name		Rev
C	G711GW		1.0
Date: Tuesday, April 16, 2019		Sheet 19 of 103	

HD Audio



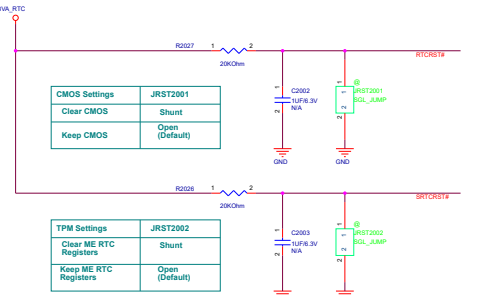
RF requirement



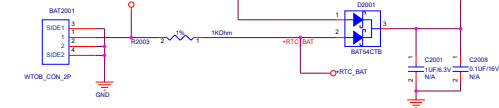
ACZ_SDOUT:
(1)PCH:
Internal PD 20k ohm,
VIN=0.35V, VIN=0.65~3.3V
(2)ALC269:
VIL<0.35+3.3V, VIN>0.65+3.3V

ACZ_SDOUT is a signal used for Flash
Descriptor security Override/ME debug mode
HIGH : get override/en, LOW : disable override

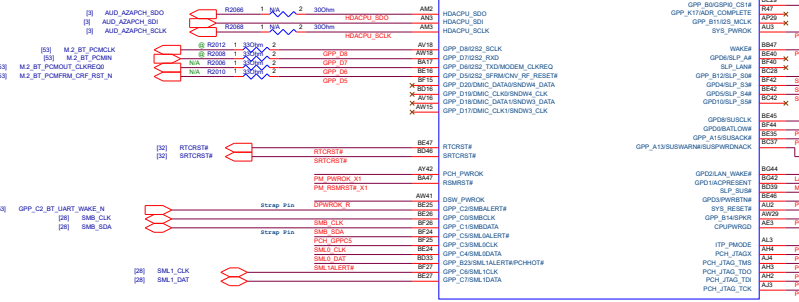
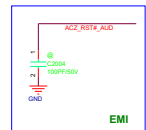
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
	+1.05VSD	+VCCST		
	+1.2V			
AC_BAT_SYS	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSD	+3VSD_PCH	+V3_3A_V1_3A_VCCP2D
	+3VS			



RTC battery

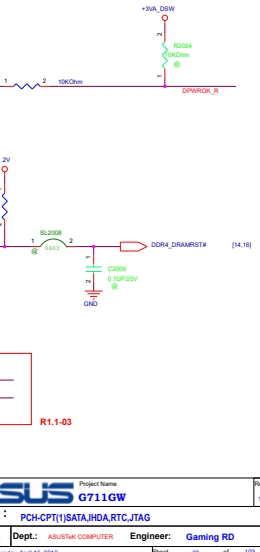
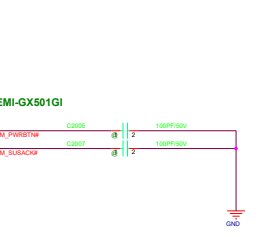
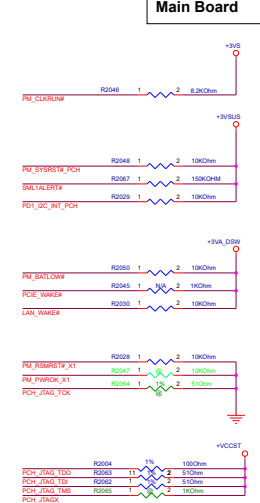
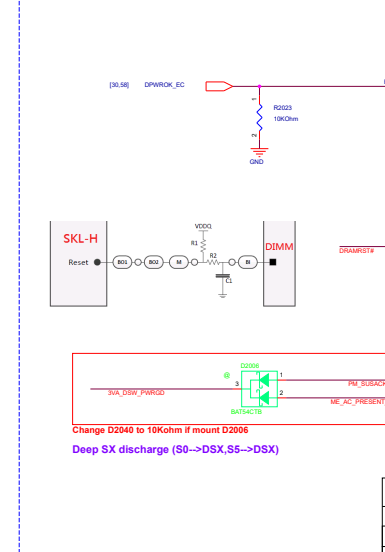
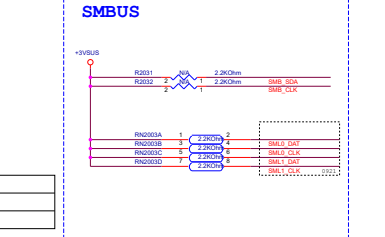
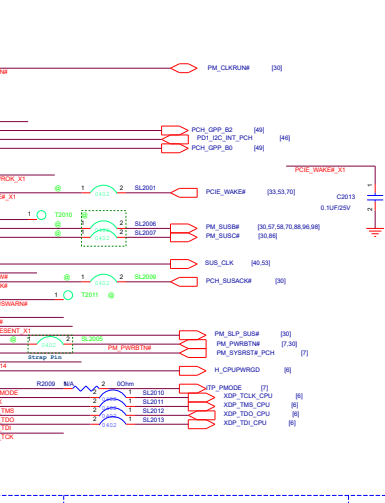
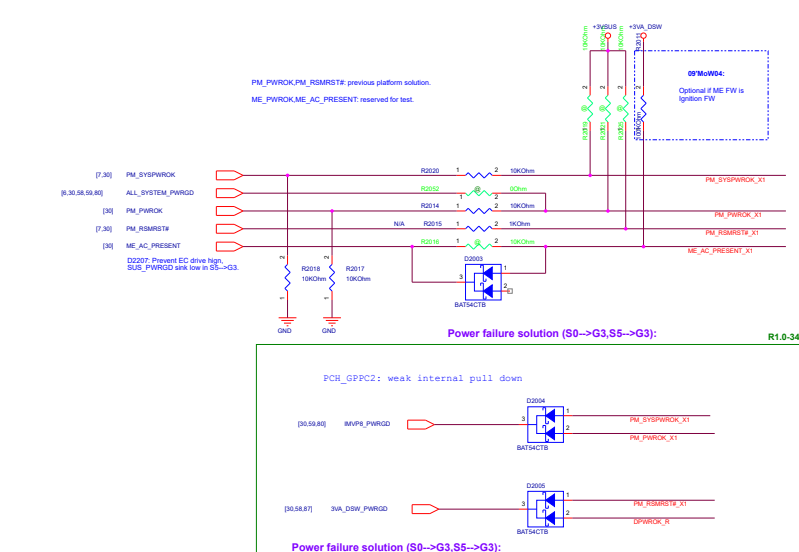


1st :12017-0002000
2nd :12027150002C
USE RTC Battery:
PIN: 0B100-00040500 BATT-LI CR1220 3V

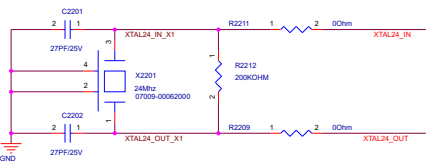


Power failure solution (S0->G3,S5->G3):

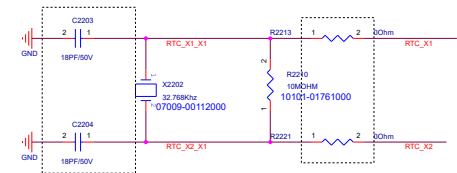
eSPI or LPC		TIS Confidentiality		Top Swap Override	
PU	eSPI	PU	Enable	PU	Enable
PD	LPC (default)	PD	Disable (default)	PD	Disable (default)



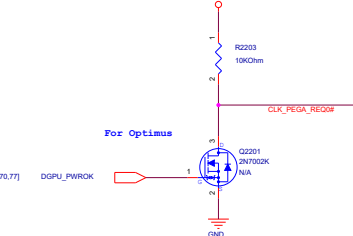
XTAL 24MHz



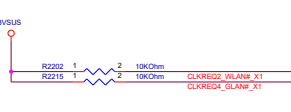
RTC CRYSTAL 32.768KHz



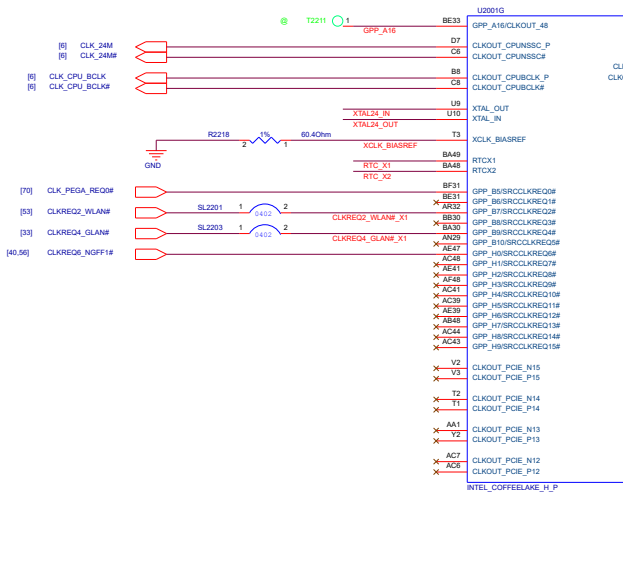
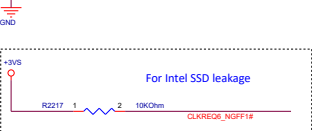
DGPU CLKReq#



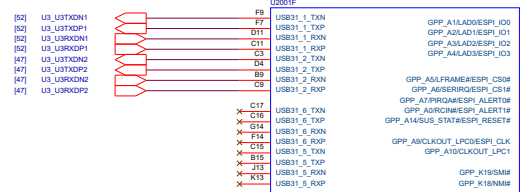
PCH CLKREQ Setting:



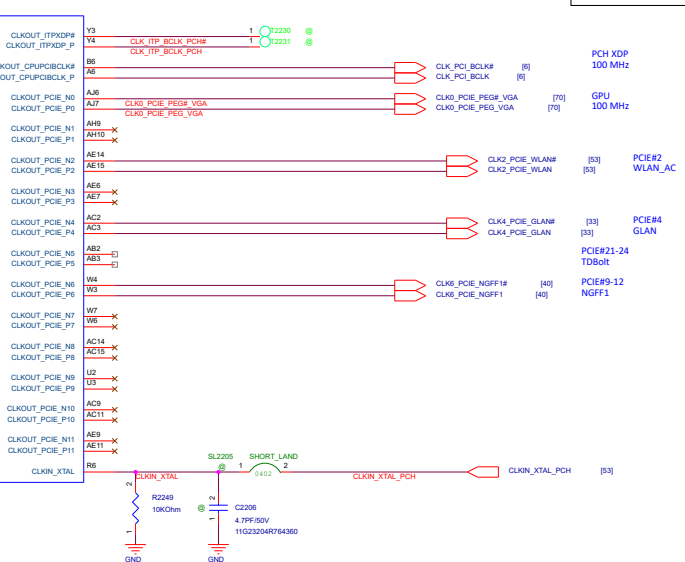
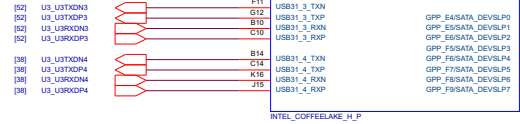
For Intel SSD leakage



MB USB3.0 : NIA

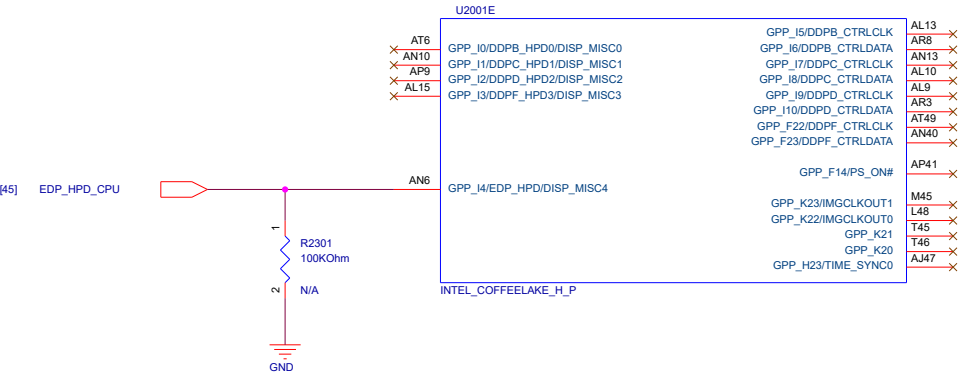


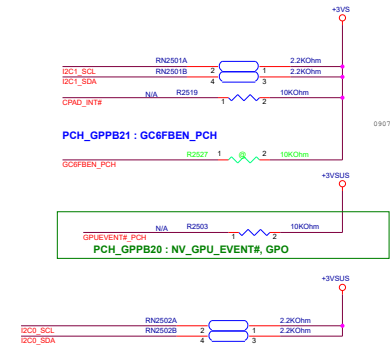
USB3.0 Port3 : NIA



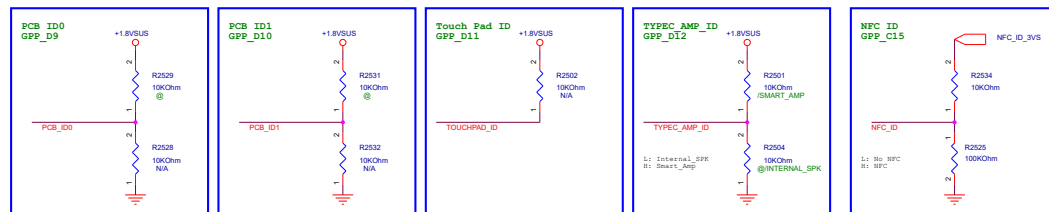
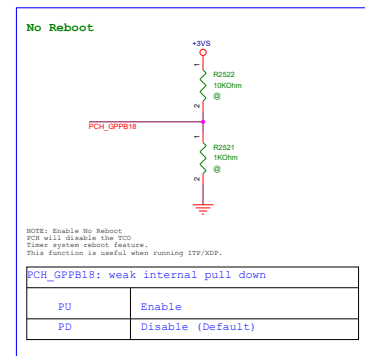
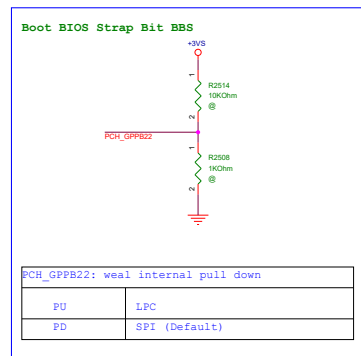
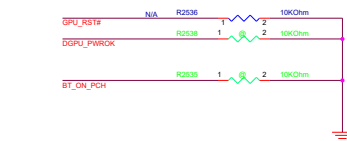
HPD0 to DP
HPD1 to HDMI
HPD2 to TBT
HPD3 to VGA
HPD4 to EDP Panel

DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected



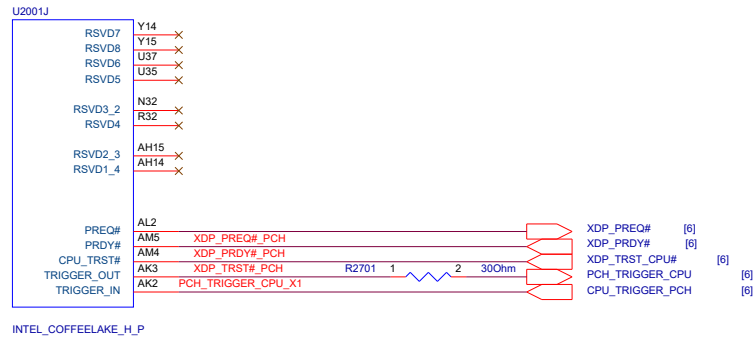
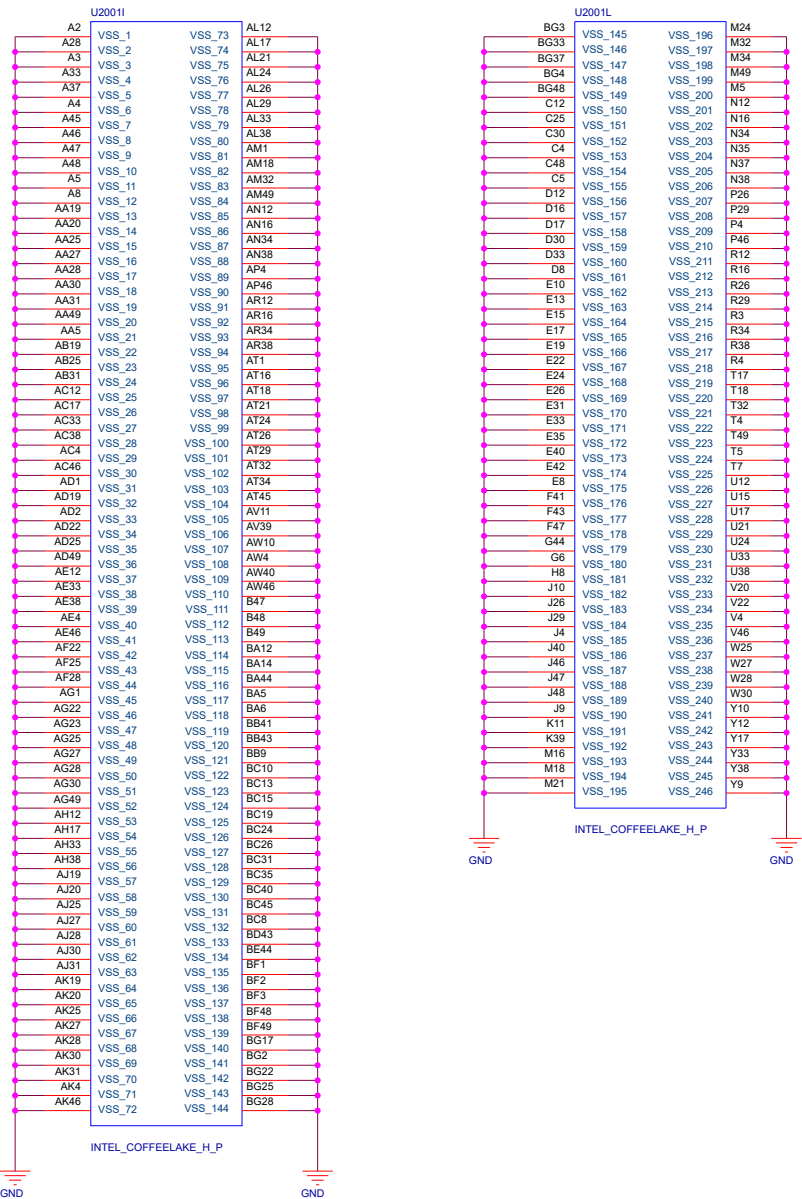


PCH_GPPC21 : DGPU_RST#
PCH_GPPC22 : DGPU_PWR_EN#

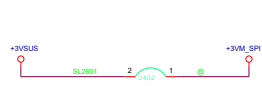


X-tal Frequency Select

- ### Cannon Lake PCH-IP
- XTAL_Freq_Select = GPP_H21
 - Pin Strap for XTAL frequency selection
 - An external 4.7k to 10k Ohm $\pm 5\%$ pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation
- ### Cannon Lake PCH-H
- XTAL_Freq_Select = GPP_J4
 - Pin Strap for XTAL frequency selection
 - An external 4.7k to 10k Ohm $\pm 5\%$ pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

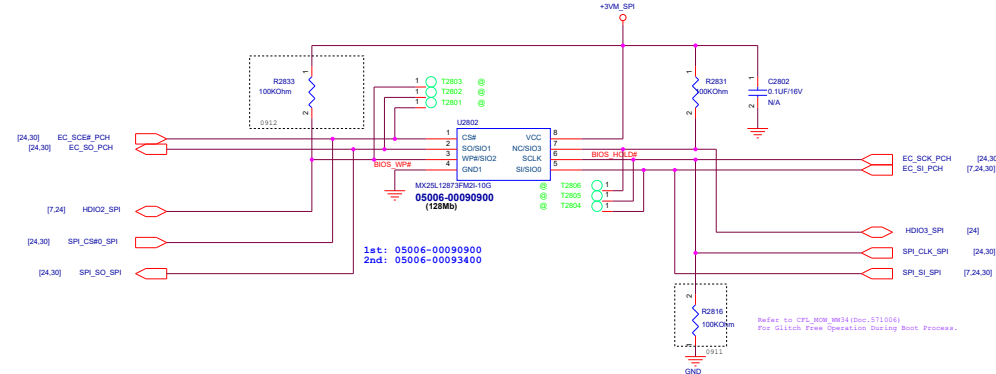


SPI Power



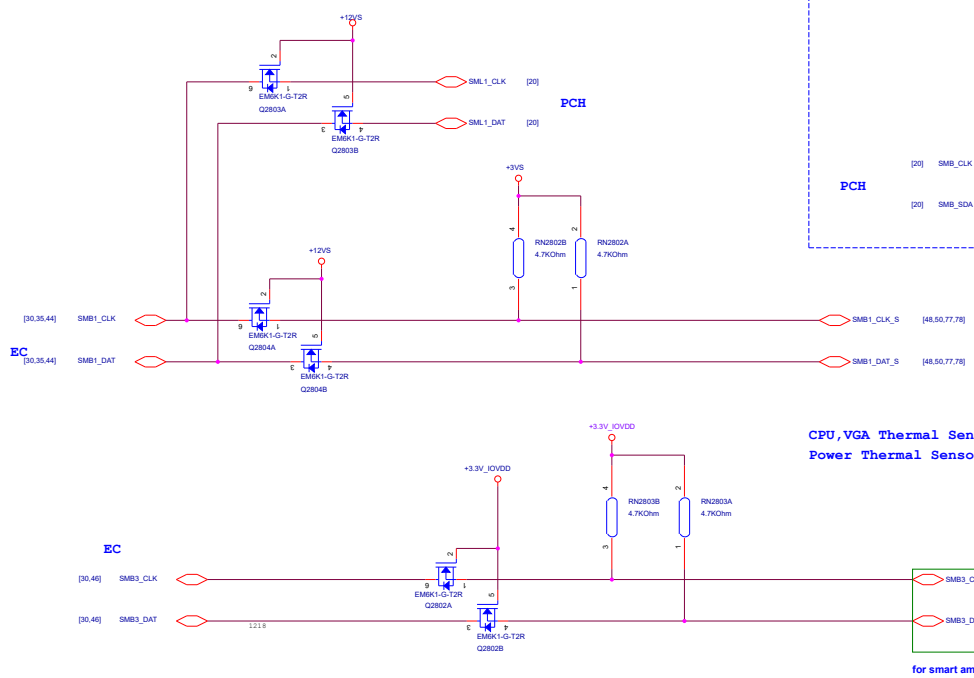
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873PM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

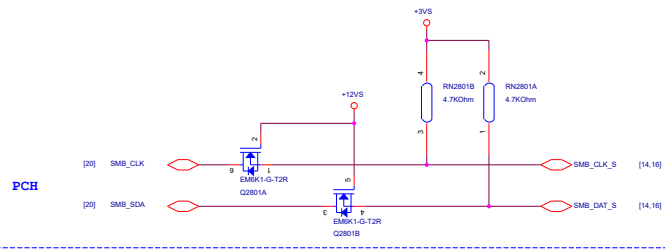


Refer to CPL_ROM_M534(Dec-571006)
For Glitch Free Operation During Boot Process.

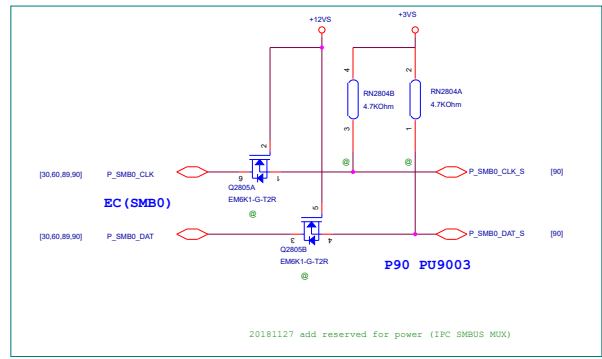
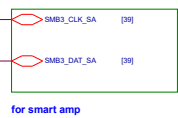
System Management Interface




SMBus Interface



CPU,VGA Thermal Sensor
Power Thermal Sensor



		Project Name G711GW		Rev 1.0
Title : PCH-XDP				
Size A	Dept.: ASUSTeK COMPUTER		Engineer: Gaming RD	
Date: Tuesday, April 16, 2019			Sheet 29	of 103

EC 8995

Only 3V Torrence

GPB[0,1,2,3,4,5,6]

GPC[3,4,5,6,7]

GPD[0,4,6,7]

GPE[4]

GPF[6,7]

GPH[7]

GPI[0:7]

GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPB0~GPA3

GPB0~GPB7

GPD0~GPD7

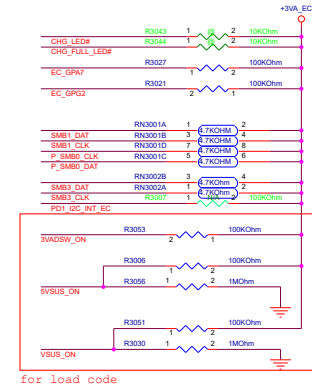
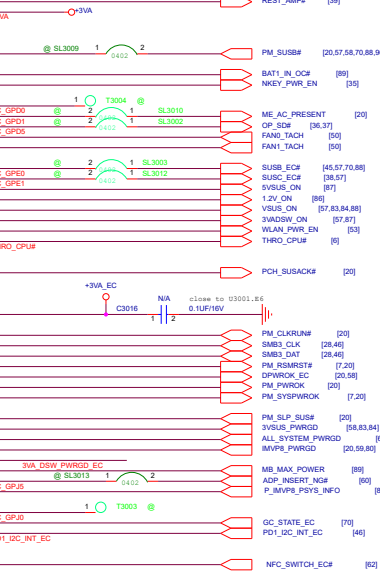
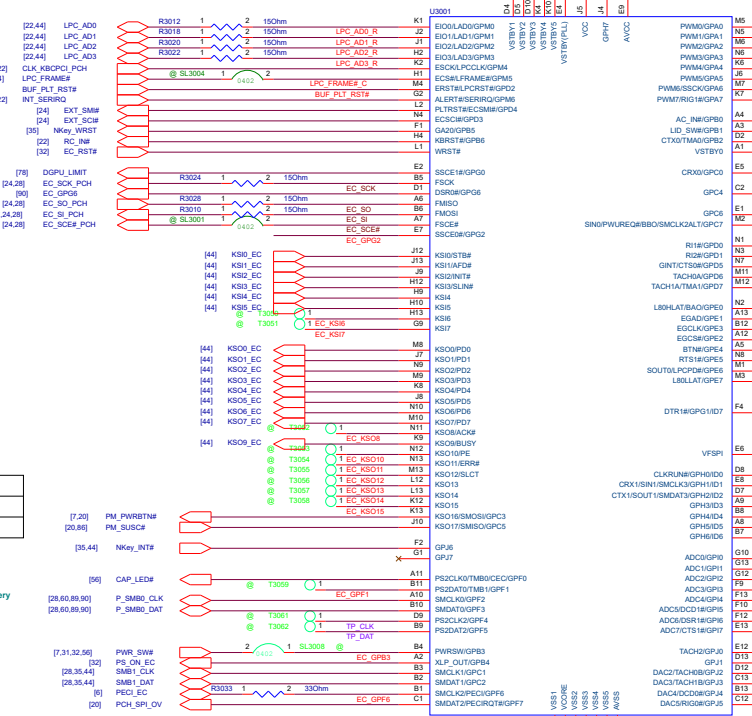
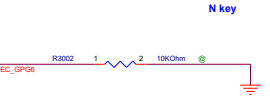
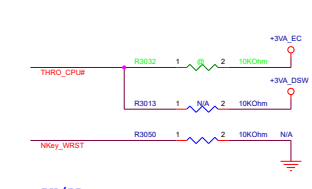
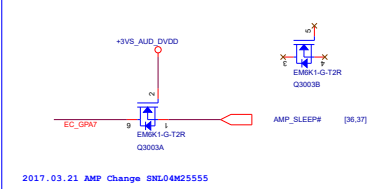
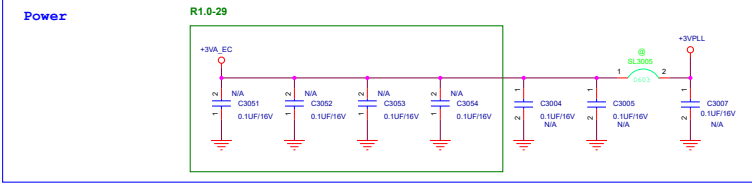
GPB0~GPB7

GPB0~GPF7

GPB0~GPB6

GPJ0~GPJ5

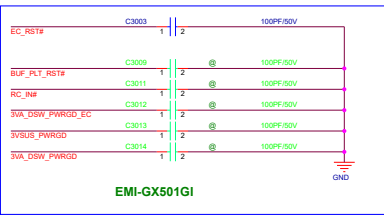
EC Require



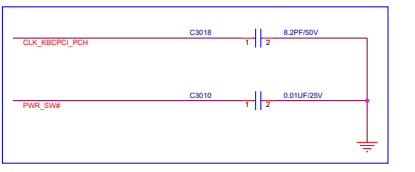
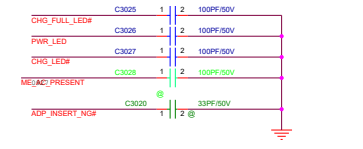
ITE Version	ASUS P/N
IT8225VG/BX	06037-00260000

Battery

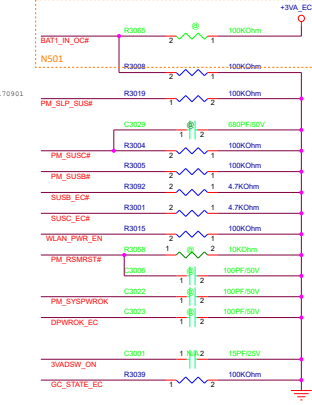
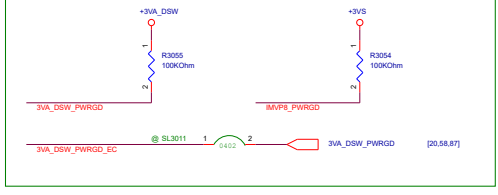
Thermal sensor



For EMI



R1.0-34

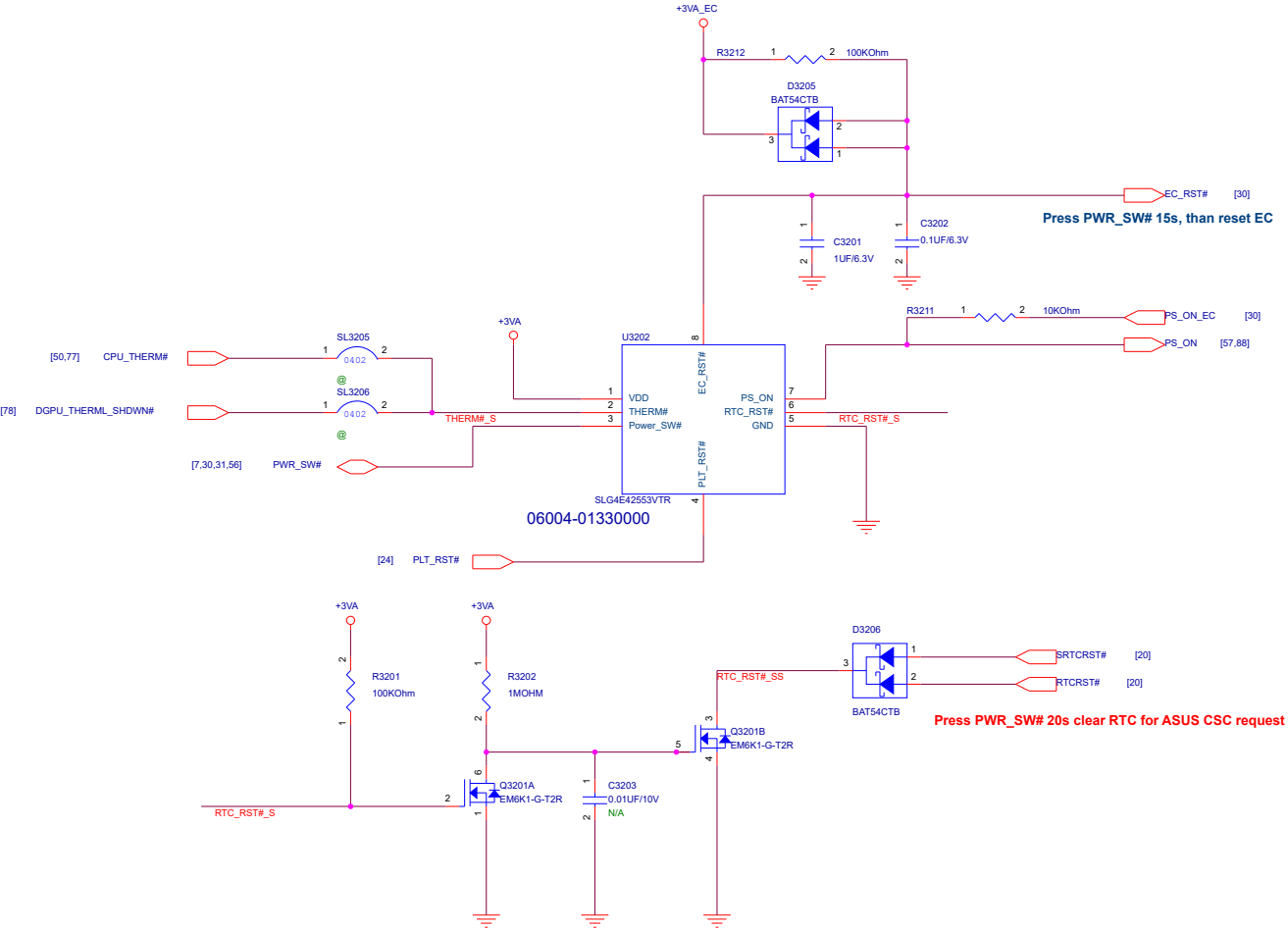


<Variant Name>

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

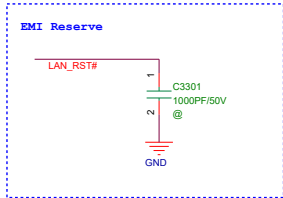
<https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components>
UX362FA R1.3 board will verify this circuit 7/E



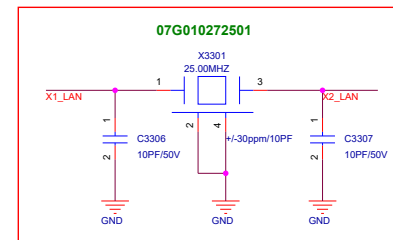
The distance from U3301.24 to L3301 within 200 mil.

The distance from L3301 to C3347 within 200 mil.

33/34 pin ground pad
need ground via



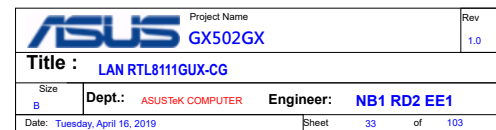
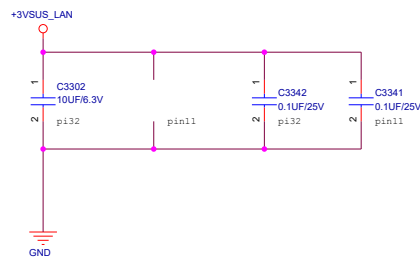
CLKREQ_GLAN#, PCIE_WAKE#
should be PU on the host side

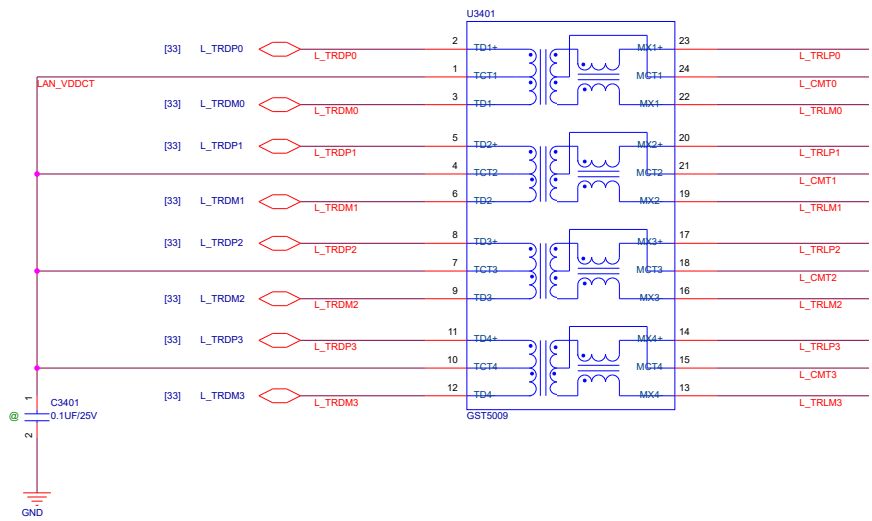


1st: P/N:07G010272501 TXC/7V25000011

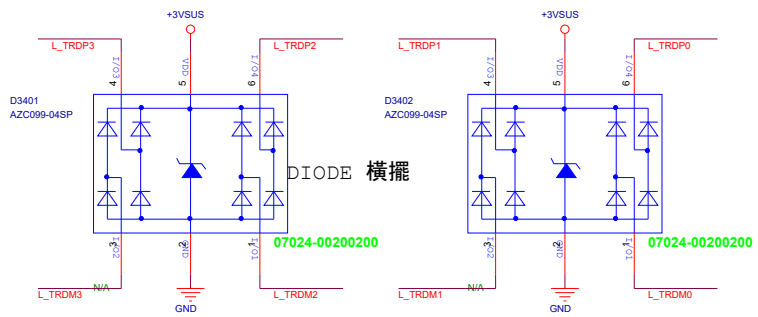
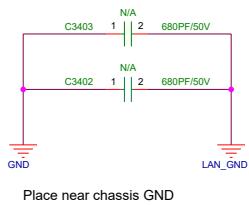
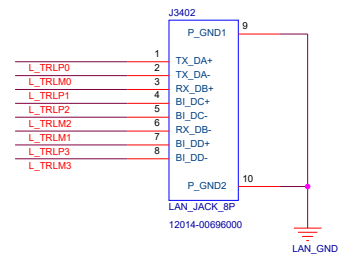
2nd: P/N:07G010952500 HOSONIC/E3ER

Realtek suggests 3V_LAN raise time >1ms

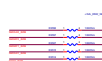
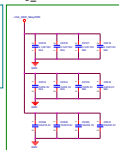
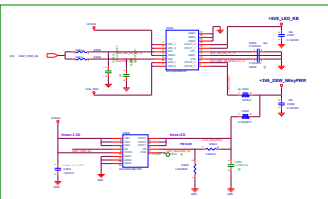




LAN Connector

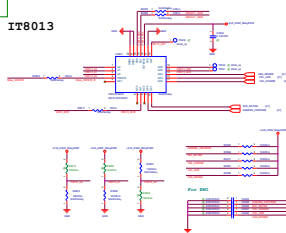


D3401,D3402 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

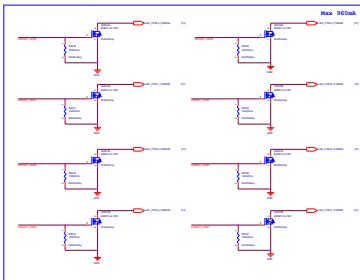


IT8299E

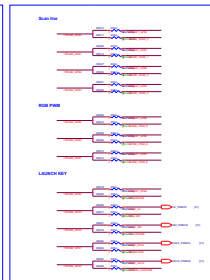
IT8013



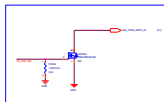
KB RGB Per Key LED



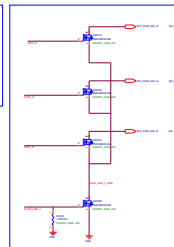
KB RGB co-layout



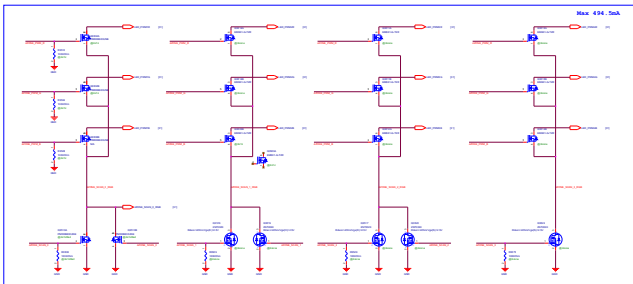
TP LED



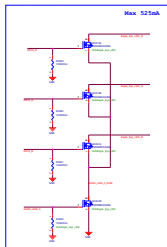
NFC RGB LED



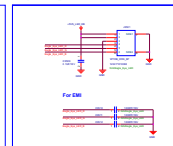
KB RGB 4Zone and 12Zone LED

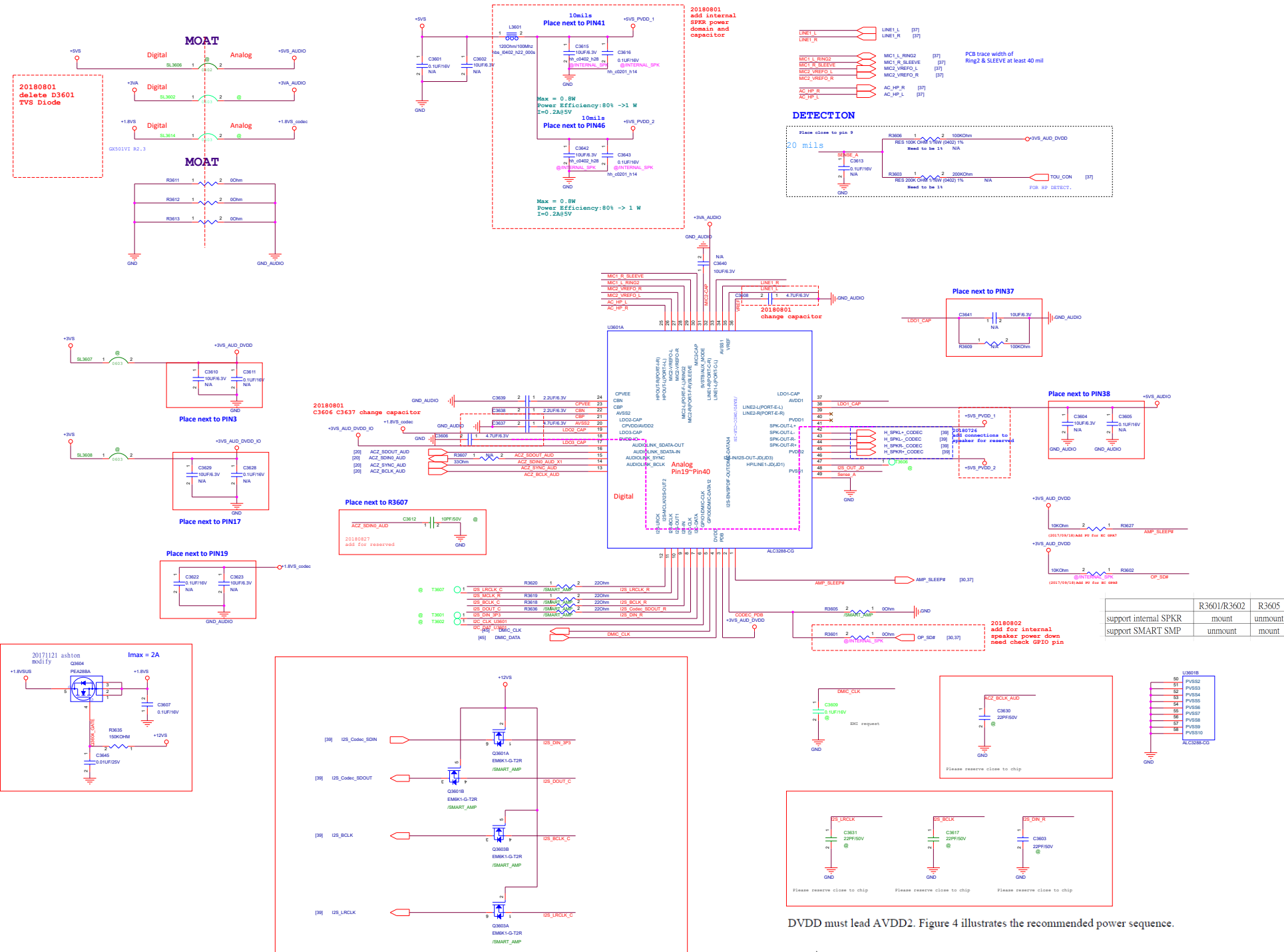


Eagle Eye LED



Eagle Eye LED Conn





DVDD must lead AVDD2. Figure 4 illustrates the recommended power sequence.

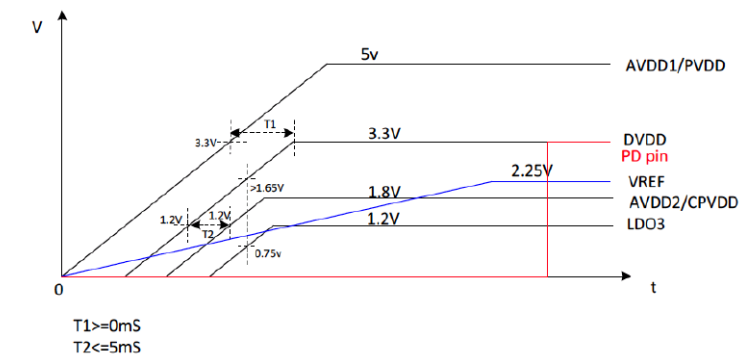
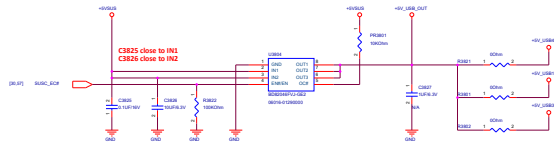


Figure 4. Power sequence

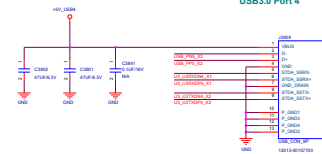


USB3.0_PORT4 (Support USB Charge Circuit)

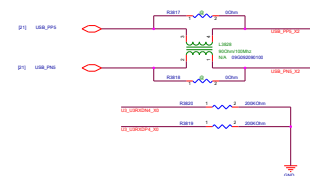
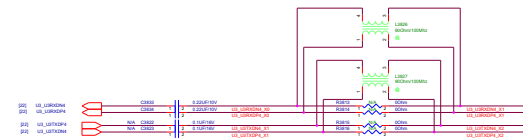
J3809 USB3.0 Connector
1st Source: P/N: 12813-0018309 FOXCONN/UEA1111-AM4862-7H
2nd Source: P/N: 12813-0088408 SINGATRON/2J8-4086-31810F

USB Charge Circuit (For PORT 4)

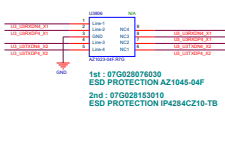
USB3.0 Port 4



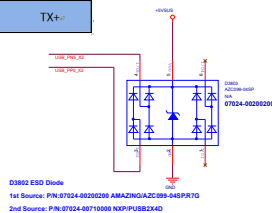
USB3.0_PORT4

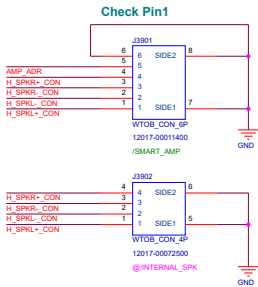
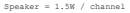
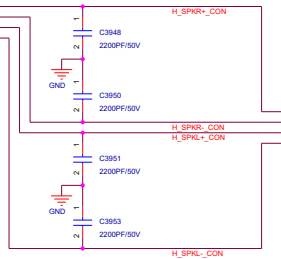
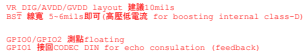
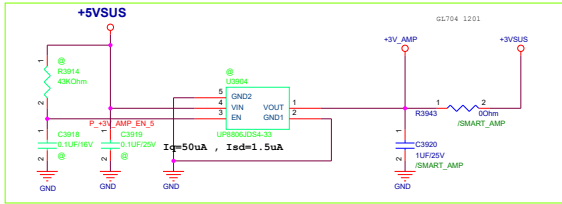


USB3.0 ESD-Protection

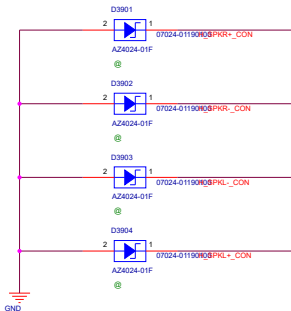


USB3.0 Pin define	
1-	VBUS-
2-	D-
3-	D+
4-	GND-
5-	RX-
6-	RX+
7-	GND-
8-	TX-
9-	TX+

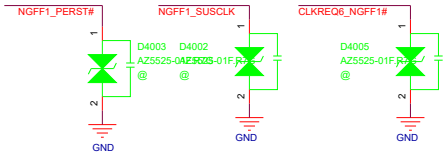





20180823
add



PCIe12/SATA1a
GFF1 PCIe Lane0
SATA Port1



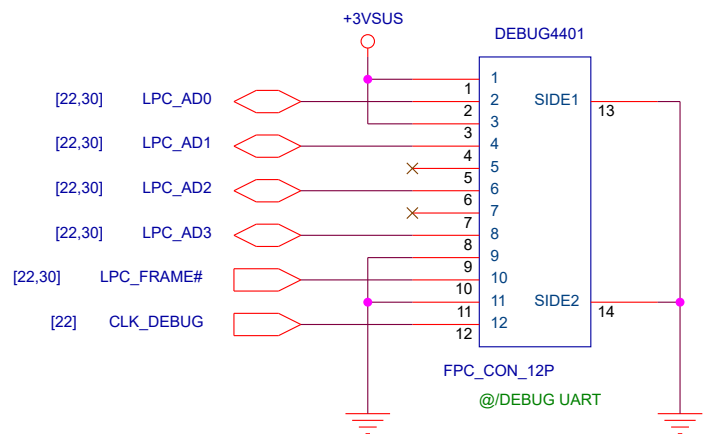
<Variant Name>

		Title : CB_*****	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size	Project Name		Rev
C	G711GW		1.0
Date: Tuesday, April 16, 2019		Sheet 41 of 103	

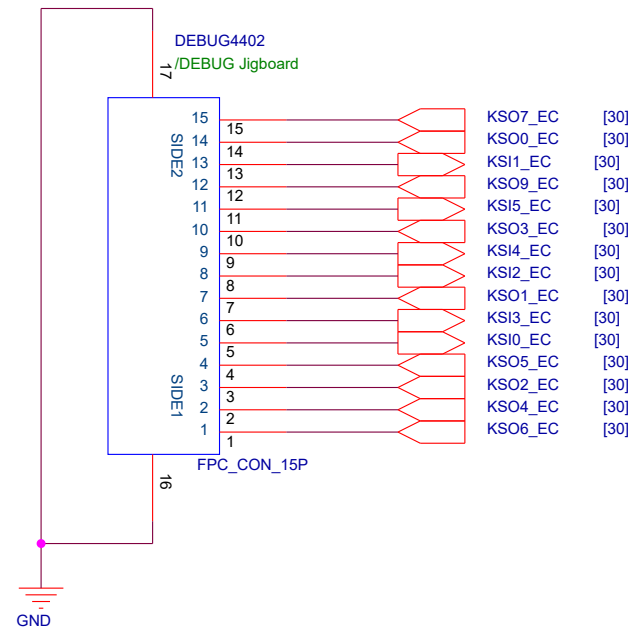
<Variant Name>

		Title : HDMI_DP_Switch	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size	Project Name		Rev
C	G711GW		1.0
Date:	Tuesday, April 16, 2019	Sheet	42 of 103

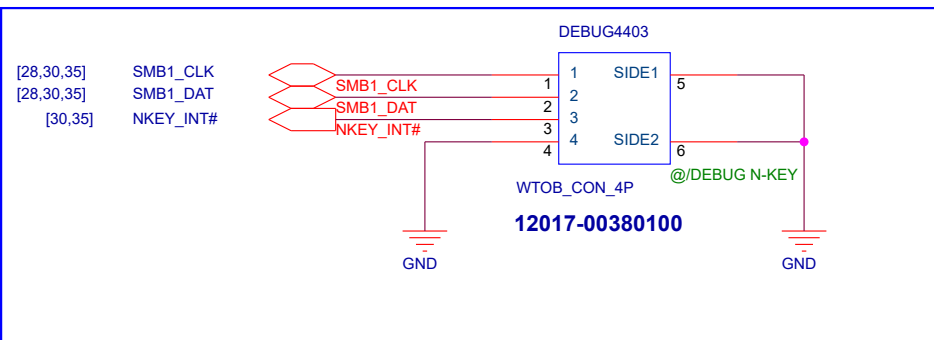
LPC Debug Port




ER2 stuff



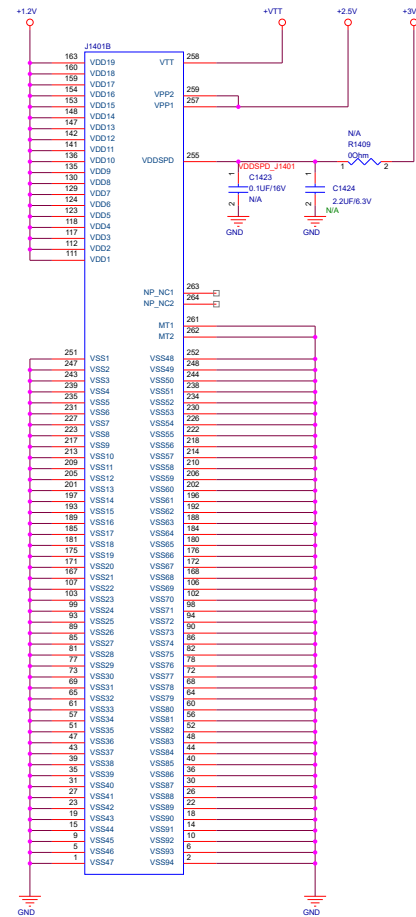
N-KEY Debug Connector



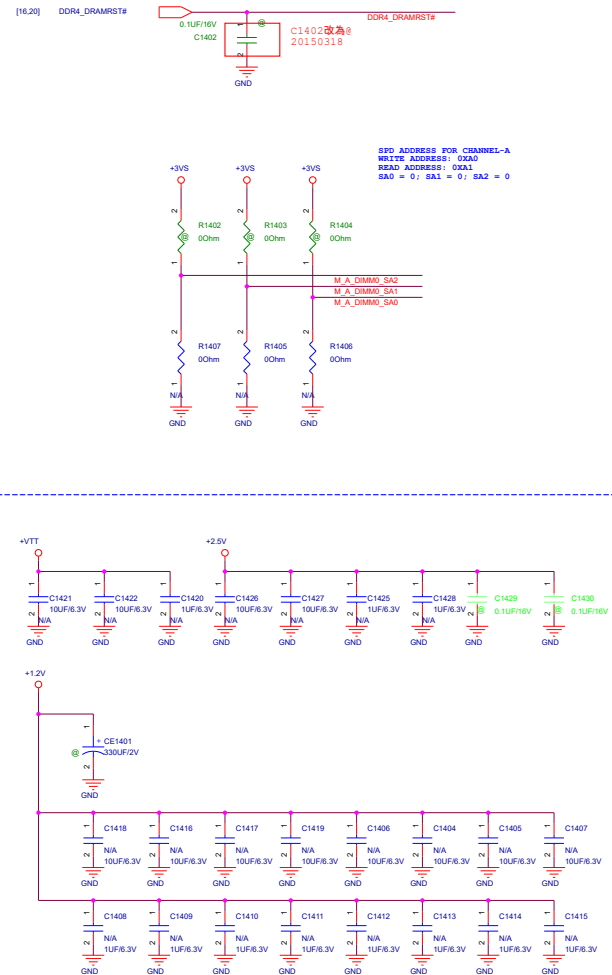
<Variant Name>

		Title : DEBUG_LPC	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size A	Project Name G711GW		Rev 1.0
Date: Tuesday, April 16, 2019		Sheet 44 of	103

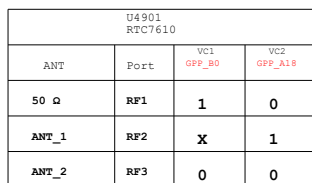
[16,20] DDR4_DRAMRST#



EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



ANT 2



X:	don't care
0:	-0.2v~0.3v
1:	1.6v~3.6v

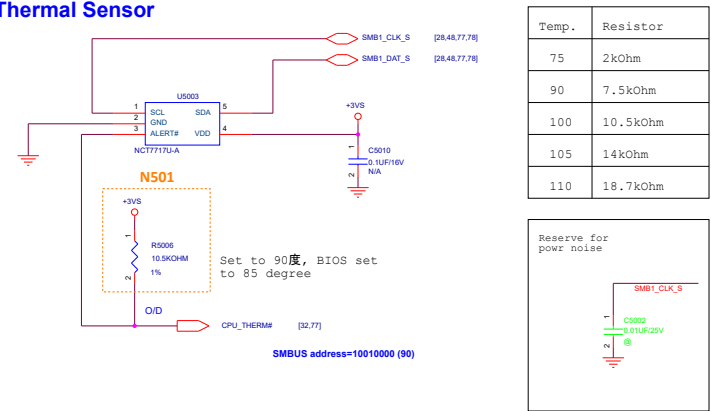
ANT 3



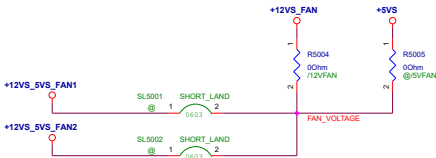
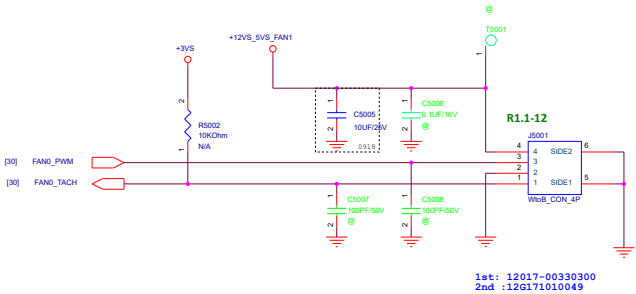
U4902 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Q	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X:	don't care
0:	-0.2v~0.3v
1:	1.6v~3.6v

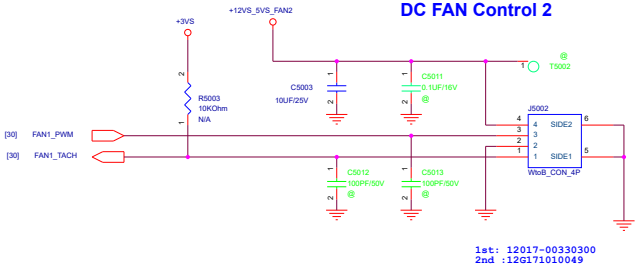
CPU Thermal Sensor



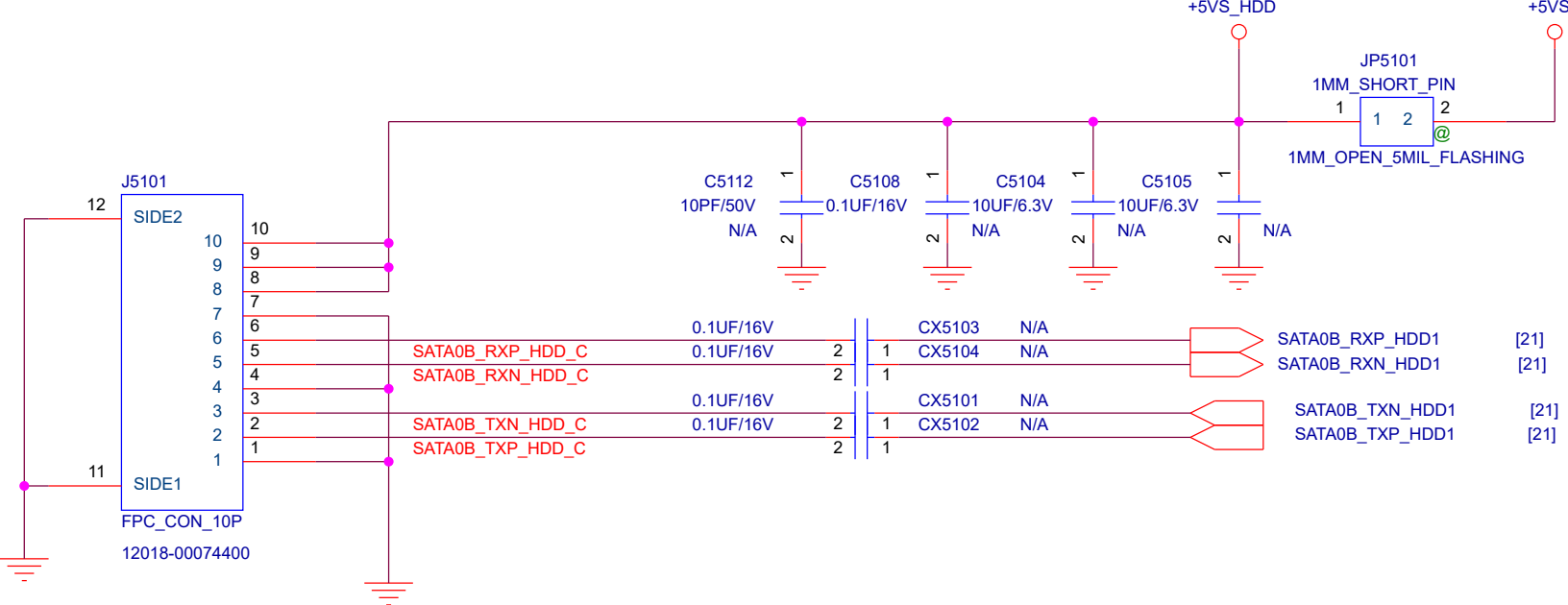
DC FAN Control 1



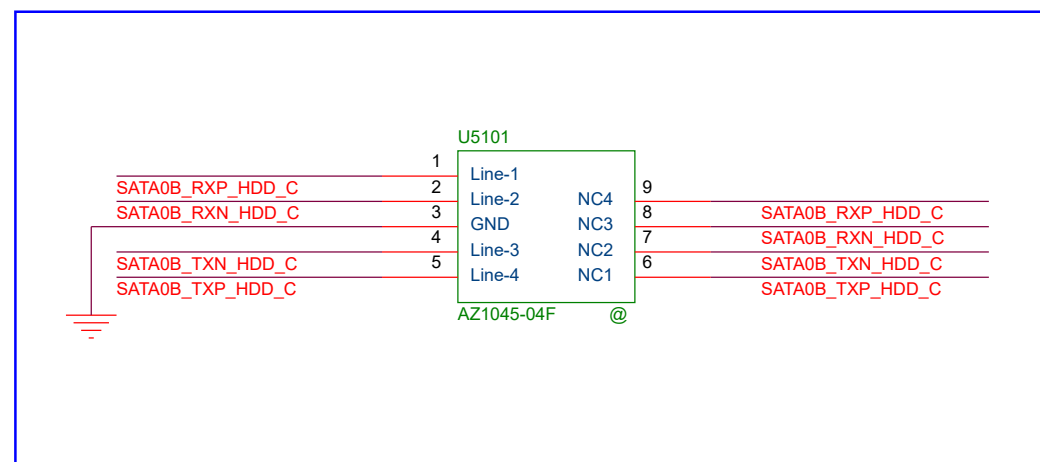
DC FAN Control 2




<Variant Name>

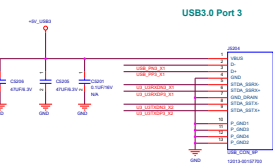
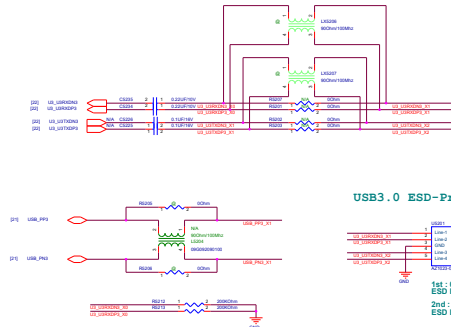
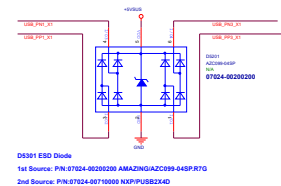
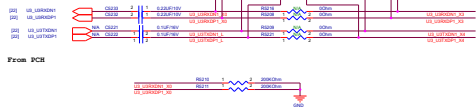
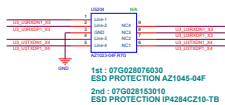
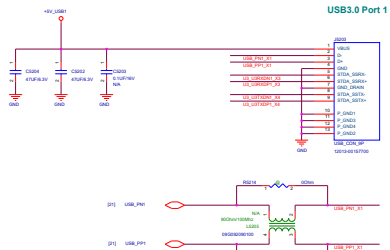


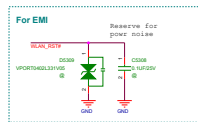
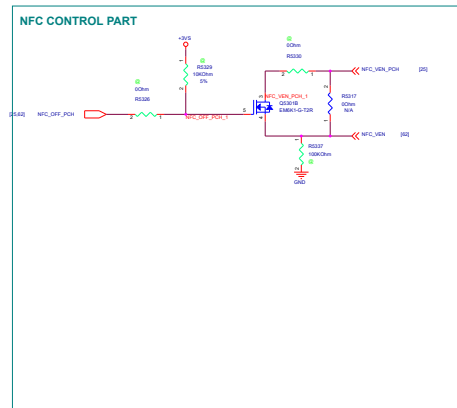
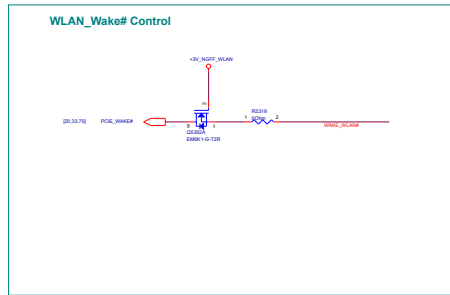
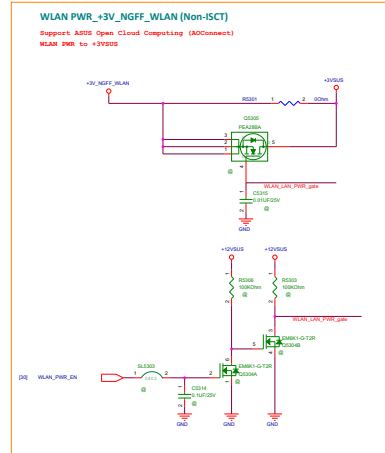
PIN #	Description
1	5V
2	5V
3	5V
4	GND
5	RX+
6	RX-
7	GND
8	TX-
9	TX+
10	GND



<Variant Name>

		Title : XDD_HDD & ODD CON	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size A	Project Name G711GW		Rev R1.0
Date: Tuesday, April 16, 2019	Sheet 51	of 103	




U
B

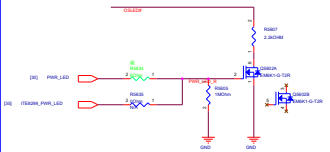
<Variant Name>

		Title :	USB3_*****
ASUSTeK COMPUTER		Engineer:	Gaming RD
Size	Project Name	Rev	
Custom	G711GW	1.0	
Date:	Tuesday, April 16, 2019	Sheet	54 of 503

<Variant Name>

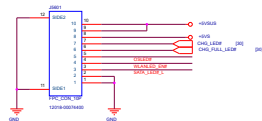
		Title : IO Con. to MB	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size	Project Name		Rev
Custom	G711GW		1.0
Date: Tuesday, April 16, 2019		Sheet 55 of 103	

OS LED

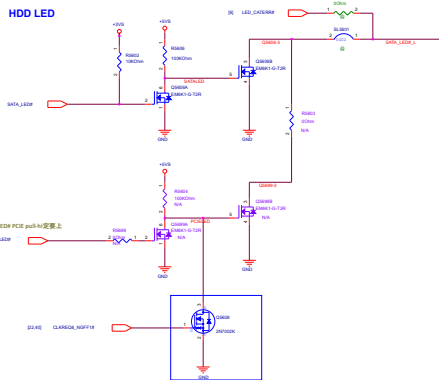


Charger LED

LED Board



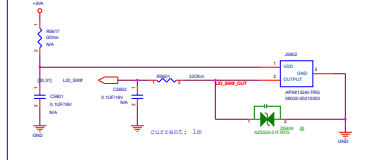
2014/05/29 Add HDD & SSD LED control circuit.



BT/WLAN LED

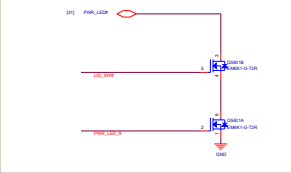


HALL SENSOR

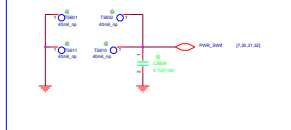


CAP LED

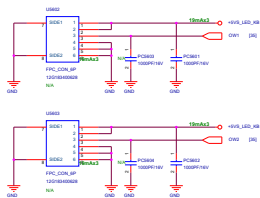
Power KEY LED



POWER button



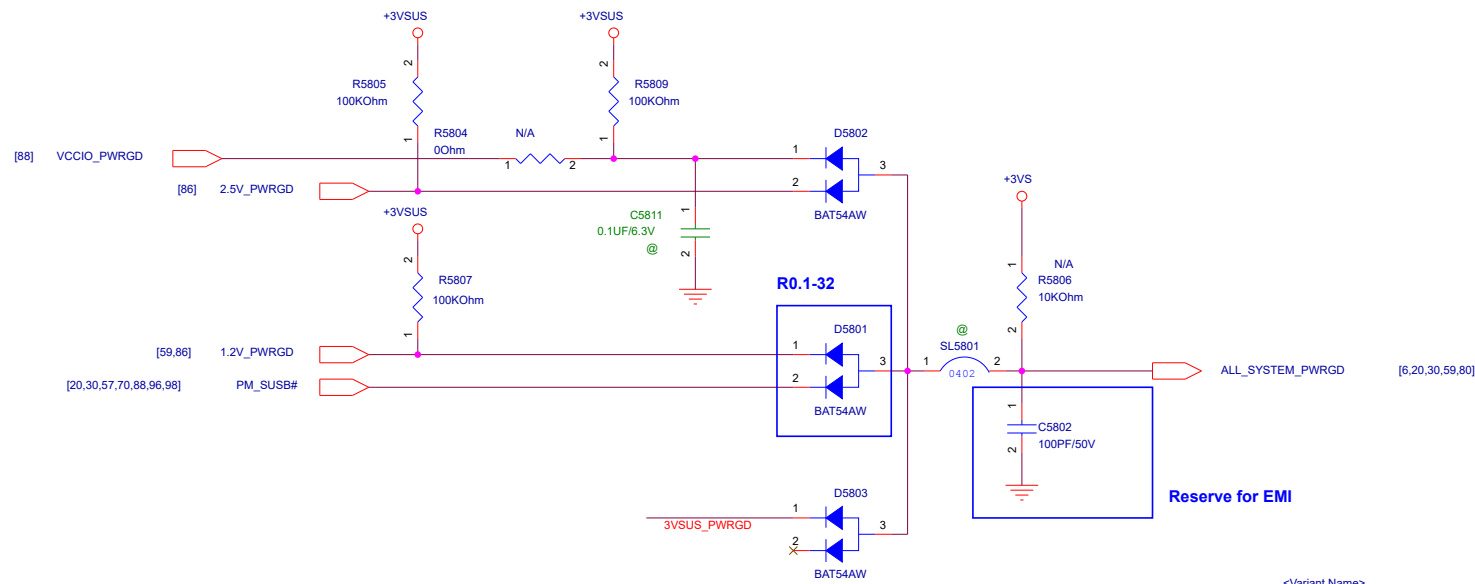
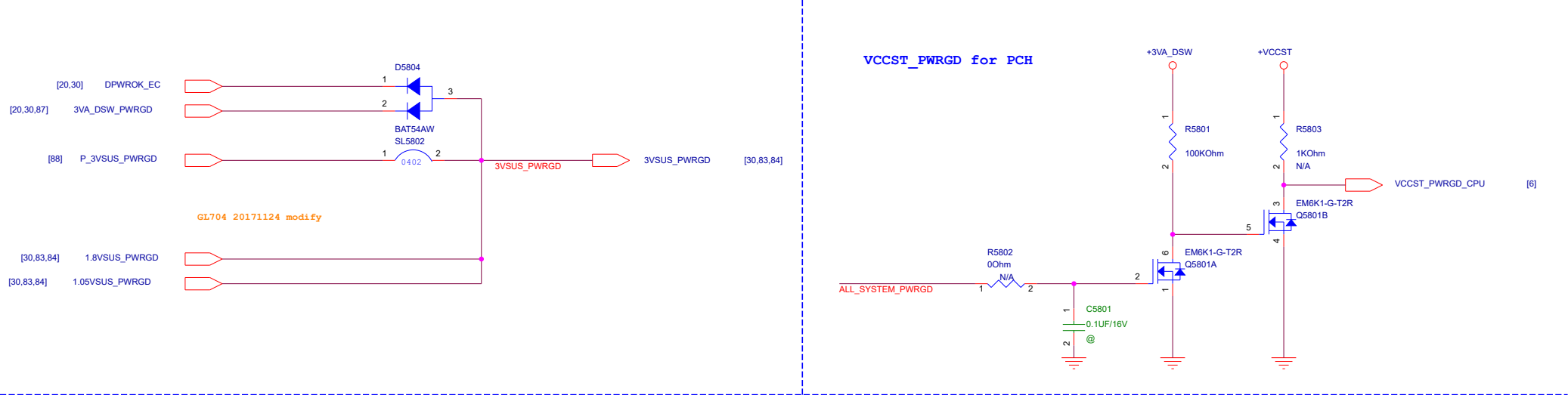
One-wire Connect to LED



Project Name

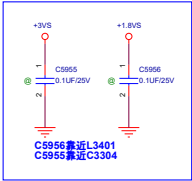
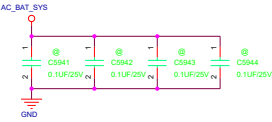
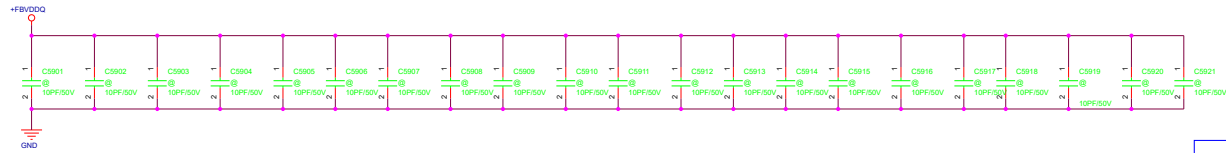
ASUS		Title : LED A UB
Engineer: Gaming RD		
Rev	Project Name	
01	G711GW	
01	01/11/2015	



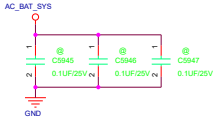


<Variant Name>

ASUS		Title : Power Protect	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size	Project Name	G711GW	Rev
Custom			1.0
Date: Tuesday, April 16, 2019		Sheet	58 of 103

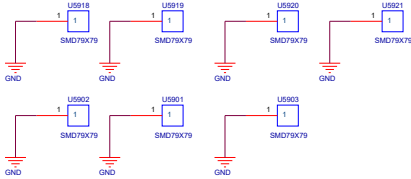


EMI

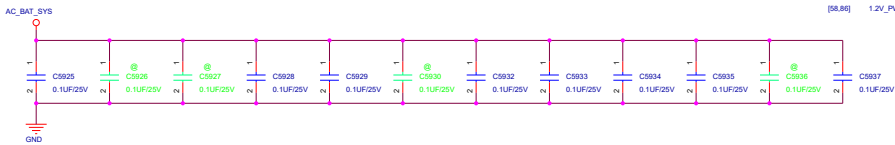
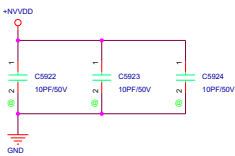


CLIP

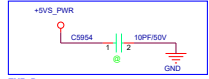
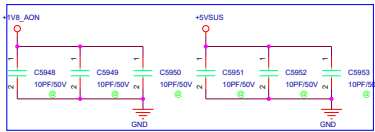
13NB0I40T01011



EMI



EMI

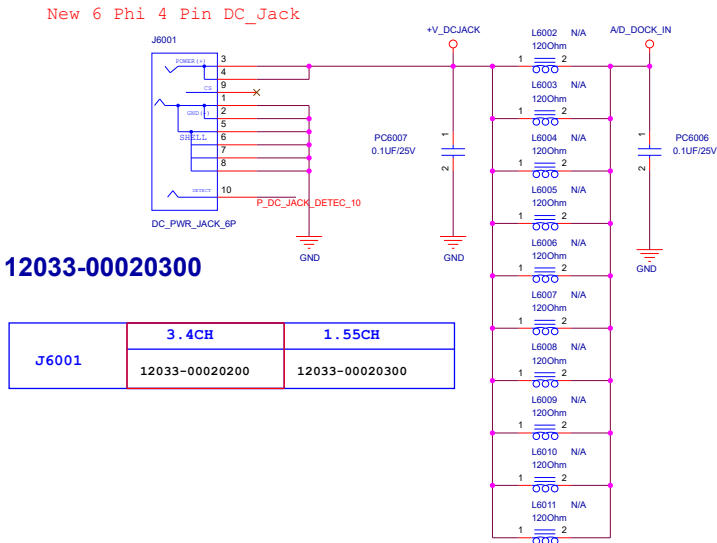


EMI Reserve

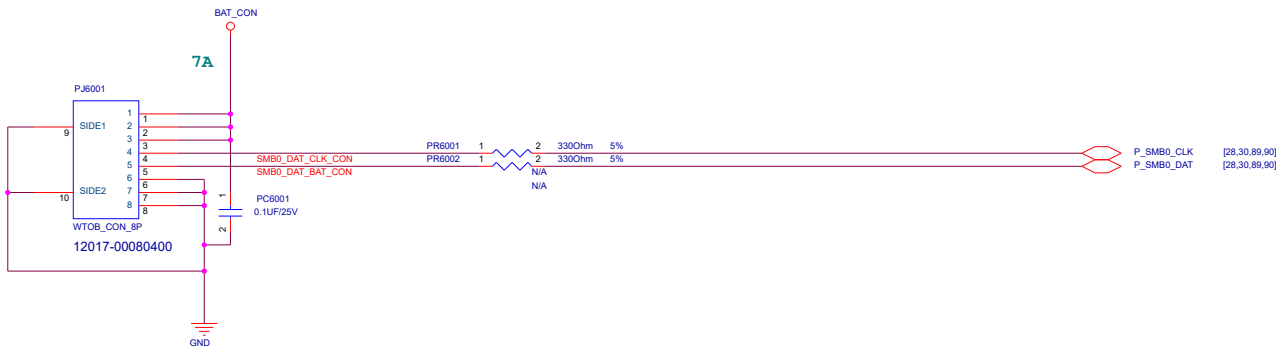
<Variant Name>

DC-IN Connector

DC Jack使用請詢用River_Hsu

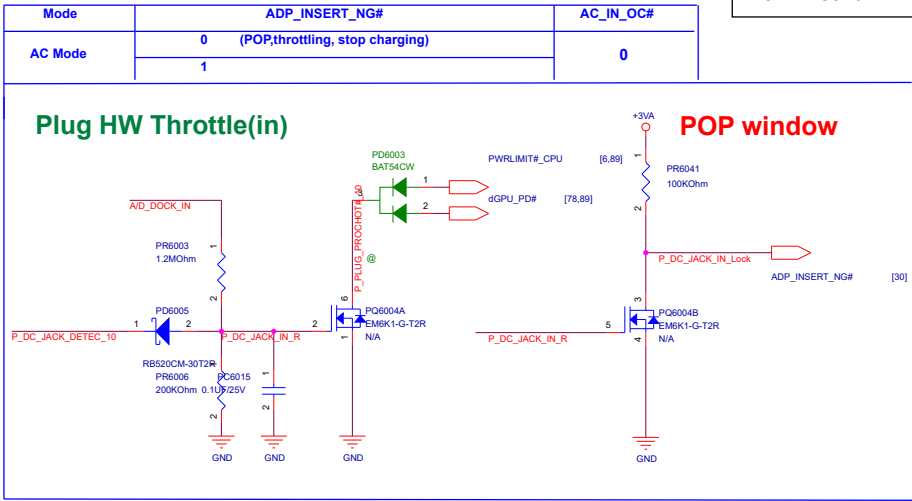


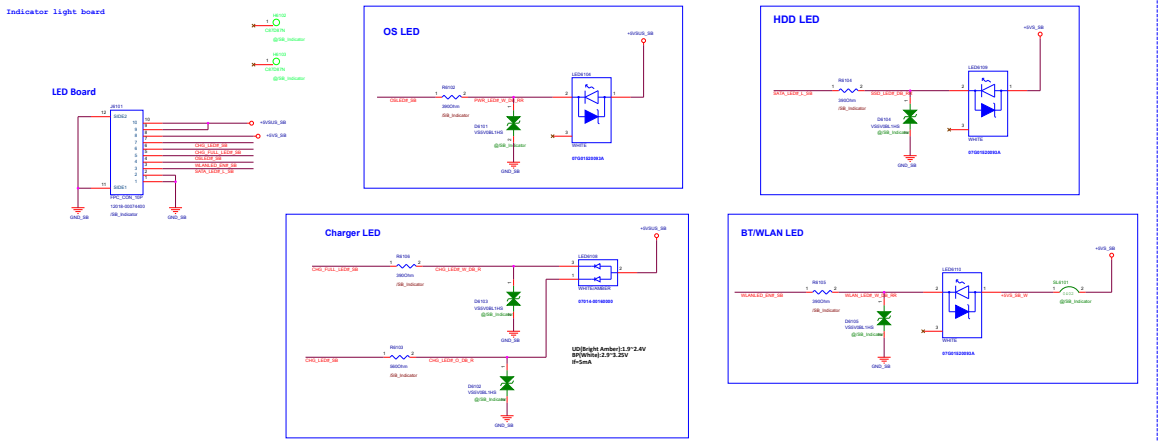
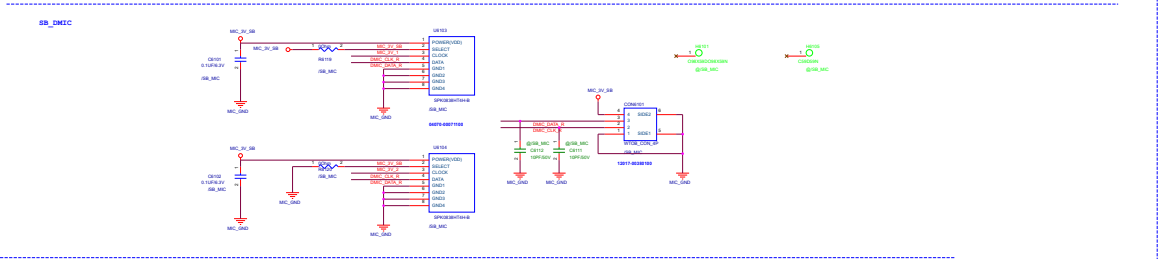
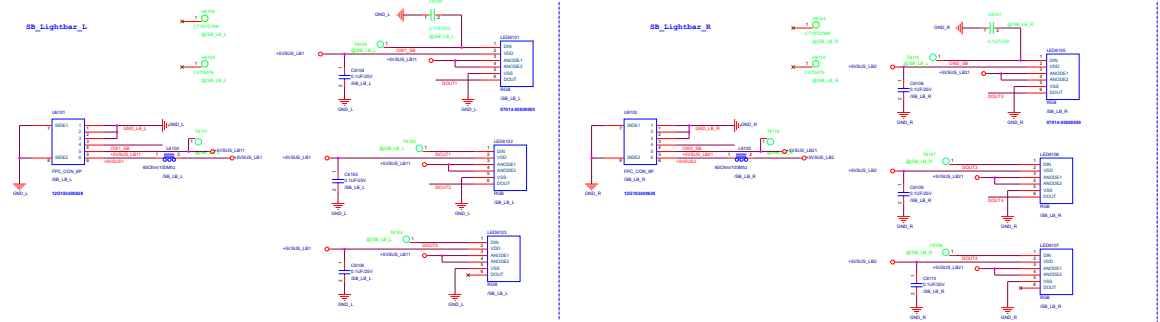
Battery Connector

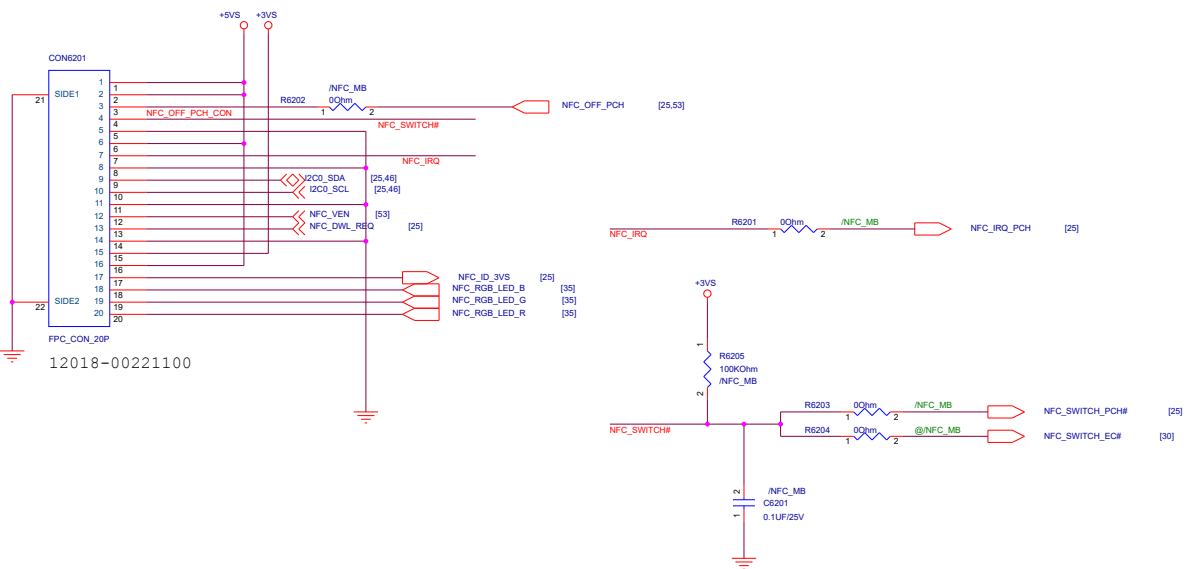


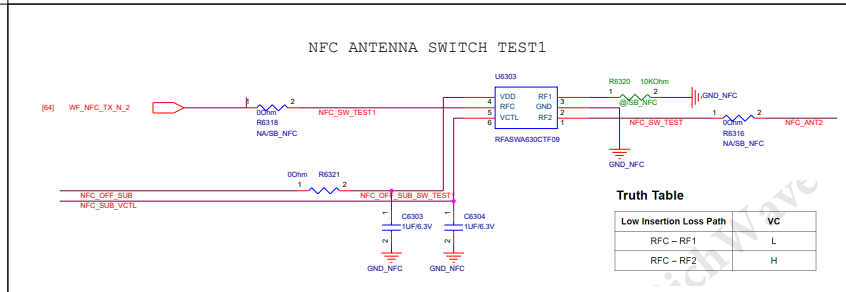
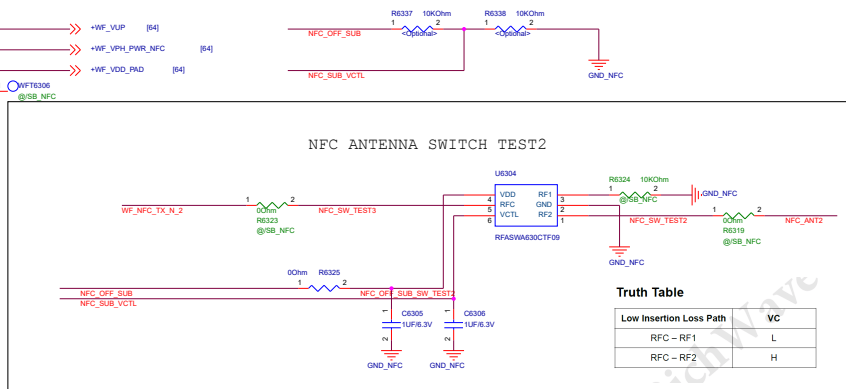
Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!

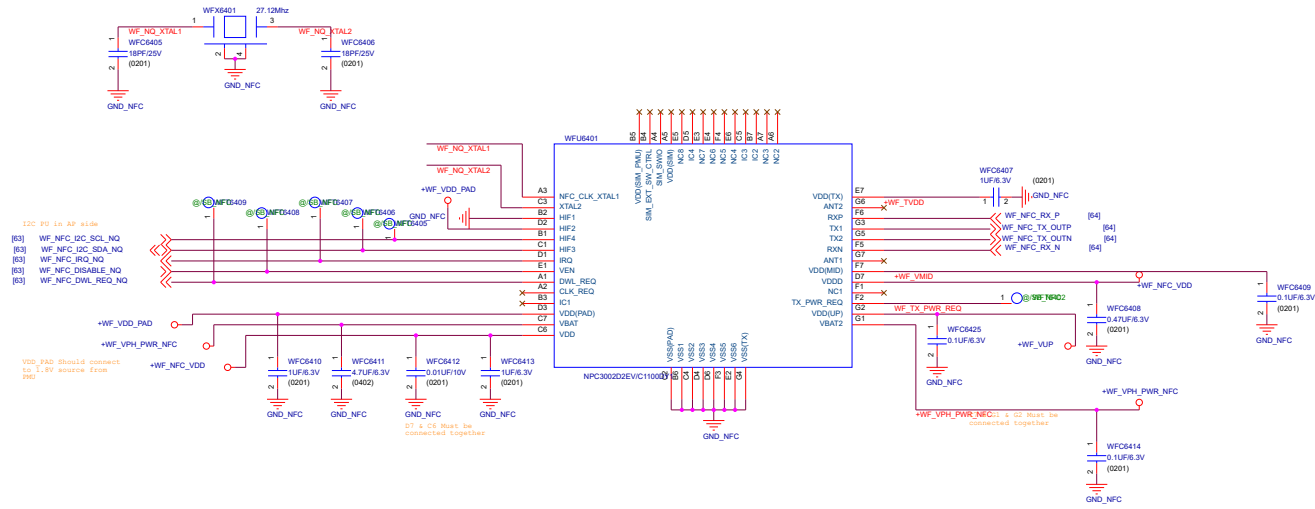
Main Board



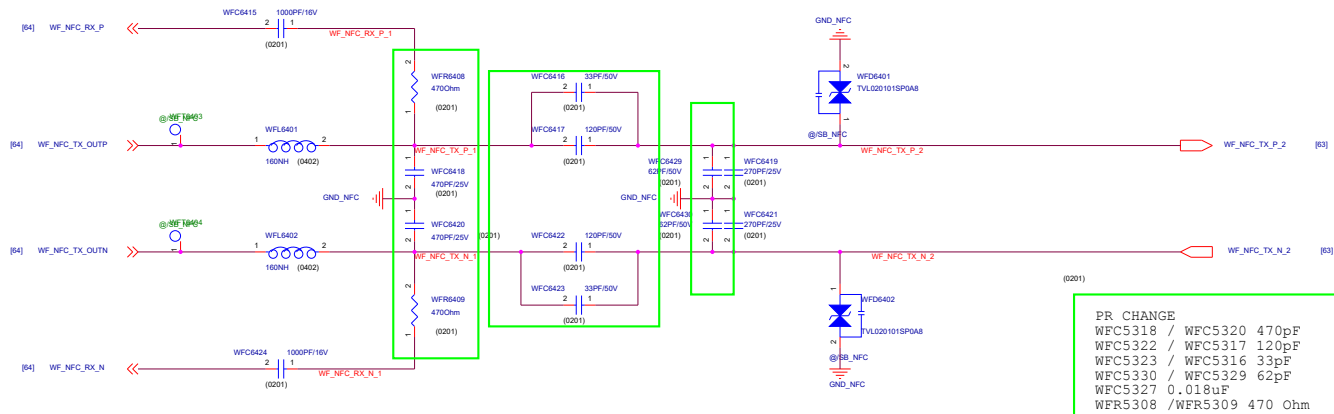








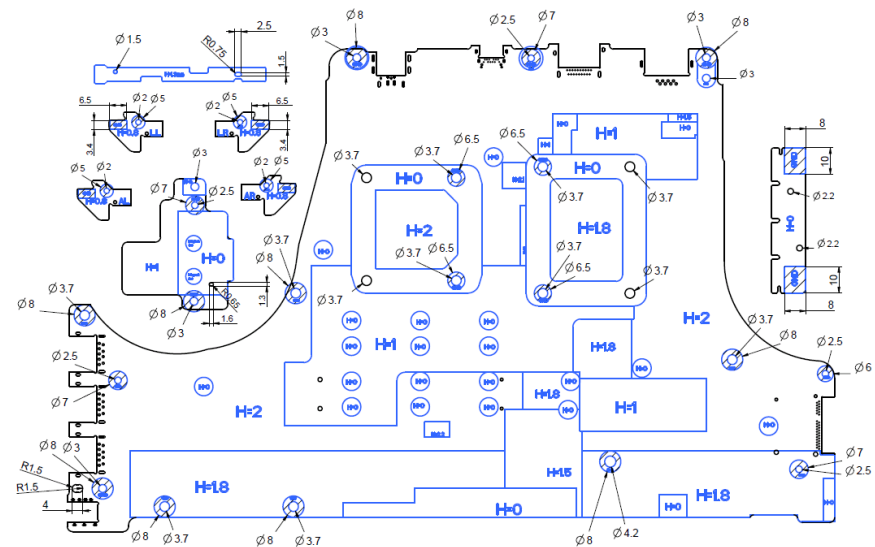
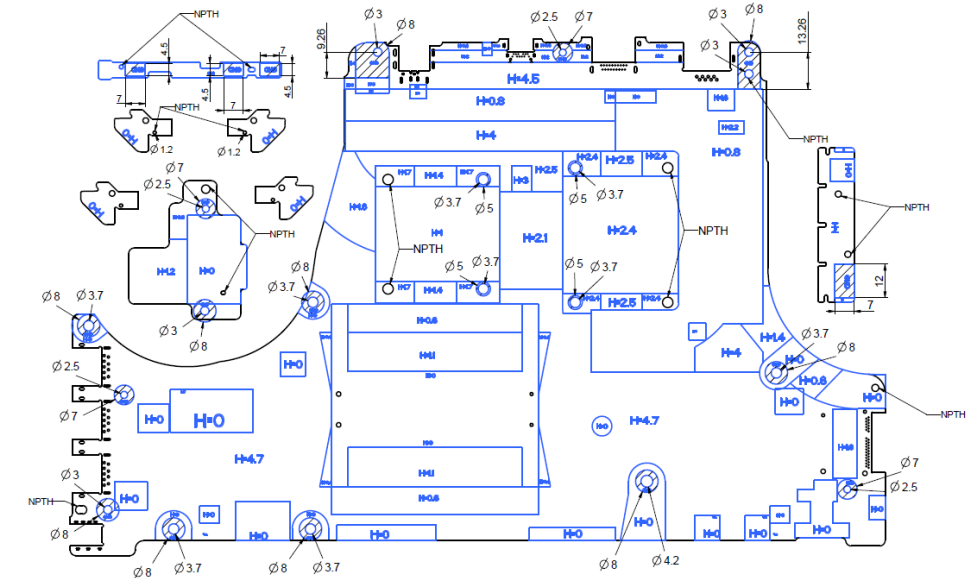
NFC Matching



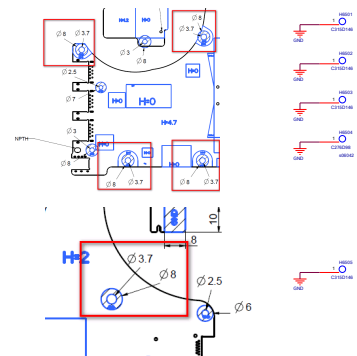
PR CHANGE
WFC5318 / WFC5320 470pF
WFC5322 / WFC5317 120pF
WFC5323 / WFC5316 33pF
WFC5330 / WFC5329 62pF
WFC5327 0.018uF
WFR5308 / WFR5309 470 Ohm

<Variant Name>

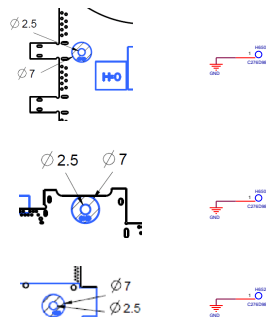
[TOP](#)



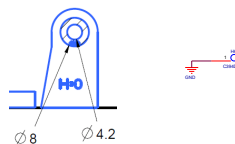
PTH 8 / 3.7mm



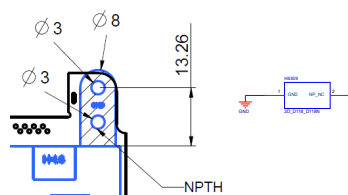
PTH 7 / 2.5mm



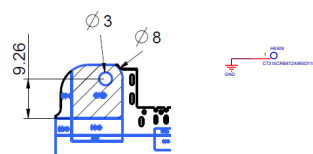
PTH 8 / 4.2 mm



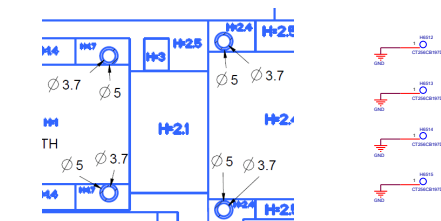
PTH 8 / 3mm+ NPTH 3mm



PTH 8/3mm (Ext.)



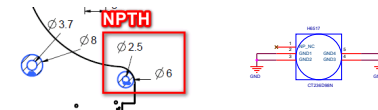
PTH 6.5 /5 /3.7 mm



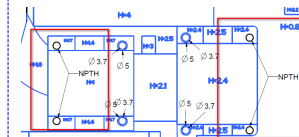
NPTH 1.5/ 4mm



NPTH 6/ 2.5 mm



NPTH 3.7 mm



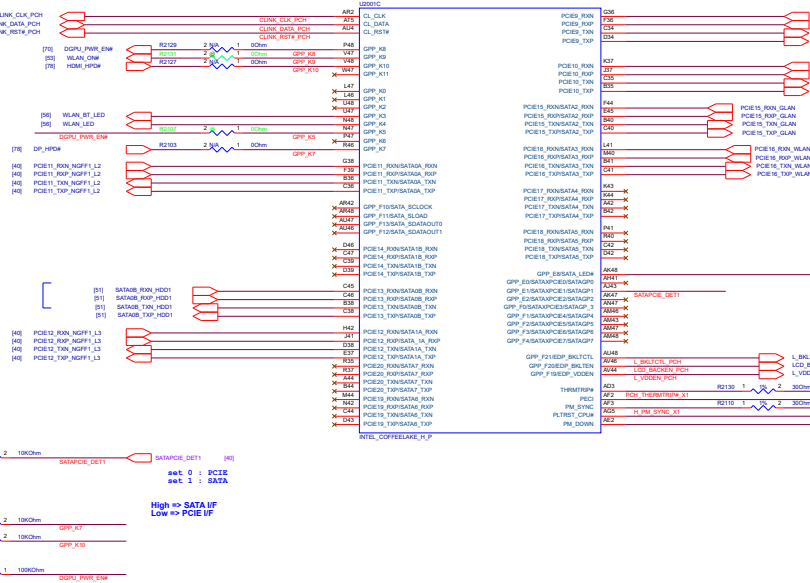
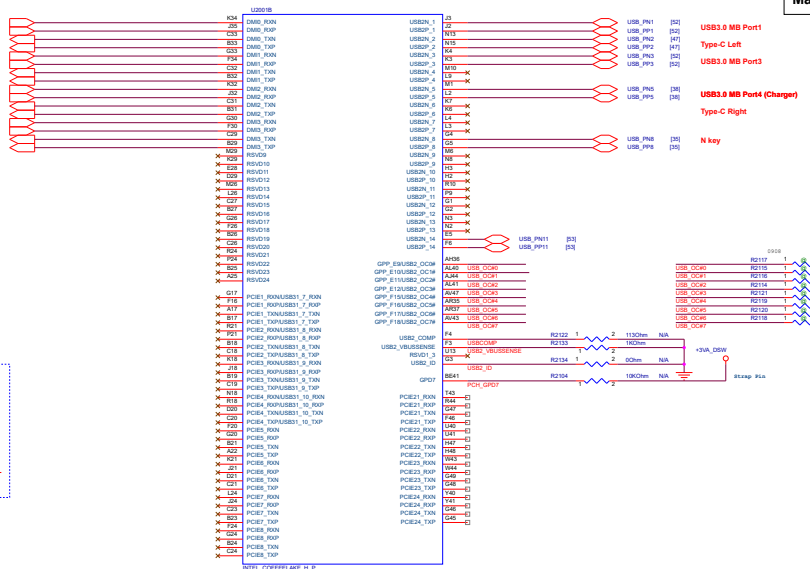
Main Board

must close to PCH


CNL HM370

[55]
[53]
[53]


PCIEx4
1st SSD




<Variant Name>


		Title :	
ASUSTeK COMPUTER		Engineer:	Gaming RD
Size	Project Name		Rev
D	G711GW		1.0
Date: Tuesday, April 16, 2019		Sheet 66 of 103	

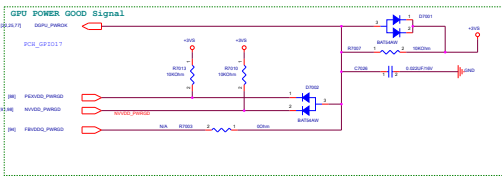
<Variant Name>

		Title : I/O board FUNC key	
ASUSTeK COMPUTER		Engineer:	Gaming RD
Size E	Project Name G711GW		Rev 1.0
Date: Tuesday, April 16, 2019		Sheet 67	of 103

		Project Name		Rev	
		G711GW		R1.0	
Title : Thunderbolt					
Size Custom	Dept.: ASUSTeK COMPUTER		Engineer:	Gaming RD	
Date: Tuesday, April 16, 2019			Sheet	68	of 103

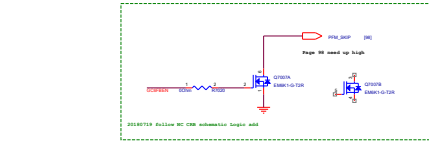
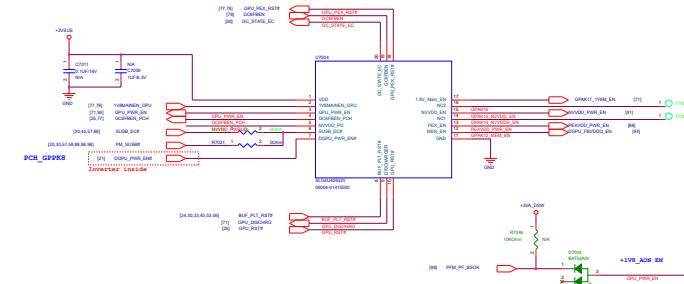
<Variant Name>

		Title : OTH_EMI	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size C	Project Name G711GW		Rev 1.0
Date: Tuesday, April 16, 2019		Sheet 69 of 103	



WVDD POWER GOOD LOOPBACK

GPU POWER SEQUENCE CONTROL

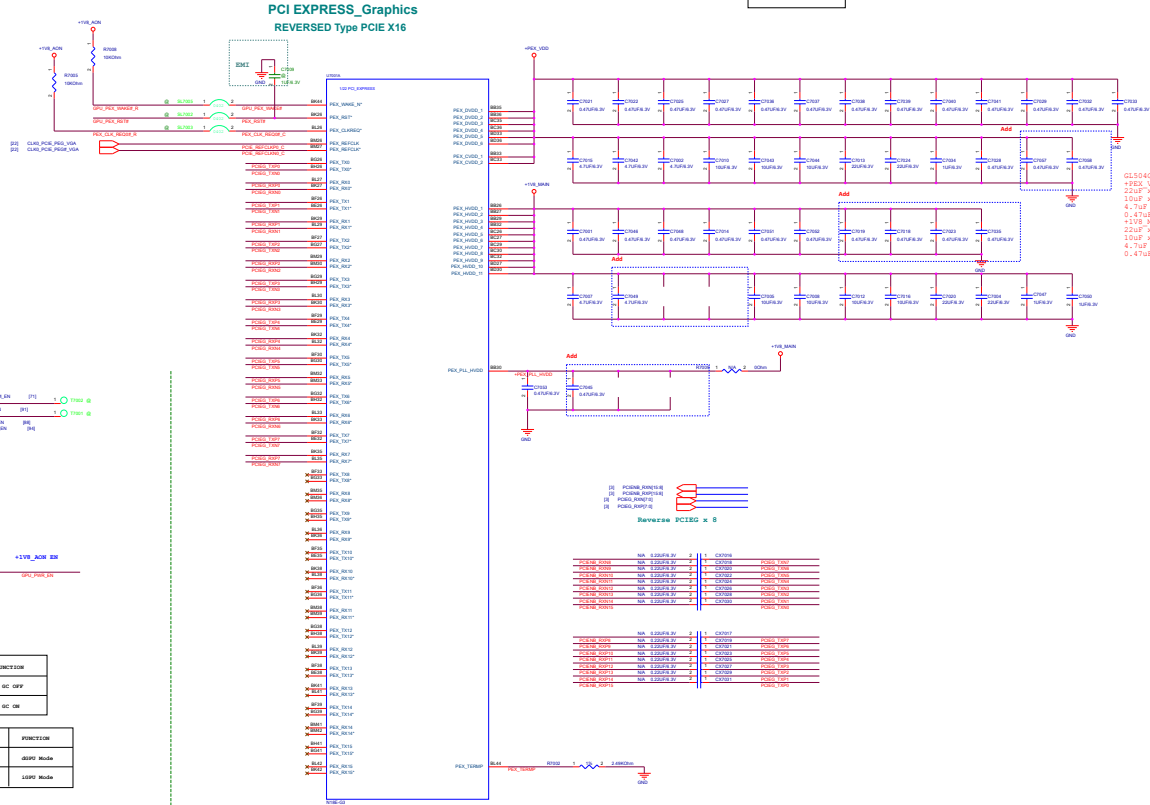


Optimize

GPU_POWER_GOOD	FUNCTION
H	MC OFF
L	MC ON

GPU_POWER_GOOD	FUNCTION
H	GPU Mode
L	GPU Mode

PCI EXPRESS_Graphics REVERSED Type PCIe X16



GS104GR	GS11GR (ORI)	GS11GR (NEW)
+5VSB 100	+5VSB 100	+5VSB 100
22uF X2	22uF X2	22uF X2
10uF X3	10uF X3	10uF X3
4.7uF X3	4.7uF X3	4.7uF X3
0.47uF X16	0.47uF X16	0.47uF X16
+10V MAIN	+10V MAIN	+10V MAIN
22uF X2	22uF X2	22uF X2
10uF X4	10uF X4	10uF X4
4.7uF X4	4.7uF X4	4.7uF X4
0.47uF X13	0.47uF X13	0.47uF X13

Reverse PCIeS x 8

NA	1	2	3	4	5	6	7	8
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS
PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS	PCIEXPRESS

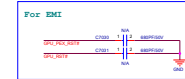
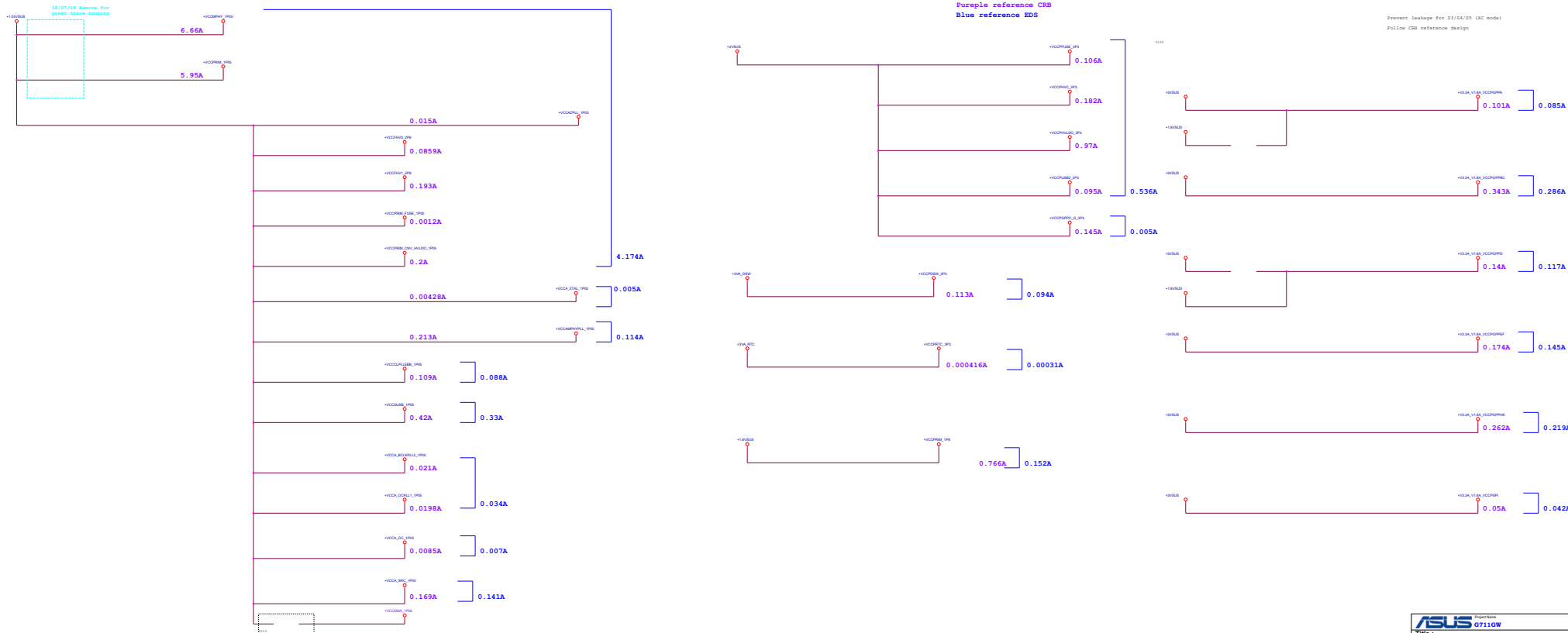
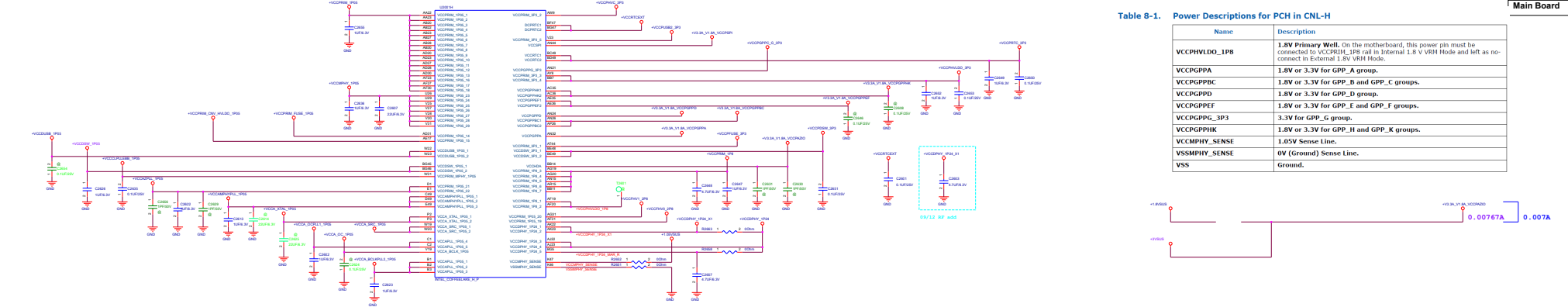
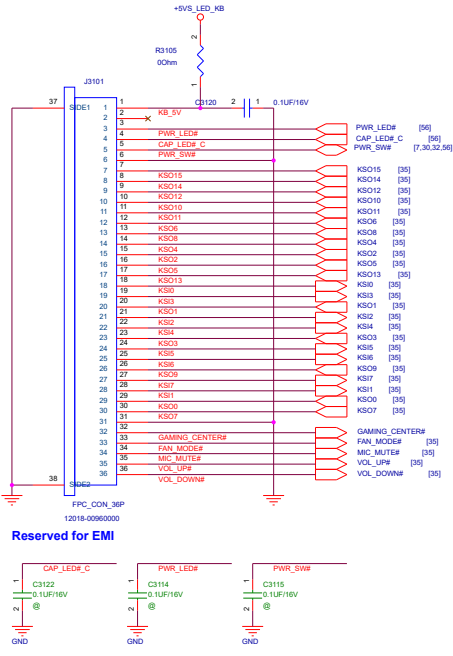


Table 8-1. Power Descriptions for PCH in CNL-H

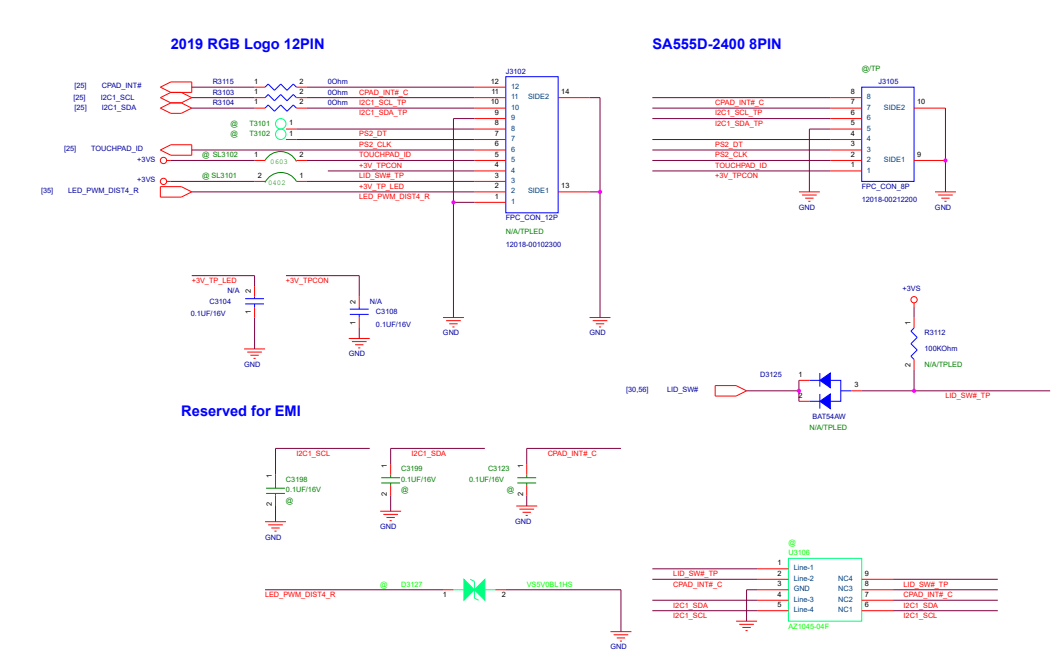
Name	Description
VCCPWHVLD0_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPWHVLD0_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCGPPPG_3P3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.



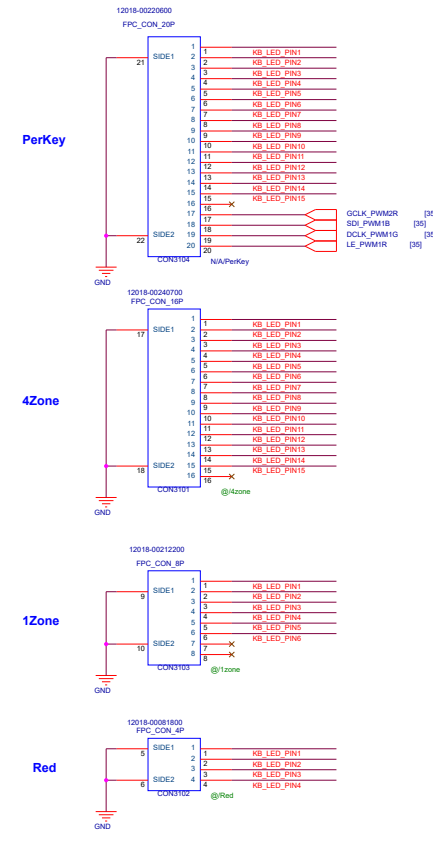
Keyboard Connector



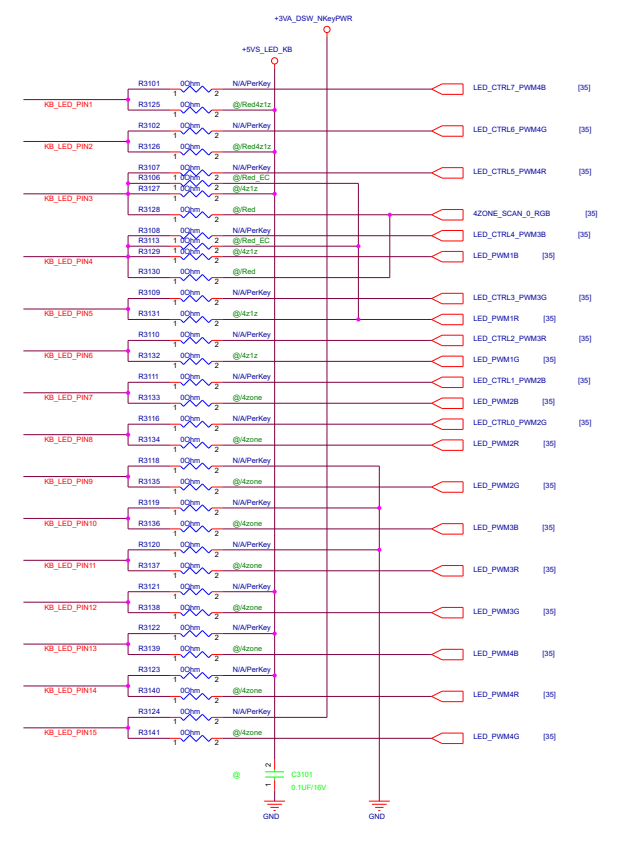
Touch Pad Connect



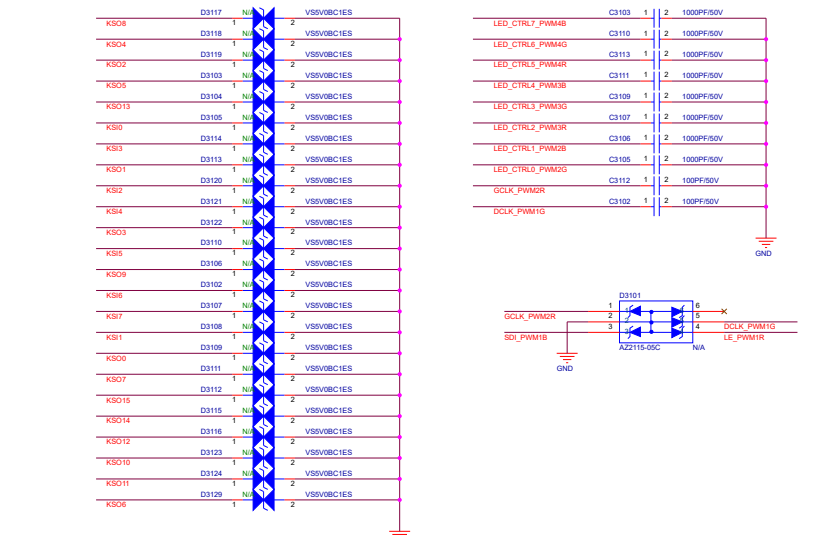
Keyboard Backlight



RED, 4zone,1zone, PerKey Co-layout

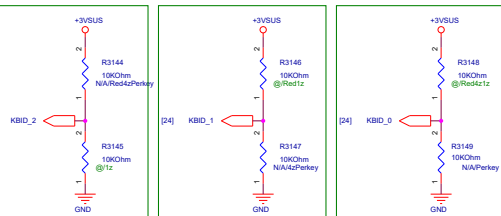


For EMI



	RED-4pin	1zone RGB 8pin	4zone-16pin	per key-20pin
pin1	VCC	VCC green	VCC green	COM7
pin2	VCC	VCC red	VCC red	COM6
pin3	GND	VCC blue	VCC blue	COM5
pin4	GND	LED1 blue	LED1 blue	COM4
pin5		LED1 red	LED1 red	COM3
pin6		LED1 green	LED1 green	COM2
pin7		NC	LED2 blue	COM1
pin8		NC	LED2 red	COM0
pin9			LED2 green	GND
pin10			LED3 blue	GND
pin11			LED3 red	GND
pin12			LED3 green	VCC
pin13			LED4 blue	VCC
pin14			LED4 red	VCC
pin15			LED4 green	VDD-33
pin16			NC	NC
pin17				GCLK
pin18				SDI
pin19				DCLK
pin20				IE

Board I




KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2	KBID 1	KBID 0
		(GPP_H18)	(GPP_H17)	(GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERTASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H

Rev	Date	Description
1.0	2017-03-03 P21	Remove CR
	2017-03-04 C5602	Q5601 change for DFX Limitation
	2017-03-10 +1V9_MAIN	+1V9_WV Follow G753 Power sequence setting
	2017-03-11 P701	Follow G702 GPU Power seq
	2017-03-11 +VDD_VDDO	GPU Sequence update
	2017-03-14 PCB104, PCB8107, PCB8106	update Cap for DFX Limit
	2017-03-14 C631V1K	Remove useless nut in P47
	2017-03-15 J5381	Connector limit update
	2017-03-15 B6714, B6706, B6724, B6723	Change Hole update
	2017-03-16 C5602	change L5D SW for Angle Simulation
	2017-03-17 B61	Reserve C5606, C5607 Cap
	2017-03-17 P60302, L4812, L4813, L4804, L4815, L4805	SWAP for Layout
1.1	2017-03-21 P30	P37, P39 AMP Change BML04G25555
	2017-03-21 B61	Reserve P30 C77360 Cap and P49 Caps and Spring
	2017-03-23 AMP	Change Reserve P37 MUTE CONTROL schematic
	2017-03-23 AMP	Change Reserve Q701
	2017-03-27 P71	+FWDDG Discharge setting Follow G753 Power sequence setting
	2017-03-29 P12	Remove TBT Power Low Switch for Layout
1.2	2017-03-30 Change Cap C7108, C7101	for Thermal request
	2017-03-30 Thermal Request for B6728	
	2017-04-05 B61	Reserve Cap and Spring in P49
	2017-04-06 Reserve C2601	for +VCCDGPU_EF Ripple
	2017-04-07 B5	DM82 Cap C1126, C1124 change for Vendor Suggest
	2017-04-07 P706	Cap C7811, C7801 change for Vendor Suggest
2.0	2017-04-11 P48	Reserve 0 ohm for BSA and SCL
	2017-04-17 P71	Add Caps for WYDOD Limitation
	2017-04-18 Q7074	Change MOS for DFX Limitation
	2017-04-20 P71	Add Caps for WYDOD Ripple
	2017-04-21 P47	Screw Hole B6705 update
	2017-04-21 P71	Add Caps for WYDOD Ripple C71119-C71122
	2017-04-26 P71	C7122, C7123, C7127, C7136, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change
	2017-04-25 P70	C7007, C7004 change to 4.7UF
	2017-05-02 B61	Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove D6913
	2017-05-02 B6711, B6712	change screw hole type dot B61 Solution
	2017-05-03 Reserve L4801 Pin 36 GND	for Factory Test
	2017-05-05 P68	P58 Remove VCCDET_PWDOD signal
	2017-05-05 P79	P45 Remove +0E Lact2 and Lact3 Signal
	2017-08-10 P31	R3121,R3122 change to unmount

[illegible]

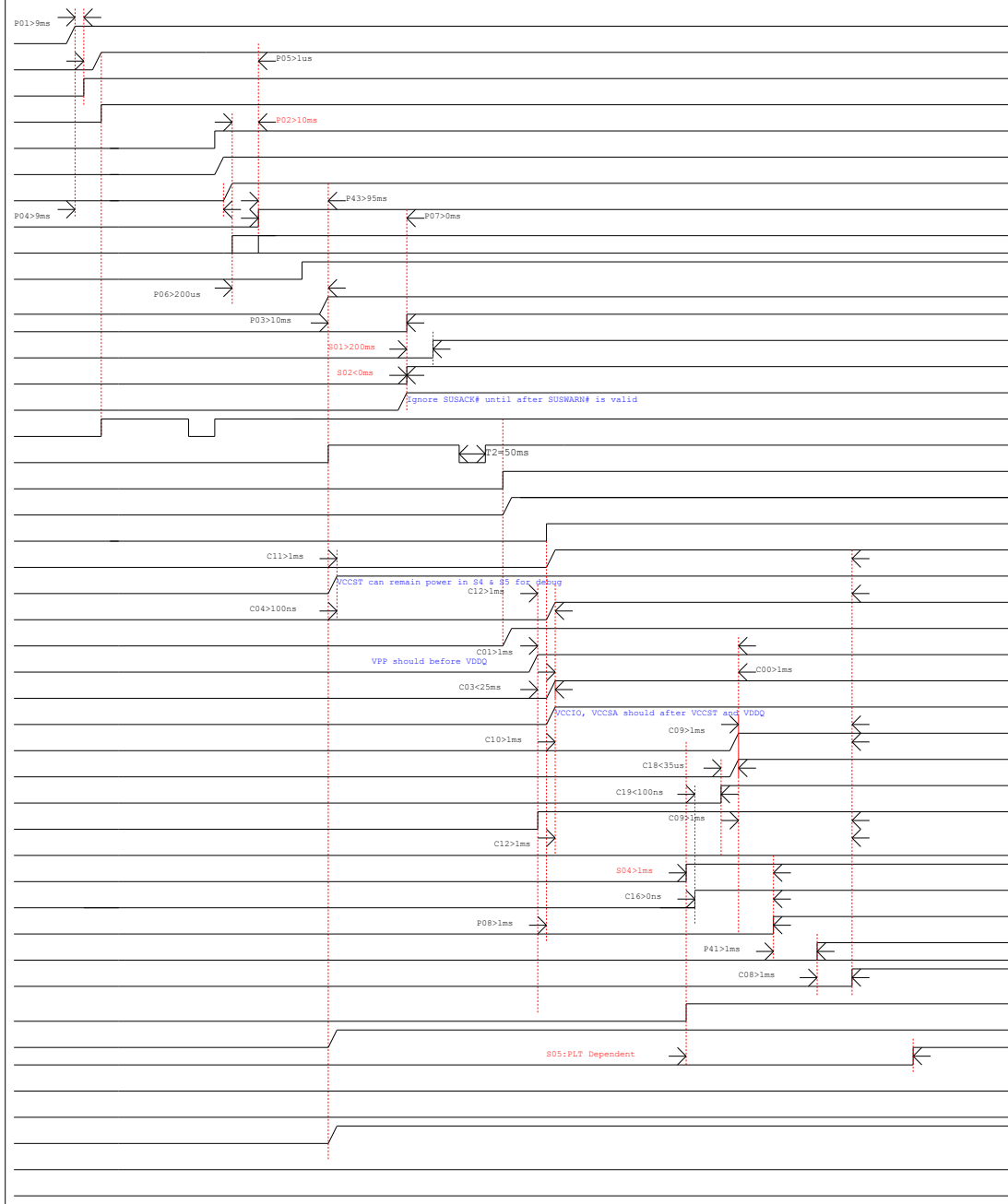
Rev	Date	Description

Rev	Date	Description


Title : Revision History
Engineer: Sammy RG

DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
P:PCH (AC_BAT_SYS)+3VA/+5VA
S:PLT (+3VA_RTC) RTCRST# (PCH)
Power (Power) AC_IN_OC# (EC)
Signal (EC) PS_ON (+3VA_EC)
(PS_ON)+3VA_EC (EC)
(3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR_Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#)+12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST, VCCPLL (VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V (2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPU_PWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



CFL H Power Sequence (DC mode)

AC-IN Mode

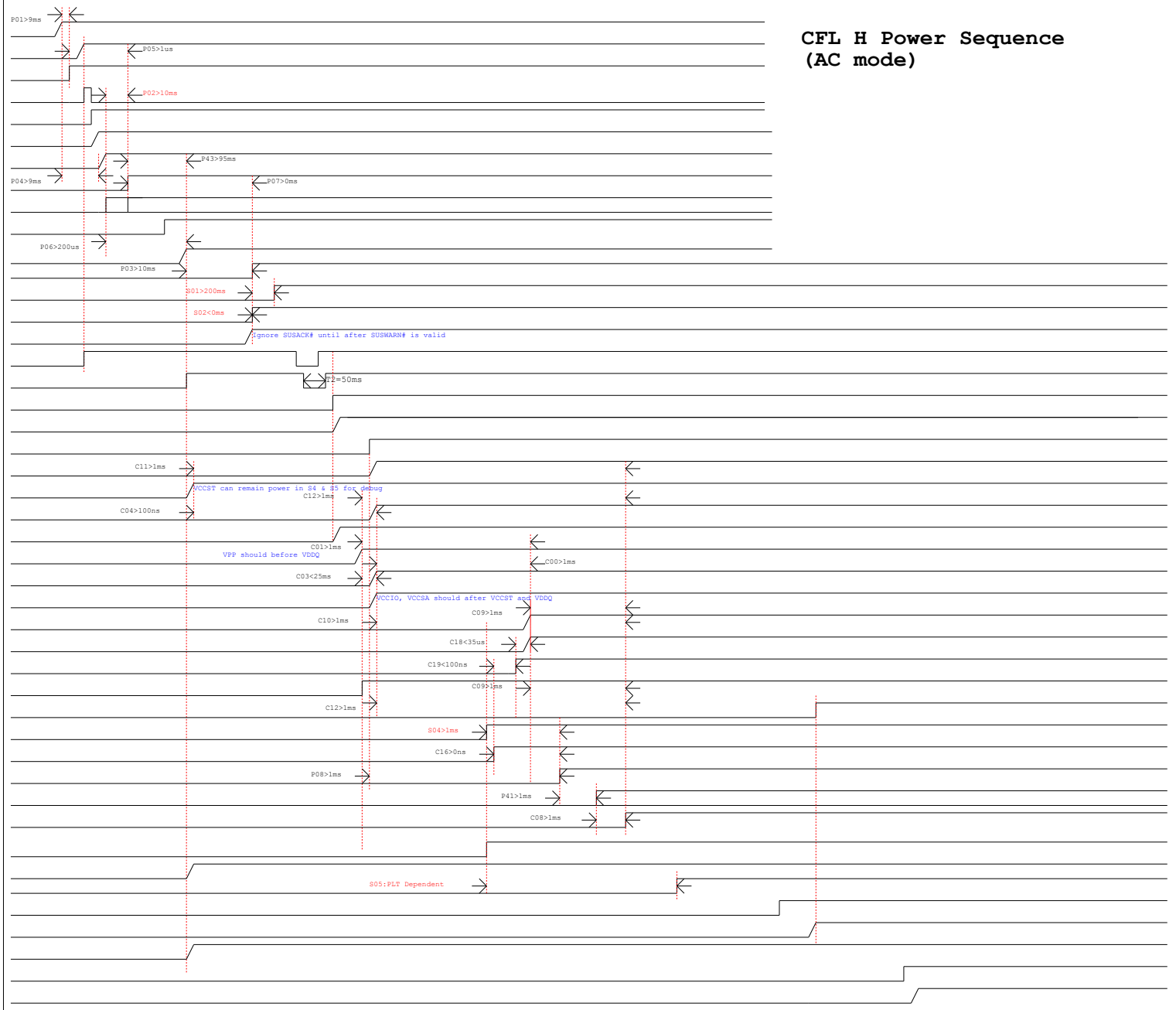
C:CPU
P:PCH
S:PLT
Power
Signal

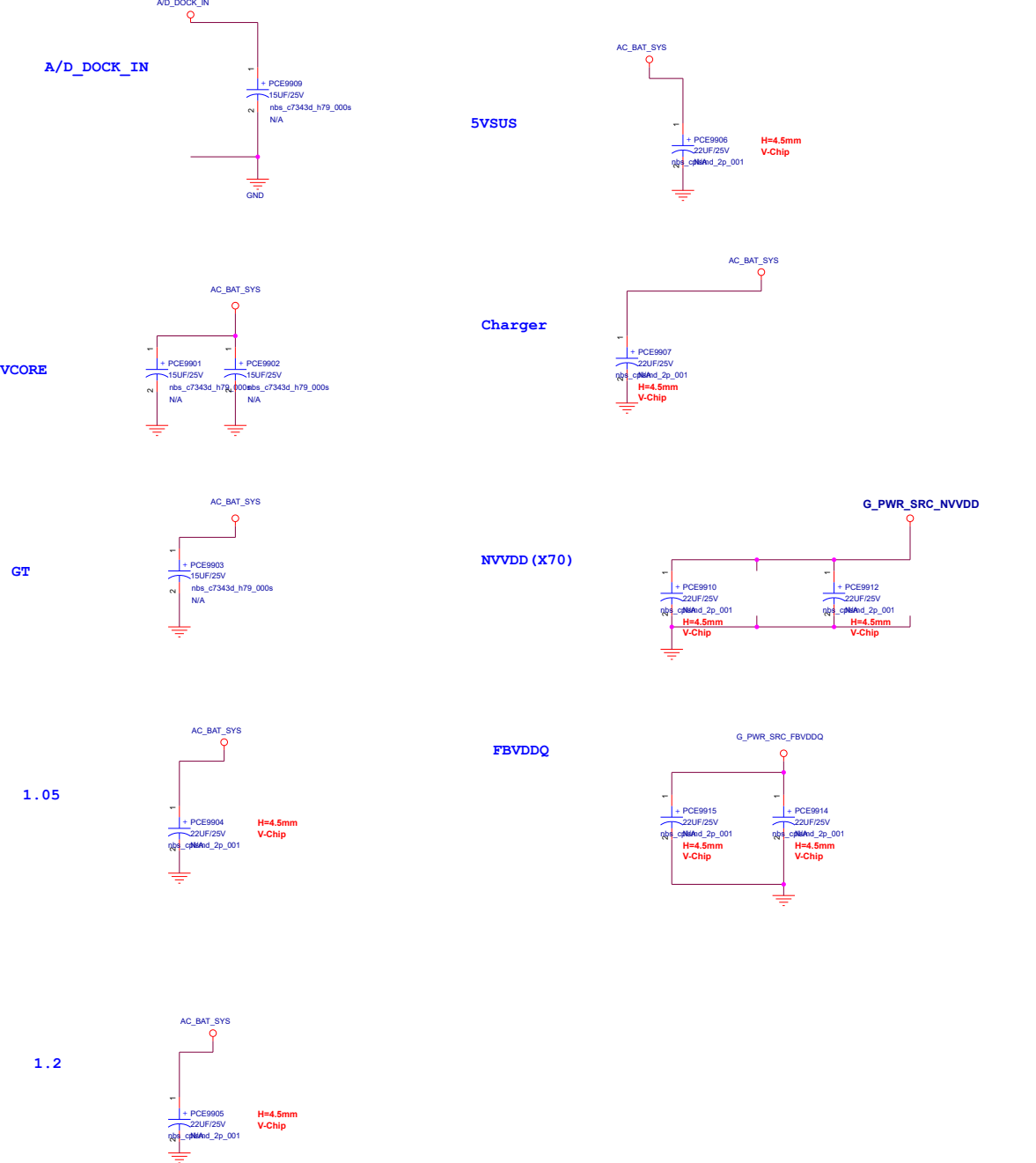
(+RTCBAT)+3VA_RTC
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC)RTCRST#(PCH)
(Power)AC_IN_OC#(EC)
(EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DPWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR_Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(SUSB_EC#)+1.0V_VCCST,VCCPLL
(SUSB_EC#)+VCCIO,(+12VS)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPUPWRGD(CPU)

(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)

+VCCGT

CFL H Power Sequence (AC mode)




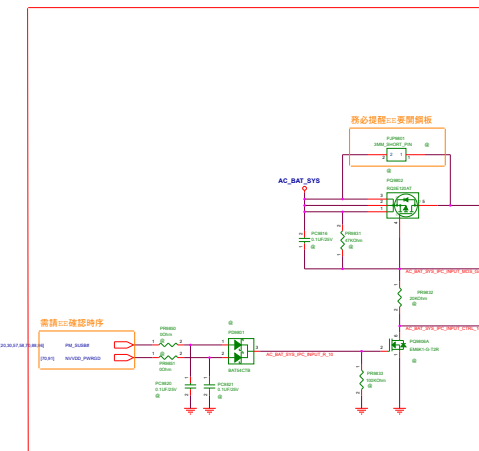


*共12顆

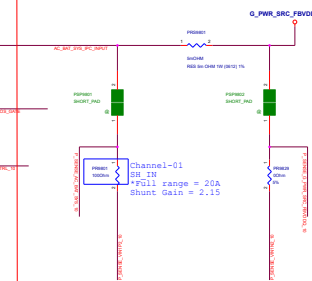
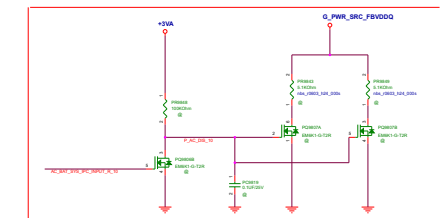
*請將對應電容放置對應PWR VRM輸入端

<|variant Name>

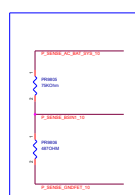
		Project Name	Rev
		GM531GX	R1.0
Title : PW_Input CAP			
Size Custom	Dept.: Power Team	Engineer: Joe	
Date: Tuesday, April 16, 2019	Sheet 99	of	102



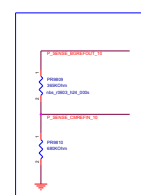
AC BAT SYS Discharge線路
 T-Discharge : 0.636s (Worst case 10 Phase)



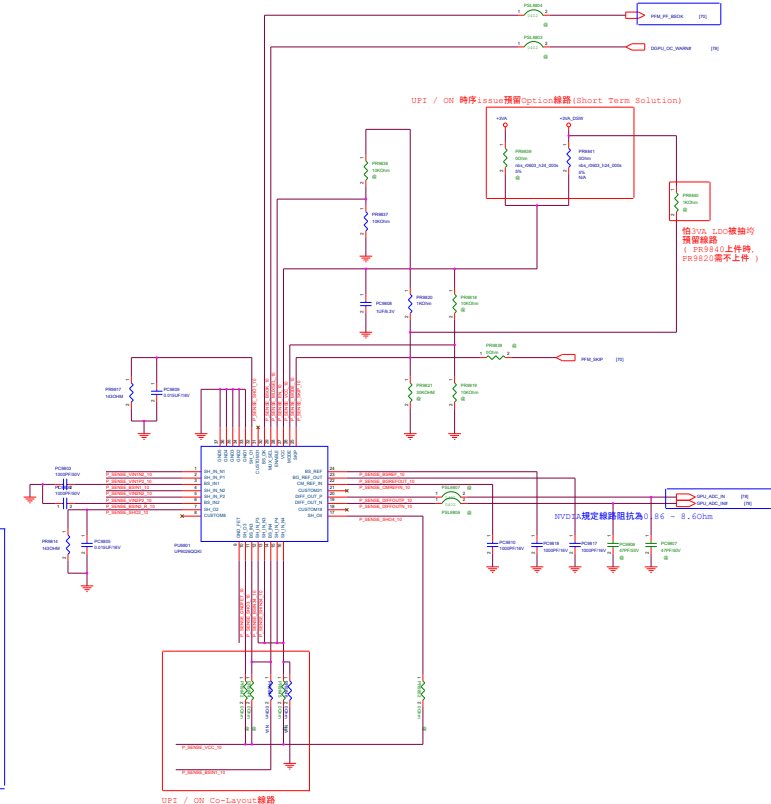
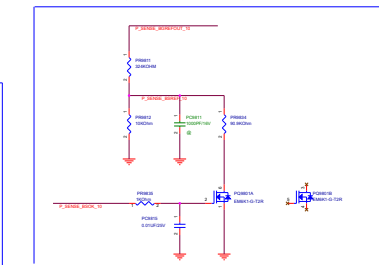
Channel-01
 RS IN
 *Full range = 19V
 Bus Gain = 6.4514m



Channel-02
 RS IN
 *Full range = 19V
 Bus Gain = 6.4514m



BS REF IN
 *6.0331V, 5.4514V (此信號小於19V, BAT電壓)
 *0.85V (實際0.8459V)



UP1 / ON 降序Issue預備Option線路 (Short Term Solution)

N18E

150W+

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

115W ~ 130W

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

100W ~ 110W

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

75W ~ 90W

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

75W-

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

N18P

75W-

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

150W+

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

115W ~ 130W

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	

75W ~ 90W

	UP9026PQR1 (UP1)	NCP45491 (ON)
PR9801	100n (10G212100014010)	
PR9817	100n (10G212127014010)	100n (10G212143014010)
PR9822	100n (10G212100014010)	
PR9814	357n (10G212127014010)	475n (10G212169014010)
PR9805	75k (10G212750214010)	
PR9806	487n (10G212487014010)	649n (10G212649014010)
PR9807	75k (10G212750214010)	
PR9808	487n (10G212487014010)	649n (10G212649014010)
PR9811	244n (10G212324314010)	243n (10G212243314010)
PR9812	10k (10G212100214010)	
PR9834	90.9k (10G212909214010)	



Project Name

GX531GM

Rev

R1.0

Title : **Type C LDO 3V3**

Size

Custom

Dept.: **ASUSTeK COMPUTER INC.** **Engineer:** **Joe**

Date: **Tuesday, April 16, 2019**


Sheet

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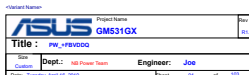
of


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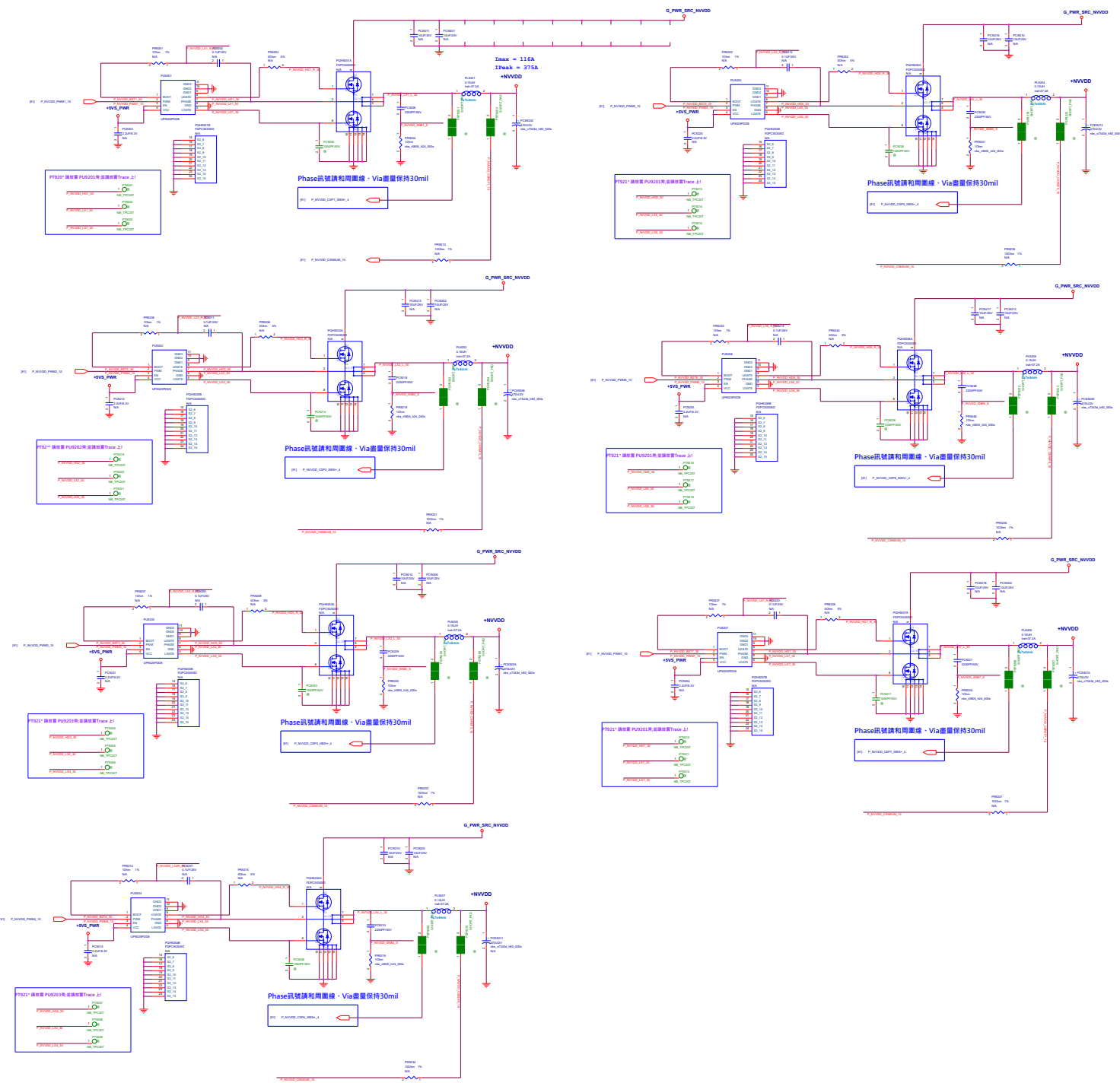
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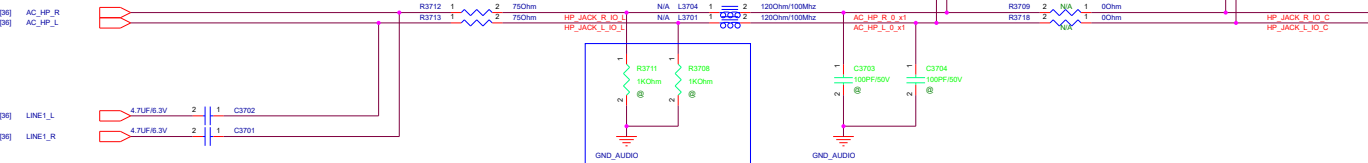
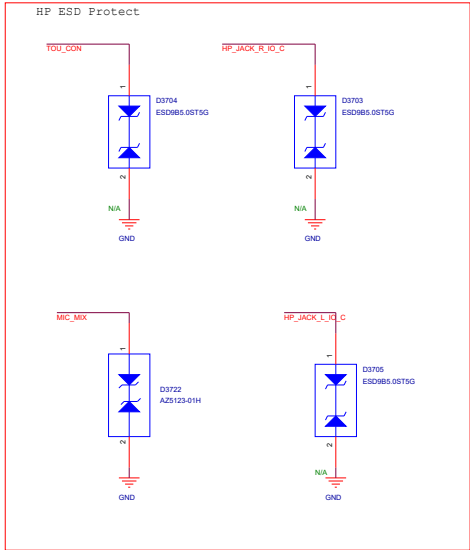
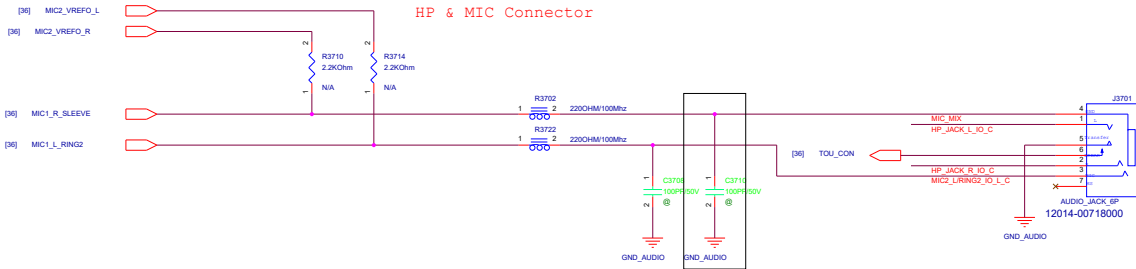
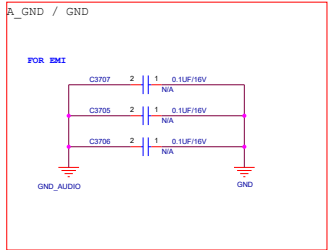
		Project Name		Rev
		GX531GM		R1.0
Title : PW_PEX_VDD/+1.8V_GPU				
Size Custom	Dept.: NB Power Team		Engineer:	Joe
Date: Tuesday, April 16, 2019			Sheet	95 of 117

PT940* 請放置 PU9401旁;並請放置Trace 上



		Project Name		Rev
		GX531GM		R1.0
Title : PW_PEX_VDD/+1.8V_GPU				
Size Custom	Dept.: NB Power Team		Engineer:	Joe
Date: Tuesday, April 16, 2019			Sheet	93 of 117

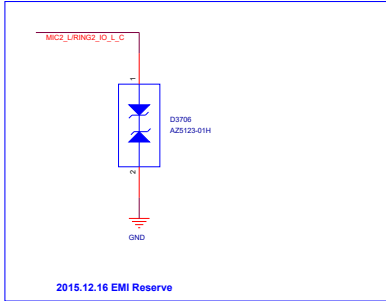
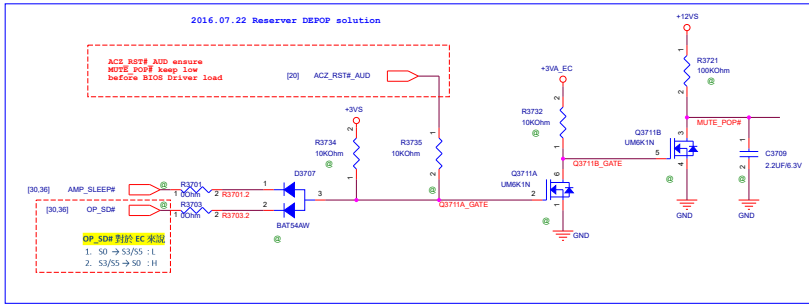




2015.04.14 3 pole mic design and VB2 Reserve

2015.08.07 Realtek Suggest

MUTE CONTROL



2015.12.16 EMI Reserve

2017.03.23 AMP Change Remove

MUTE CONTROL new solution for 1.8V HDA BUG 0318

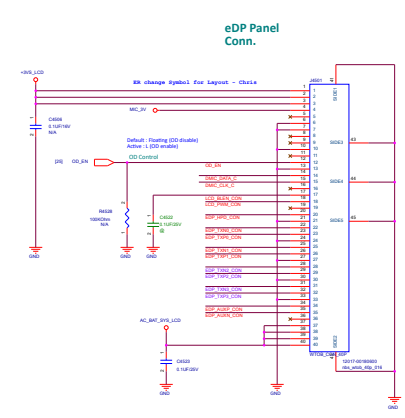
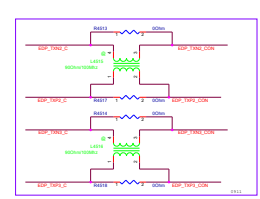
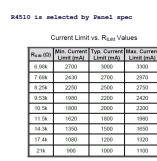
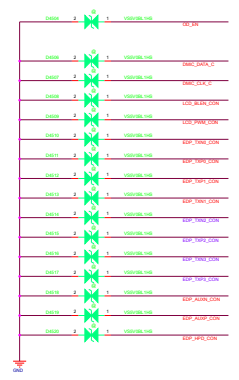
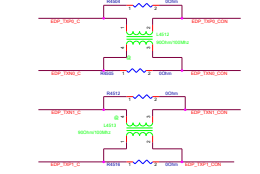
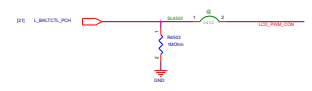
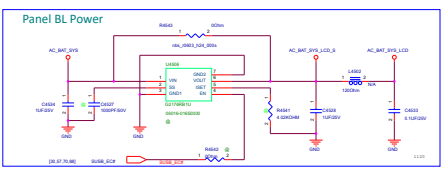
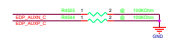
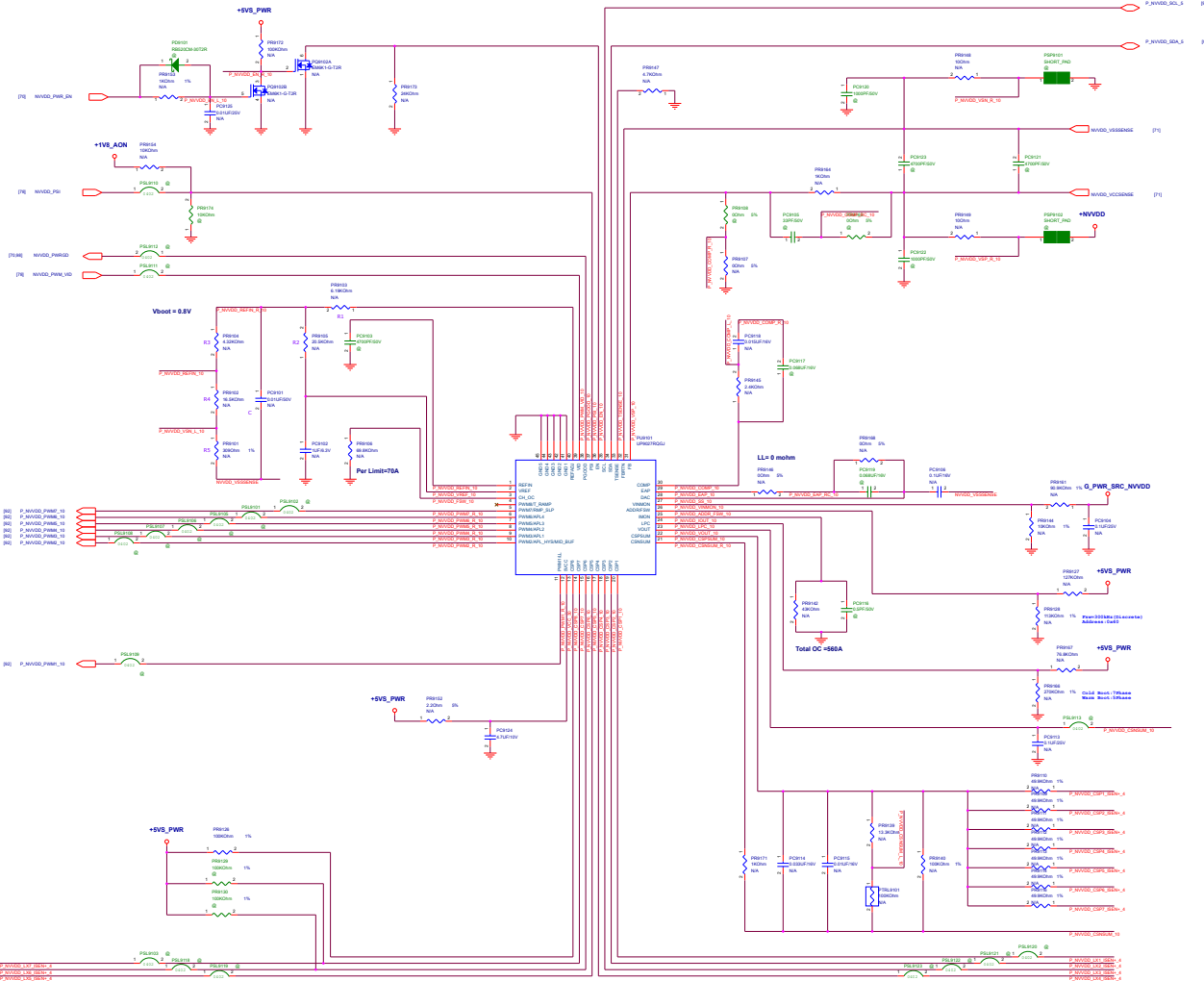


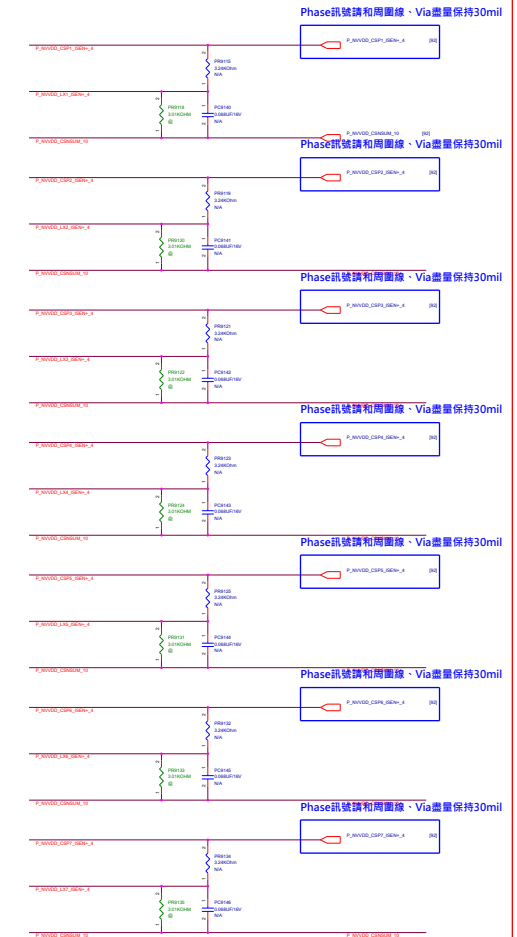
Figure 1: Schematic representation of the genomic organization of the genes. The figure shows the structure of several genes and their transcripts. Genes are represented by red boxes, and transcripts by blue lines. The genes are: EGP_TNPO, EGP_TNPO2, EGP_TNPO3, EGP_TNPO4, EGP_TNPO5, EGP_TNPO6, EGP_TNPO7, EGP_TNPO8, EGP_TNPO9, EGP_TNPO10, EGP_TNPO11, EGP_TNPO12, EGP_TNPO13, EGP_TNPO14, EGP_TNPO15, EGP_TNPO16, EGP_TNPO17, EGP_TNPO18, EGP_TNPO19, EGP_TNPO20, EGP_TNPO21, EGP_TNPO22, EGP_TNPO23, EGP_TNPO24, EGP_TNPO25, EGP_TNPO26, EGP_TNPO27, EGP_TNPO28, EGP_TNPO29, EGP_TNPO30, EGP_TNPO31, EGP_TNPO32, EGP_TNPO33, EGP_TNPO34, EGP_TNPO35, EGP_TNPO36, EGP_TNPO37, EGP_TNPO38, EGP_TNPO39, EGP_TNPO40, EGP_TNPO41, EGP_TNPO42, EGP_TNPO43, EGP_TNPO44, EGP_TNPO45, EGP_TNPO46, EGP_TNPO47, EGP_TNPO48, EGP_TNPO49, EGP_TNPO50, EGP_TNPO51, EGP_TNPO52, EGP_TNPO53, EGP_TNPO54, EGP_TNPO55, EGP_TNPO56, EGP_TNPO57, EGP_TNPO58, EGP_TNPO59, EGP_TNPO60, EGP_TNPO61, EGP_TNPO62, EGP_TNPO63, EGP_TNPO64, EGP_TNPO65, EGP_TNPO66, EGP_TNPO67, EGP_TNPO68, EGP_TNPO69, EGP_TNPO70, EGP_TNPO71, EGP_TNPO72, EGP_TNPO73, EGP_TNPO74, EGP_TNPO75, EGP_TNPO76, EGP_TNPO77, EGP_TNPO78, EGP_TNPO79, EGP_TNPO80, EGP_TNPO81, EGP_TNPO82, EGP_TNPO83, EGP_TNPO84, EGP_TNPO85, EGP_TNPO86, EGP_TNPO87, EGP_TNPO88, EGP_TNPO89, EGP_TNPO90, EGP_TNPO91, EGP_TNPO92, EGP_TNPO93, EGP_TNPO94, EGP_TNPO95, EGP_TNPO96, EGP_TNPO97, EGP_TNPO98, EGP_TNPO99, EGP_TNPO100. The transcripts are labeled with their corresponding gene names and the exon number. The figure also shows the location of the genes on the chromosome, with the green box representing the EGP_TNPO gene and the red box representing the EGP_TNPO2 gene. The figure is a schematic representation of the genomic organization of the genes, showing the structure of the genes and their transcripts.



+NVVDD [For DGPU]



請放靠近PU9101



Altium Name:

Project Name:

0711GW

File: PWR-NVDD.DWG

Sheet: 1 of 1

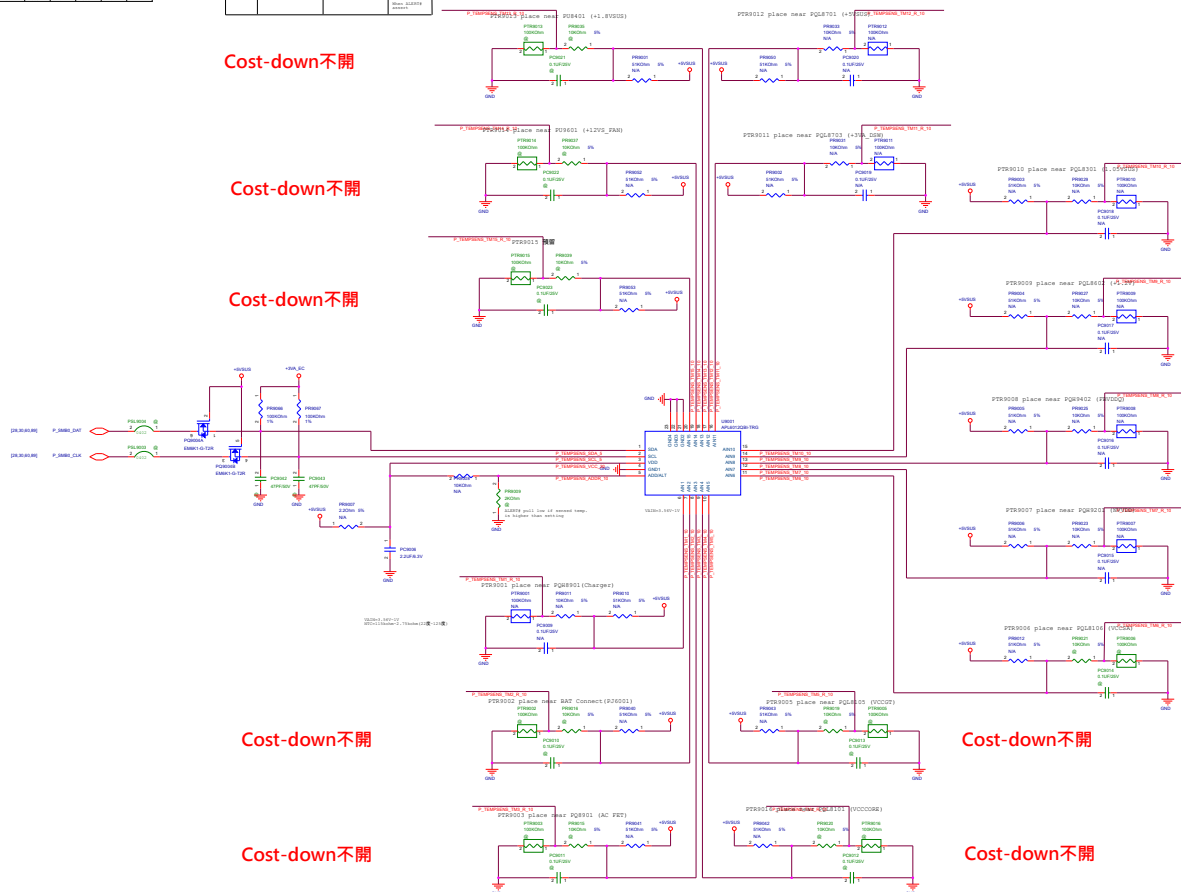
Engineer: Nat

Date: 2023/07/11

Address Selection Table									
Address	SA[2]	SA[1]	SA[0]	SA[3]	SA[2]	SA[1]	SA[0]	SA[3]	SA[2]
0x0000	0	0	0	0	0	0	0	0	0
0x0001	1	0	0	0	0	0	0	0	0
0x0002	0	1	0	0	0	0	0	0	0
0x0003	1	1	0	0	0	0	0	0	0
0x0004	0	0	1	0	0	0	0	0	0
0x0005	1	0	1	0	0	0	0	0	0
0x0006	0	0	0	1	0	0	0	0	0
0x0007	1	0	0	1	0	0	0	0	0
0x0008	0	0	0	0	1	0	0	0	0
0x0009	1	0	0	0	1	0	0	0	0
0x000A	0	0	0	0	0	1	0	0	0
0x000B	1	0	0	0	0	1	0	0	0
0x000C	0	0	0	0	0	0	1	0	0
0x000D	1	0	0	0	0	0	1	0	0
0x000E	0	0	0	0	0	0	0	1	0
0x000F	1	0	0	0	0	0	0	1	0

Register Address									
Address	SA[2]	SA[1]	SA[0]	SA[3]	SA[2]	SA[1]	SA[0]	SA[3]	SA[2]
0x0000	0	0	0	0	0	0	0	0	0
0x0001	1	0	0	0	0	0	0	0	0
0x0002	0	1	0	0	0	0	0	0	0
0x0003	1	1	0	0	0	0	0	0	0
0x0004	0	0	1	0	0	0	0	0	0
0x0005	1	0	1	0	0	0	0	0	0
0x0006	0	0	0	1	0	0	0	0	0
0x0007	1	0	0	1	0	0	0	0	0
0x0008	0	0	0	0	1	0	0	0	0
0x0009	1	0	0	0	1	0	0	0	0
0x000A	0	0	0	0	0	1	0	0	0
0x000B	1	0	0	0	0	1	0	0	0
0x000C	0	0	0	0	0	0	1	0	0
0x000D	1	0	0	0	0	0	1	0	0
0x000E	0	0	0	0	0	0	0	1	0
0x000F	1	0	0	0	0	0	0	1	0

PROTECTION



Cost-down不開

Cost-down不開

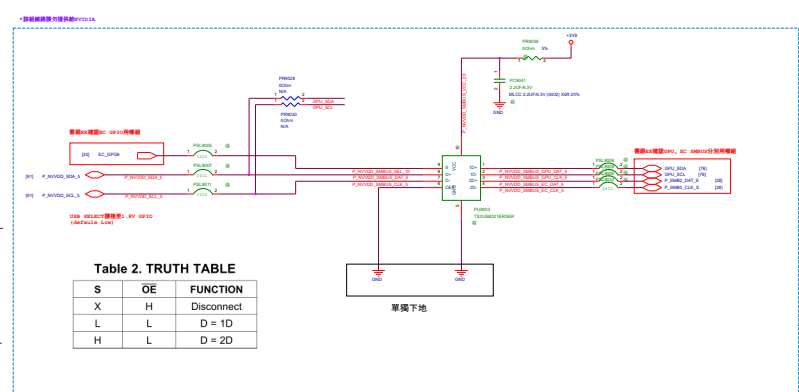
Cost-down不開

Cost-down不開

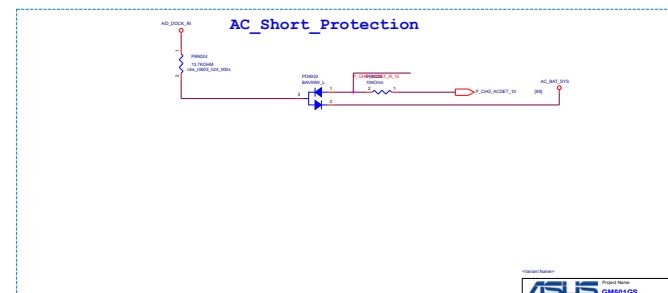
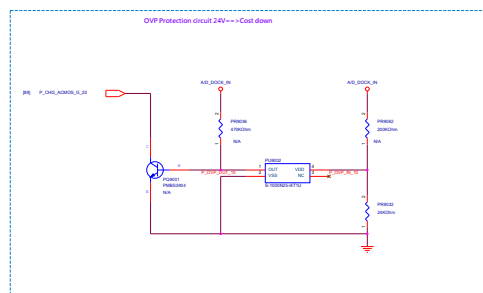
Cost-down不開

Cost-down不開

Cost-down不開

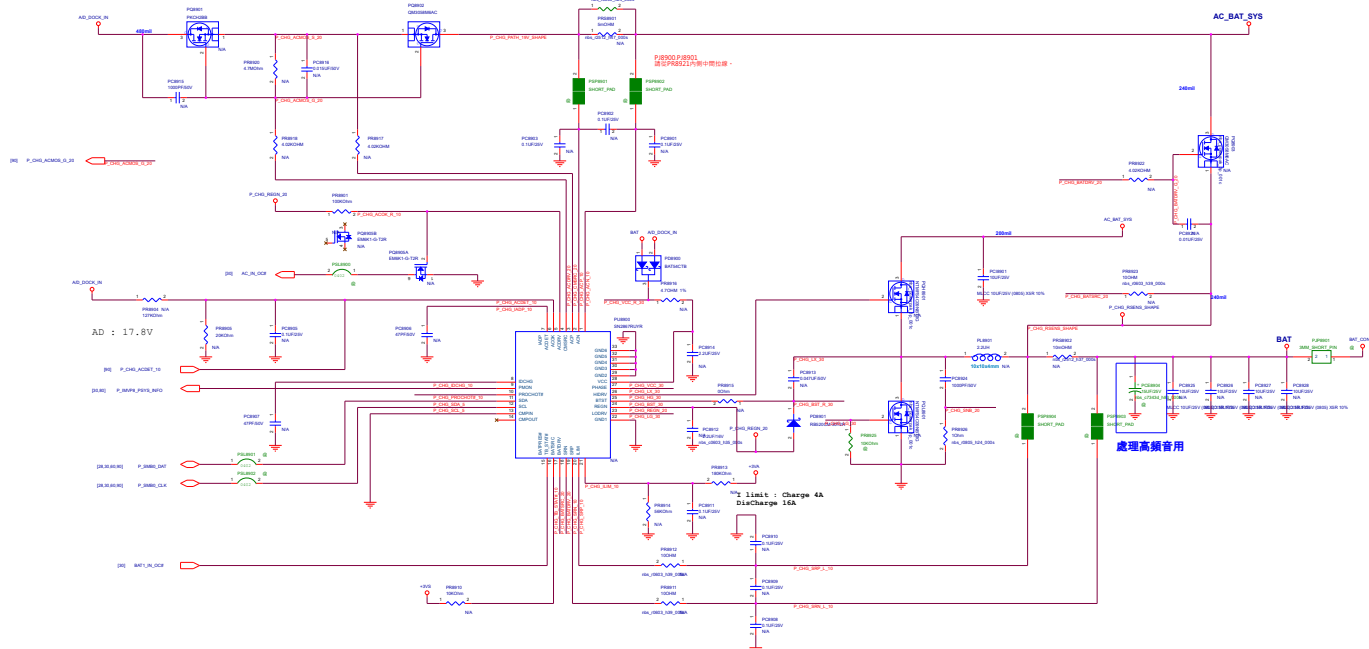


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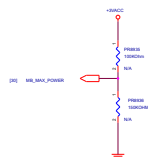


P9B901	ADP<120W	ADP<230W	ADP<330W
	TBD	5m	2m
	10101-0000000	10101-0000001	10101-0000001

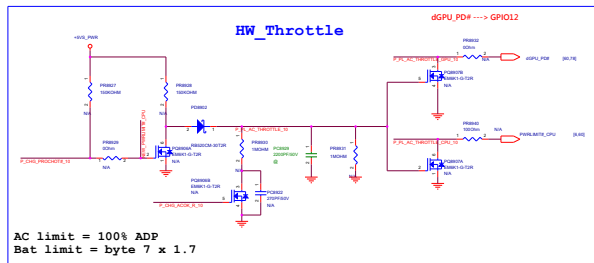
P9B903	ADP=120W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	560m
	10101-0000001	10101-0000001	X	X	10101-0000001

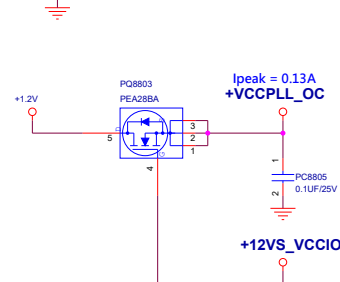
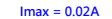
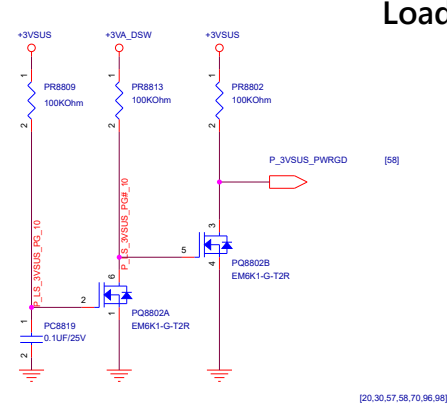


Adaptor select
total power = 90% ADP

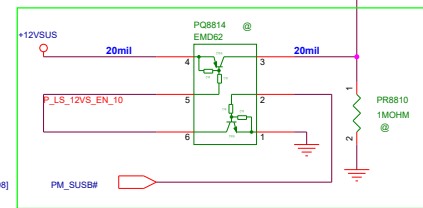
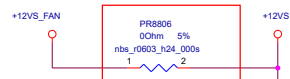


Adaptor select				
	M Series	D Series		
P9B921		10m	5m	
P9B936				
14K	0.4V	30W	120W	
31.6K	0.8V	40W	150W	
56K	1.2V	45W	180W	
93.1K	1.6V	65W	230W	
150K	2.0V	75W	280W	
270K	2.4V	90W	330W	
560K	2.8V	120W	400W	

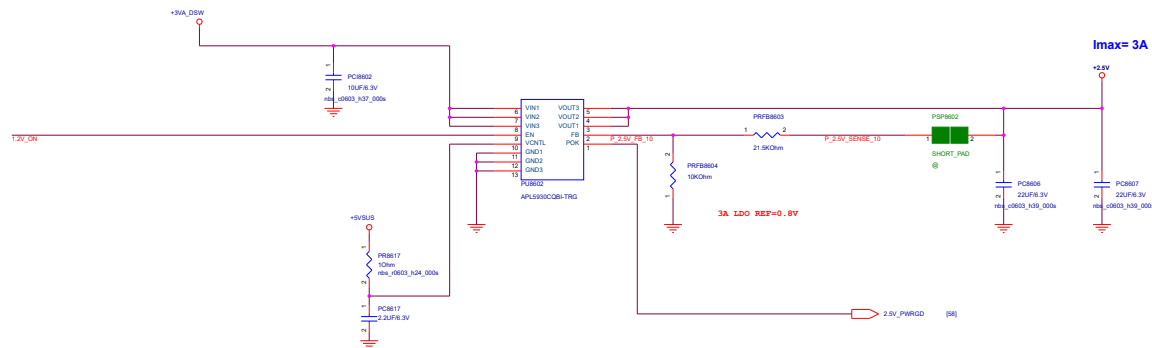
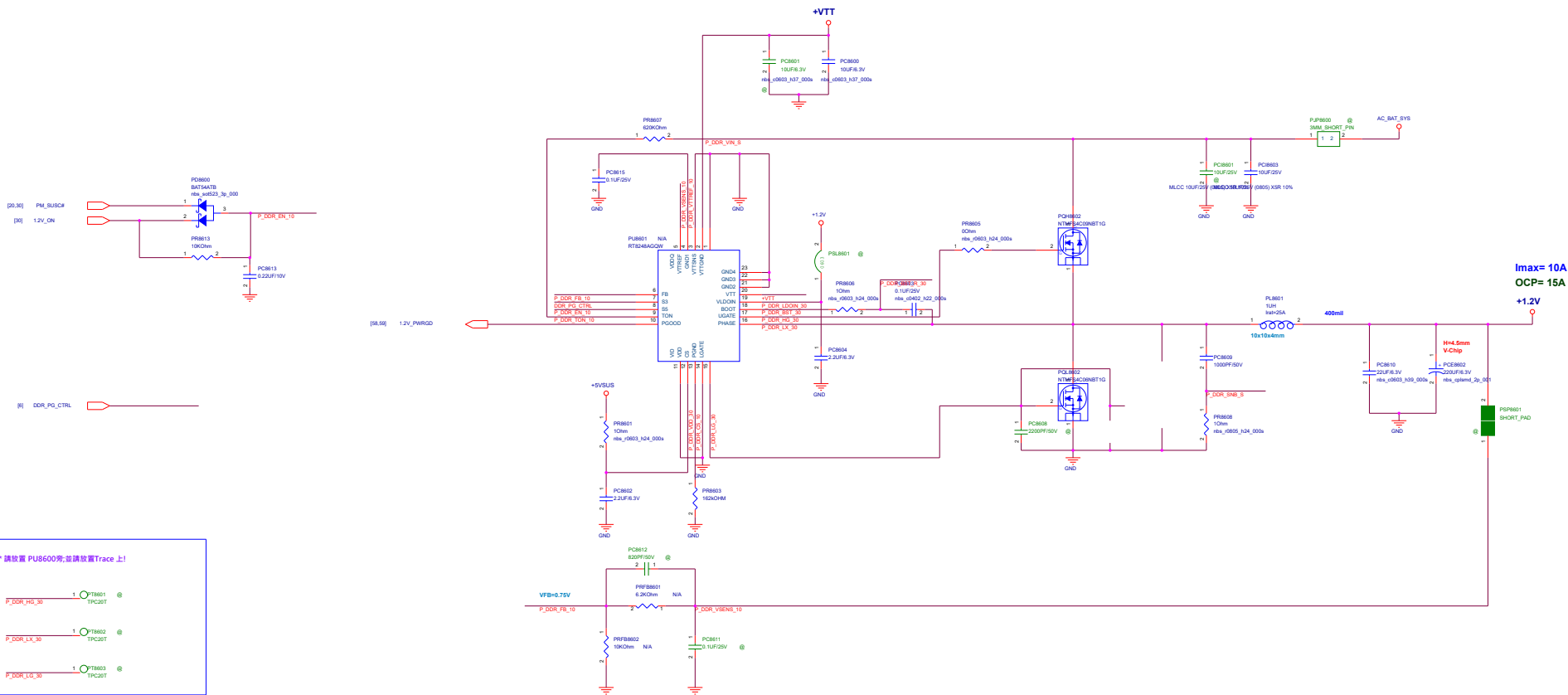





有12V FAN要上件



+1.2V / +VTT / +5V[For Memory]

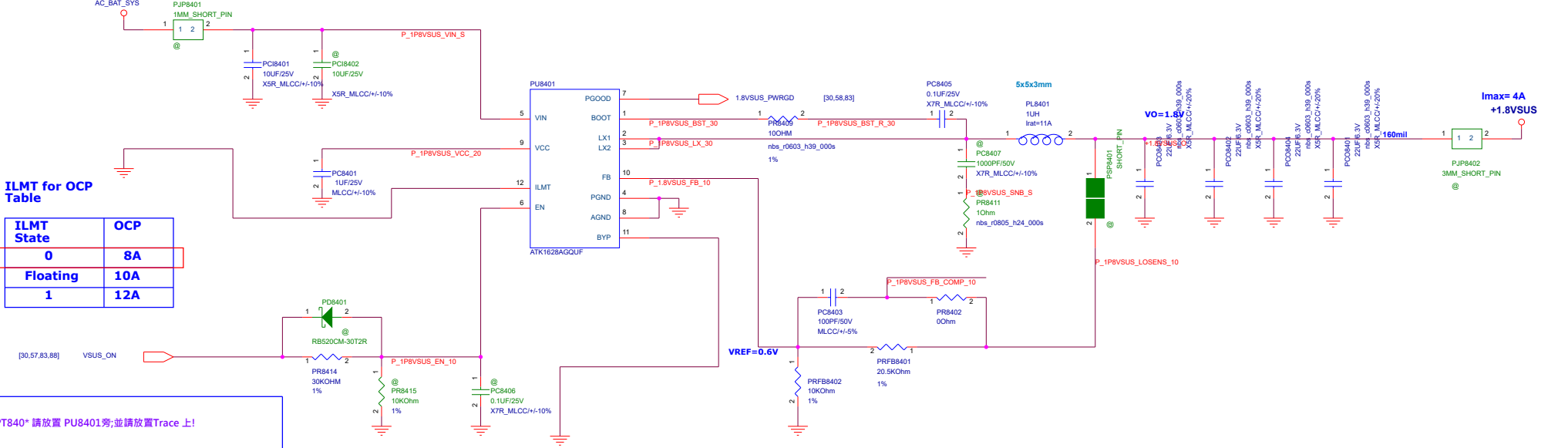


		Project Name		Rev	
		GM531GX		R1.0	
Title : Thunderbolt					
Size	Custom	Dept.:	ASUS Power Team	Engineer:	Joe
Date: Tuesday, April 16, 2019			Sheet	85	of 103

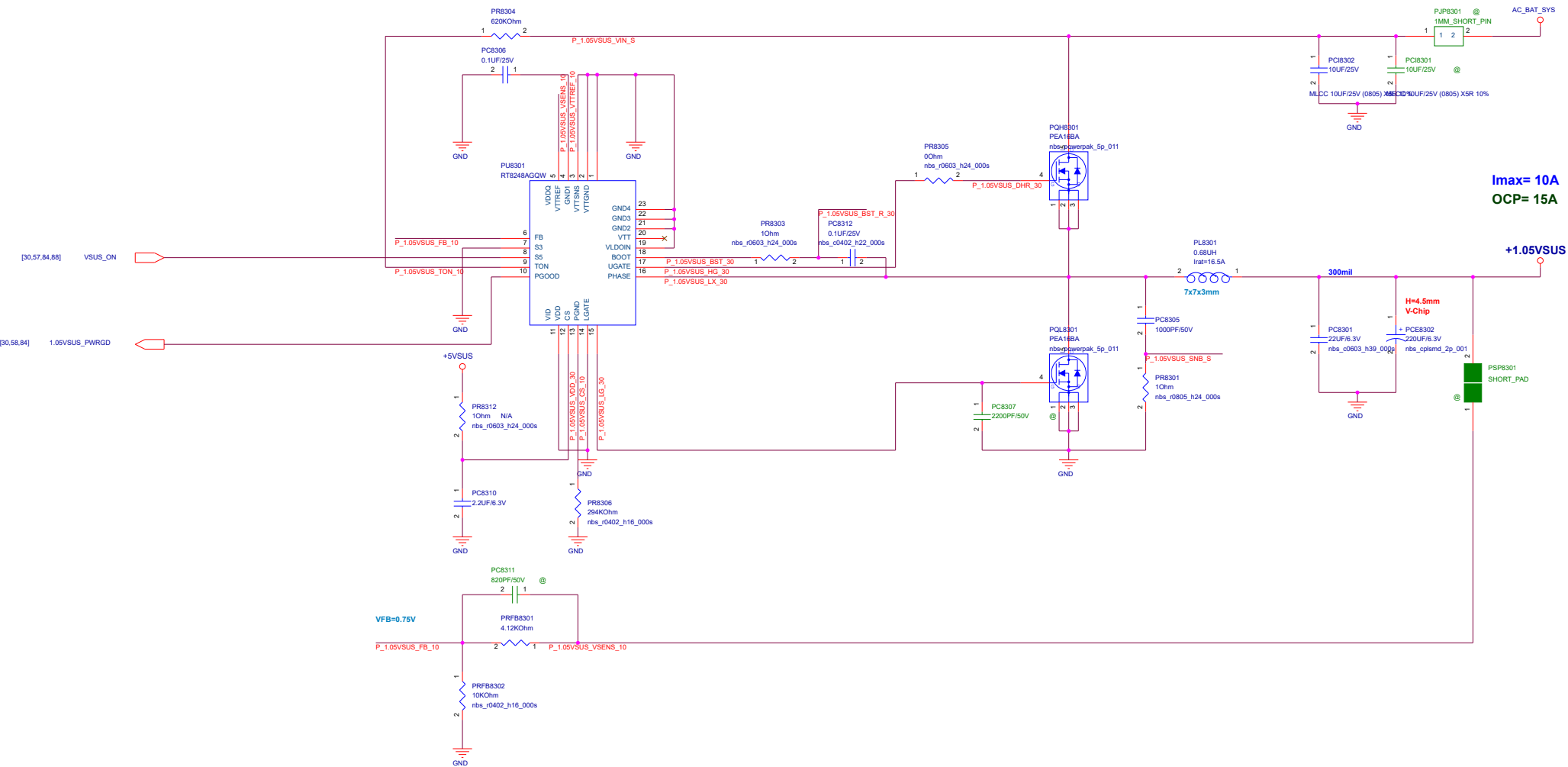
ILMT for OCP
Table

ILMT State	OCP
0	8A
Floating	10A
1	12A

PT840* 請放置 PU8401旁;並請放置Trace上!

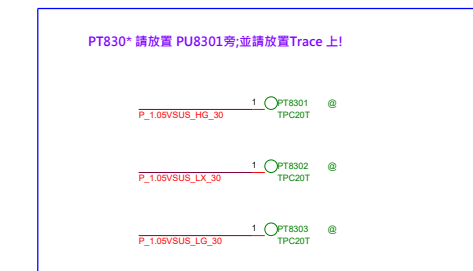



+1.05VSUS [For PCH]

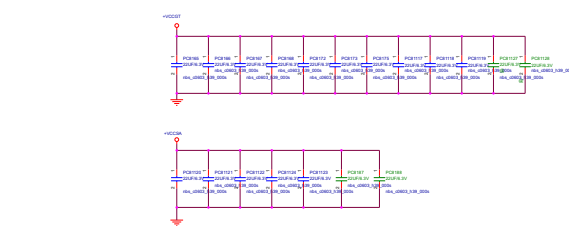
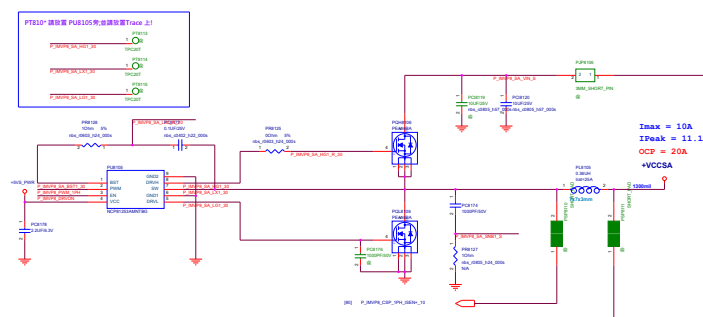
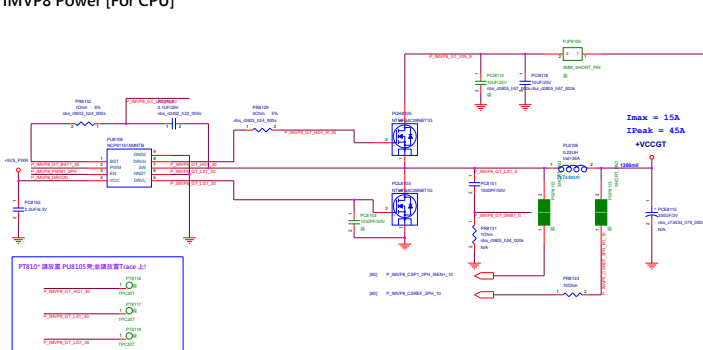
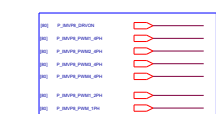
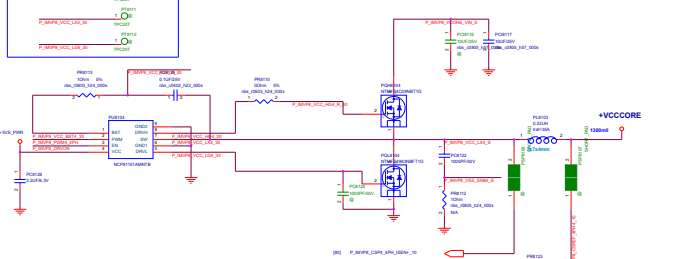
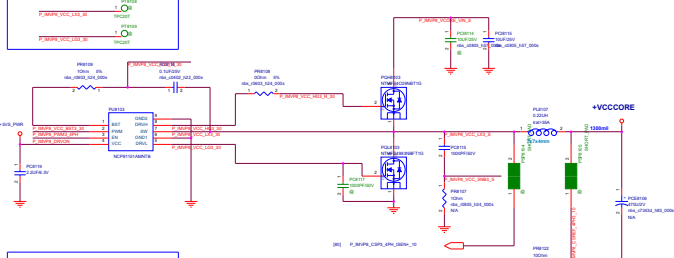
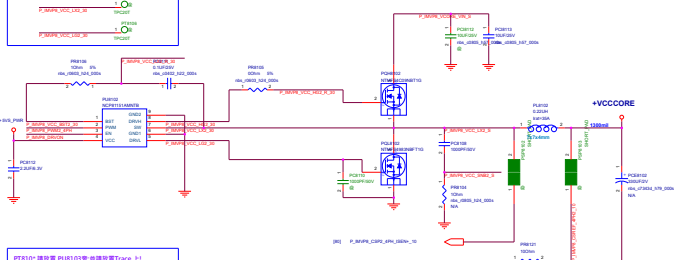
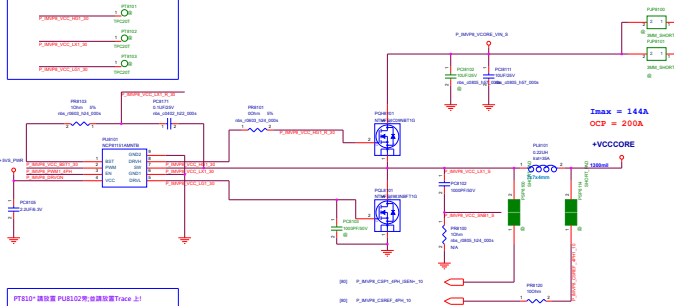


I_{max} = 10A
OCP = 15A

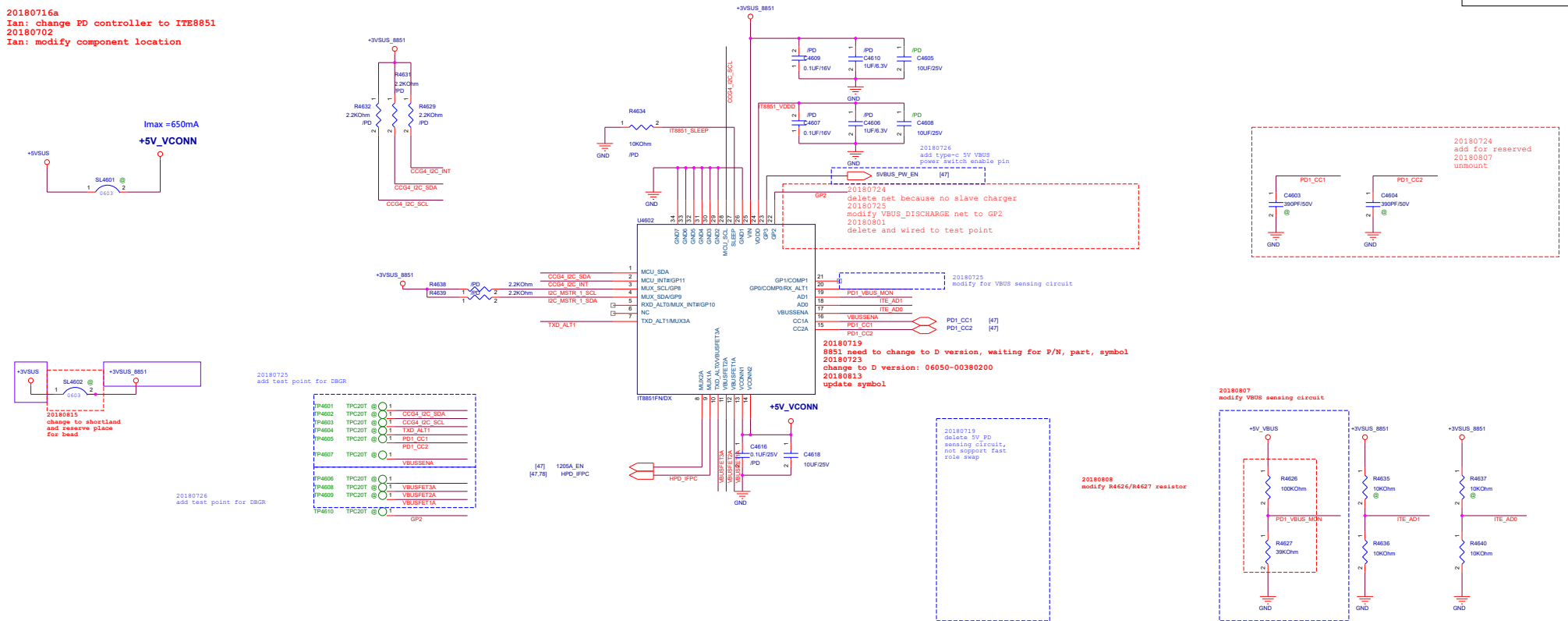
+1.05VSUS



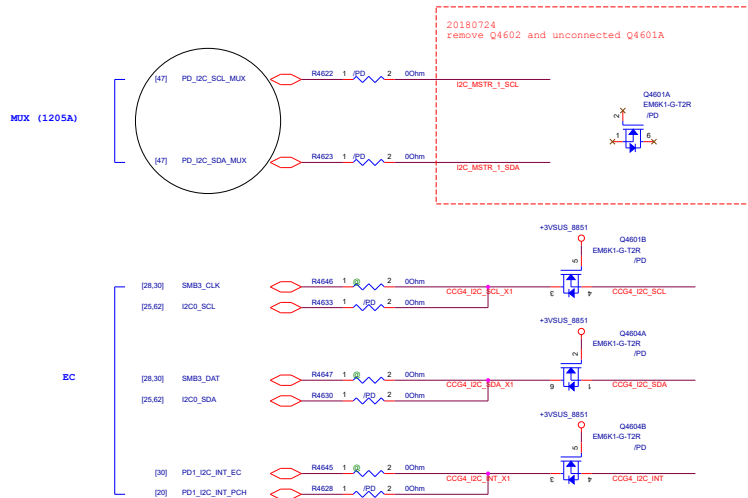
		Project Name		Rev	
		GM531GM		R1.0	
Title : PW_+VCCIO					
Size	A3	Dept.:	NB Power team	Engineer:	Joe
Date: Tuesday, April 16, 2019			Sheet	82	of 103



20180716a
Ian: change PD controller to ITE8851
20180702
Ian: modify component location



Different power plan prevent leakage



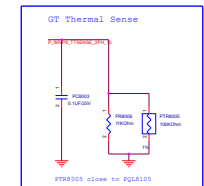
6.3 I2C0 Slave ID Decode

IT8851 provides one I2C slave interface, I2C0, for communication and four different slave ID decodes for I2C0 slave.

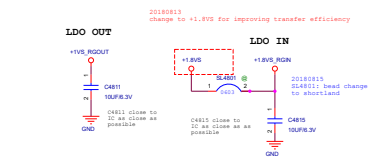
Table 6-1. I2C0 Slave ID Decode

AD1	AD0	Slave ID
0	0	7'h40
0	1	7'h42
1	0	7'h50
1	1	7'h52

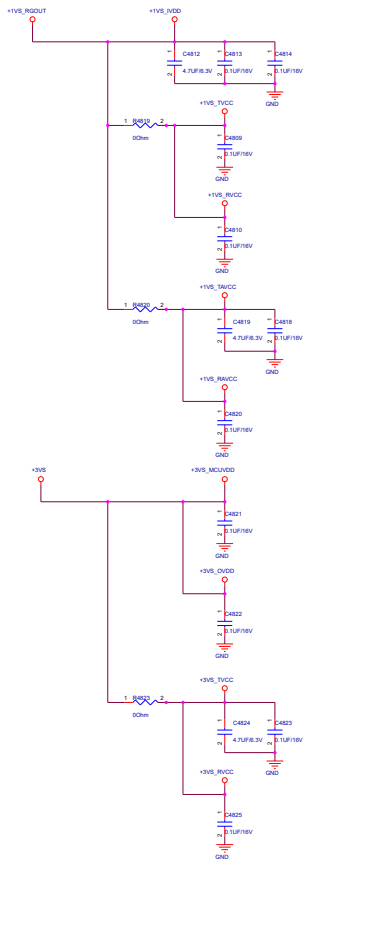
PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm



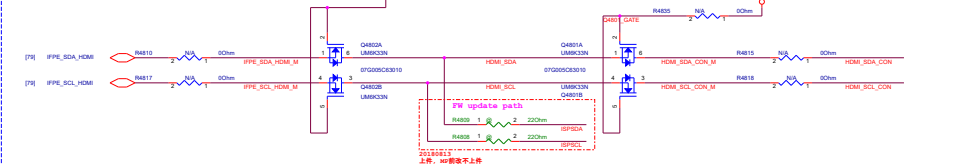
Internal Regulator option



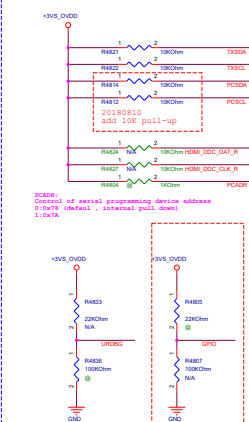
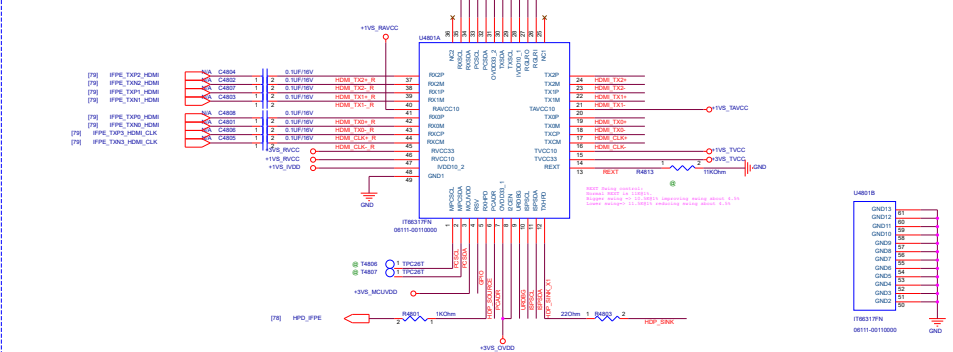
20180815 delete short land



HDMI Active-Level Shift



20180731 change HDMI retimer to IT66317

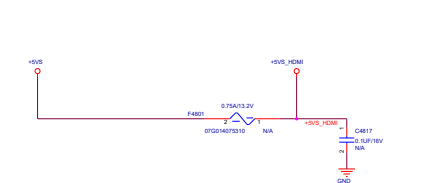


Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

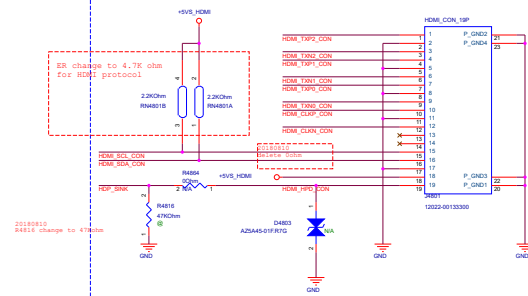
20180807 add for output swing HW control

Main Board

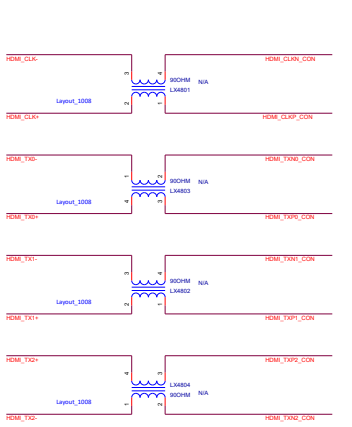
HDMI PWR_+5VS_HDMI

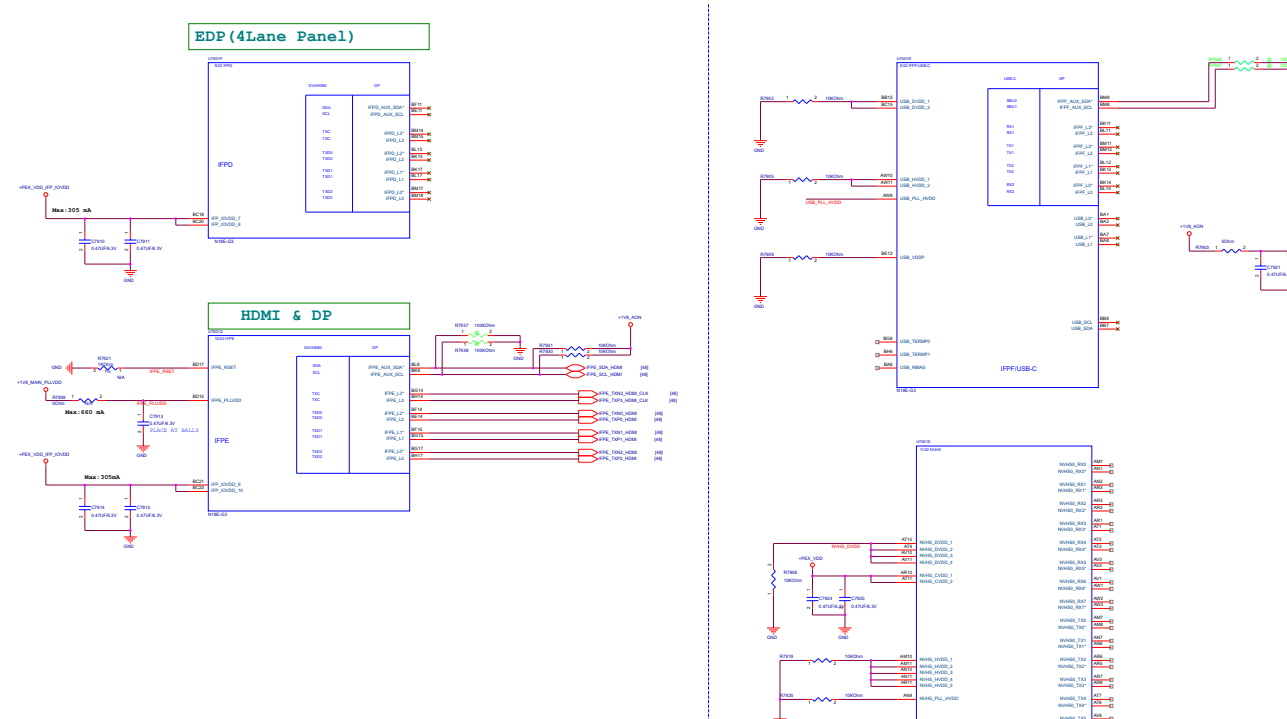


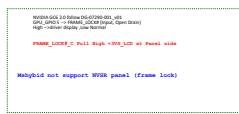
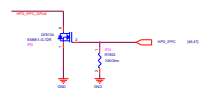
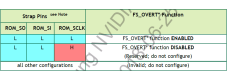
HDMI Conn.

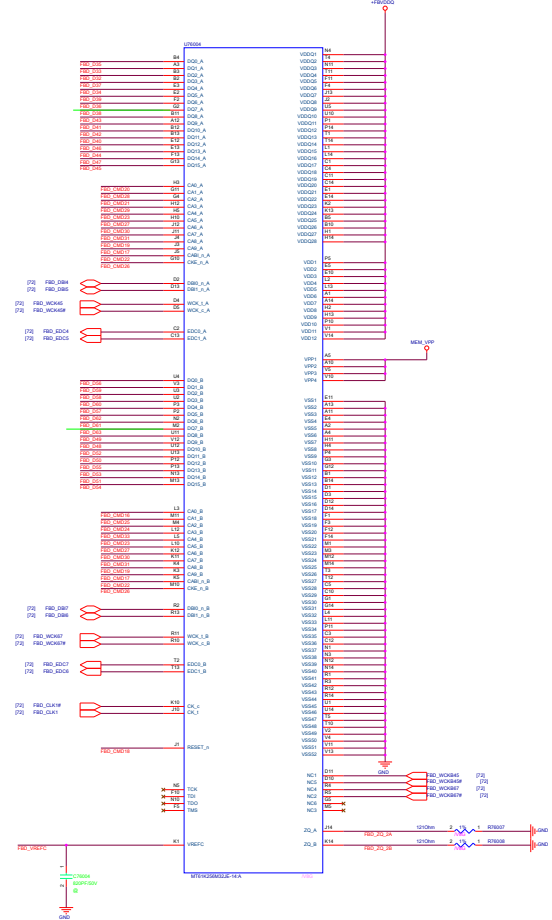
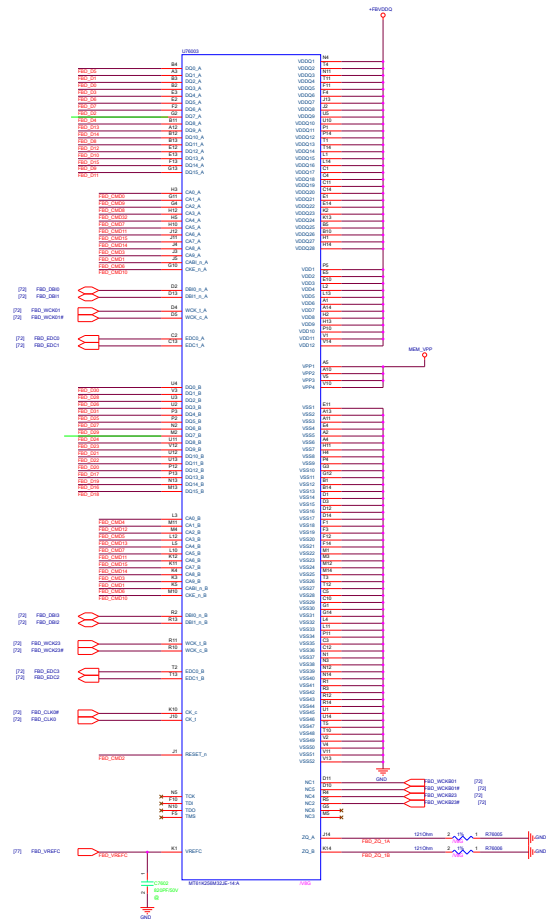


HDMI EMI

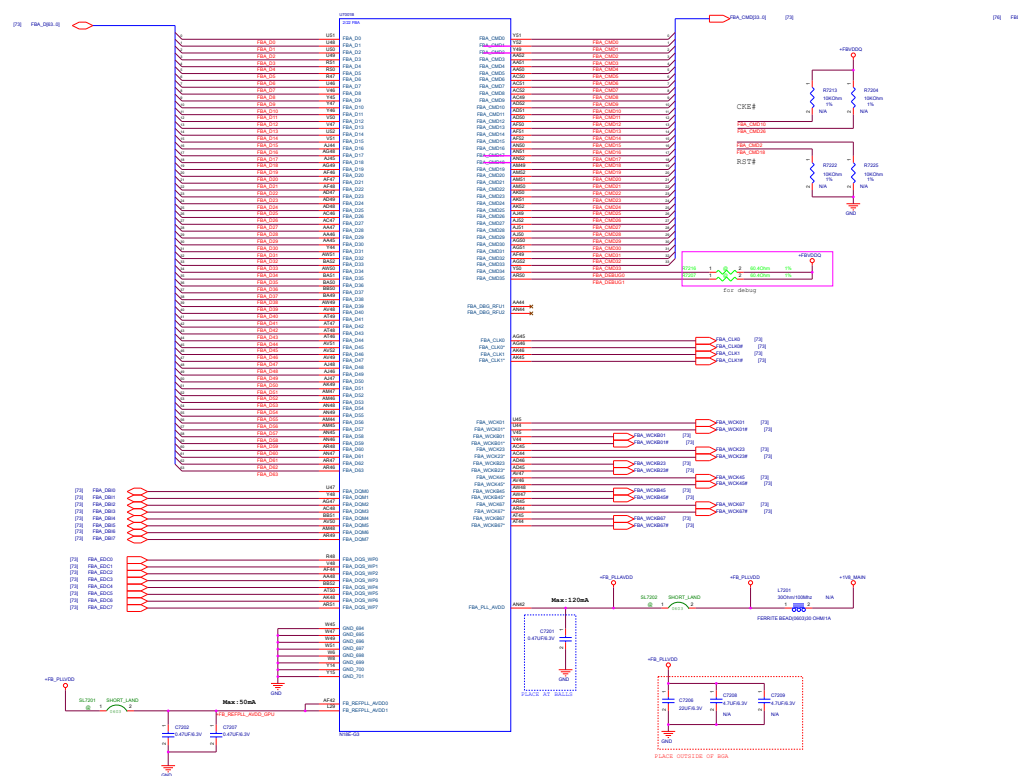




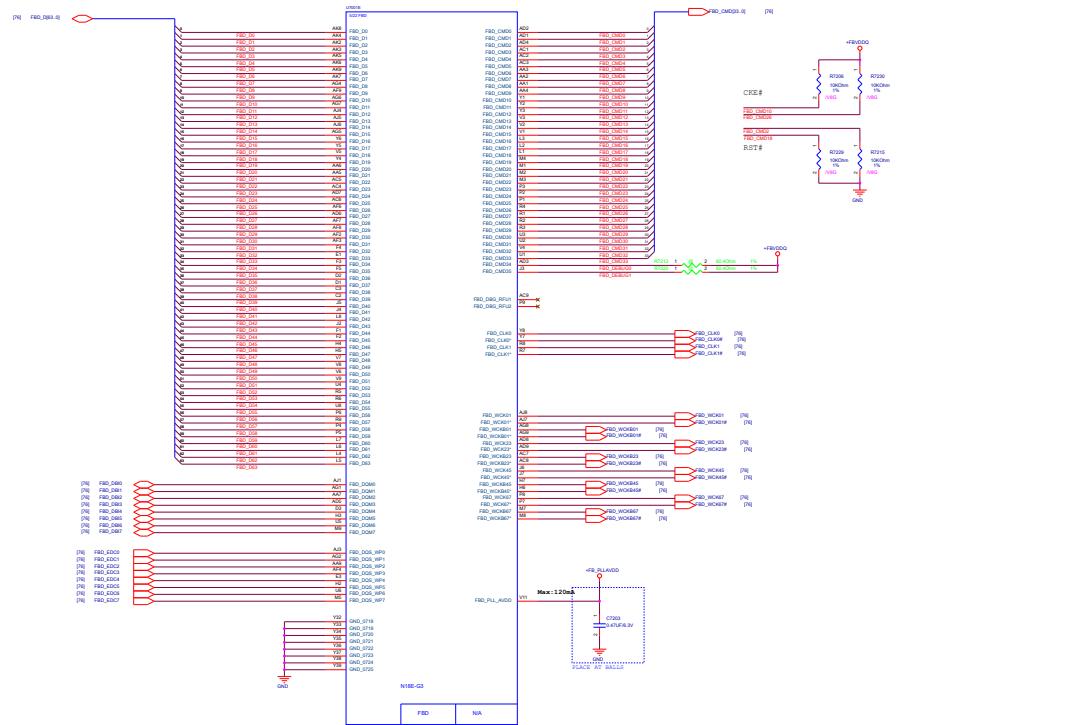




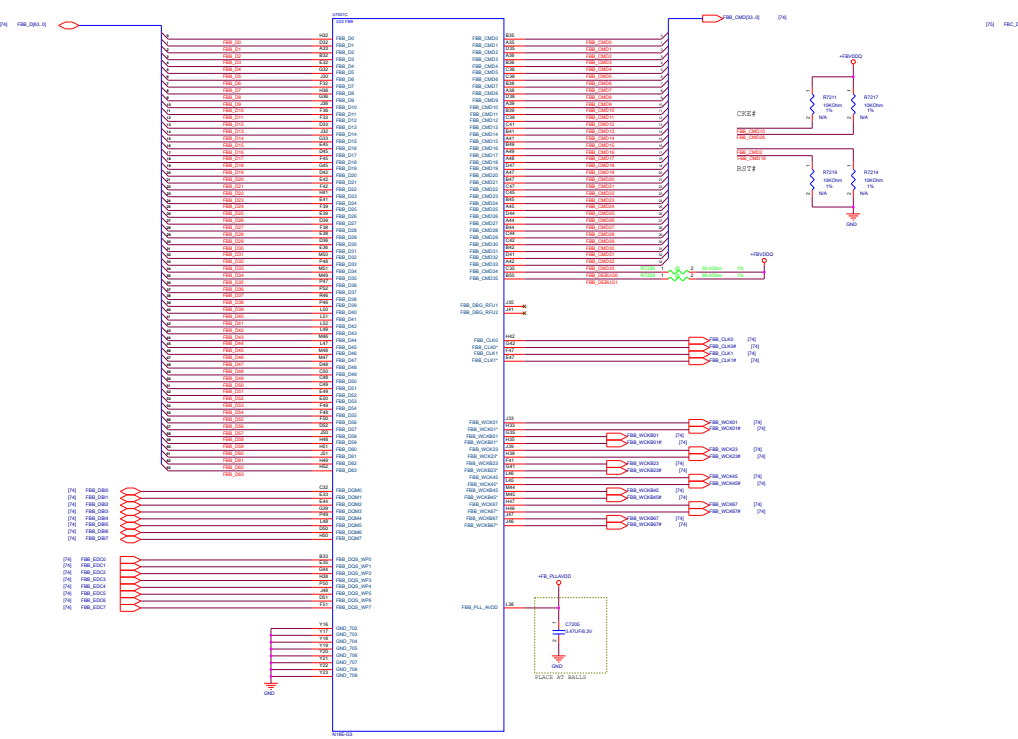
MEMORY: GPU FB Partition A



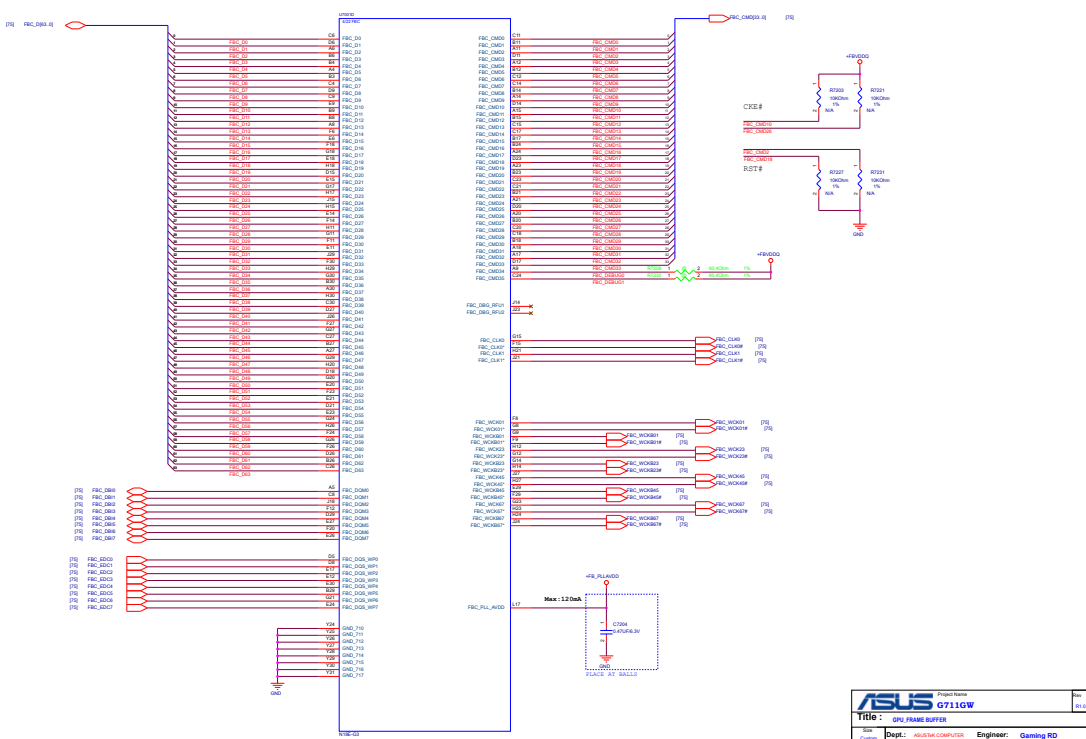
MEMORY: GPU FB Partition D

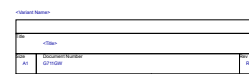


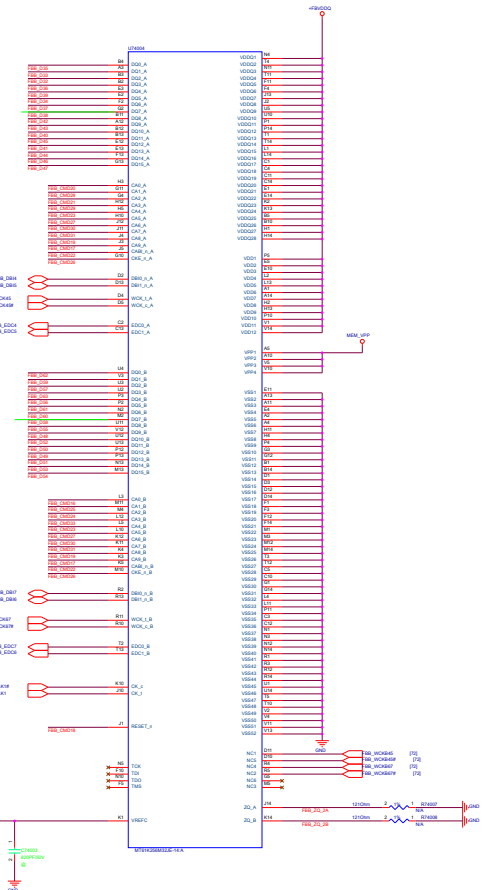
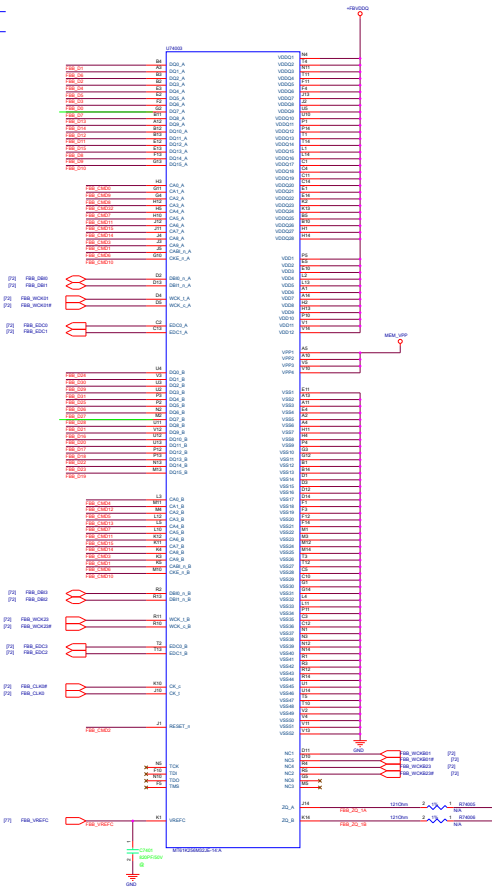
MEMORY: GPU FB Partition B



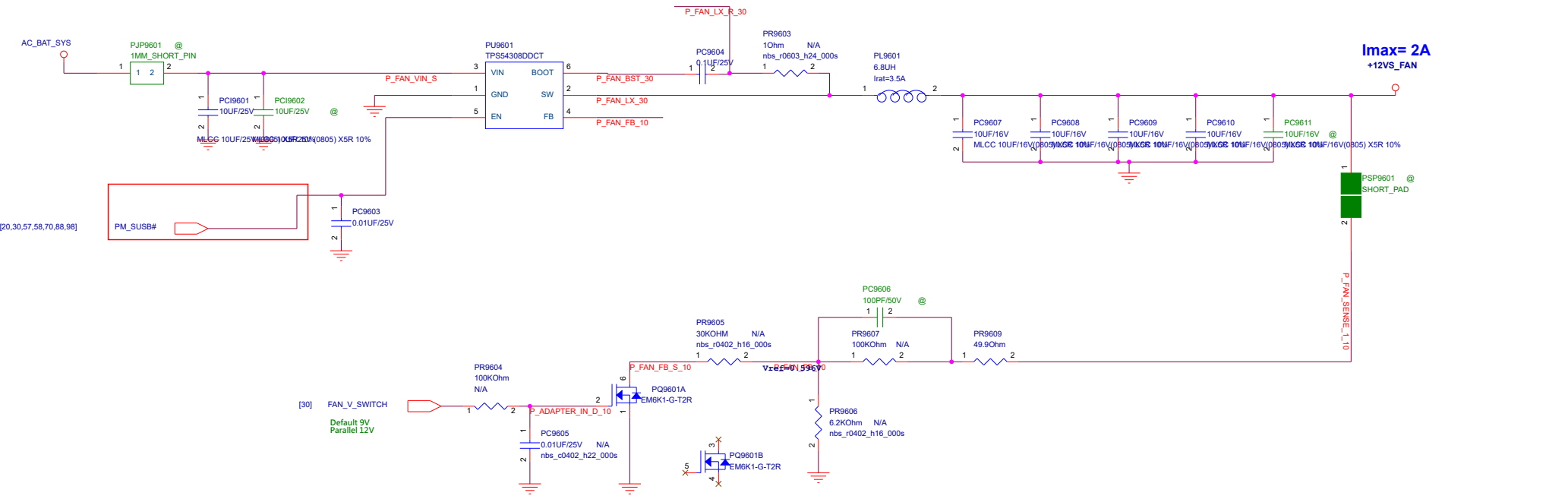
MEMORY: GPU FB Partition C








+12VS_FAN [For FAN]

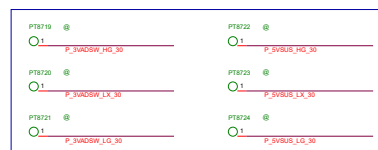
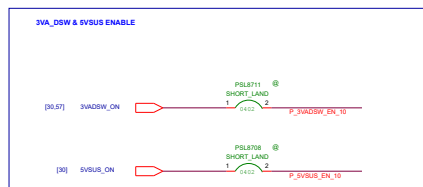


<Variant Name>

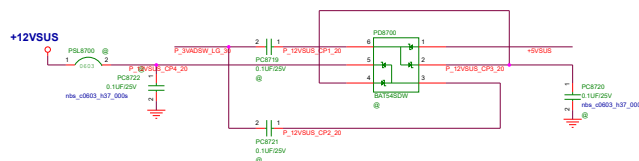
		Project Name		Rev
		Coffeelake-H		R1.0
Title : PW_+12VS_FAN				
Size B	Dept.: NB Power team		Engineer: Hon	
Date: Tuesday, April 16, 2019	Sheet	96	of	103



Imax= 12A
OCP=20A
+5VSUS



Imax= 10A
OCP= 15A
+3VA_DSW



請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

