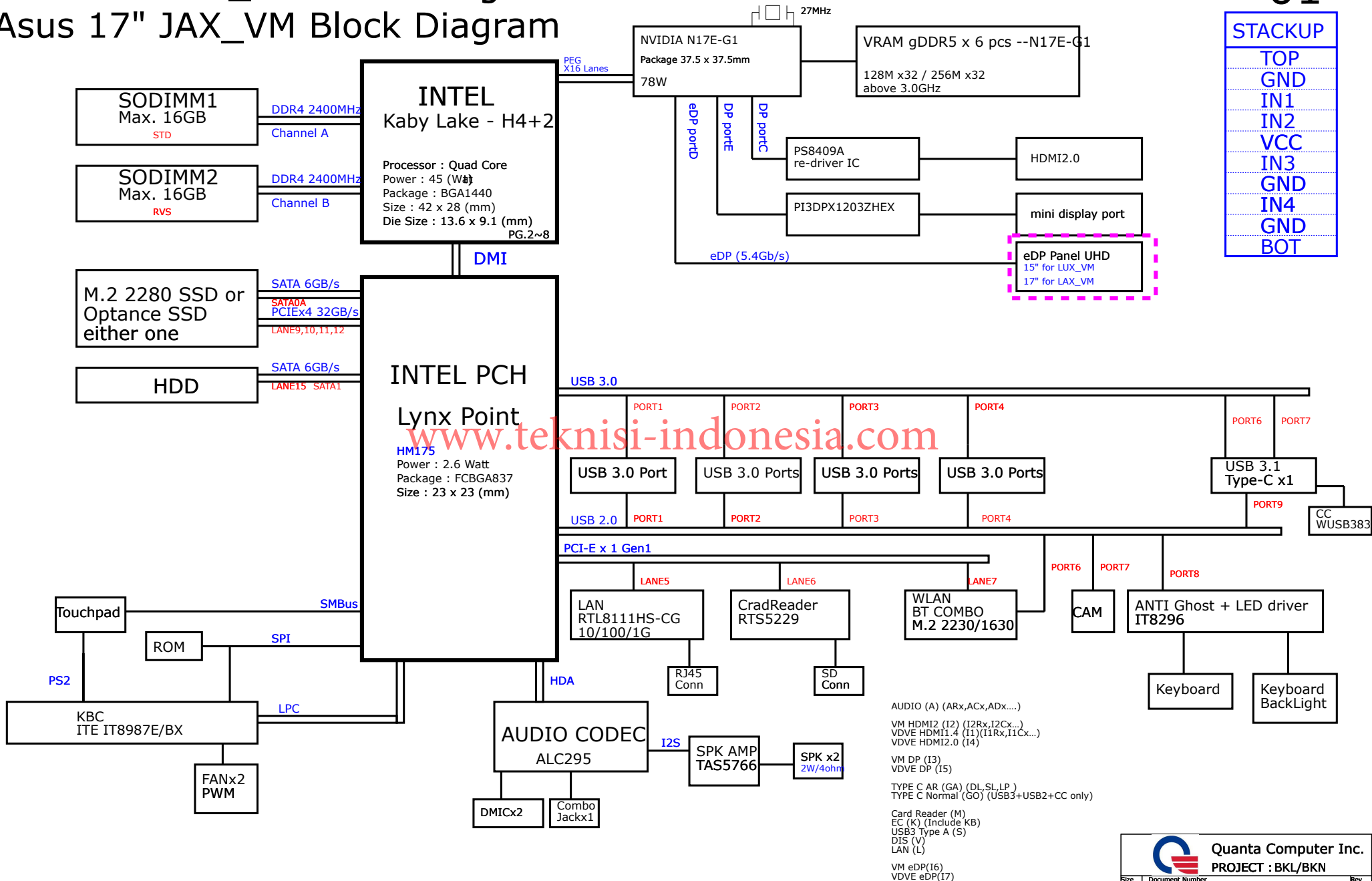


Asus 15" LUX_VM Block Diagram

Asus 17" JAX_VM Block Diagram

01



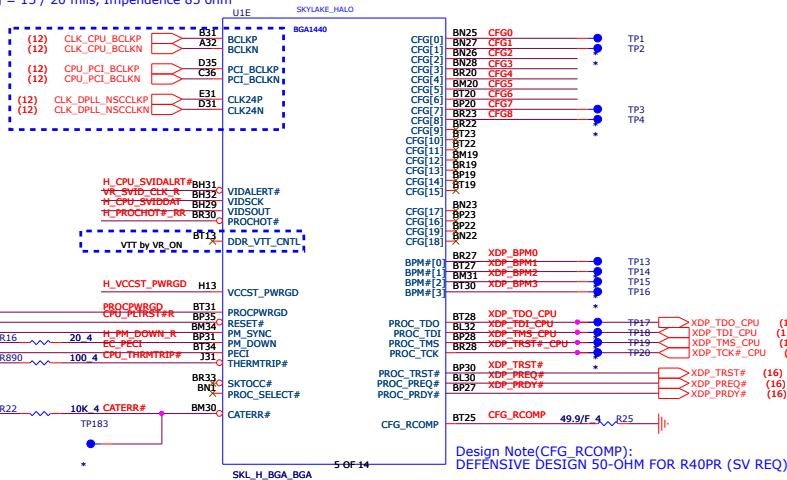
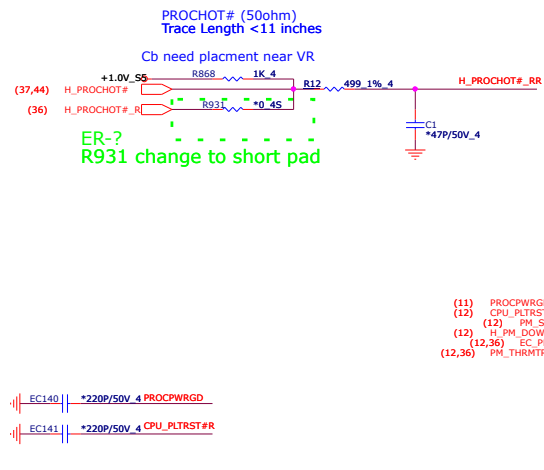
BKL
BKN

MP-01:change net SIO_EXT_SMI# connection to GPP_C22
MP-02 add KR133,KR134,KR135,KR136 15ohm, add KC95 for noise issue
MP-03 Add KR131 and KR132 for SHDN# debug
MP-04 Change KR72 from 200K to no-mount for MP
MP-05 DEL F2LED# net
MP-06 Add EMI_GND_PAD, EMI1,EMI2,EMI3,EMI4
MP-07 Add LED_PWR#KB net for separate LED for KB or LED board
MP-08 Add MF1 for Card reader power
MP-09 add VC435 to reduce noise
MP-10 change AC65,AC69,AC71,AC74 1000P to 2200P
MP-11 change AC4,AC5,AC6,AC7 1000P to mount
MP-12 change R945,R946,R947,R948,R949,R950 to 390ohm from 200ohm
MP-13 change PD10 to RB500-40 from 1SS355 for GC6 timing
MP-14 change PC295 to 220p from 2200p for GC6 timing
MP-15 change PR274 to 1K from 20K for GC6 timing
MP-16 change VR166 to 10K from 47K for GC6 timing
MP-17 Add R980,R981,Q48 for PCIE_SSD_LED# circuit (0725)

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KABY LAKE Processor (CLK,MISC,JTAG)

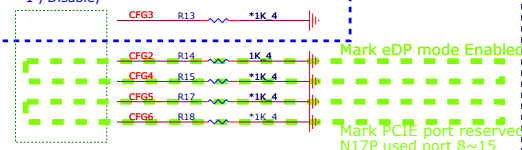
Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedence 85 ohm



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 . Disable:

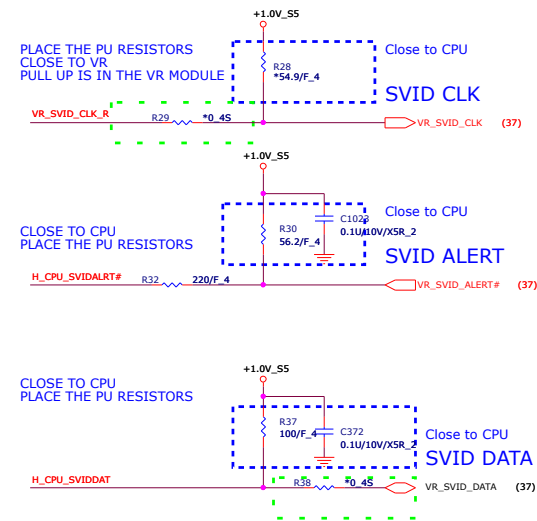


Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

CPU CORE SVID

Layout note:

1. Need routing together
2. ALERT need between CLK and DATA.



ER-?
R29,R38 change to short pad

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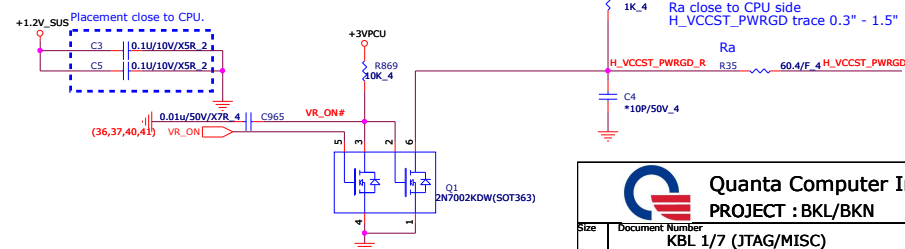
Configuration Signals:

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2] . This route is not needed on a Oxm board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS for training	

CPU VDDO

Note: please keep plane is enough for VDDQ 2.8A



KABY LAKE Processor (DMI,PEG,FDI)

03

dGPU

dGPU

AC-CAP Place on dGPU

PEG_RCOMP

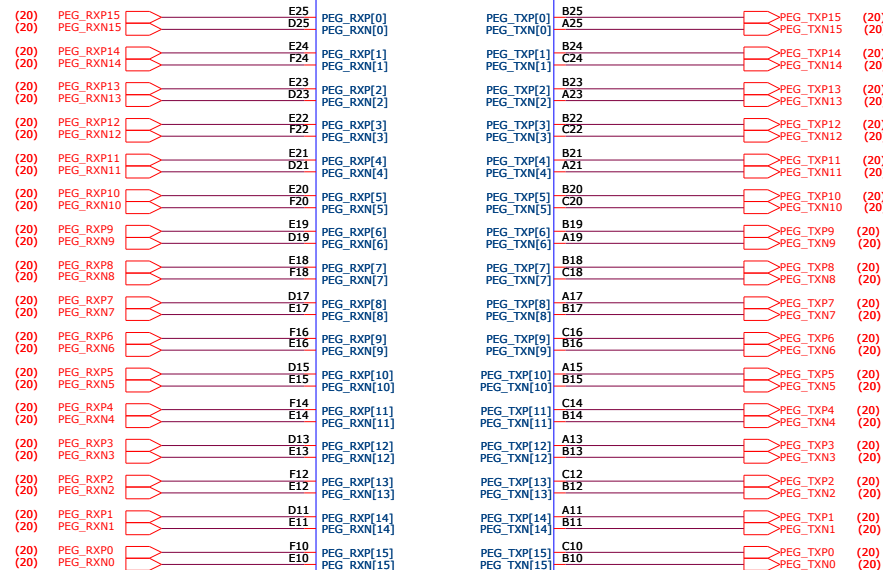
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

DMI

DMI

U1C SKYLAKE_HALO

BGA1440



+0.95V_VCCIO R40 24.9/F 4 PEG_COMP G2

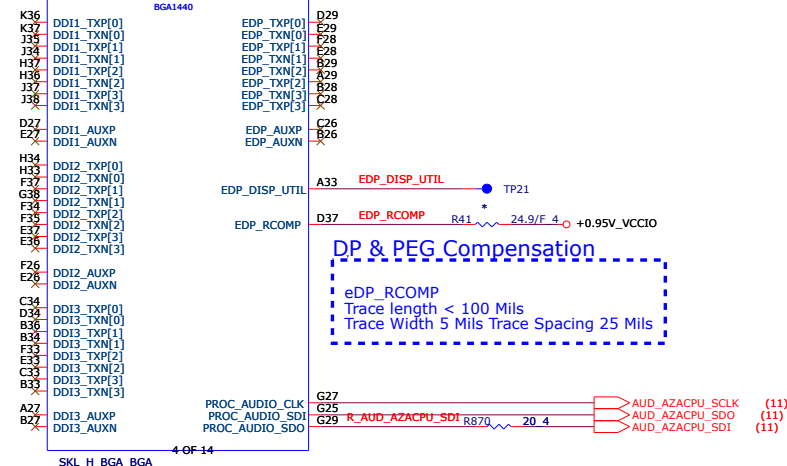
PEG_RCOMP

3 OF 14

SKL_H_BGA_BGA

U1D SKYLAKE_HALO

BGA1440



EDP_DISP_UTIL

EDP_RCOMP

DP & PEG Compensation

eDP_RCOMP
Trace length < 100 Mils
Trace Width 5 Mils Trace Spacing 25 Mils

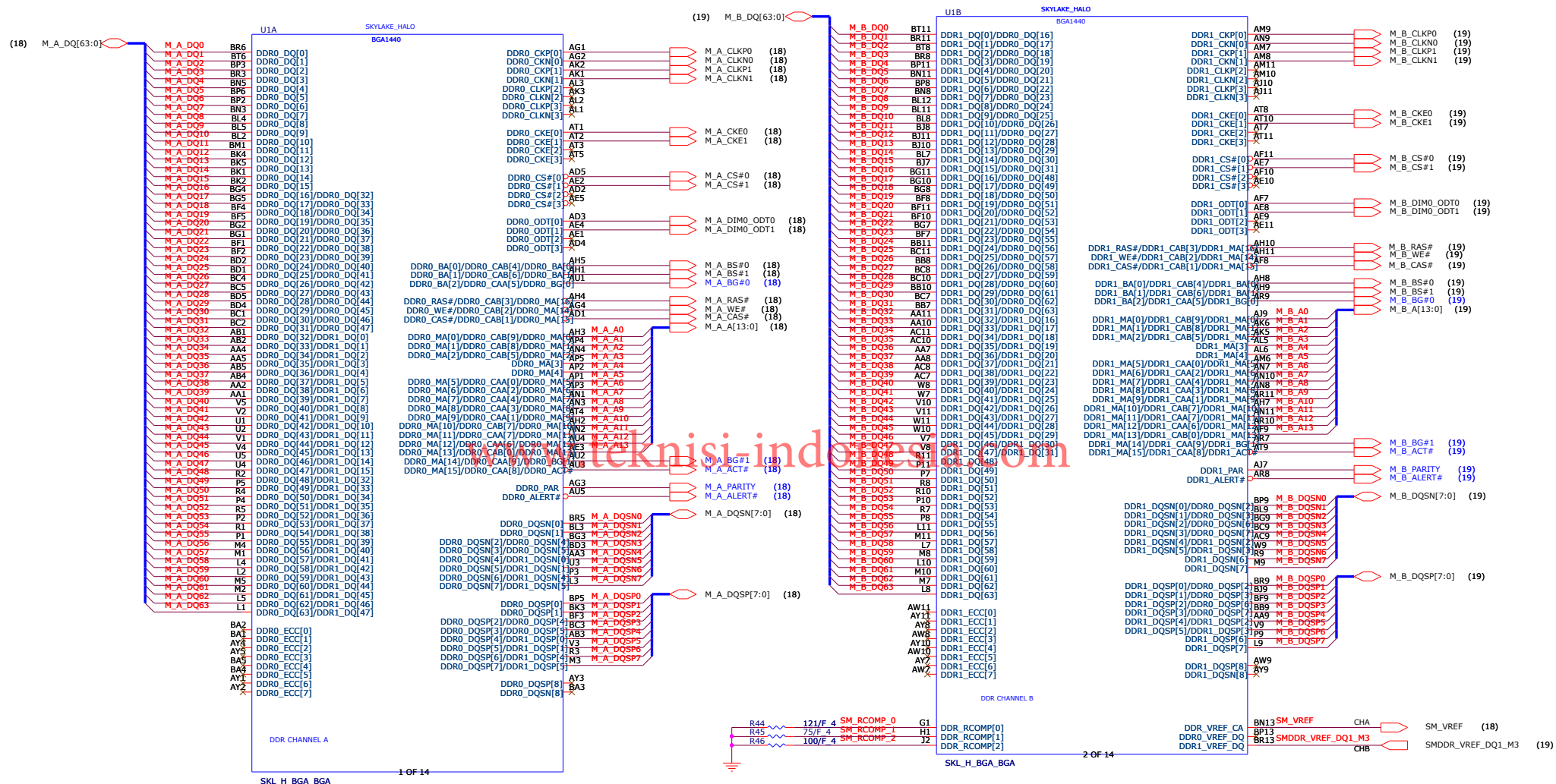
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO

AUD_AZACPU_SCLK (11)
AUD_AZACPU_SDO (11)
AUD_AZACPU_SDI (11)

4 OF 14

SKL_H_BGA_BGA

KABY LAKE Processor (DDR4)



KABY LAKE Processor (POWER)
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

UIN		SKYLAKE_HALO
		BGA1440
AJ29	VCCGT#189	
AJ30	VCCGT#188	
AJ31	VCCGT#187	VCCGTX#22
AJ32	VCCGT#186	VCCGTX#21
AJ33	VCCGT#185	VCCGTX#20
AJ34	VCCGT#184	VCCGTX#19
AJ35	VCCGT#183	VCCGTX#18
AK31	VCCGT#182	VCCGTX#17
AK32	VCCGT#181	VCCGTX#16
AK33	VCCGT#180	VCCGTX#15
AK34	VCCGT#179	VCCGTX#14
AK35	VCCGT#178	VCCGTX#13
AK36	VCCGT#177	VCCGTX#12
AK37	VCCGT#176	VCCGTX#11
AK38	VCCGT#175	VCCGTX#10
AL13	VCCGT#174	VCCGTX#9
AL29	VCCGT#173	VCCGTX#8
AL30	VCCGT#172	VCCGTX#7
AL31	VCCGT#171	VCCGTX#6
AL32	VCCGT#170	VCCGTX#5
AL33	VCCGT#169	VCCGTX#4
AL36	VCCGT#168	VCCGTX#3
AL37	VCCGT#167	VCCGTX#2
AL38	VCCGT#166	VCCGTX#1
AM13	VCCGT#165	
AM14	VCCGT#164	
AM29	VCCGT#163	
AM30	VCCGT#162	
AM31	VCCGT#161	
AM32	VCCGT#160	
AM33	VCCGT#159	
AM34	VCCGT#158	
AM35	VCCGT#157	
AM36	VCCGT#156	
AN13	VCCGT#155	
AN14	VCCGT#154	
AN21	VCCGT#153	
AN32	VCCGT#152	
AN33	VCCGT#151	
AN34	VCCGT#150	
AN35	VCCGT#149	
AN36	VCCGT#148	
AN37	VCCGT#147	
AN38	VCCGT#146	
AP13	VCCGT#145	
AP14	VCCGT#144	
AP29	VCCGT#143	
AP30	VCCGT#142	
AP31	VCCGT#141	
AP32	VCCGT#140	
AP33	VCCGT#139	
AP36	VCCGT#138	
AP37	VCCGT#137	
AP38	VCCGT#136	
AR29	VCCGT#135	
AR30	VCCGT#134	
AR31	VCCGT#133	
AR32	VCCGT#132	
AR33	VCCGT#131	
AR34	VCCGT#130	VCCGT_SENSE
AR35	VCCGT#129	VSSGTX_SENSE
AR36	VCCGT#128	VSSGT_SENSE
AT14	VCCGT#127	VCCGTX_SENSE
AT31	VCCGT#126	
AT32	VCCGT#125	
AT33	VCCGT#124	
AT34	VCCGT#123	
AT35	VCCGT#122	
AT36	VCCGT#121	
AT37	VCCGT#120	
AT38	VCCGT#119	
AU14	VCCGT#118	
AU29	VCCGT#117	
AU30	VCCGT#116	
AU31	VCCGT#115	
AU32	VCCGT#114	
AU35	VCCGT#113	
AU36	VCCGT#112	
AU37	VCCGT#111	
AU38	VCCGT#110	
	VCCGT#109	

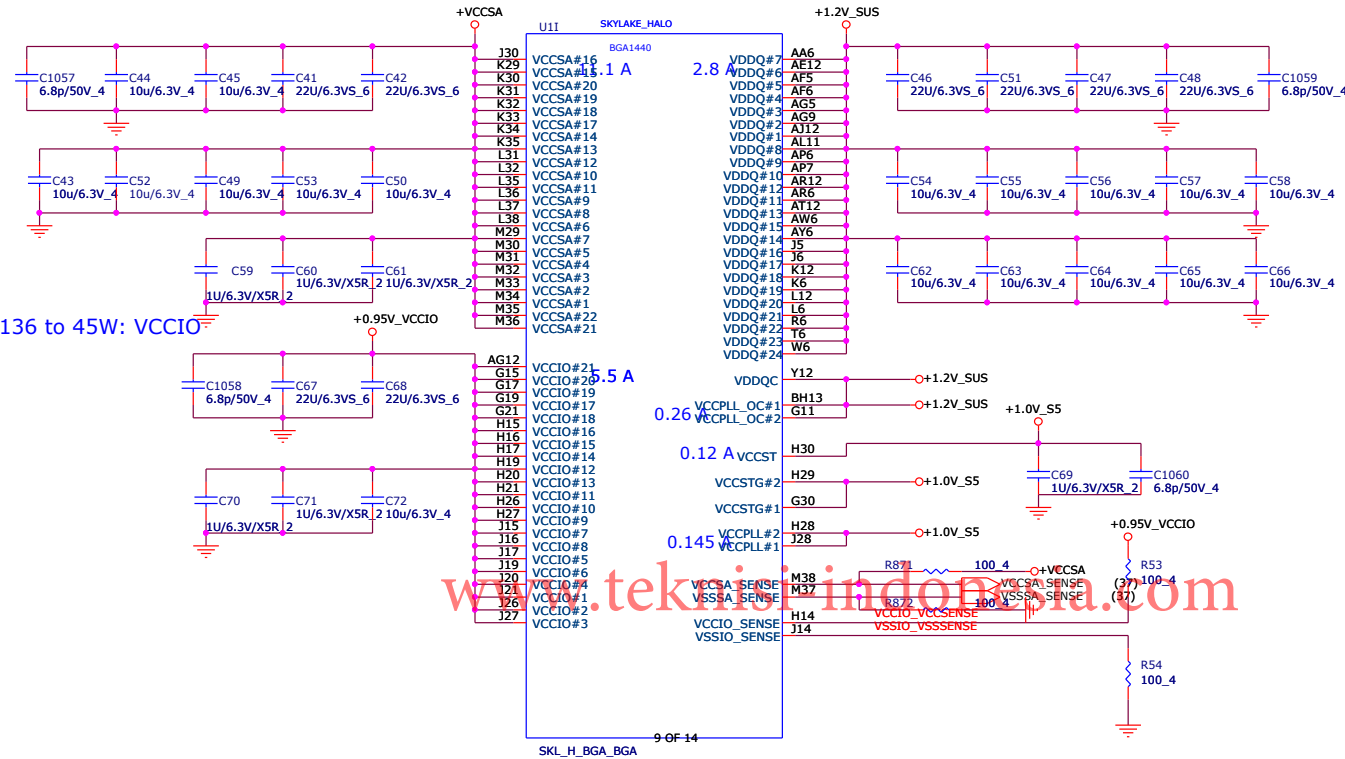
14 OF 14

SKL_H_BGA_BGA

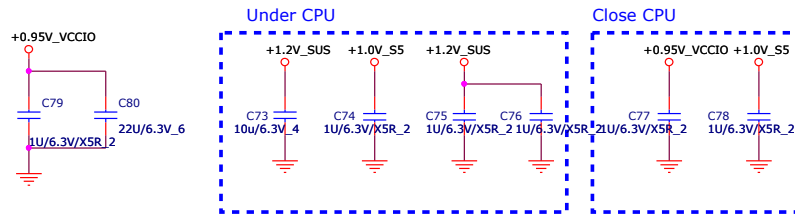
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Follow KBL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow KBL H EDS page 135 45W: VDDQ=2.8A



U11 SKYLAKE_HALO	
BGA1440	
B317	VCCOPC#9
B319	VCCOPC#8
B320	VCCOPC#10
BK17	VCCOPC#11
BK19	VCCOPC#12
BK20	VCCOPC#1
BL16	VCCOPC#2
BL17	VCCOPC#3
BL18	VCCOPC#4
BL19	VCCOPC#5
BL20	VCCOPC#13
BL21	VCCOPC#7
BM17	VCCOPC#6
BN17	VCCOPC#14
B323	RSVD#18
B326	RSVD#19
B327	RSVD#1
BK26	RSVD#2
BK27	RSVD#20
BL23	RSVD#3
BL24	RSVD#4
BL25	RSVD#21
BL26	RSVD#5
BL27	RSVD#22
BL28	RSVD#7
BM24	RSVD#6
	RSVD#17
BL15	VCCOPC_SENSE
BM16	VSSOPC_SENSE
BL22	RSVD#16
BM22	RSVD#15
BP15	VCCEPIO#1
BR15	VCCEPIO#3
BT15	VCCEPIO#2
BP16	RSVD#10
BR16	RSVD#9
BT16	RSVD#8
BN15	VCCEPIO_SENSE
BM15	VSSPIO_SENSE
BP17	RSVD#11
BN16	RSVD#12
BM14	VCC_OPC_IP8#1
BL14	VCC_OPC_IP8#2
B335	RSVD#14
B336	RSVD#13
AT13	ZVM#
AW13	MSM#
AU13	ZVM2#
AY13	MSM2#
BT29	OPC_RCOMP
BR25	OPCE_RCOMP
BP25	OPCE_RCOMP2
10 OF 14	
SKL_H_BGA_BGA	



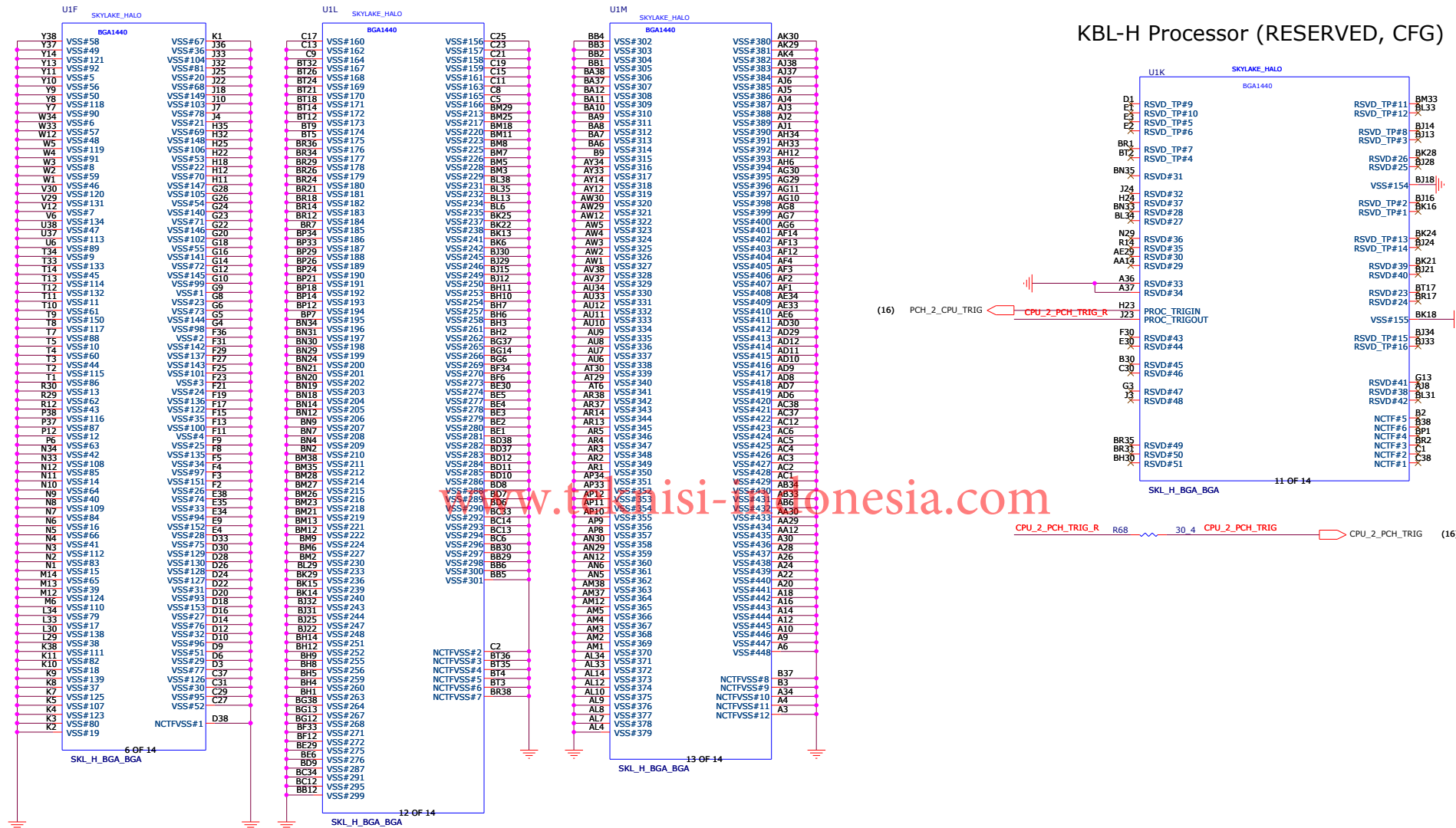
Follow KBL H EDS page 131 to 45W(GT2): VCC_CORE=68A

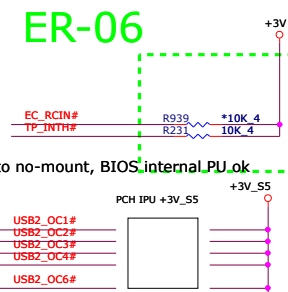


Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impedance 50 ohm

KBL-HProcessor (GND)

KBL-H Processor (RESERVED, CFG)





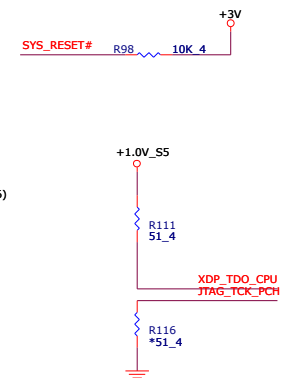
USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 MB
PORT3	USB3 MB
PORT4	USB3 MB
PORT5	USB3 MB
PORT6	NC



```

- ACZ_RST#AUDI
HDA Bus(CLG)

```



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RTC

+3V_RTC

30mS

R129 *0.4/S

R130 *10M_4

C176 1U/6.3V/X5R_2

R132 20K/F_4

R137 20K/F_4

C174 1U/6.3V/X5R_2

C177 1U/6.3V/X5R_2

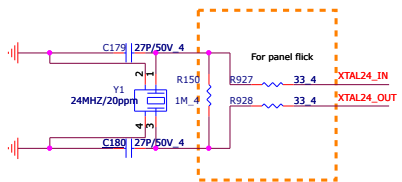
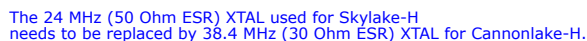
J1 *SOLDER JUMPER_2

RTC_RST#

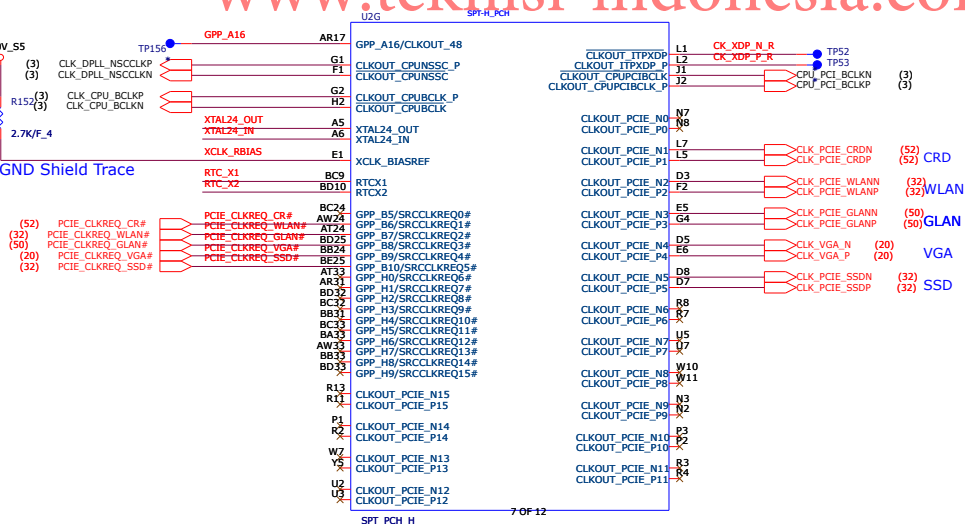
SRCT_RST#

ER-05

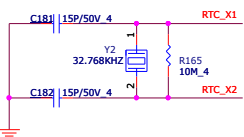
ER-05

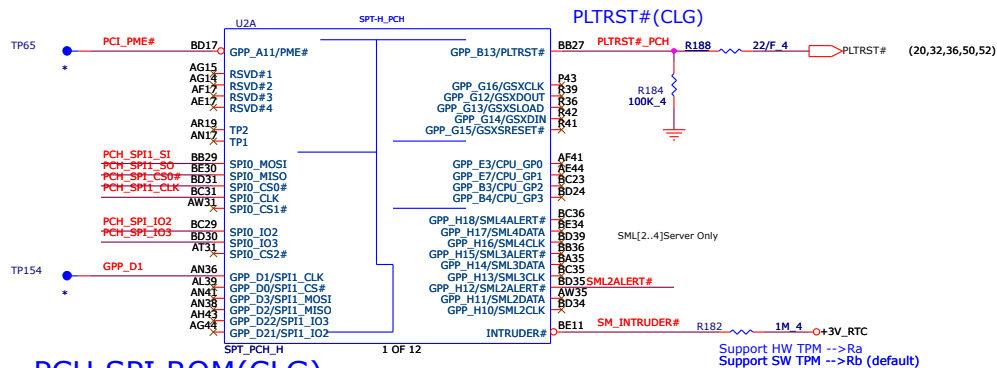


Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out: 4-10 mil Wide GND Shield Trace

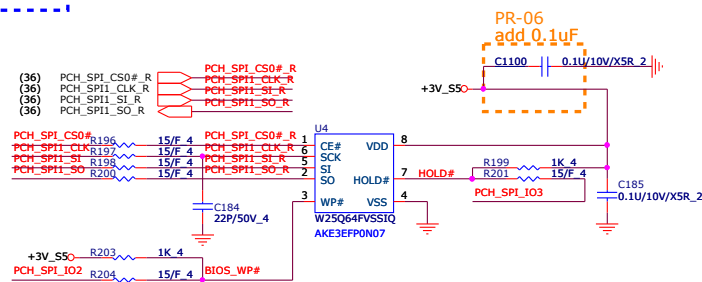
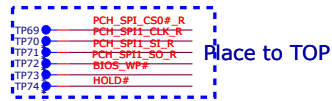


RTC Clock 32.768KHz





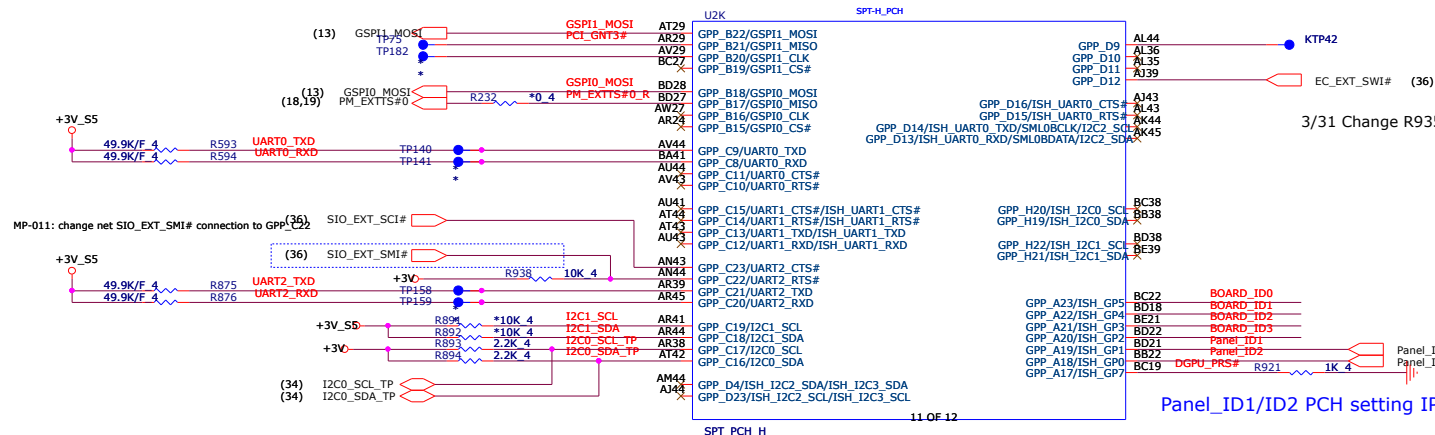
PCH SPI ROM (CLG)



Skylake-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	xx* PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) Default 1 = Enable Top Swap Mode	
GPP_B18 (GSP10_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) Default 1 = Enable No Reboot Mode	TP171 → GSP10_MOSI (14)
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS (iPD 20K) Default 1 = Enable Intel ME Cryp to TLS to support AMT TLS	+3V_SS0 → R930 → 1K 4 → SMBALERT# (11)
GPP_B22 (GSP11_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	0 = *SPI (iPD 20K) Default 1 = LPC	TP172 → GSP11_MOSI (14)
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) Default 1 = eSPI selected for EC	TP162 → SML0ALERT# (11)
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP166 → SML1ALERT# (11)
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) Default 1 = Disable Flash Descriptor Security (Override)	
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) (Default) 1 = Port B is detected	
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) (Default) 1 = Port C is detected	
GPP_I10 (DDPD_CTRLDATA)	Display Port D Detected	PCH_PWROK	0 = *Port D is not detected (iPD 20K) Default 1 = Port D is detected	
GPP_H12 (SML2ALERT#)	Reserved	RSMRST#	(iPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP163 → SML2ALERT#

+3V_S5

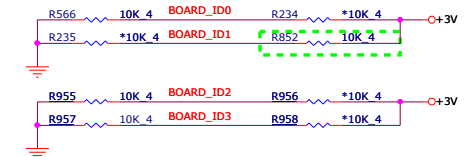


3/31 Change R935 and R936 form 10K to no-mount, BIOS internal PU ok

R need place to BOT

GPIO Pull-up/Pull-down(CLG)

4/14:Change R852 mount and R235 no mount for VD15 MB ID



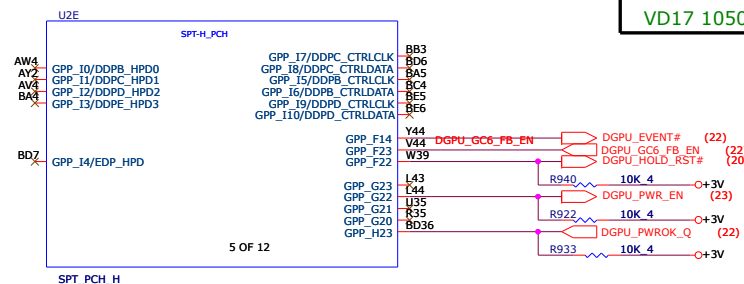
Panel_ID1/ID2 PCH setting IPU

R need place to BOT

	Panel ID1	Panel ID2
FHD	1	1
4K2K	1	0
HD	0	1

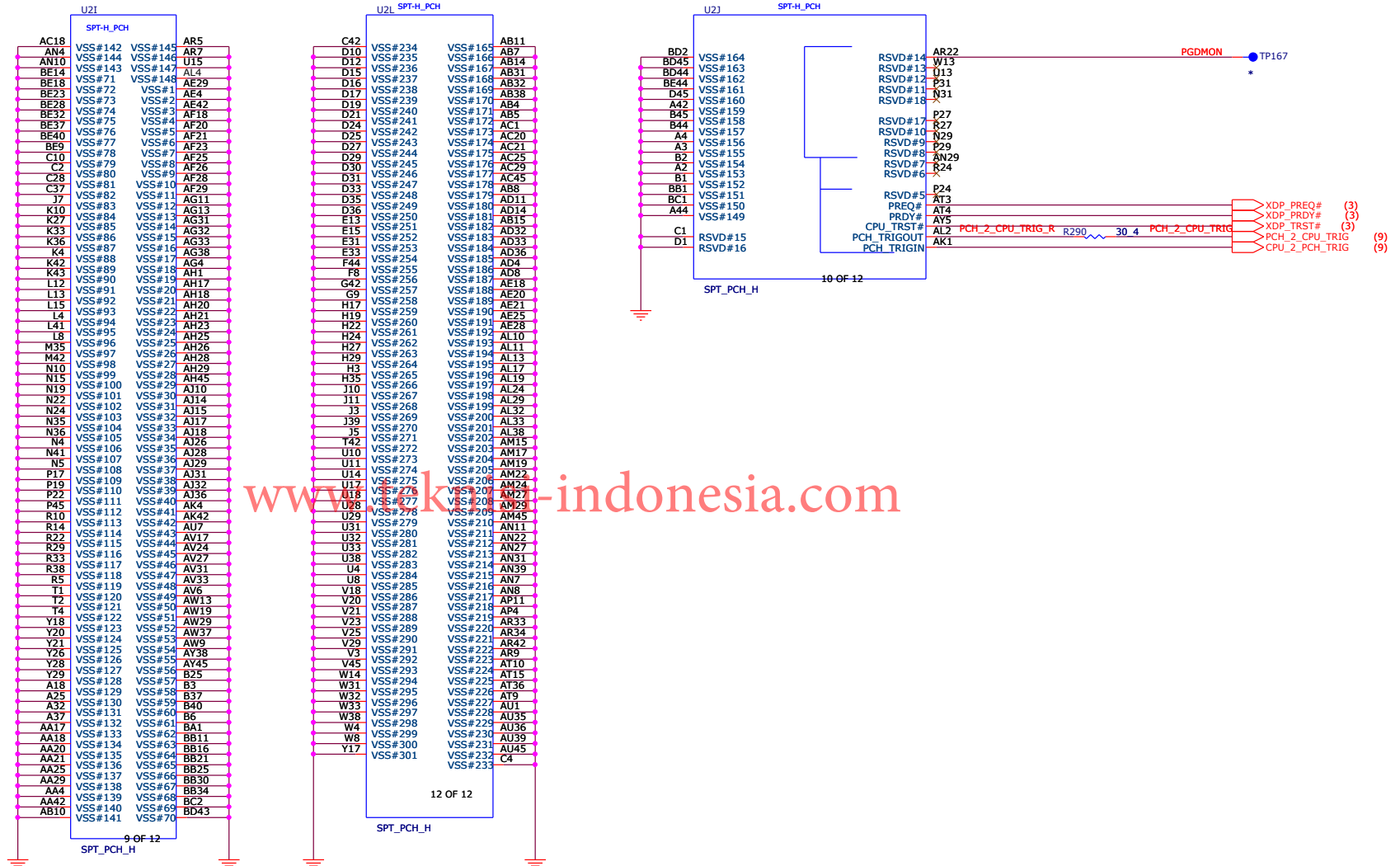
```
HPD0 --> HDMI1.4
HPD2 --> DP++
```

- This signal has a weak internal pull-down.
- 0 = Port C and D is not detected.
- 1 = Port C and D is detected.

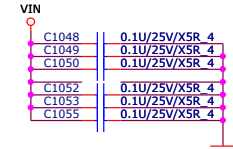


	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
VM15 1060 ID1 ROG	0	1	0	0
VM15 1060 ID2	0	1	0	1
VD15 1050 ID1 ROG	1	0	0	0
VD15 1050Ti ID1 ROG	1	1	0	0
VD15 1050Ti ID2	1	1	0	1
VD15 1050 ID2	1	0	0	1
VM17 1060 ID1 ROG	0	1	1	0
VM17 1060 ID2	0	1	1	1
VE17 1050 ID1 ROG	1	0	1	0
VD17 1050 ID2	1	0	1	1
VD17 1050Ti ID1 ROG	1	1	1	0
VD17 1050Ti ID2	1	1	1	1

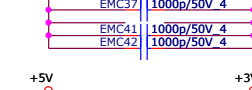
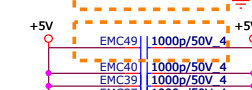
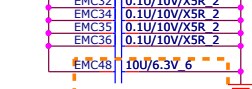
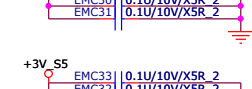
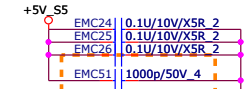
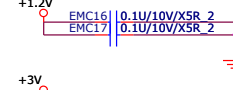
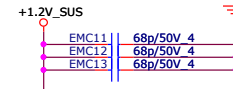
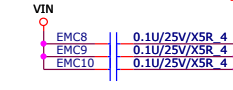
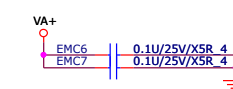
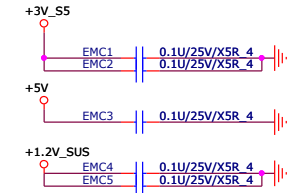
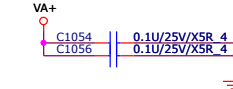




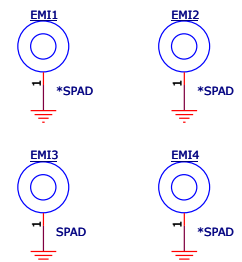
placement on TOP SIDE VIN Plane



placement on TOP SIDE VA+ Plane

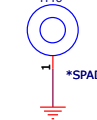
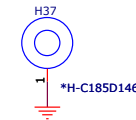
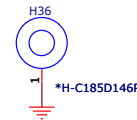
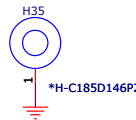
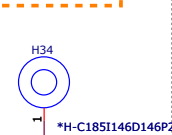
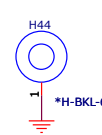
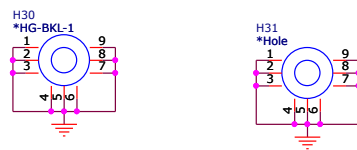
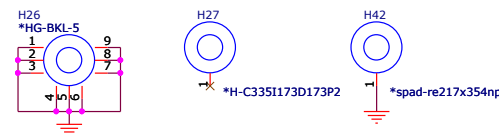
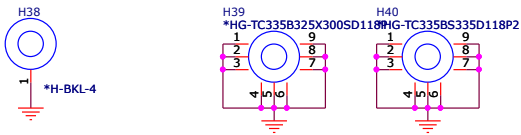
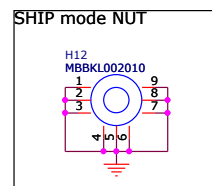
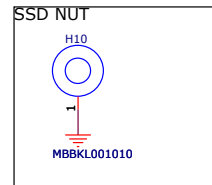
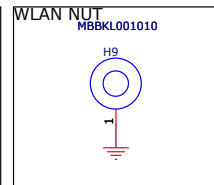
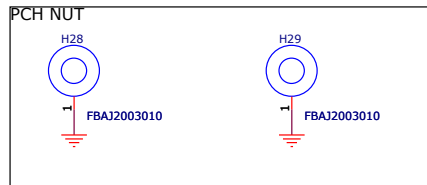
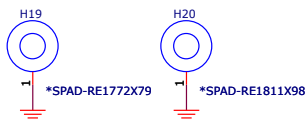
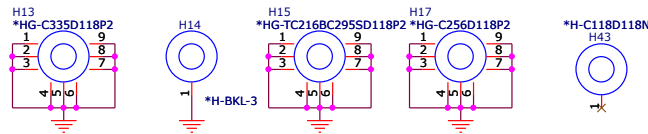
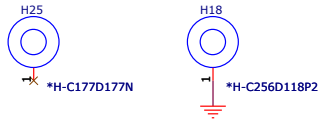
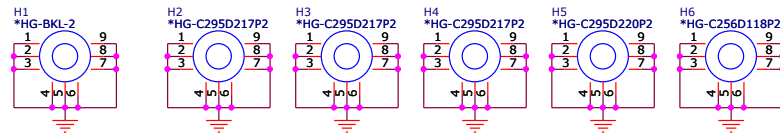


MP-6 Add EMI pad



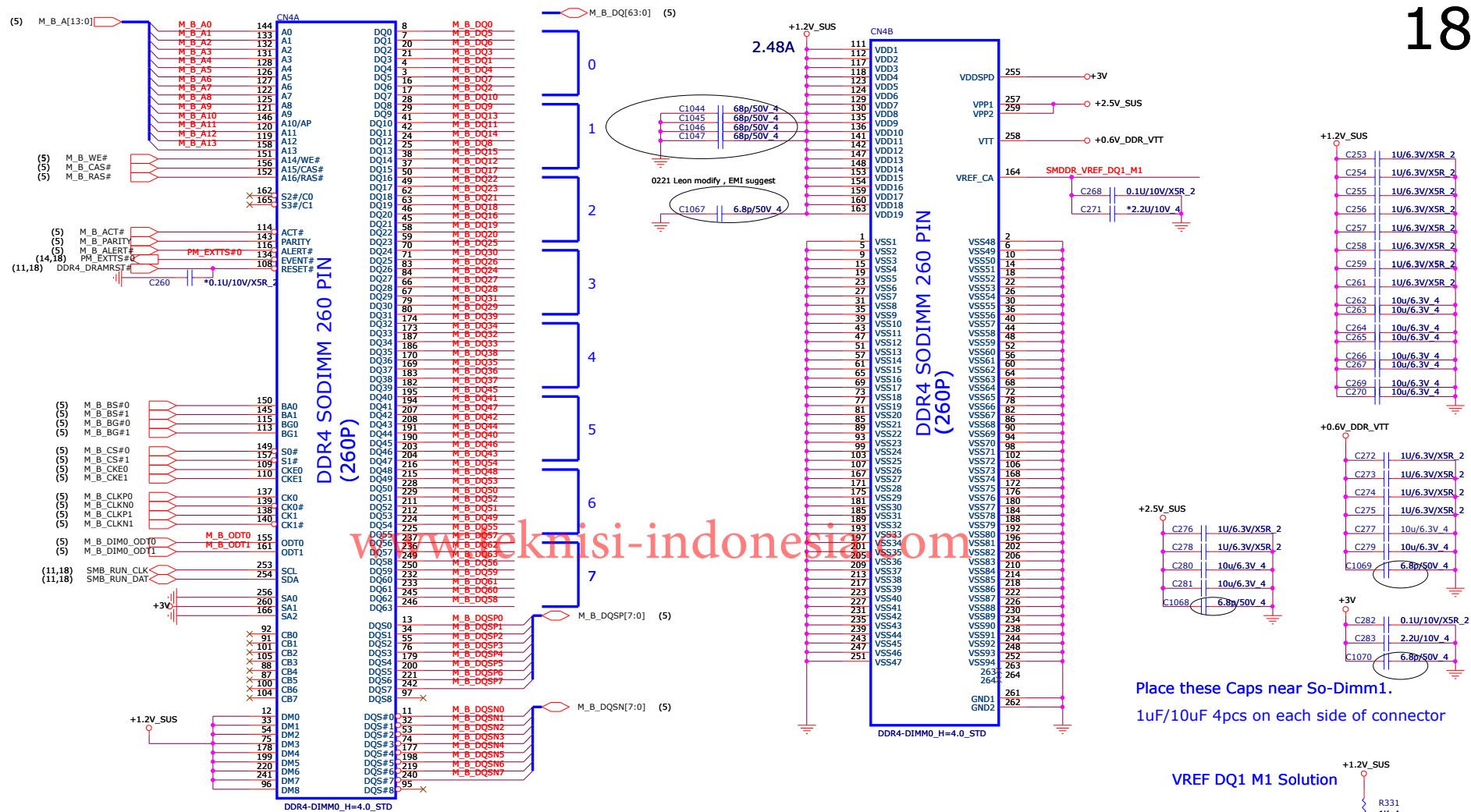
ER-14
4/7:H16 ADD 0ohm x2 to GND for ESD verify.

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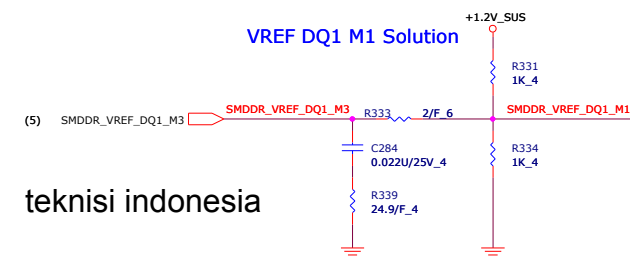


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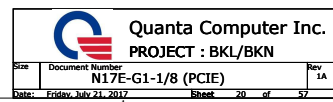


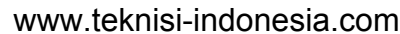


Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector



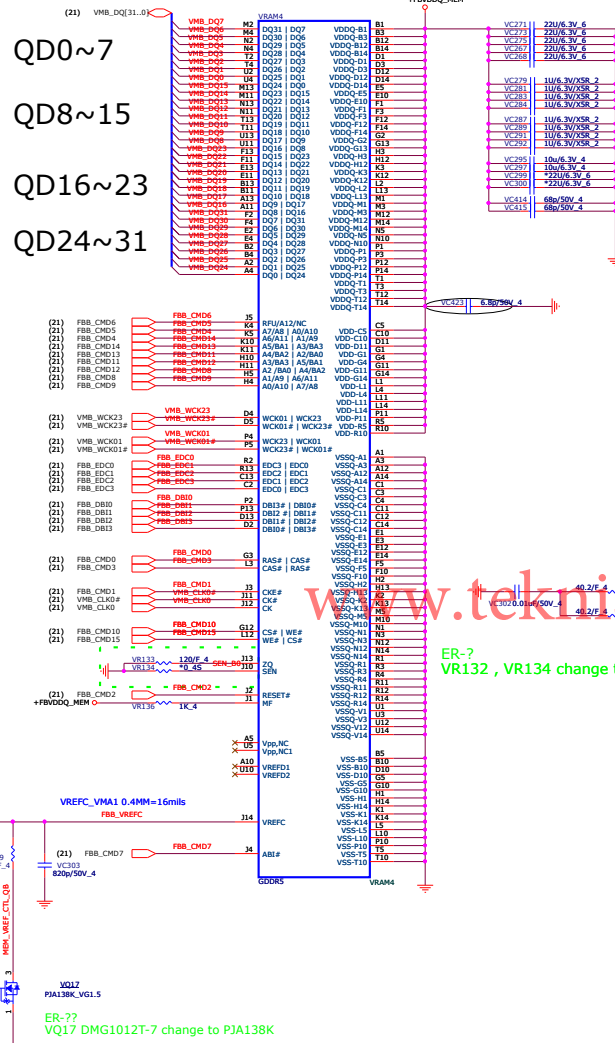
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Channel 0
<0-31>

MF=1 mirrored

Channel 1
<0-31>

MF=0 Non-mirrored

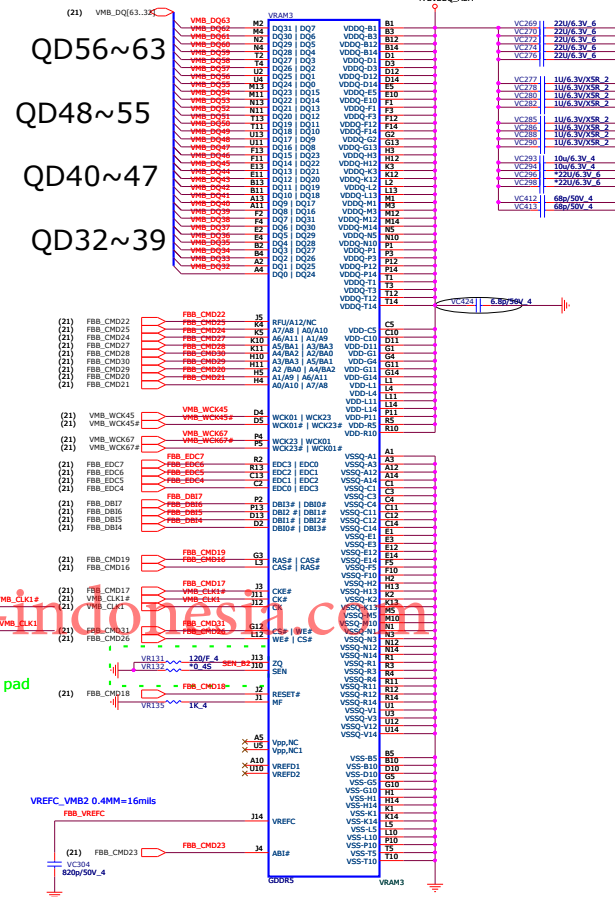


Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CM00	CAS*	CM016	CAS*
CM01	CKE	CM017	CKE
CM02	RST*	CM018	RST*
CM03	RAS*	CM019	RAS*
CM04	A0_A9	CM020	A1_A9
CM05	A0_A10	CM021	A0_A10
CM06	A12_RFU	CM022	A12_RFU
CM07	AB*	CM023	AB*
CM08	A6_A11	CM024	A6_A11
CM09	A7_A8	CM025	A7_A8
CM10	WE*	CM026	WE*
CM11	A5_BA1	CM027	A5_BA1
CM12	A4_BA2	CM028	A4_BA2
CM13	A3_BA0	CM029	A3_BA0
CM14	A3_BA3	CM030	A3_BA3
CM15	CS*	CM031	CS*

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

MF=0 Non-mirrored

MF=0 Non-mirrored

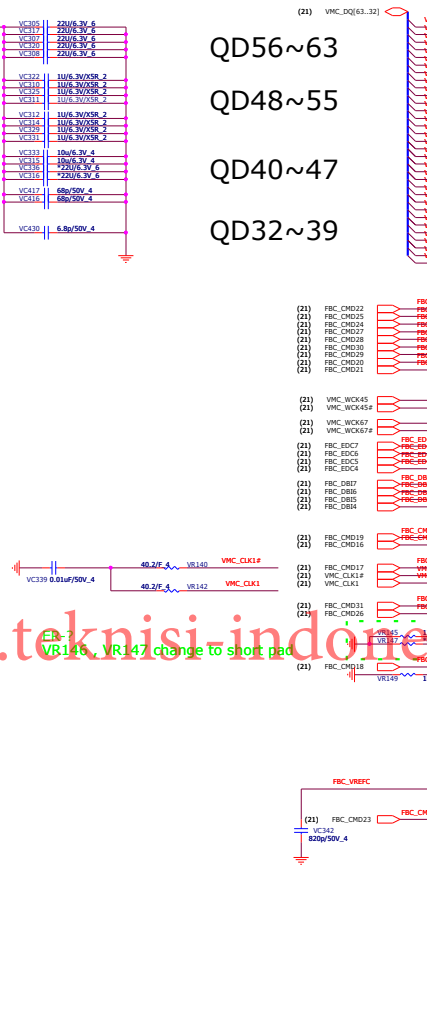
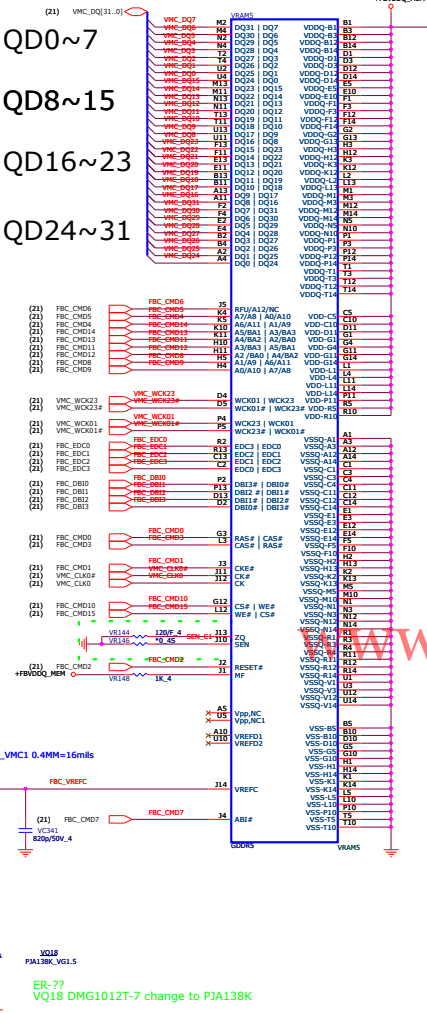


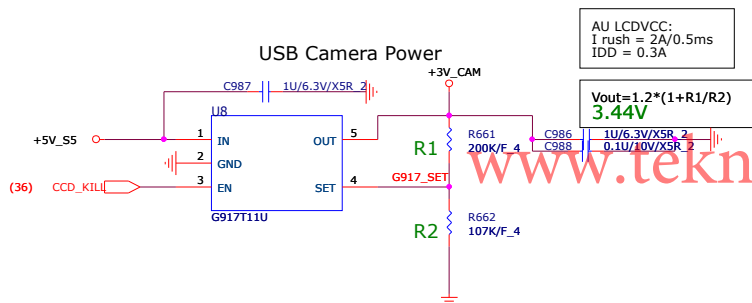
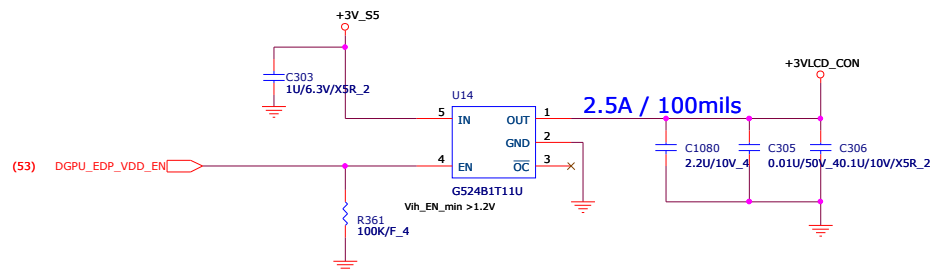
Table 7-5. GDDR5 Mode F Mapping

G83-256	Channel 0 0..31	G83-256	Channel 1 32..63
CM00	CAS*	CM016	CAS*
CM01	CKE	CM017	CKE
CM02	BS*	CM018	BS*
CM03	BAS*	CM019	BAS*
CM04	A1_A9	CM020	A1_A9
CM05	A0_A10	CM021	A0_A10
CM06	A12_RFU	CM022	A12_RFU
CM07	AB*	CM023	AB*
CM08	A6_A11	CM024	A6_A11
CM09	A7_A8	CM025	A7_A8
CM010	WE*	CM026	WE*
CM011	A5_BA1	CM027	A5_BA1
CM012	A4_BA2	CM028	A4_BA2
CM013	A2_BA0	CM029	A2_BA0
CM014	A3_BA3	CM030	A3_BA3
CM015	CS*	CM031	CS*

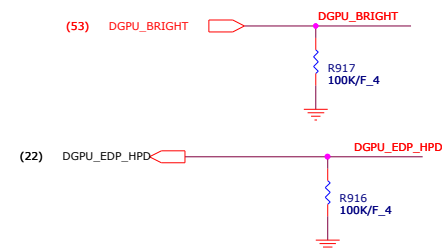
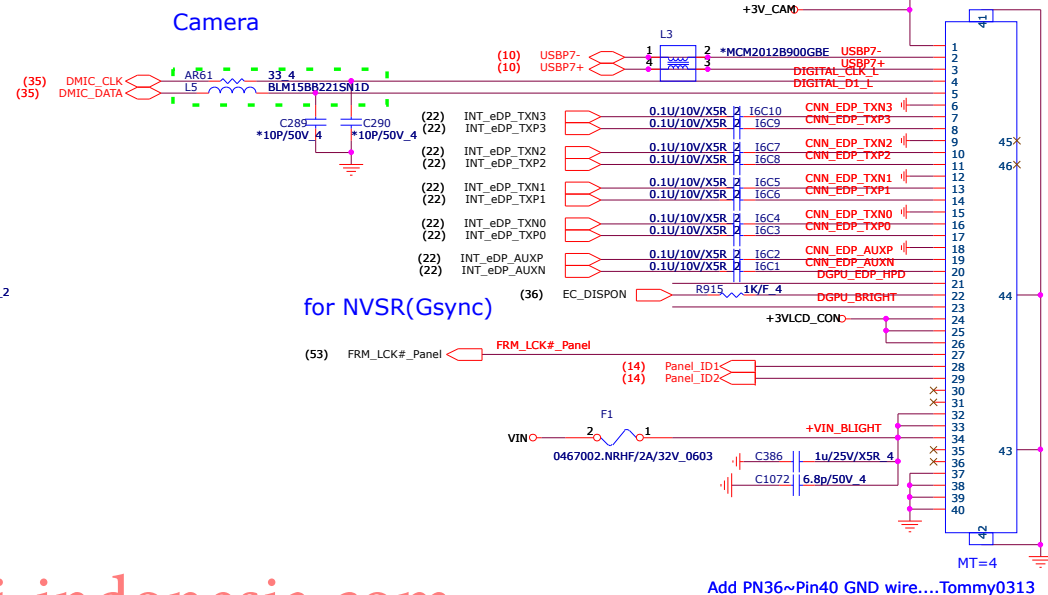
G83-256 Channel 0 & 1

CM032	Hot used
CM033	Hot used
CM034	DEBUG*
CM035	DEBUG*

Notes:
1. GPU debug pins not connected to DRAM. See section 7.1.13.



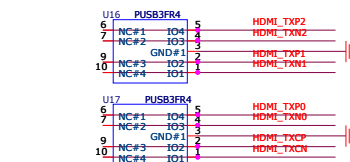
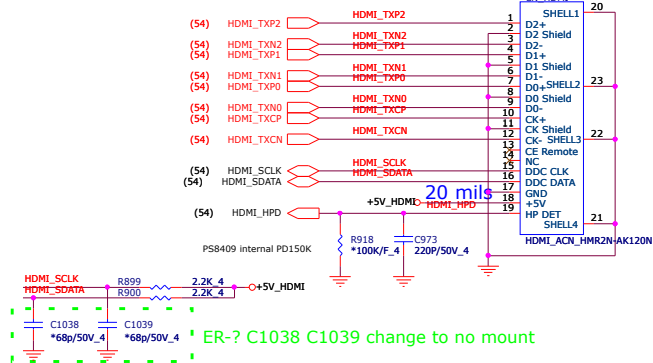
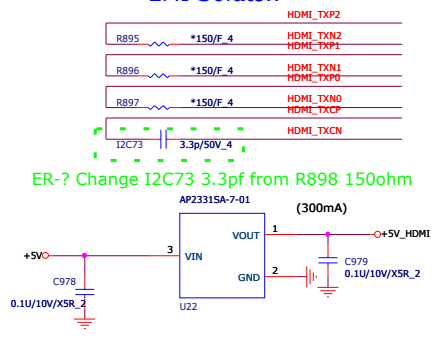
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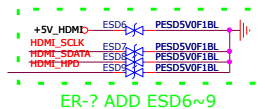
Add PN36~Pin40 GND wire....Tommy0313

HDMI

EMI Solution



For ESD Layout note: Place close to HDMI Conn



Mini-DP

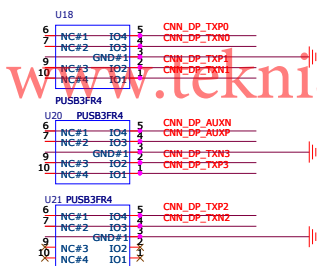
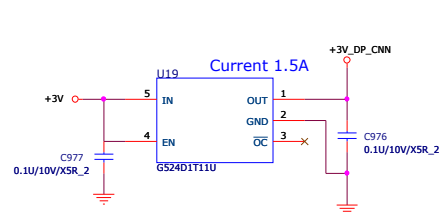
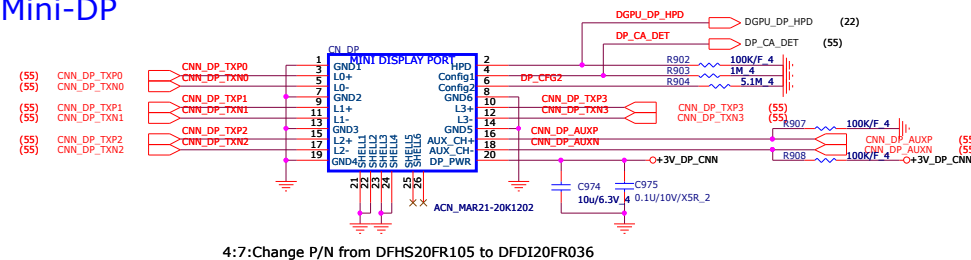
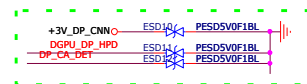
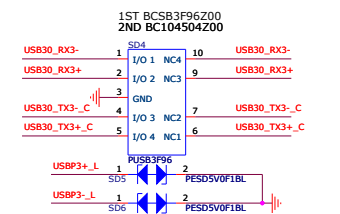
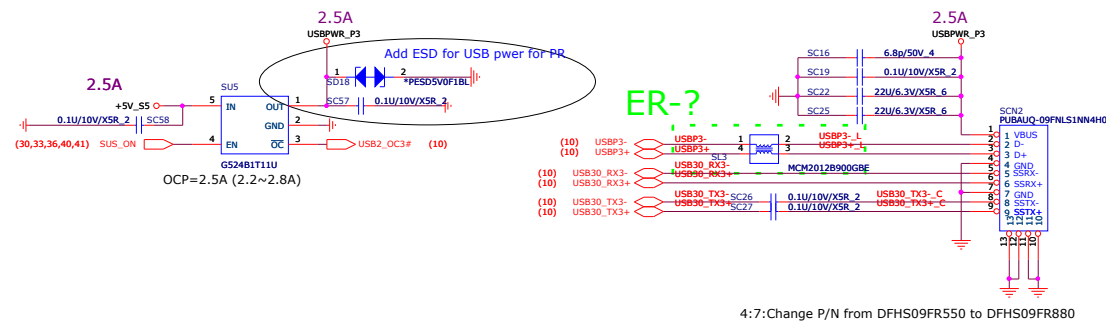
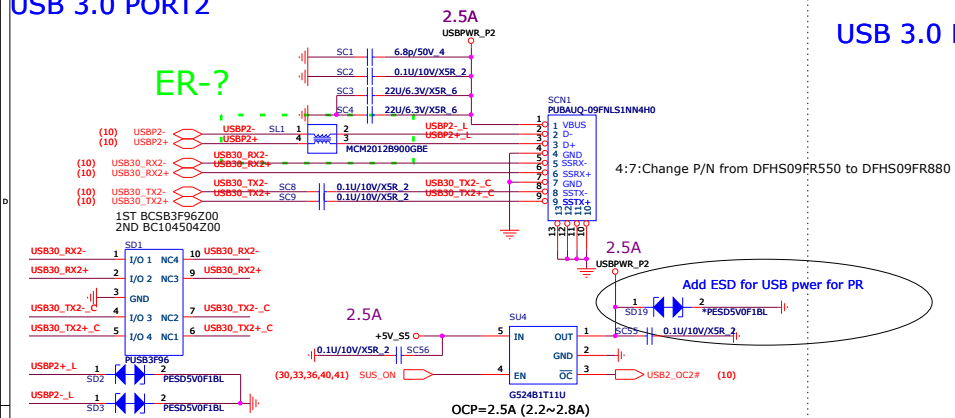


Table 2-1: Source-Side Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR



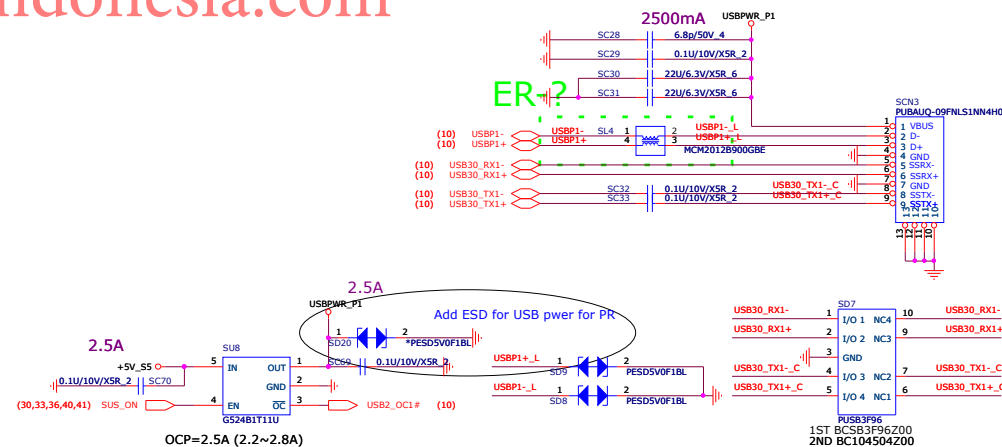
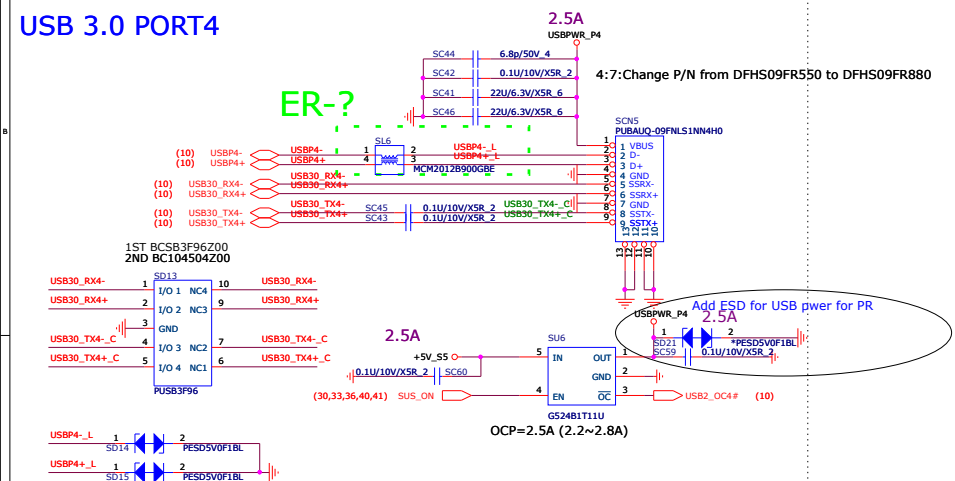
USB 3.0 PORT2



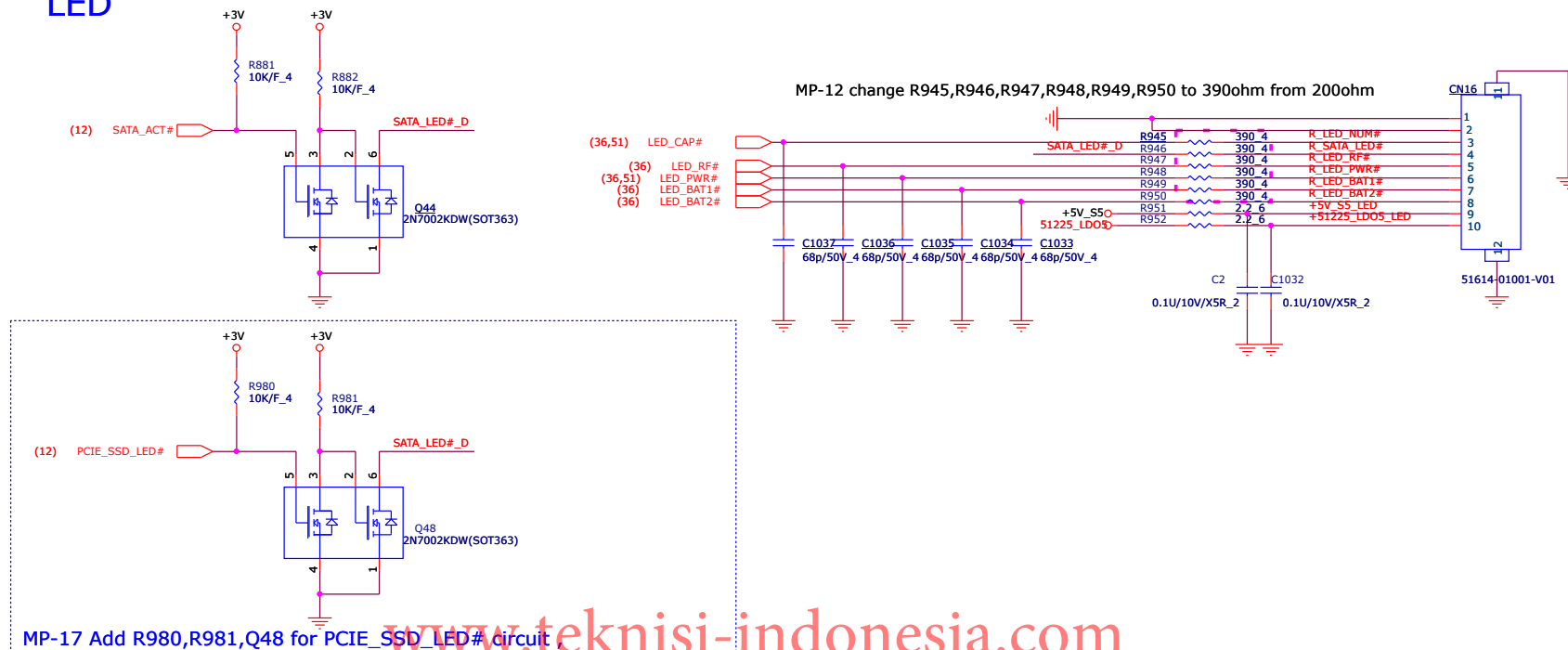
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USB 3.0 PORT1

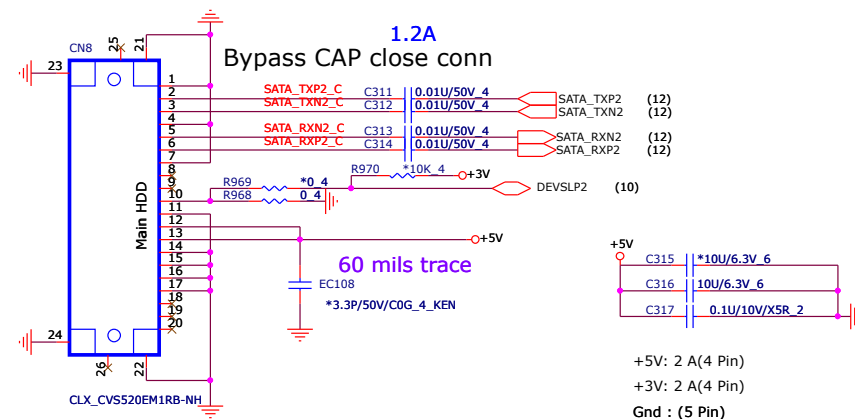
USB 3.0 PORT4



LED

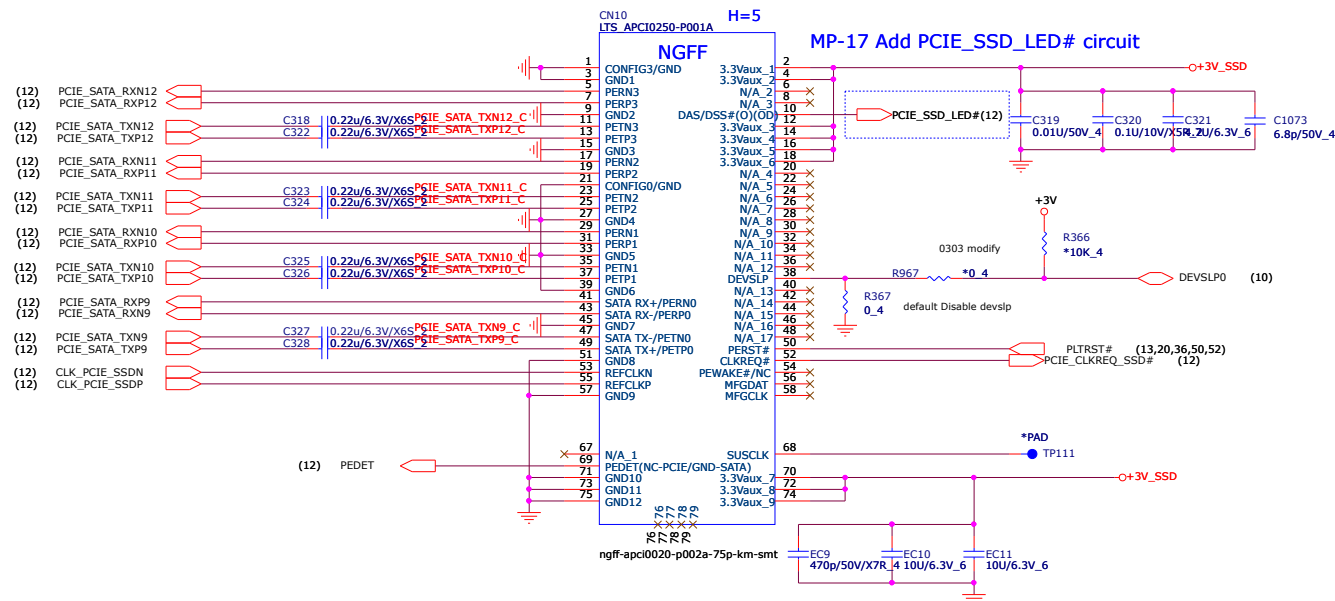


SATA HDD Connector(Cable type)



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SSD



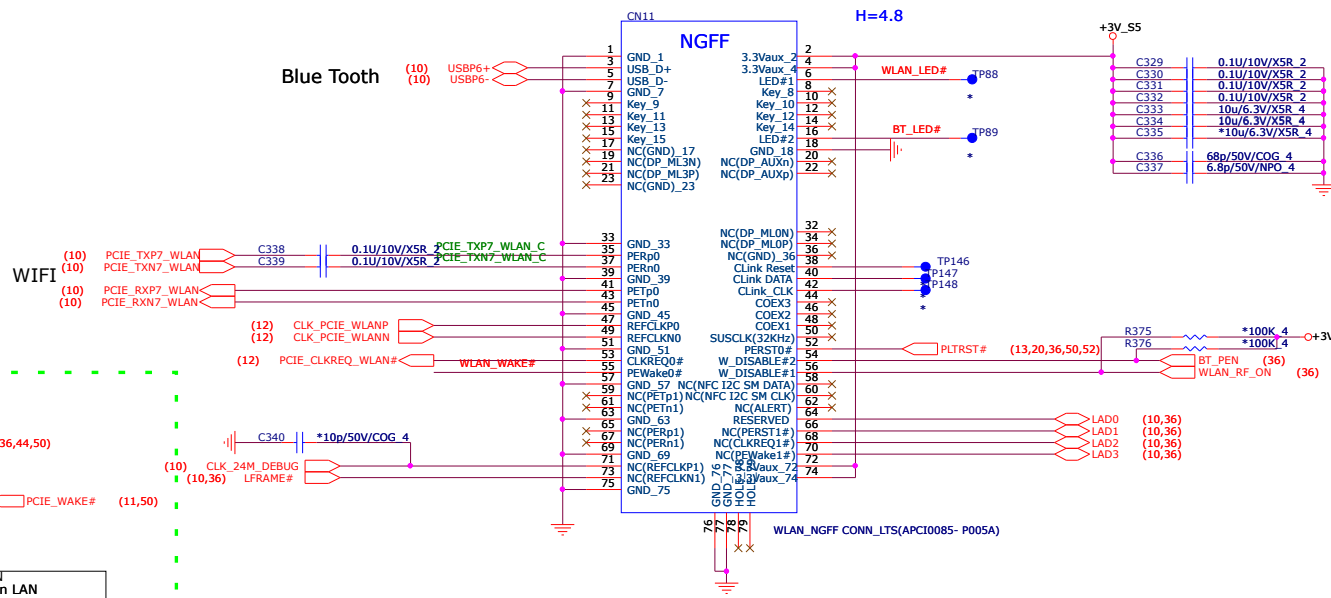
WLAN/BT

4.7: Change P/N from DFHS75FR300 TO DFHS75FR435
NGFF Wifi/BT (Type E)

NGFF Wifi/BT (Type E)

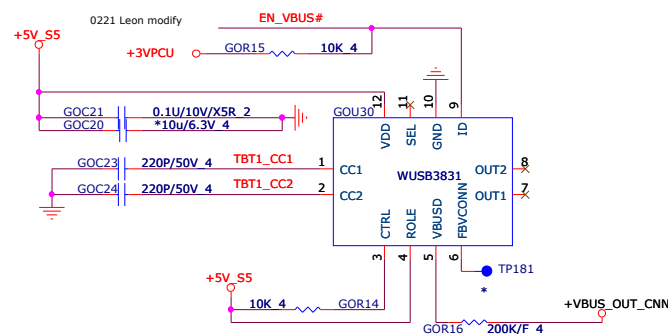
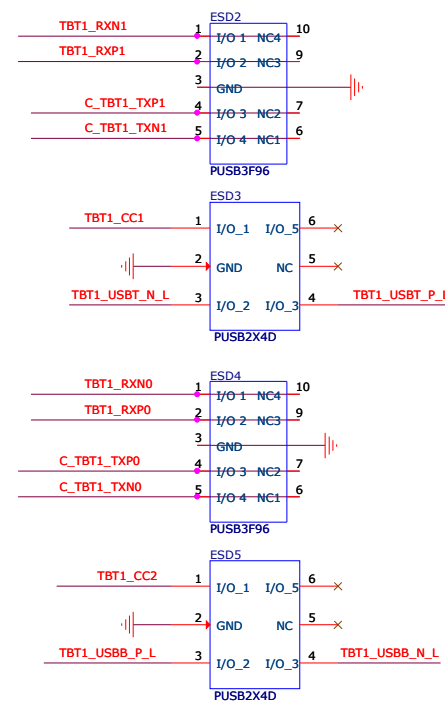
DRE(12-0004-01) RDC STD
DFHS75FR026

+3.3V_ NGFF_WLAN
Max Current : 1000mA

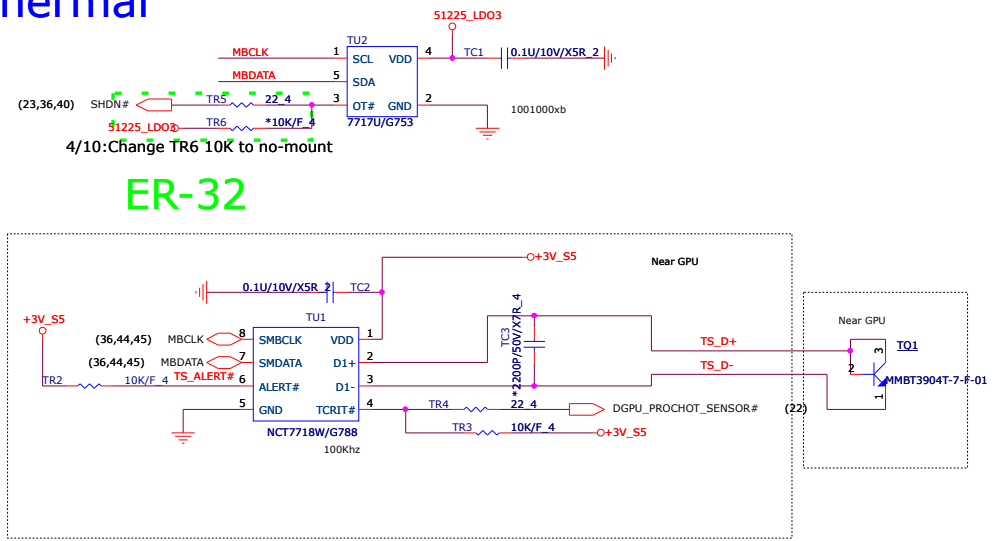


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Size	Document Number SSD/WLAN	Rev 1A
Date:	Tuesday, July 25, 2017	Sheet 32 of 57

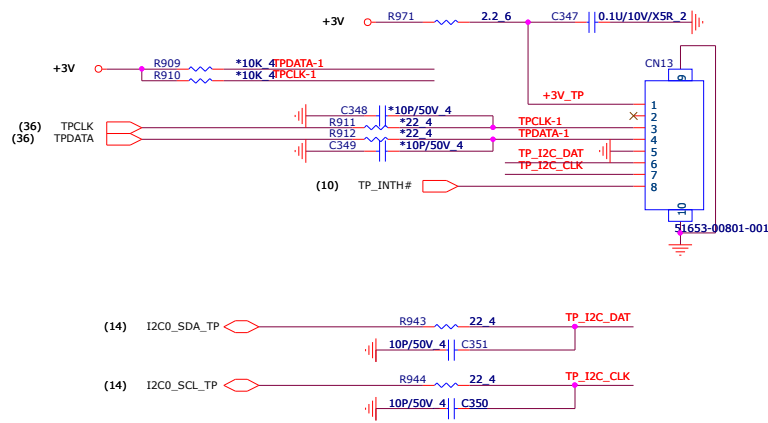


Thermal



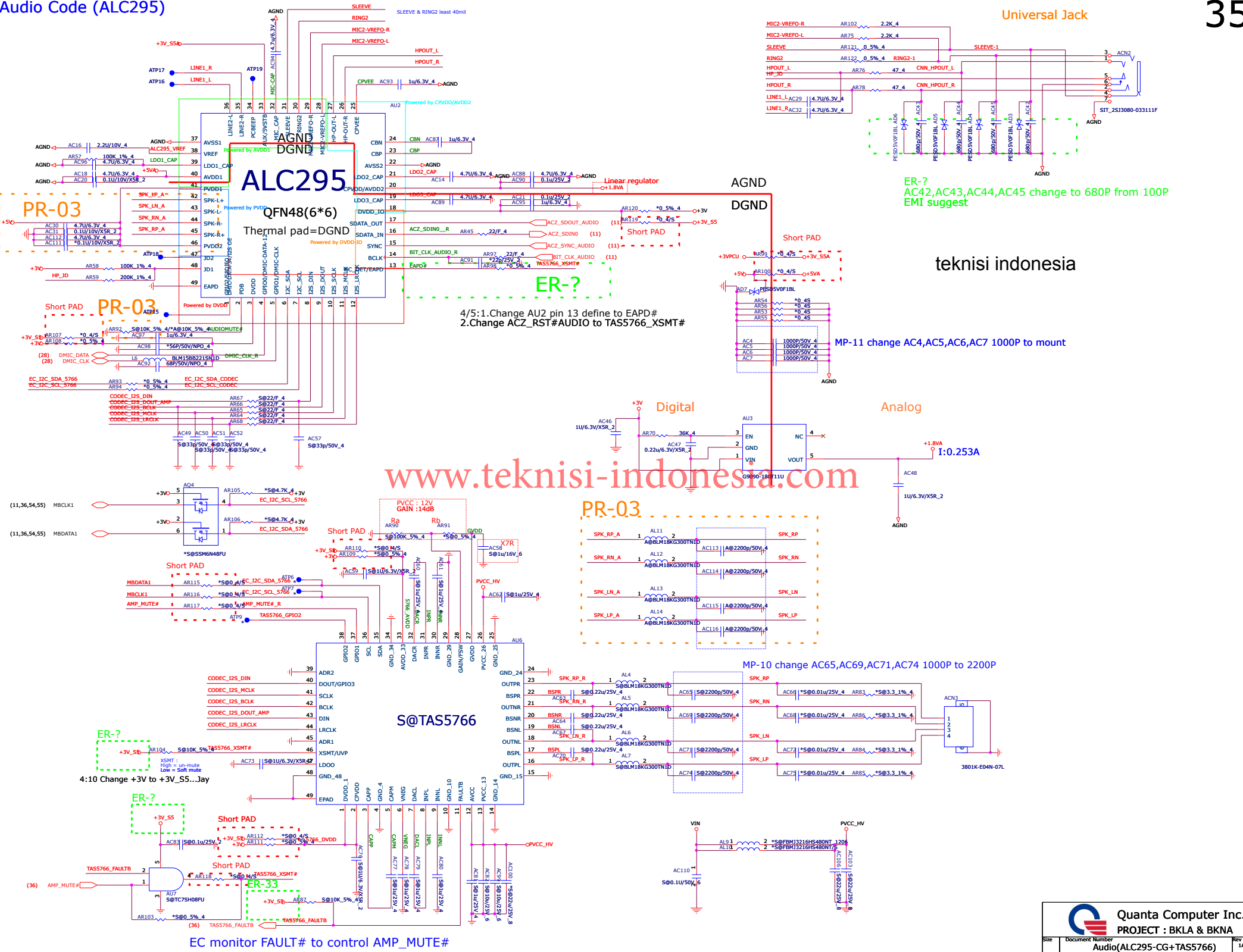
ER-32

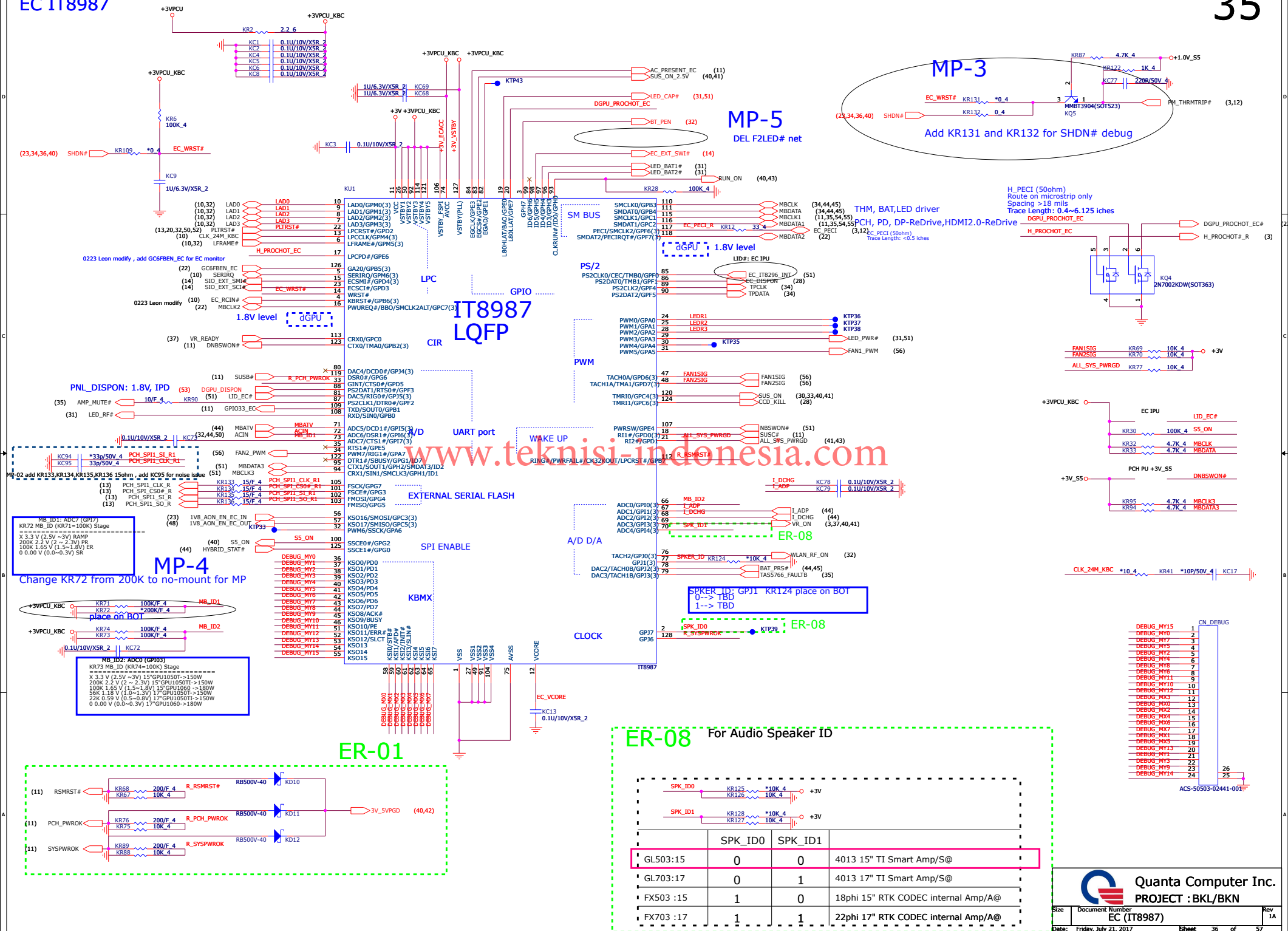
Touch Pad Connector AA type

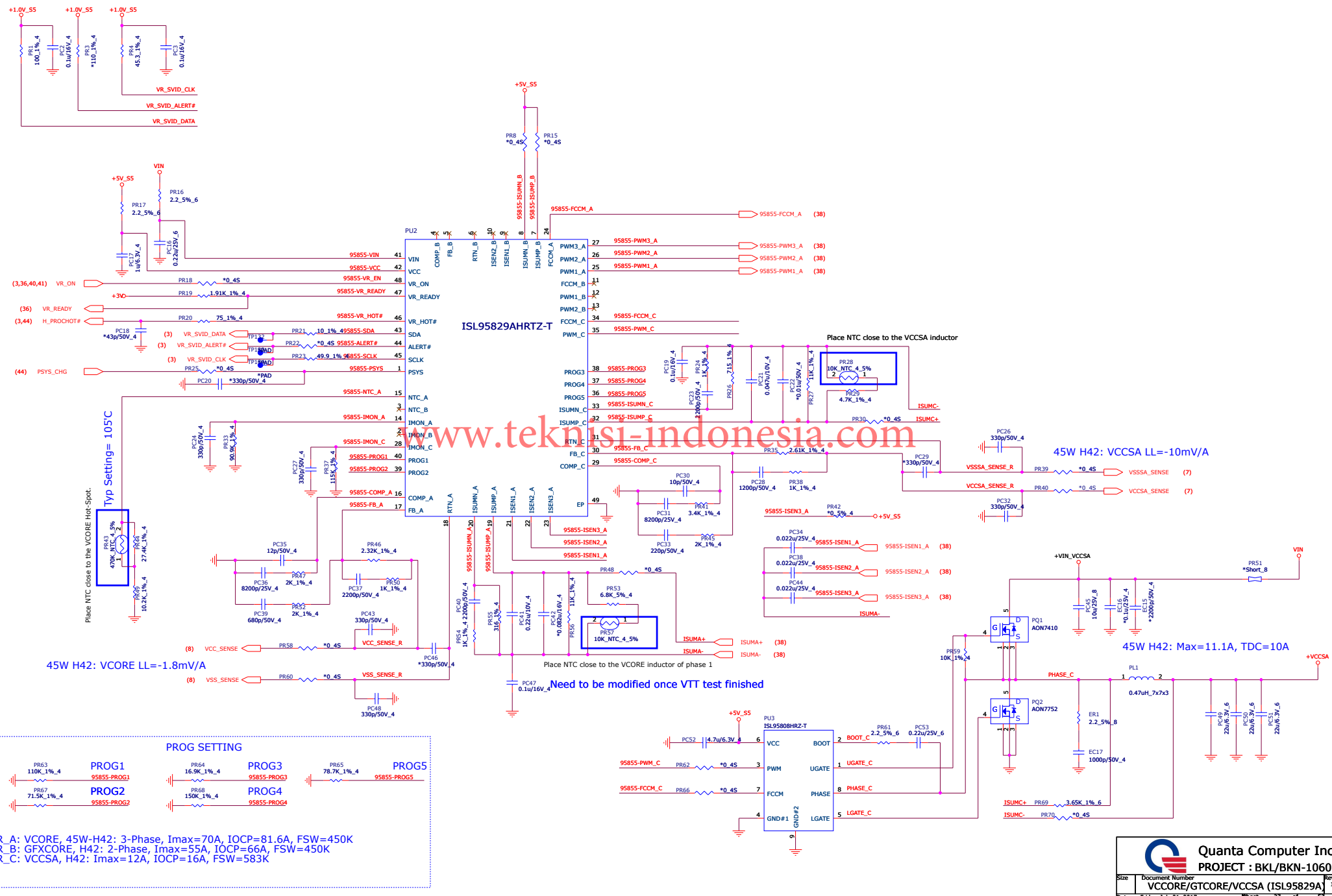


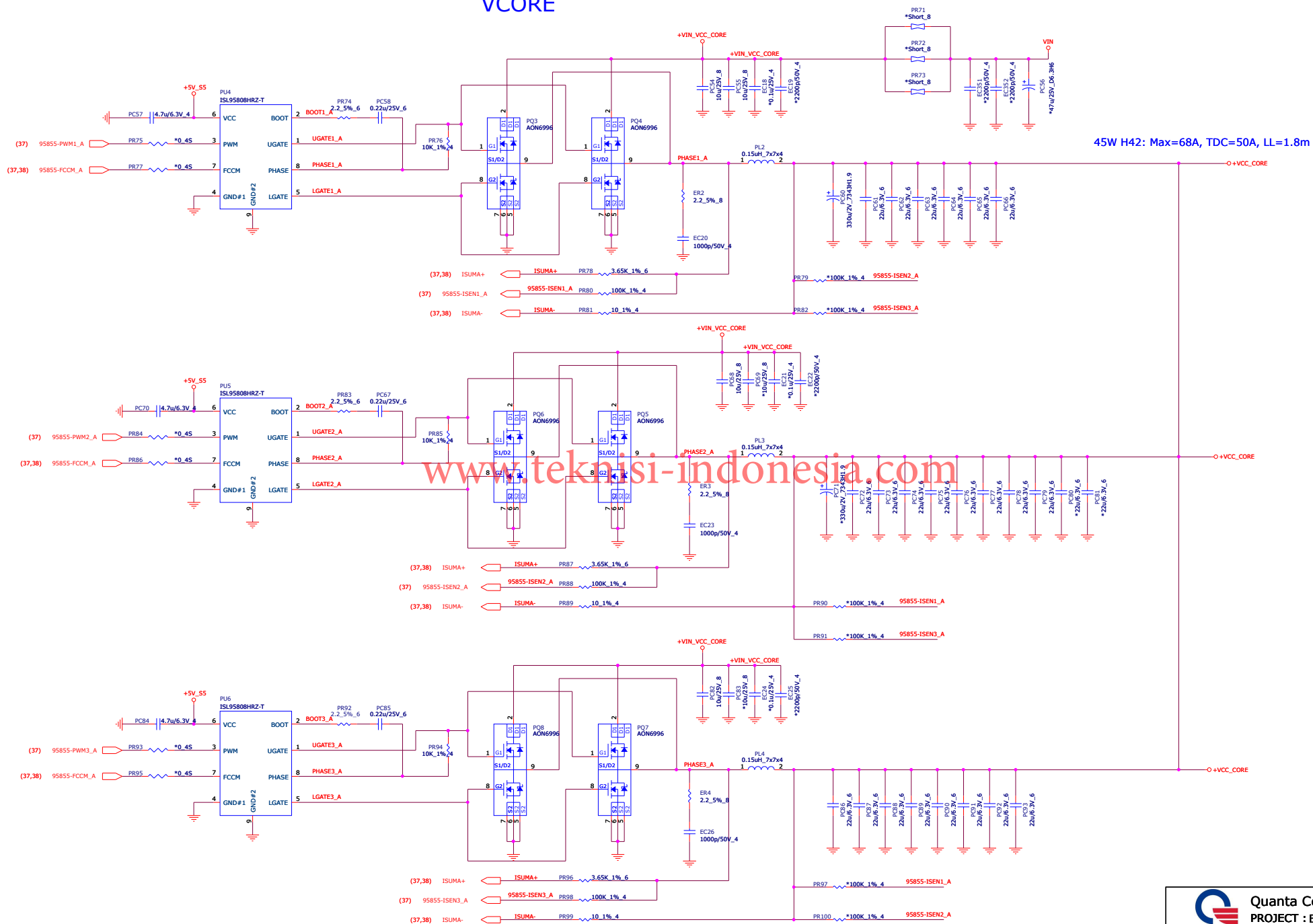
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Audio Code (ALC295)







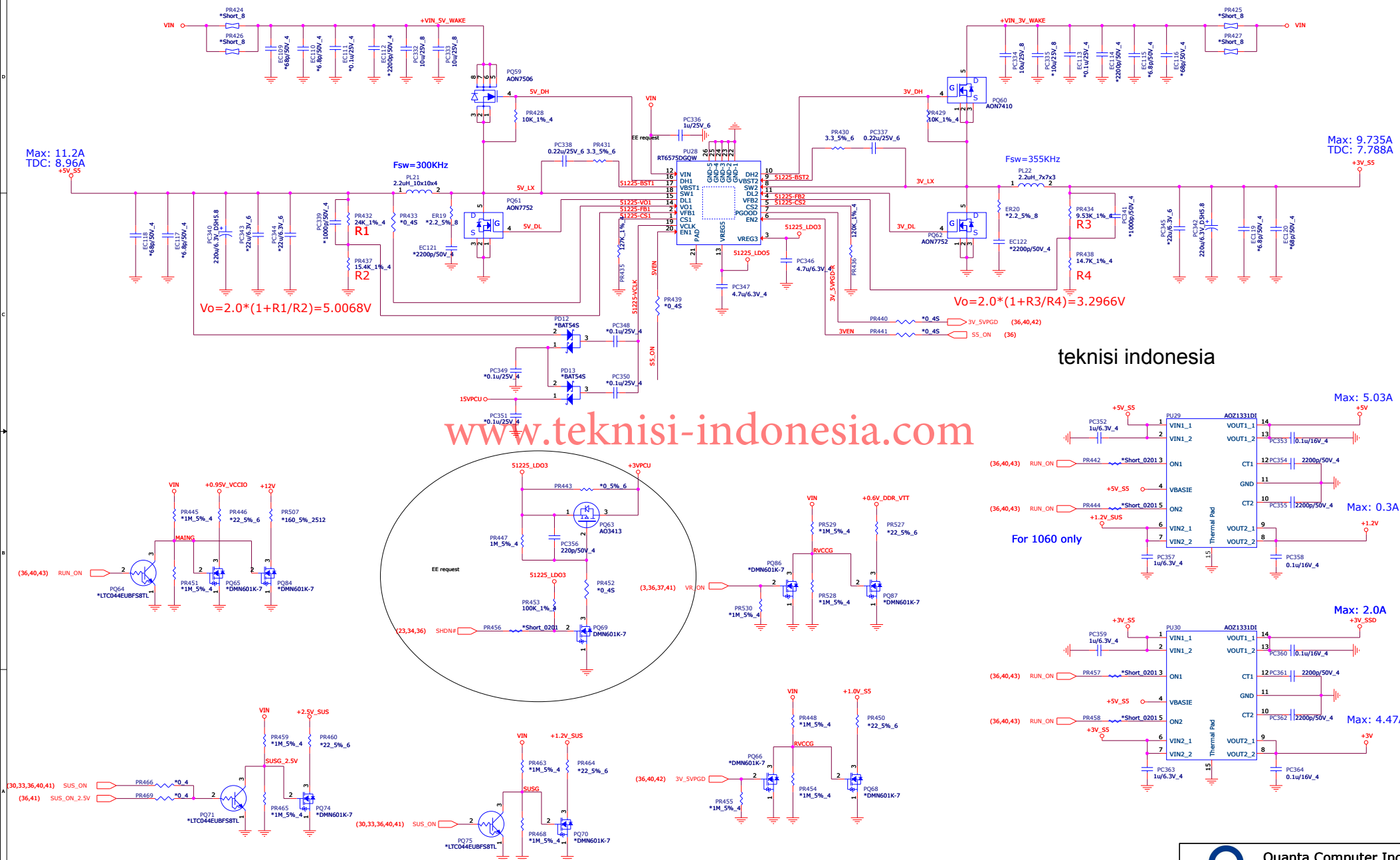


Support G-Sync

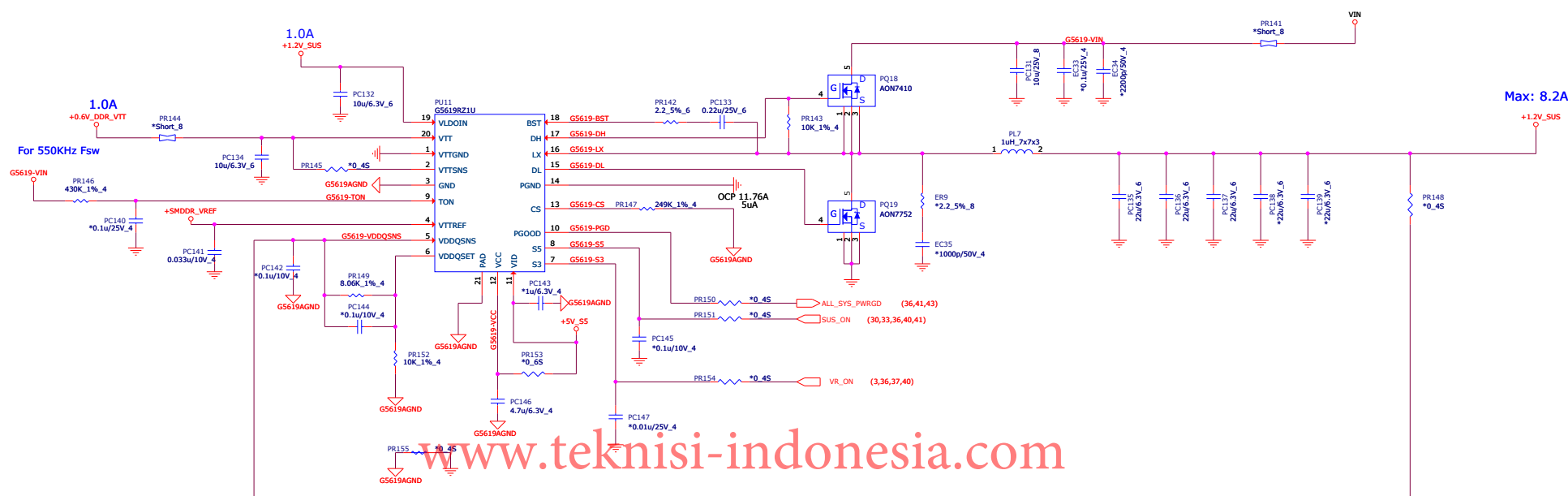
GT_VCORE : NI

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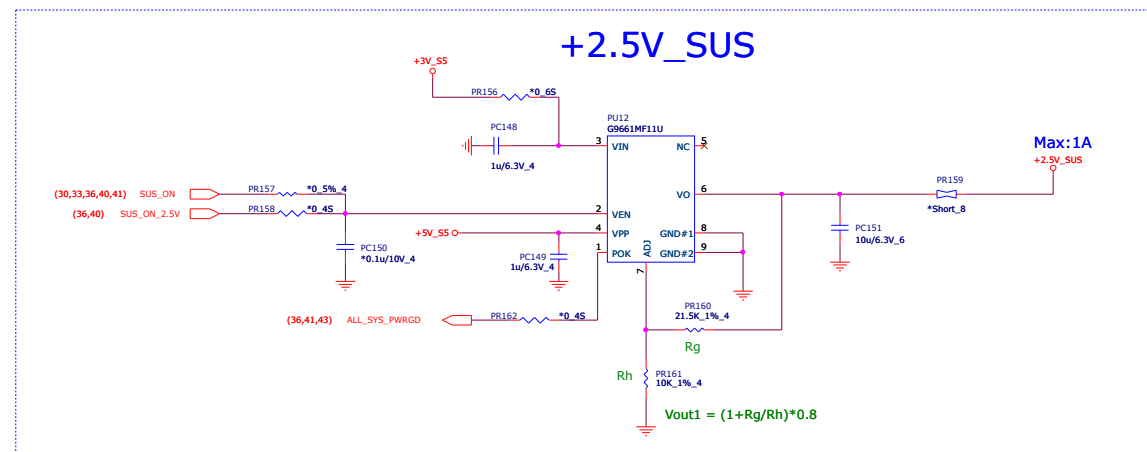
3.3V & 5V



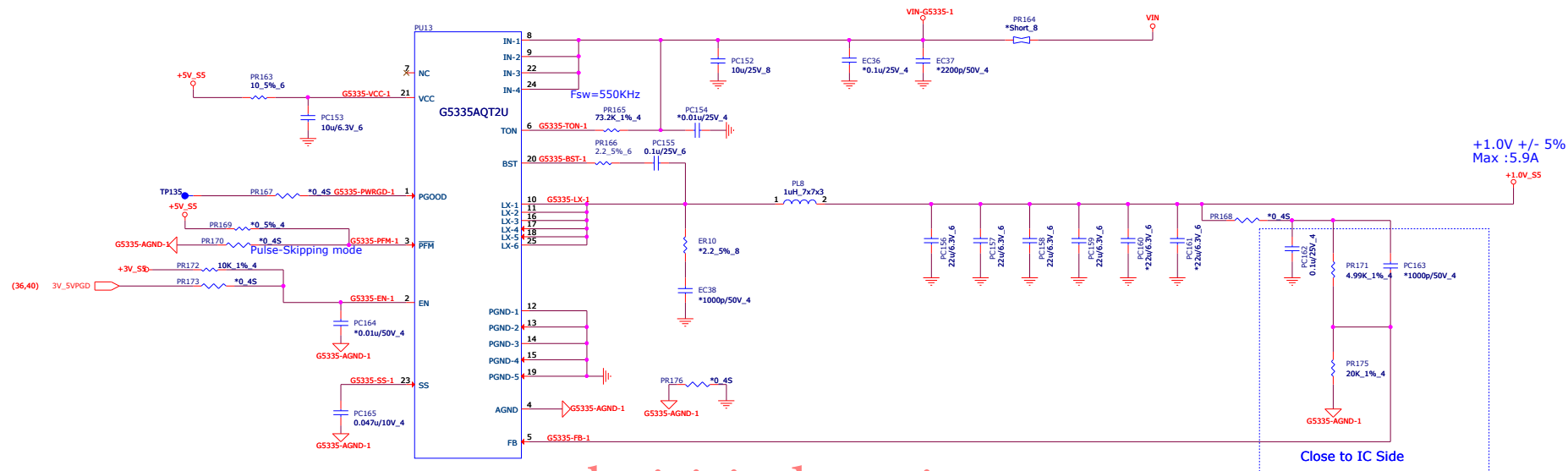
1.2VSUS & VTT_MEM



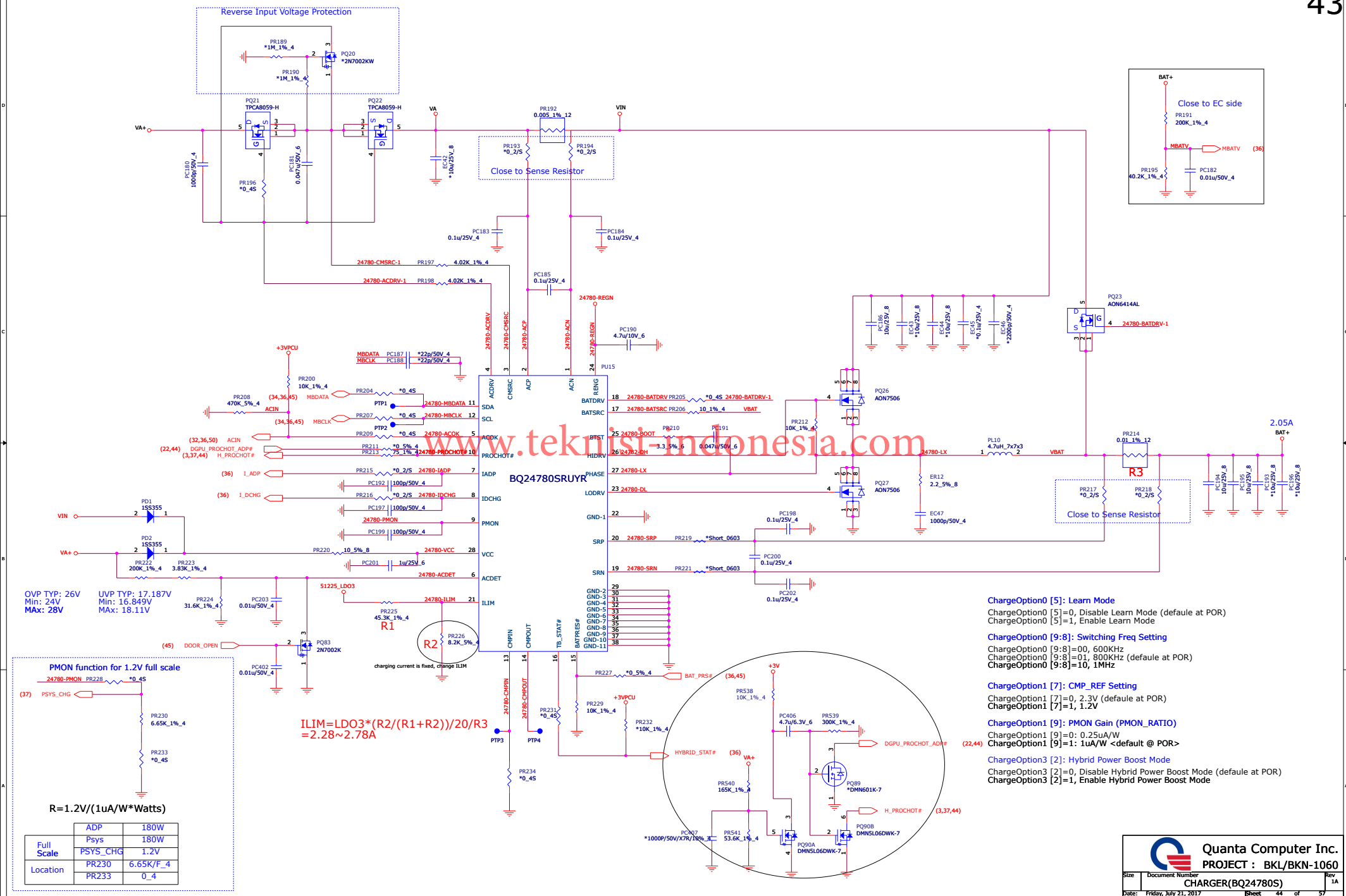
STATE	S3	S5	1.35VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



+1.0V_S5



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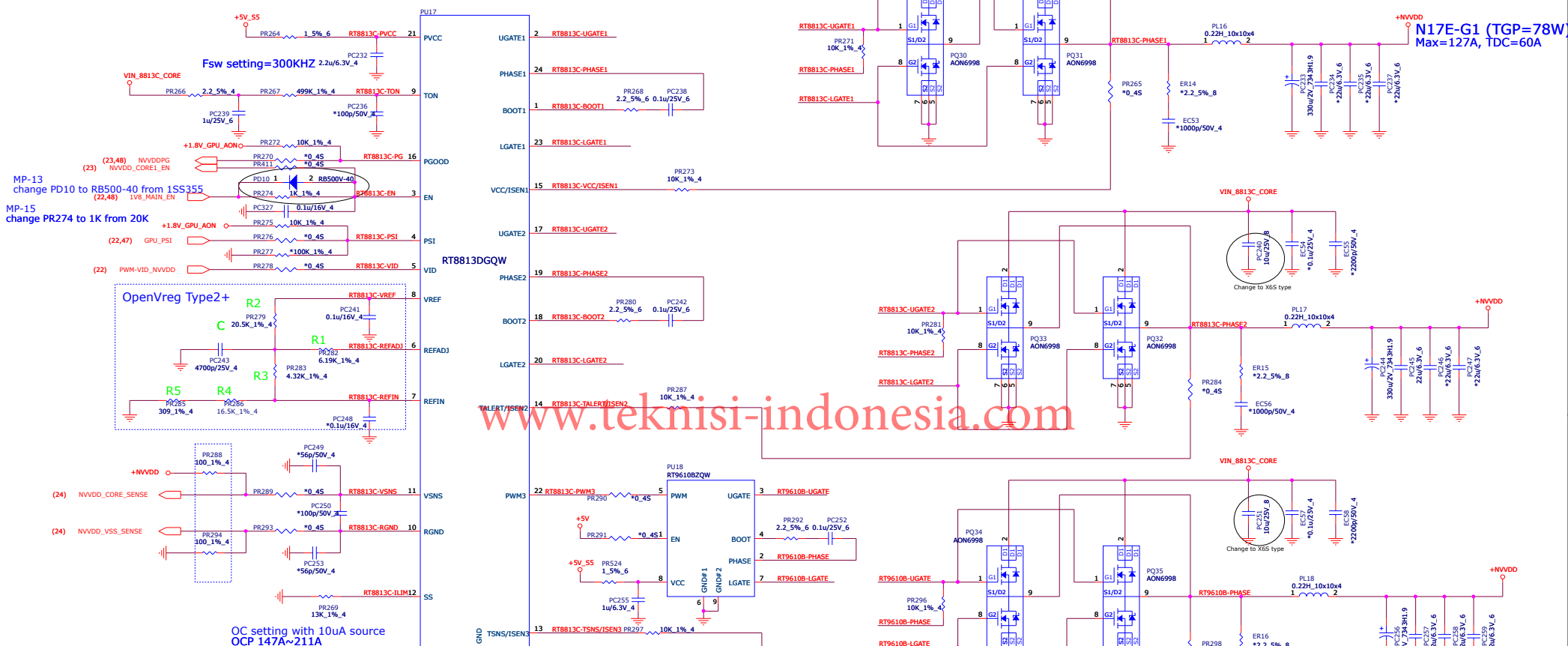




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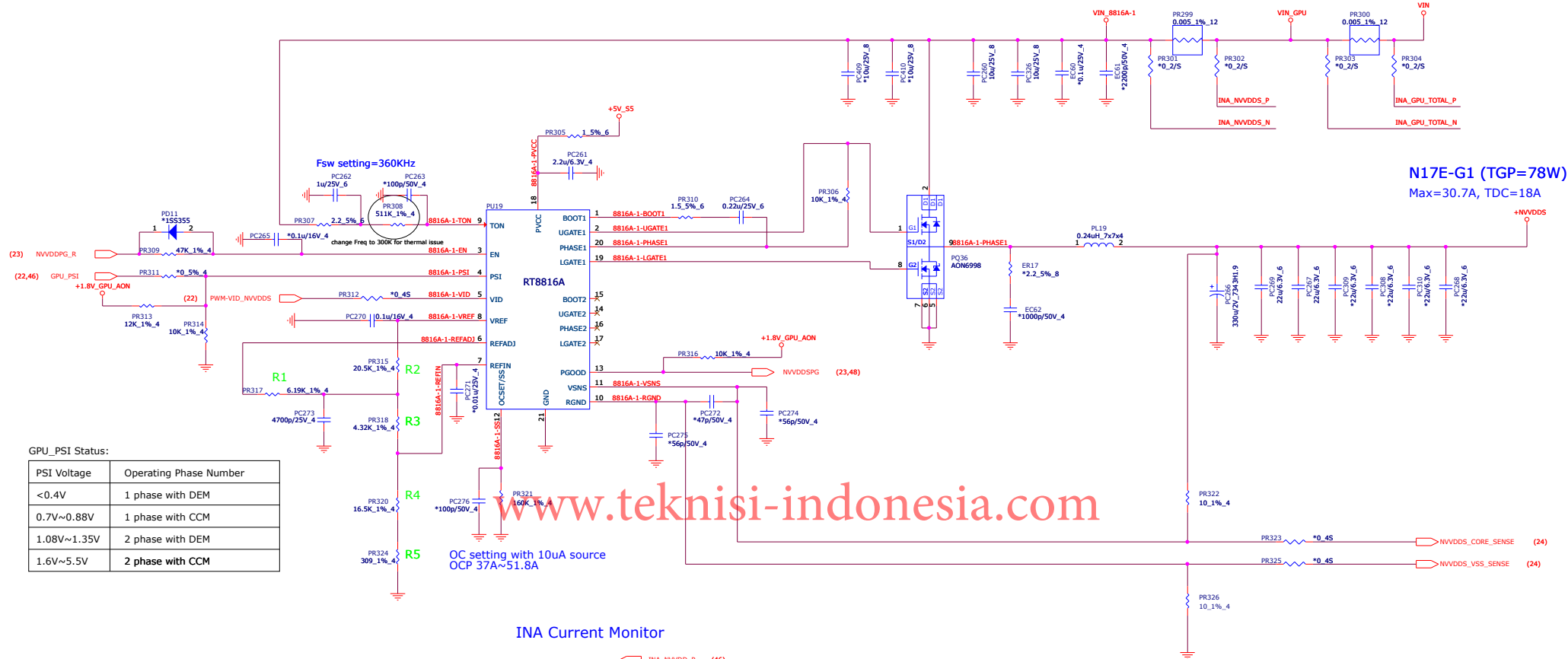
+NVVDD



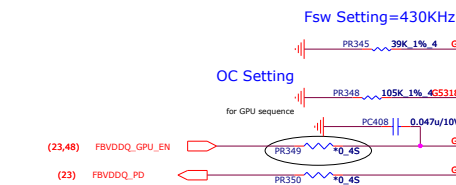
GPU_PSI Status:

PSI Voltage	Operating Phase Number
0V~0.4V	1 phase with DEM
0.8V~1V	1 phase with CCM
1.4V~5.5V	Active phase with CCM (Only for 2 or 3 phases)

+NVVDDS



FBVDDQ - 1.5V_GPU



FBVDDQ Voltage Setting: 1.55V / 1.35V

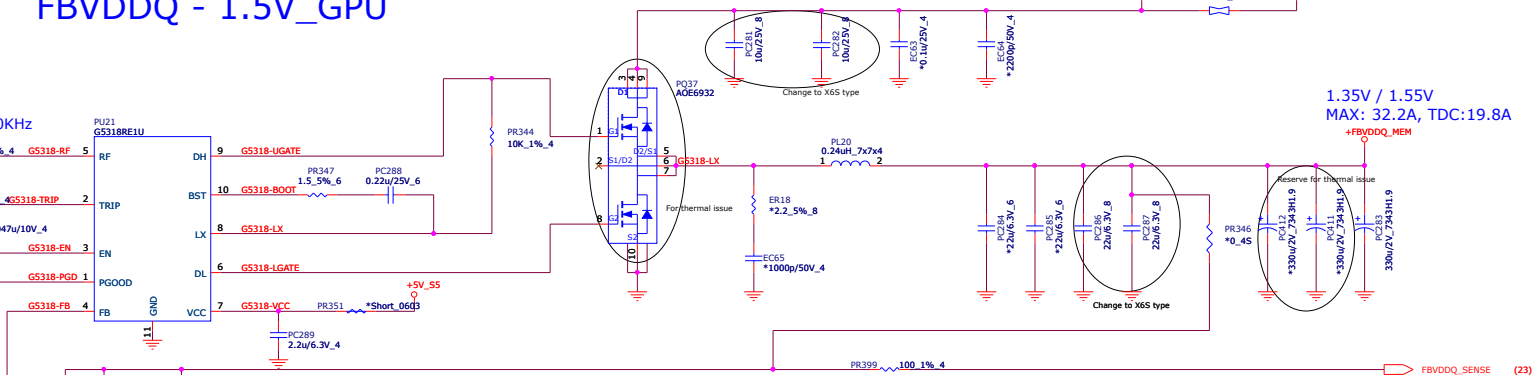
FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	11.8K	3.57K	1.55V
0	11.8K	3.57K	1.35V

Fine tune output voltage

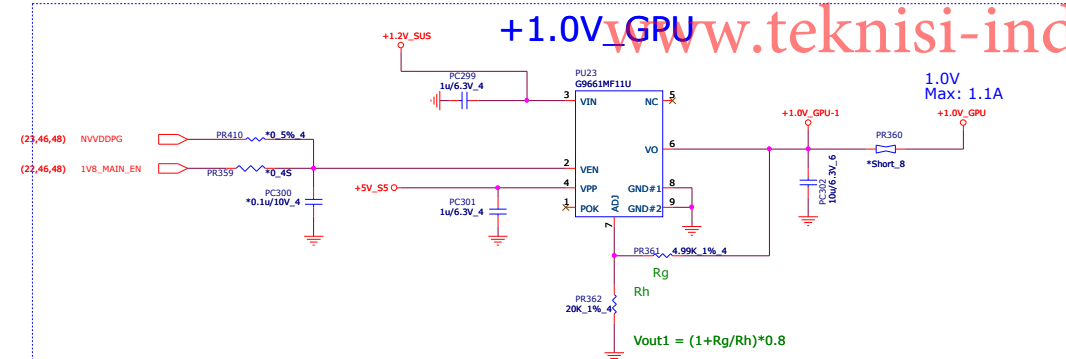
FBVDDQ Voltage Setting: 1.50V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12.4K	2.94K	1.50V
0	12.4K	2.94K	1.35V

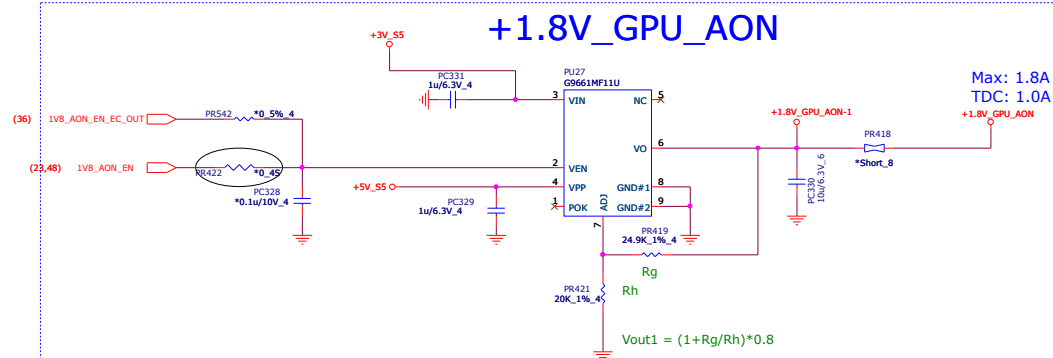
Fine tune output voltage



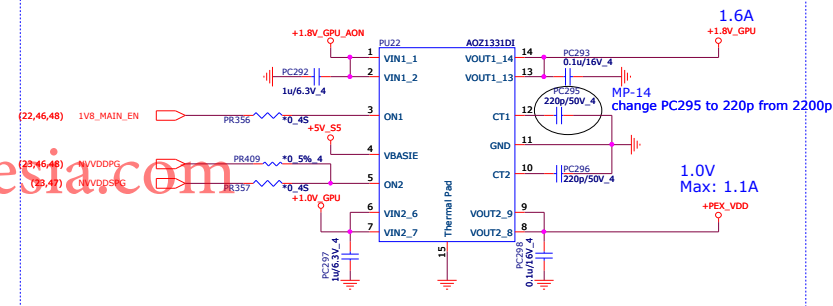
+1.0V GPU



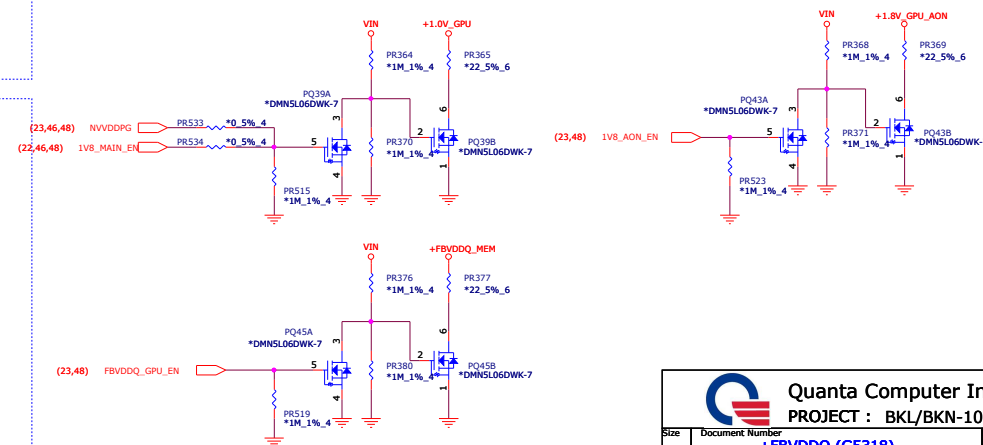
+1.8V GPU AON



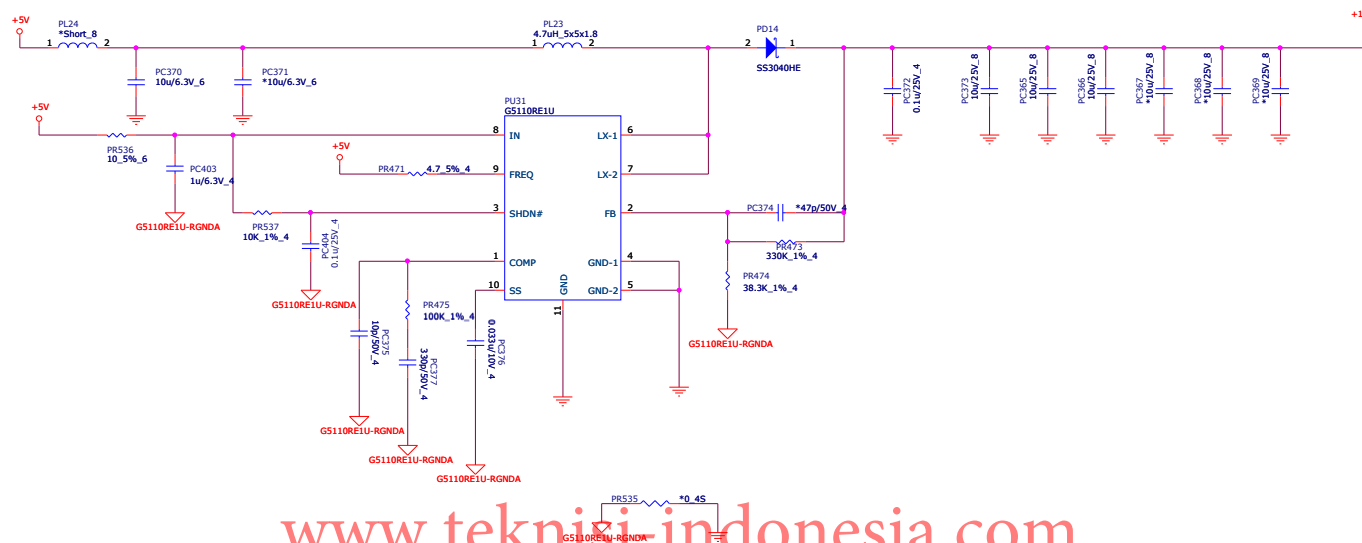
Load Switch for GPU



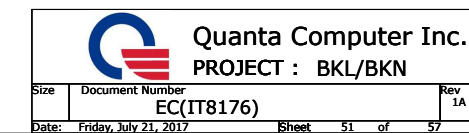
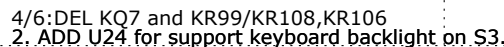
Discharge

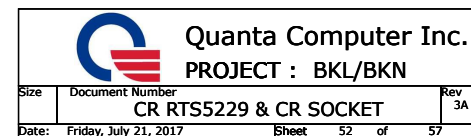


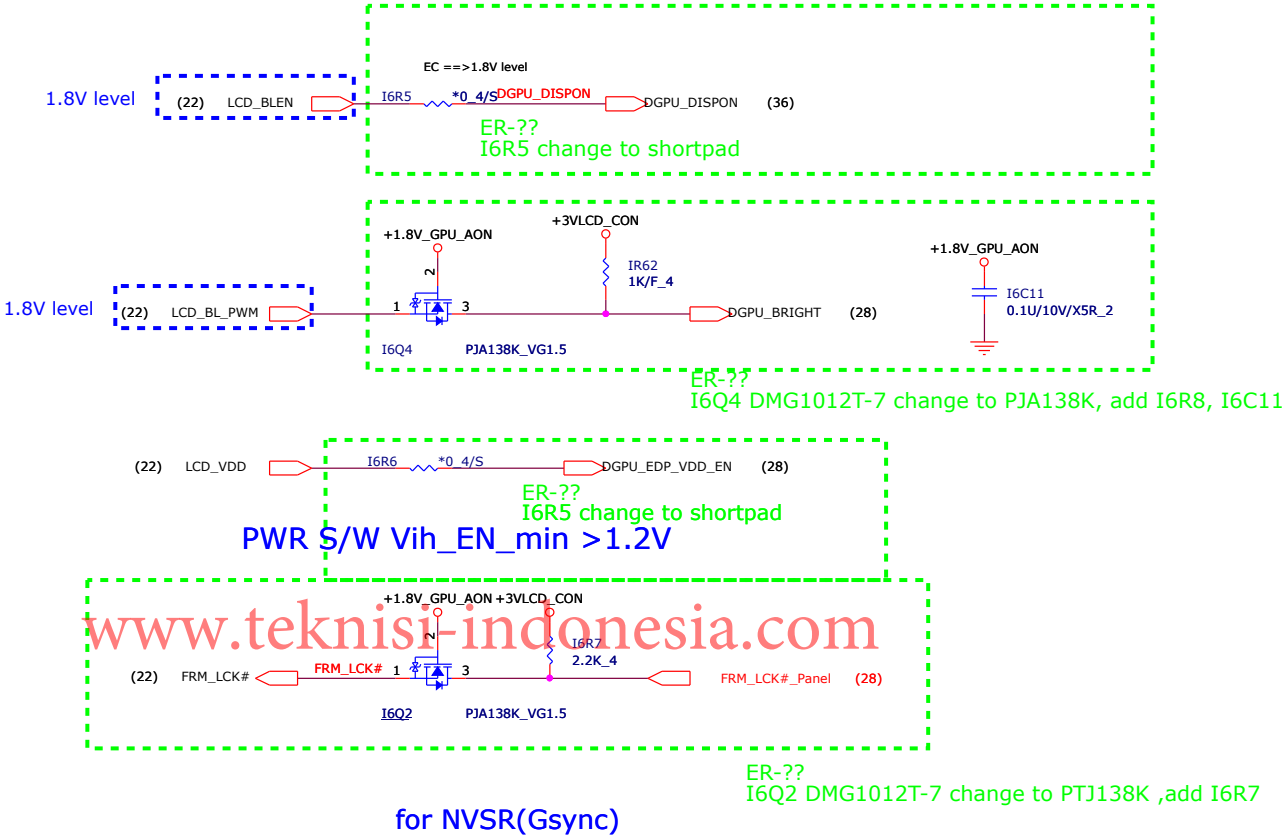
+12V for FAN



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HDMI 2.0 Re-Drive

53

From DGPU

ER-?
GAR77, GAR78 change to short pad

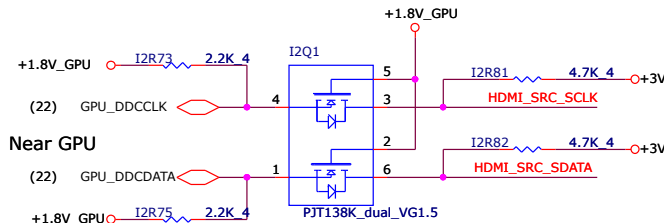
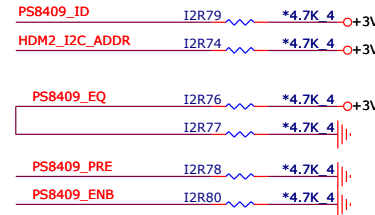
ER-??
add I2C74 for EMI

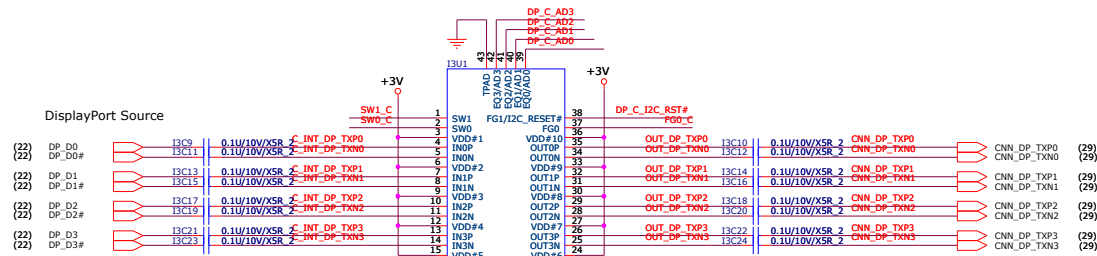
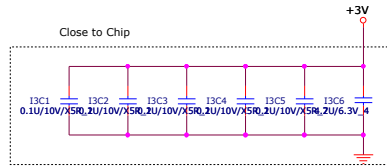
MAX <2"

ER-?
change to 2.2ohm from 10ohm

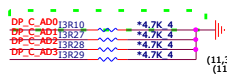
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I2C address : 0x10-0x2F





Input Equalization Selection for Main Link



EQ3	EQ2	EQ1	EQ0	8 Gbps Input EQ(dB)
0	0	0	0	3.3
0	0	0	1	3.8
0	0	1	0	4.3
0	0	1	1	4.8
0	1	0	0	5.4
0	1	0	1	5.8
0	1	1	0	6.3
0	1	1	1	6.8
1	0	0	0	7.2
1	0	0	1	7.7
1	0	1	0	8.1
1	0	1	1	8.5
1	1	0	0	8.9
1	1	0	1	9.2
1	1	1	0	9.6
1	1	1	1	9.9

ER-?
ADD GAR79 for Pin control mode
I3R30 change to no mount
GAR77, GAR78 change to no mount
I3R10 change to no mount for EQ 9.9dB

I2C enable pin.
1 : register access I2C slave mode
Middle/Float : read external EEPROM Master mode
0 : Pin-Strapping control mode

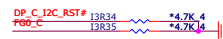
*Middle(M) is 50% of VDD

Output -1dB Compression Setting



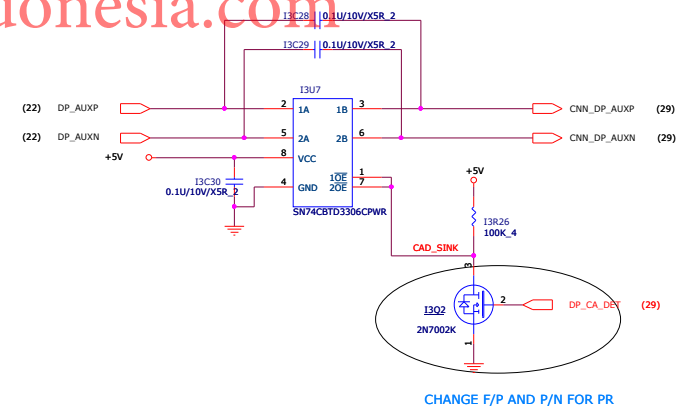
SW1	SW0	mVppd@8 Gbps
0	0	700
0	1	800
1	0	900
1	1	1000

Flat Gain Setting



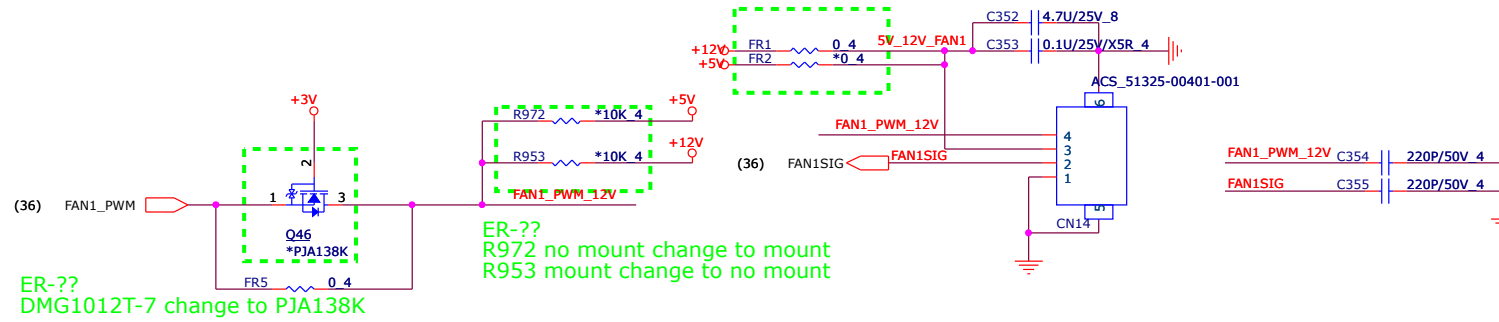
FG1	FG0	Gain
0	0	-4 dB
0	1	-2 dB
1	0	+0 dB
1	1	+2 dB

Dual-Mode DisplayPort (DP++) : DP / HDMI

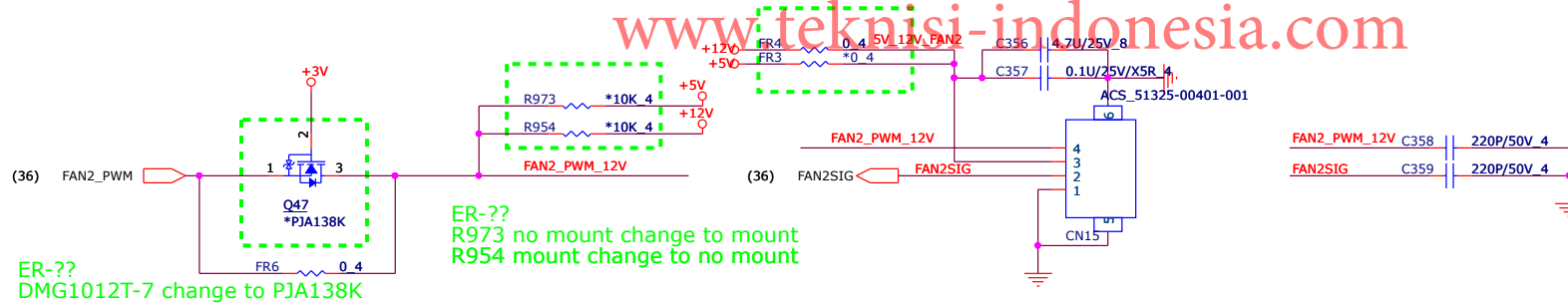


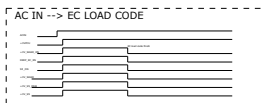
CHANGE F/P AND P/N FOR PR

FAN1 for Nvidia GPU

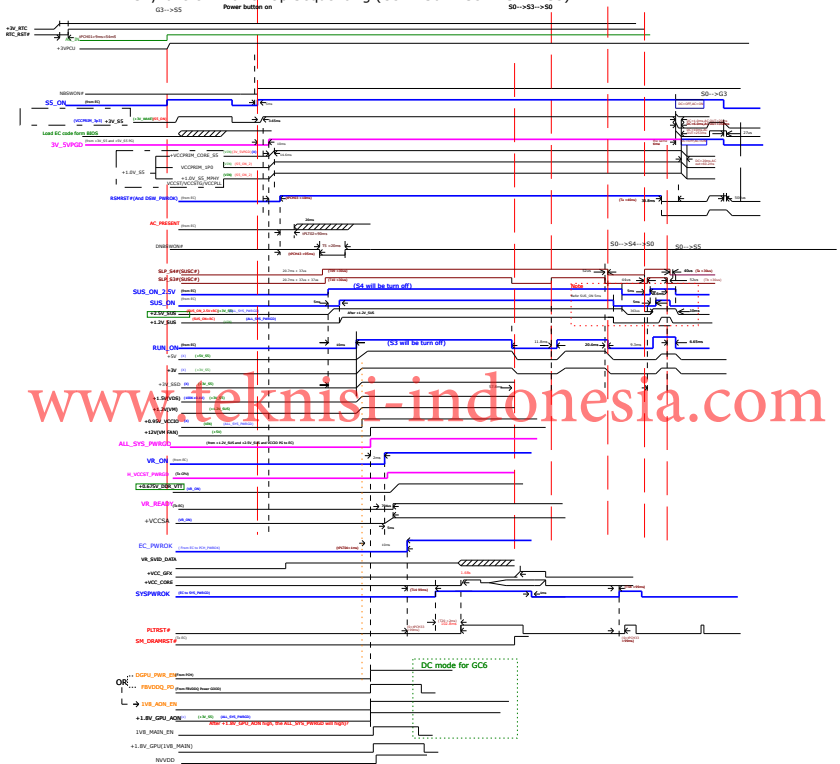


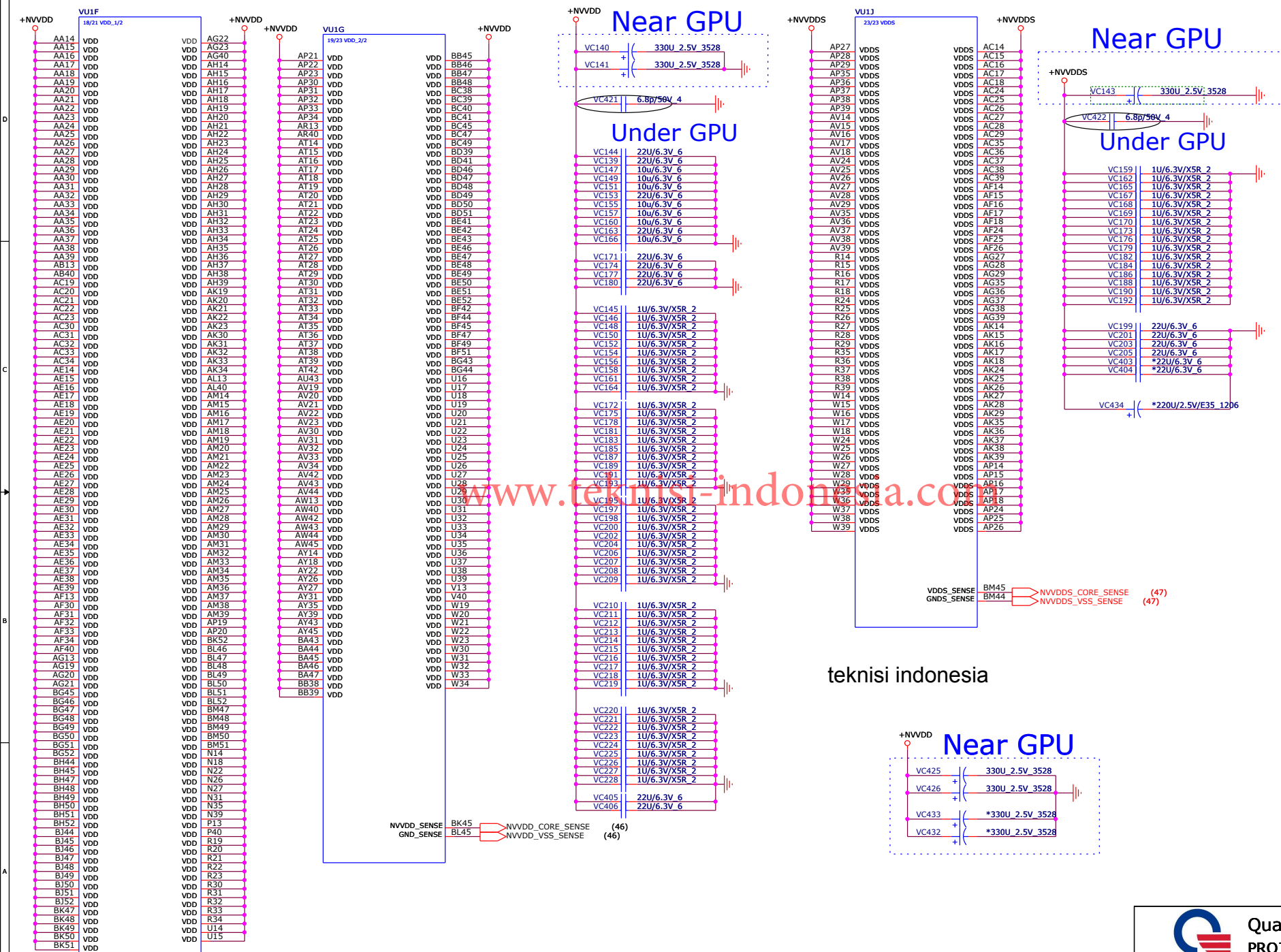
FAN2 for CPU





SkyLake ULT Power-Up Sequencing (G3-->S0-->S3-->S4-->S5)





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PROJECT : BKL/BKN

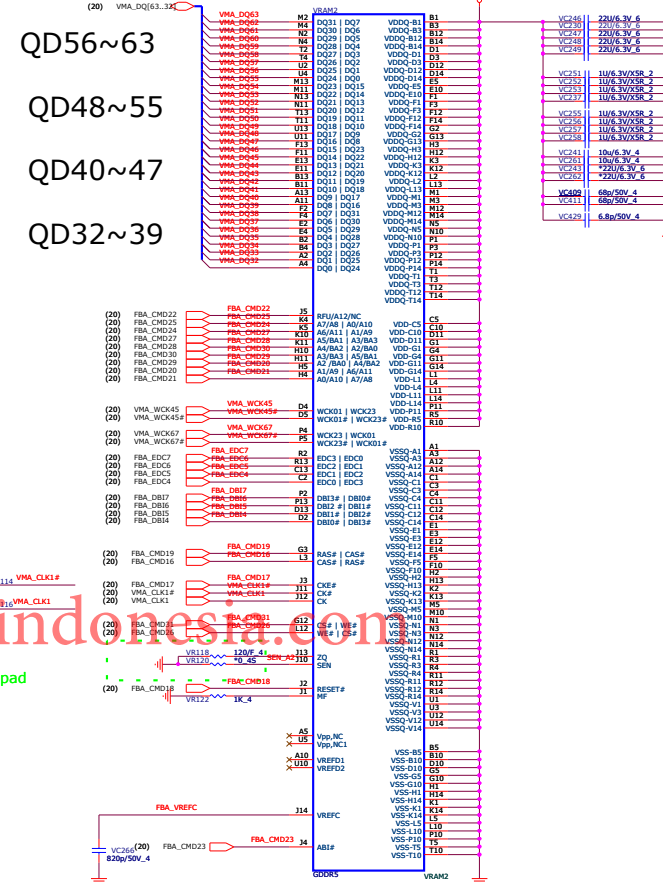
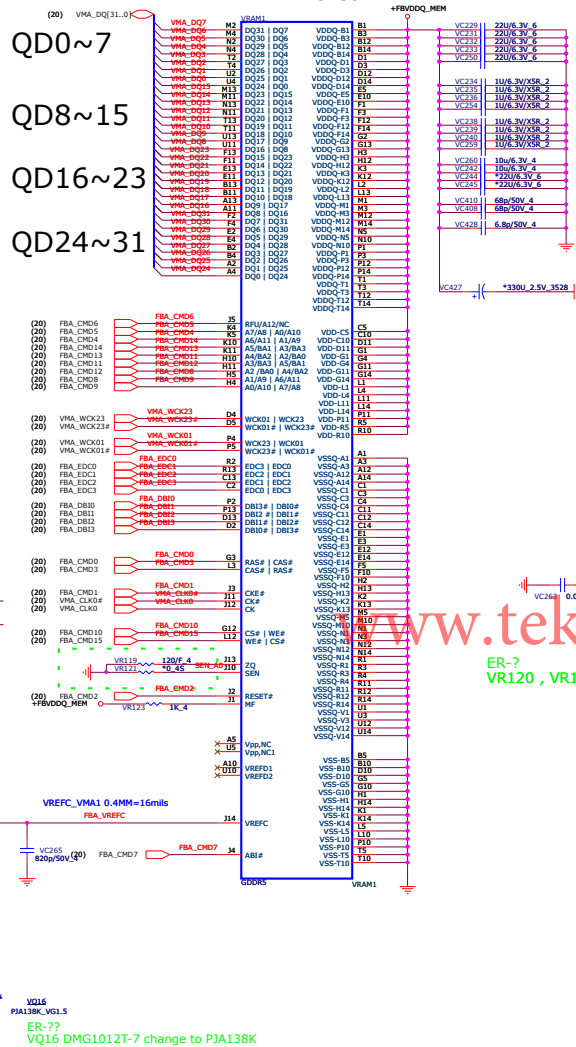


Table 7-5. GDDR5 Mode F Mapping

GB3-256 Channel 0_Q_31		GB3-256 Channel 1_Z_63	
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RS5*	CMD18	RS5*
CMD3	RA5*	CMD19	RA5*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	AB*	CMD23	AB*
CMD8	AB_A11	CMD24	AB_A11
CMD9	A7_AB	CMD25	A7_AB
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256 Channel 0 & 1			
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0		
CMD35	DEBUG1		

Notes:

1. GPU debug pins; not connected to DRAM. See section 7.1.13.

Notes:

1. GPU debug pins; not connected to DRAM. See section 7.1.13.

