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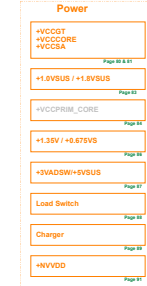
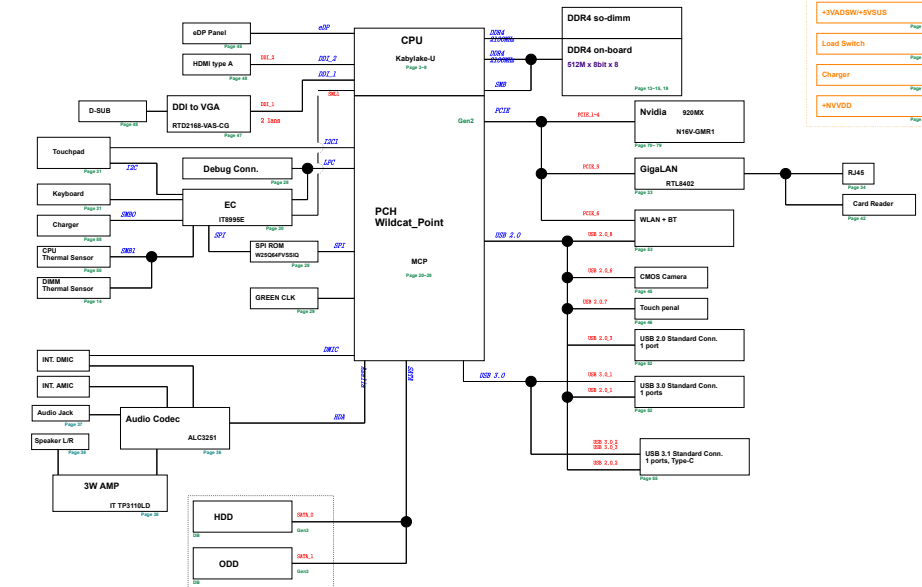
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075	VGA_VIDIA_H16V/S_ROM_XTAL
076	VGA_VIDIA_H16V/S_DPDI
077	VGA_VIDIA_H16V/S_POWER
080	PW_IMVPS (1)(RT3618CG0W)
081	PW_IMVPS (2)(RT3618CG0W)
083	PW_+1.0VBUS / +1.8VBUS
084	PW_+1.2VS
085	PW_1.35V/+0.675V (LP9011Q)
087	PW_+3VADSW/+5VUS (RT8249C)
088	PW_LOAD SWITCH
089	PW_CHARGER(BQ24780)
090	PW_PROTECTION
091	PW_DGPU_5PHASE(RT815A)

BLOCK DIAGRAM

X541UAK/UVK SCHEMATIC Revision 1.1

(UAK : UMA)
(UVK : DGPU = Nvidia N16V-GMR1, 920MX)

Non Connected Standby



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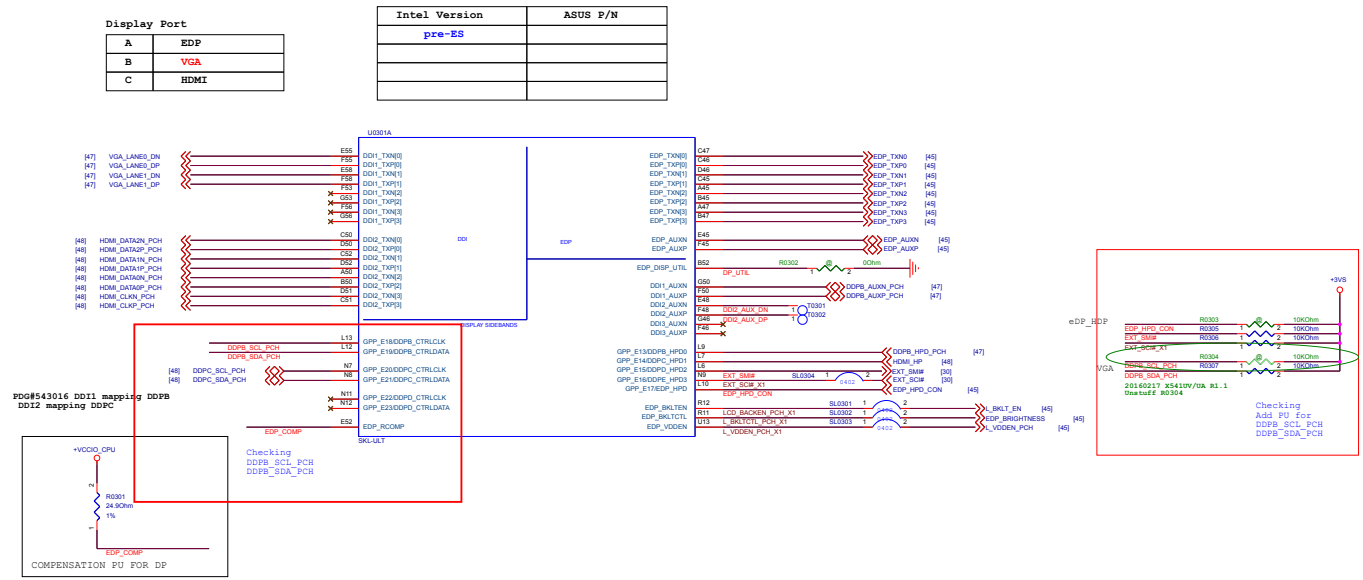
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ASUS Project Name		Rev
X540UV/UA		R1.0
Title : CPU_DISPLAY		
Size	Dept.: ASUS/TK COMPUTER INC.	Engineer: NB2_EEZ
Custom	Date: Thursday, September 01, 2016	Sheet 3 of 102

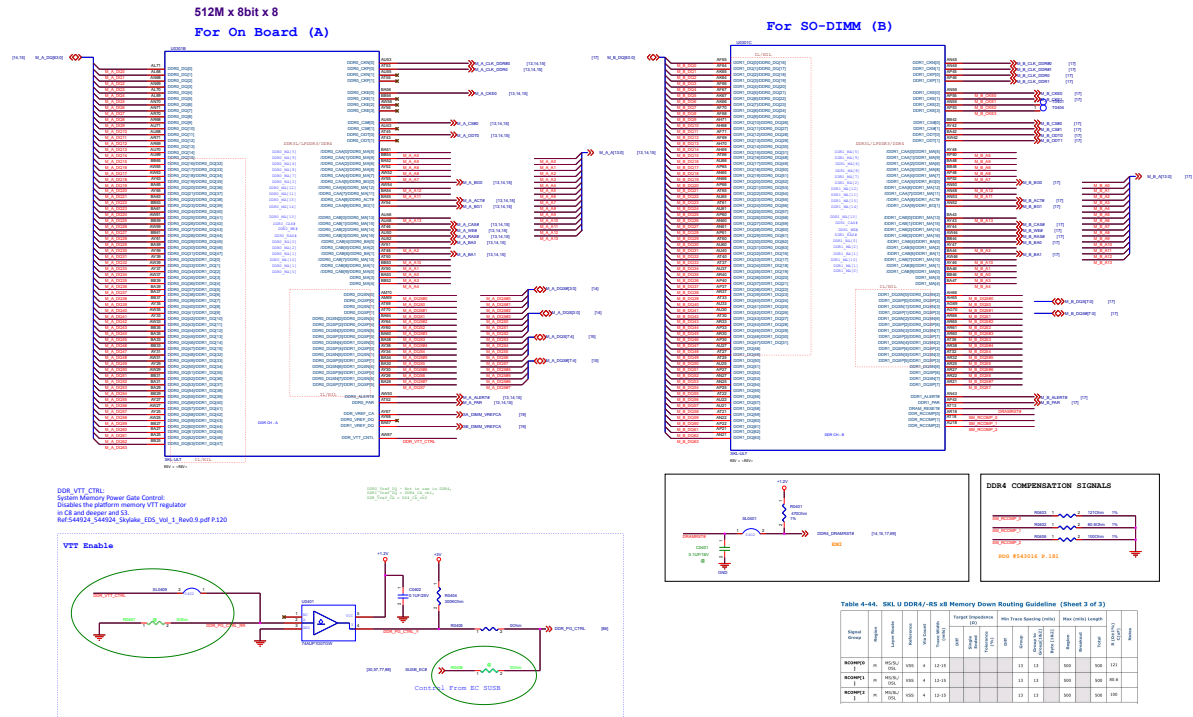
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Table 4-44. SCL U DDR4-ES x8 Memory Down Routing Guideline (Sheet 3 of 3)

Signal Name	Pin	Package	Pin	Target Impedance (Ω)	Min Trace Length (mm)	Max (cm) Length	Min (cm) Length	Min (cm) Length	Min (cm) Length
AD0000	10	PGA	10	12.115		11	11	100	121
AD0001	11	PGA	11	12.115		11	11	100	121
AD0002	12	PGA	12	12.115		11	11	100	121
AD0003	13	PGA	13	12.115		11	11	100	121



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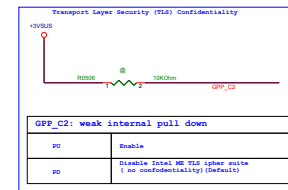
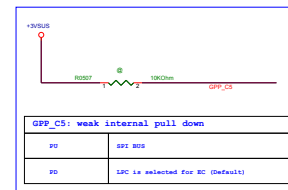
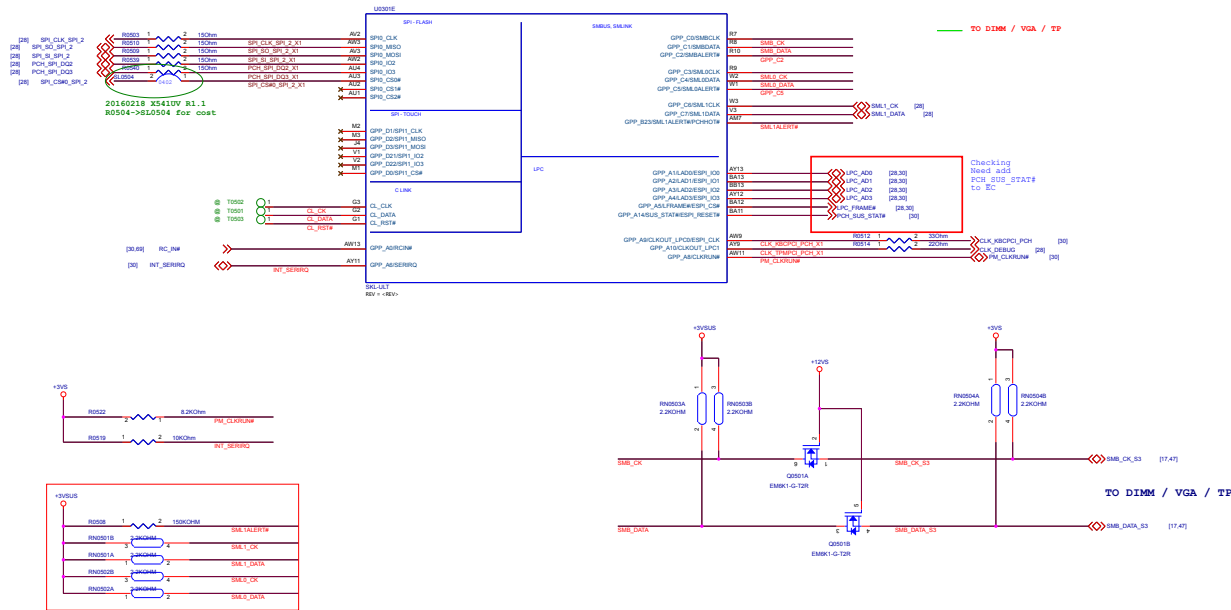
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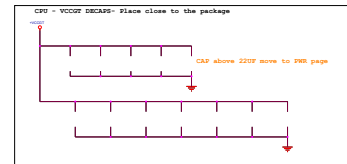
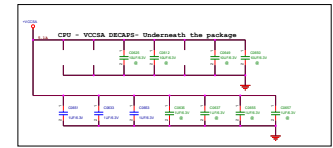
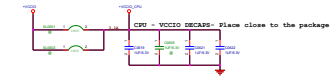
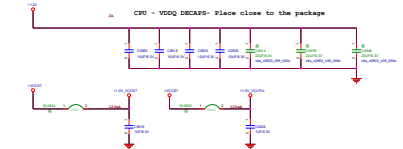
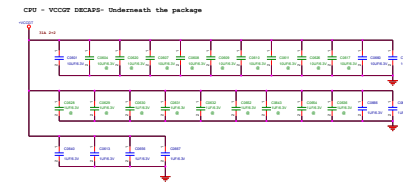
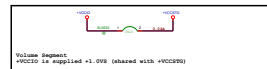
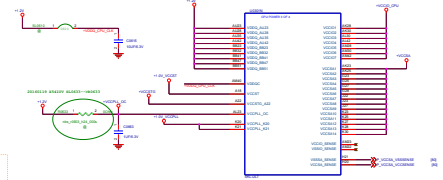
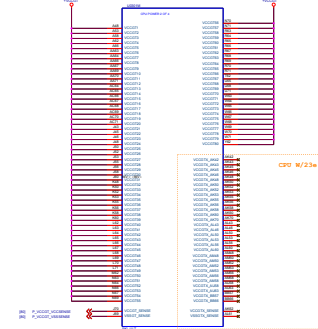
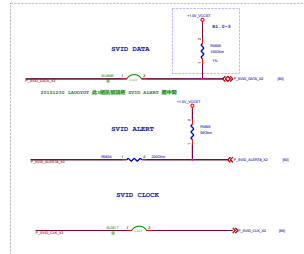
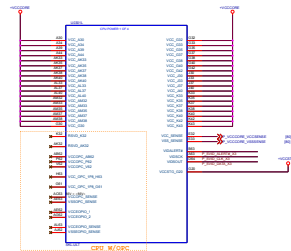
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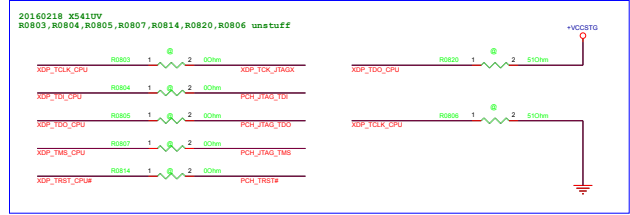
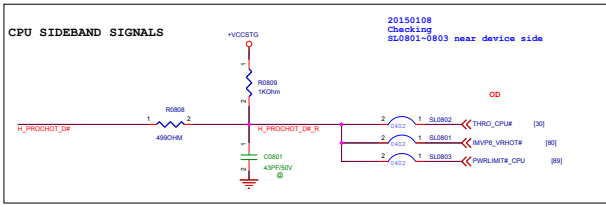
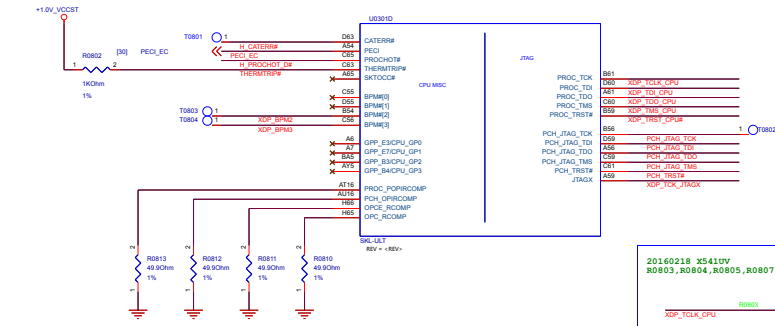
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BOM		Project Name	Rev
ASUS		X540UV/UA	R1.0
Title : CPU_MISC,JTAG,CLK			
Size	Dept.: ASUS/TK COMPUTER INC. Engineer: NB2_EE2		
8	Date: Thursday September 01, 2016	Sheet	8 of 102

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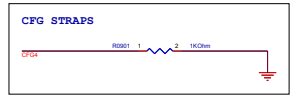
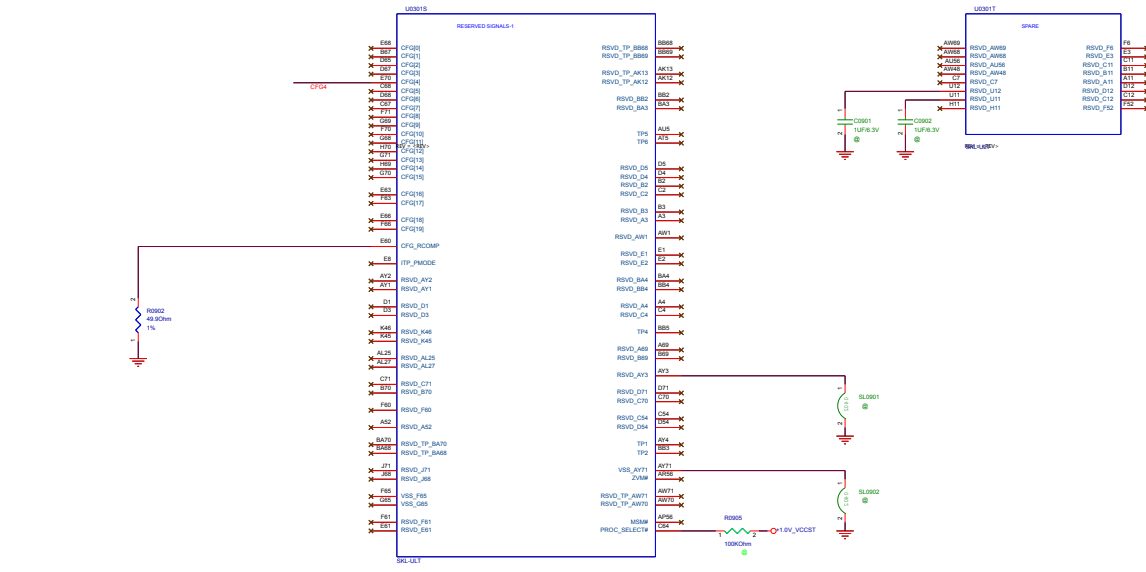
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	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCP PILL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

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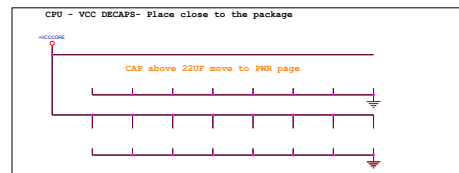
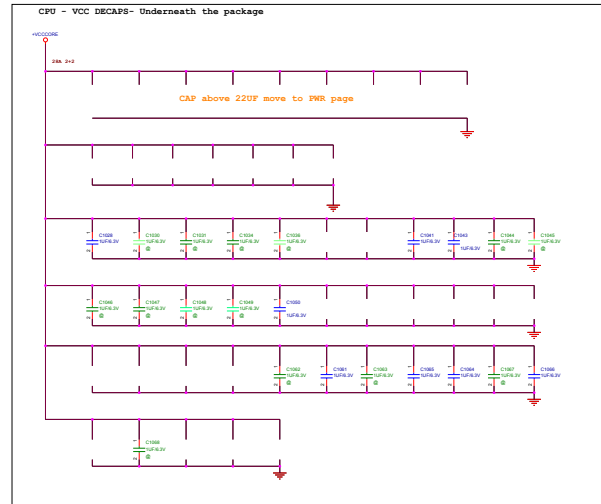
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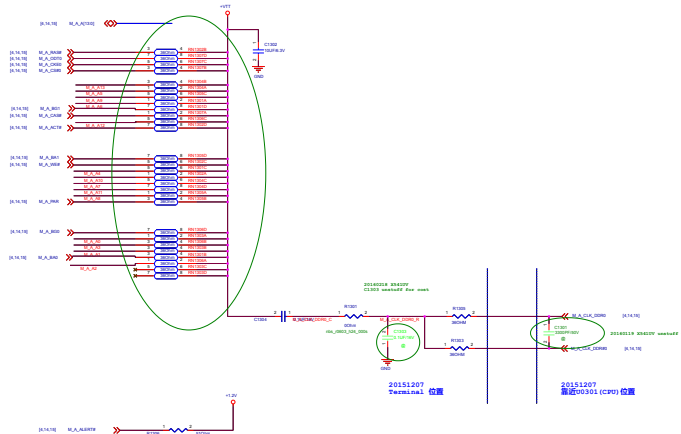


Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4 / RS SO-DIMM+ECC	DDR4 / RS SO-DIMM no ECC	DDR4 / RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CA[9:0], CA[8:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]
ECC strobe	DQSP[8], DQSN[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

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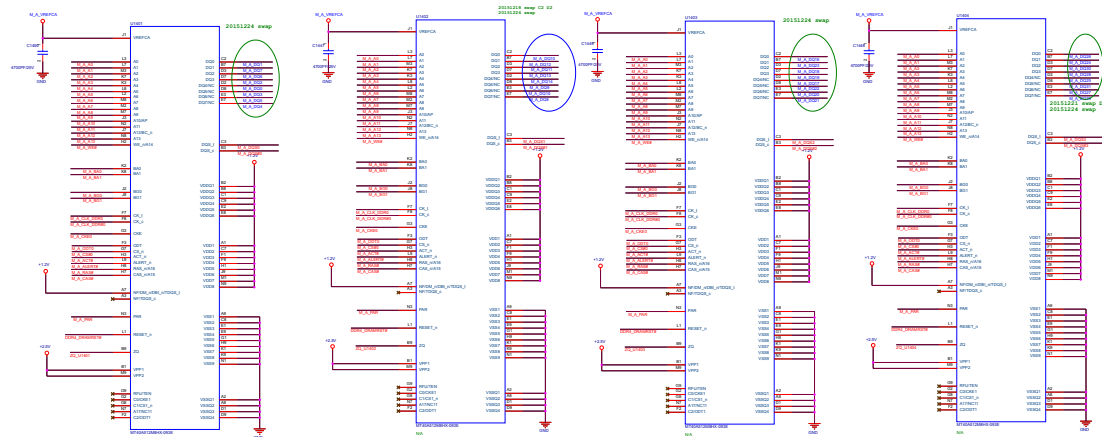
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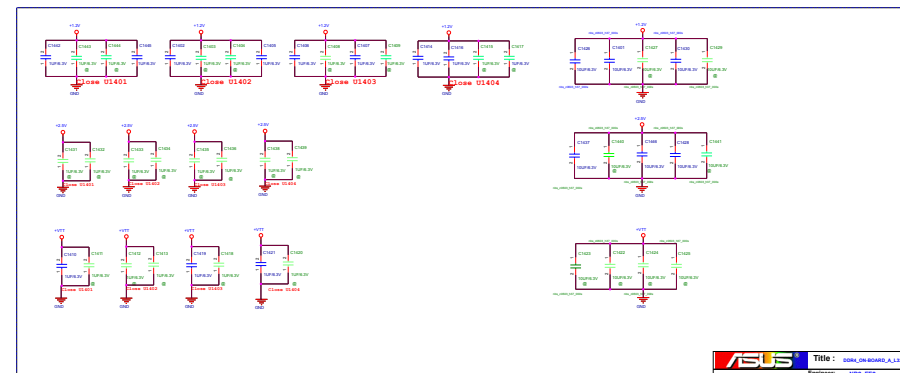
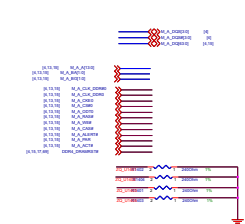
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Onboard Memory Source

ASB #/M	Memory	Vendor
03012-0010100	MEM_001	MCIXON/MT68A122M00-032E
03013-0003000	MEM_002	RAMSIBU/68A03000-BC7A
03013-0003000	MEM_003	RAMSIBU/68A03000-BC7A
03013-0003010	MEM_004	MCIXON/MT68A1000-032E_A



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- 021_CPU_PCH_CGPIIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
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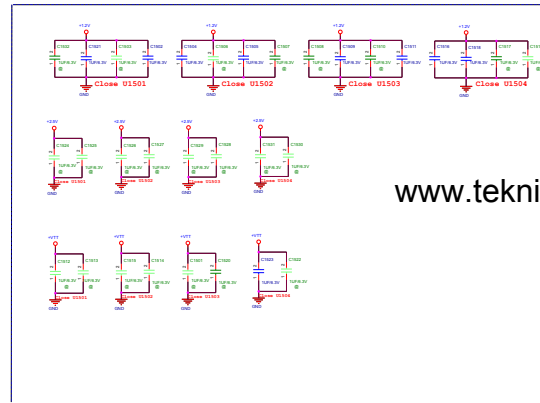
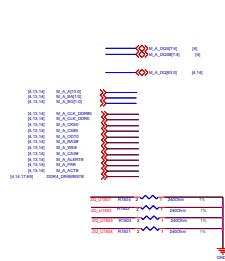
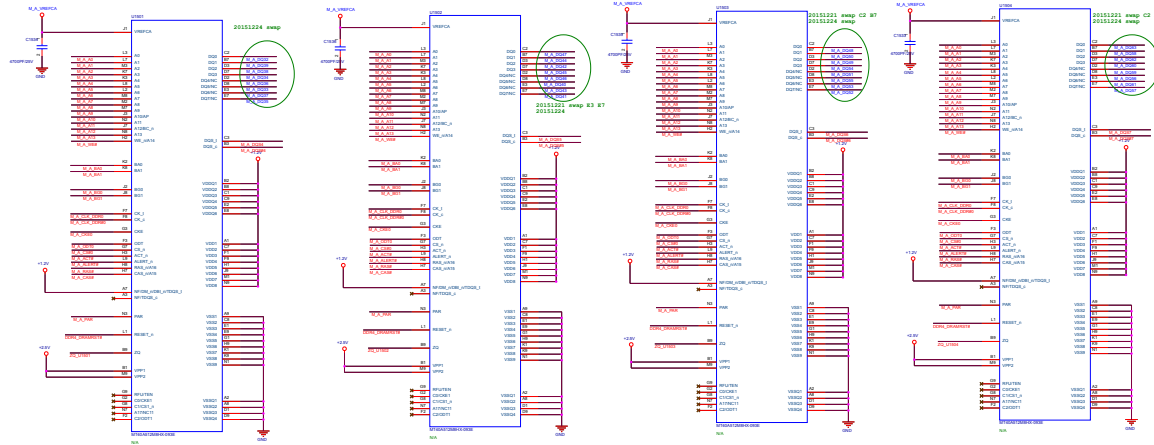
027

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	Title : SDH_ON-BOARD_A_00
Engineer: NB2_EE2	
X540V/JA	

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- 018_DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPI0, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040

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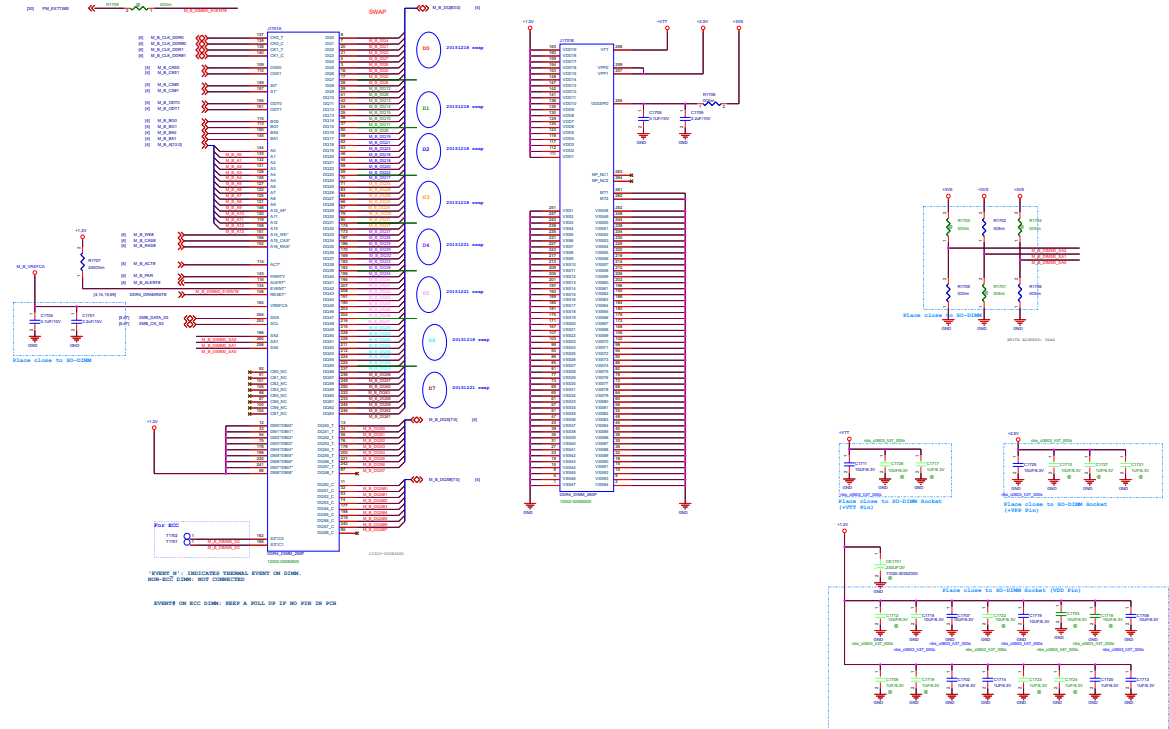
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- 018.DDR4_CA VOLTAGE
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- 020_CPU_PCH_CSI2,EMMC
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- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
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Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down VREF-CA Overview

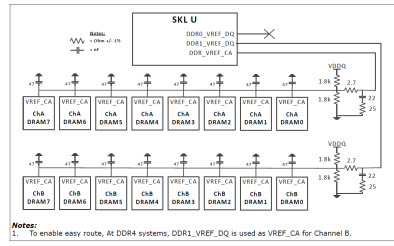
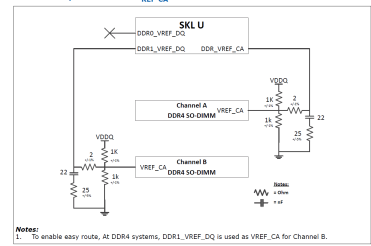
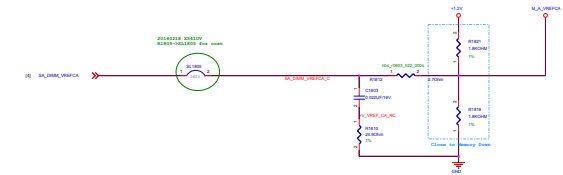
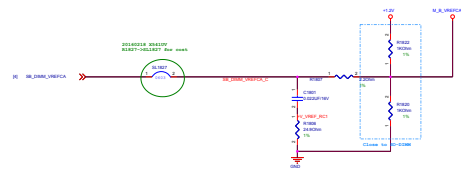


Figure 4-49. SKL U DDR4/-RS SODIMM VREF-CA Overview



All Vref trace must be 20 mils width



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Hide

- 018.DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
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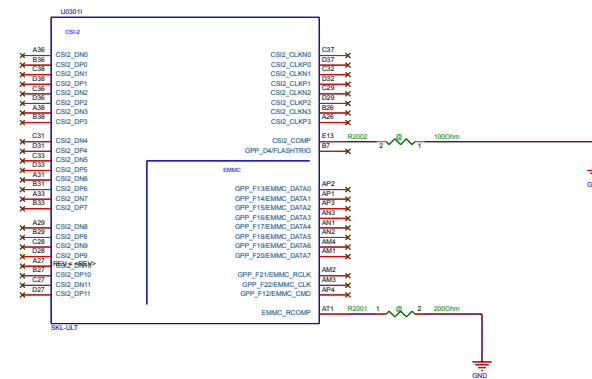
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BOM		Project Name		Rev
ASUS		X540UV/UA		R1.0
Title : CPU_PCH_CSI2,EMMC				
Size	Dept:	ASUSTEK COMPUTER INC.	Engineer:	NB2_EE2
B	Date:	Thursday, September 01, 2016	Sheet:	20 of 102

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- 018.DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
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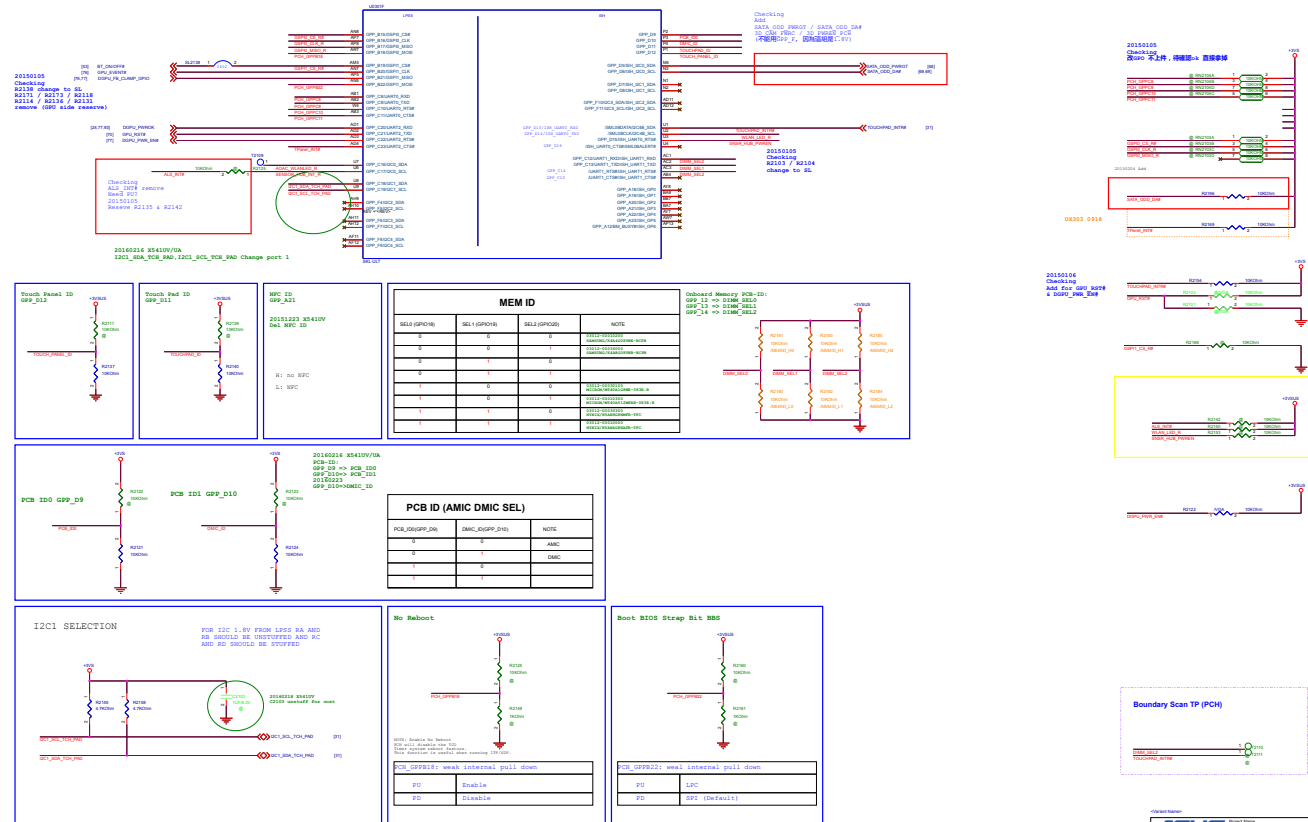
Toggle FullScreen

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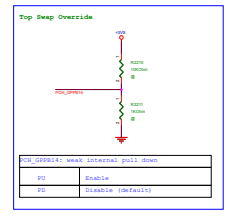
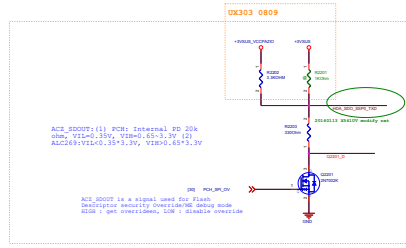
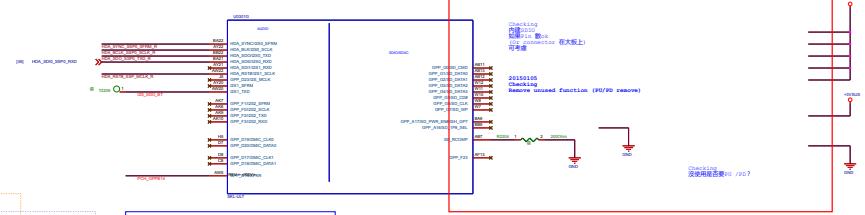
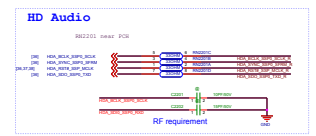
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Hide

- 018.DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
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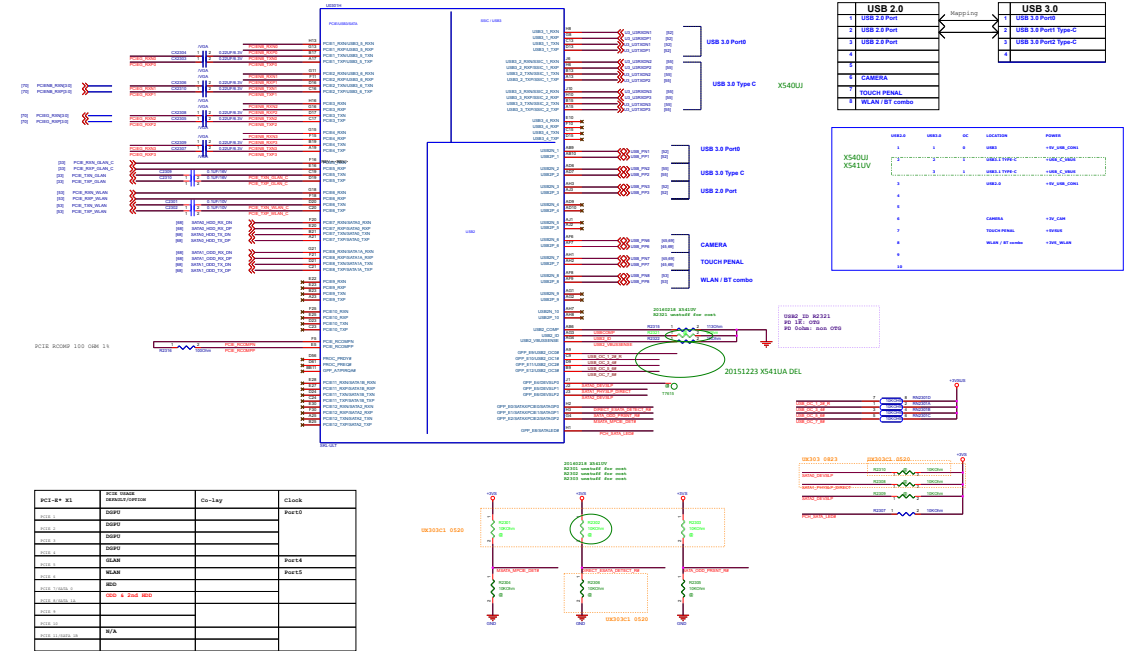
Hide

- 016.DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
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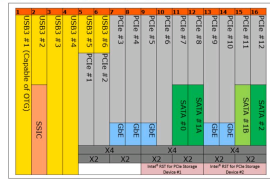
015	017	018	020	021	022	023	024	025	026	027
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PCB #/ XL	PCB USAGE	Co-Lay	Class
0000	SSD0		Part0
0001	SSD0		Part0
0002	SSD0		Part0
0003	SSD0		Part0
0004	SSD0		Part0
0005	SSD0		Part0
0006	SSD0		Part0
0007	SSD0		Part0
0008	SSD0		Part0
0009	SSD0		Part0
0010	SSD0		Part0
0011	SSD0		Part0
0012	SSD0		Part0
0013	SSD0		Part0
0014	SSD0		Part0
0015	SSD0		Part0
0016	SSD0		Part0
0017	SSD0		Part0
0018	SSD0		Part0
0019	SSD0		Part0
0020	SSD0		Part0
0021	SSD0		Part0
0022	SSD0		Part0
0023	SSD0		Part0
0024	SSD0		Part0
0025	SSD0		Part0
0026	SSD0		Part0
0027	SSD0		Part0
0028	SSD0		Part0
0029	SSD0		Part0
0030	SSD0		Part0
0031	SSD0		Part0
0032	SSD0		Part0
0033	SSD0		Part0
0034	SSD0		Part0
0035	SSD0		Part0
0036	SSD0		Part0
0037	SSD0		Part0
0038	SSD0		Part0
0039	SSD0		Part0
0040	SSD0		Part0

Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in SKL U



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- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
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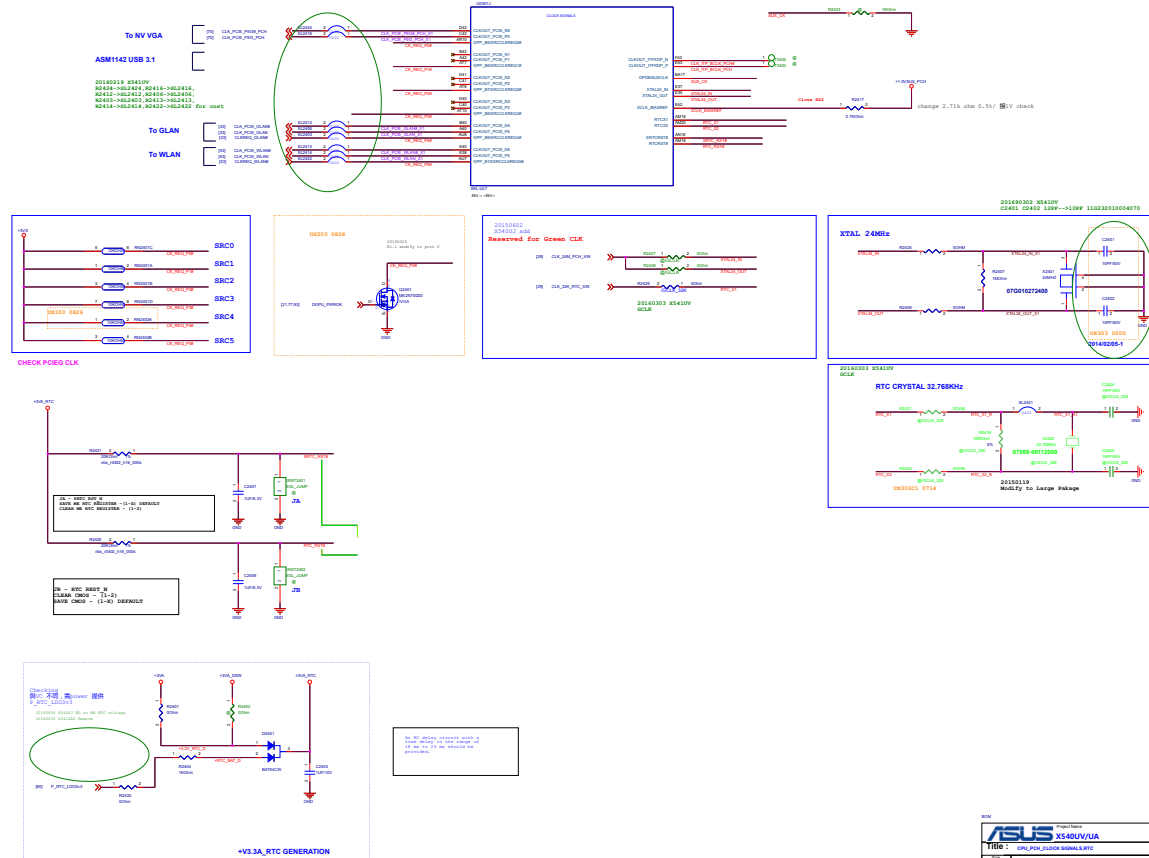
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- 018_DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
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- 036_AUD-ALC3251
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- 038_AMP_Speaker
- 039_
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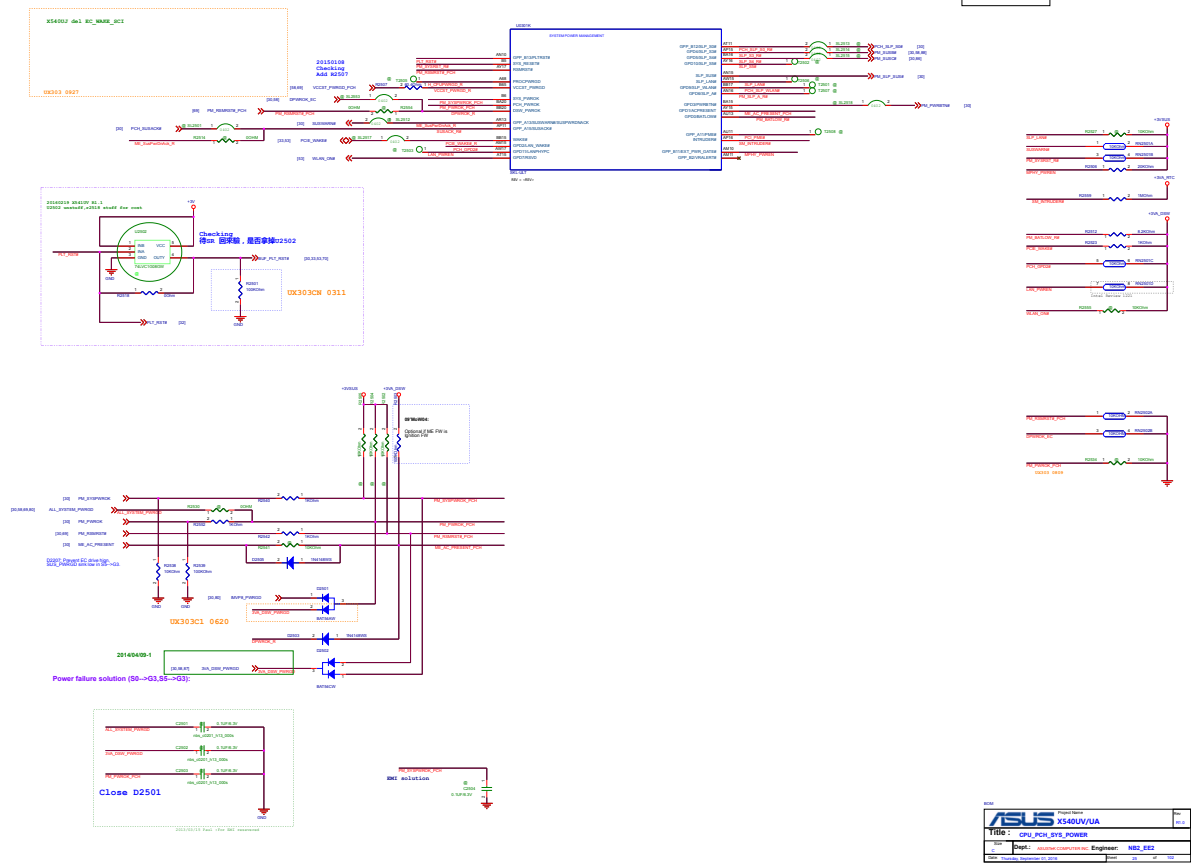
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ASUS		Project Name	Doc. No.
ASUS X540UV/UA			
Title: CPU_PCH_SYS_POWER		Engineer: NSD_EE2	
Date: 2018/08/06		Check: NSD_EE2	
Drawn: NSD_EE2		Appr: NSD_EE2	

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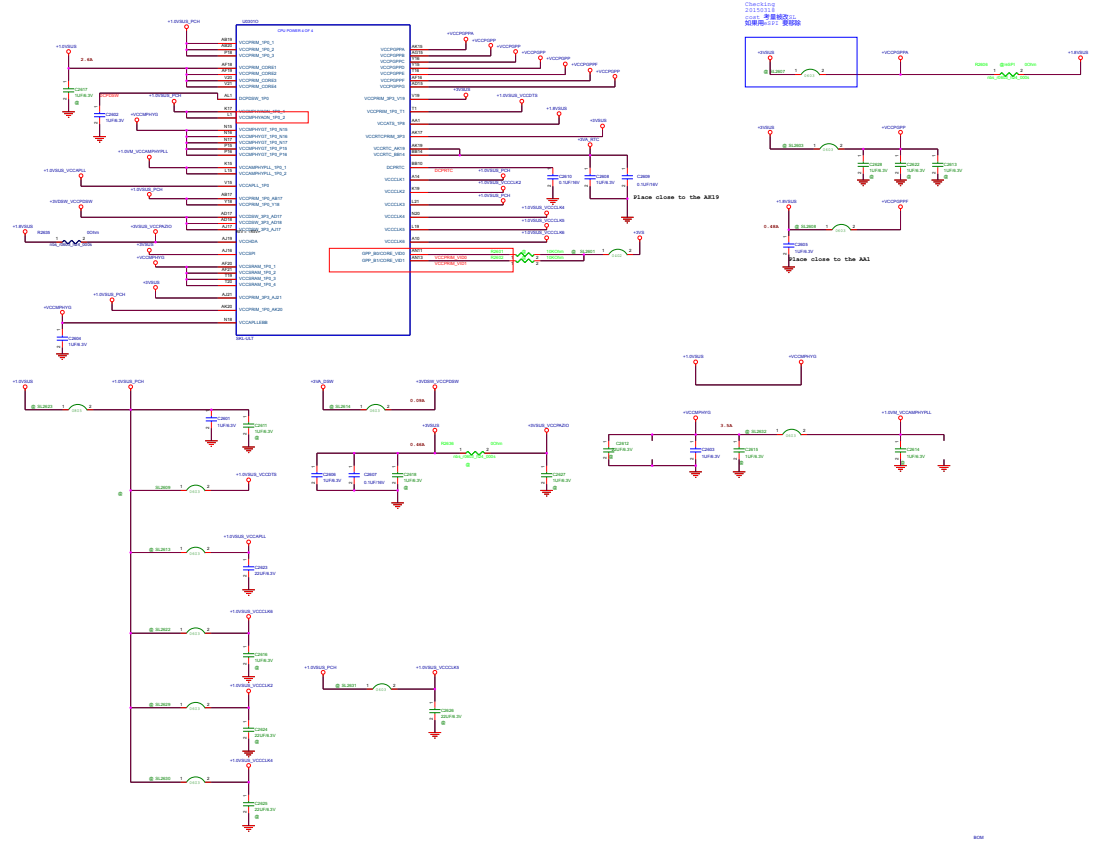
Hide

- 018.DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC

- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen____
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
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019_DDR4_****

020_CPU_PCH_CSI2,EMMC

021_CPU_PCH_CGPIIO, LPIO, MI SC

022_CPU_PCH_AUDIO,SDIO,SD XC

023_CPU_PCH_PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL S,RTC

025_CPU_PCH_SYS_POWER

026_CPU_PCH_POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH,DEBUG

029_Silego_Green_CLK_Gen____

030_IT8995E-128/CX

031_KBC_KB,TP,KB-light

032_RST_Reset Circuit

033_RTL8402 (LAN+CR)

034_RTL8402_RJ45

035_****

036_AUD-ALC3251

037_AUD-HEADPHONE JACK

038_AMP_Speaker

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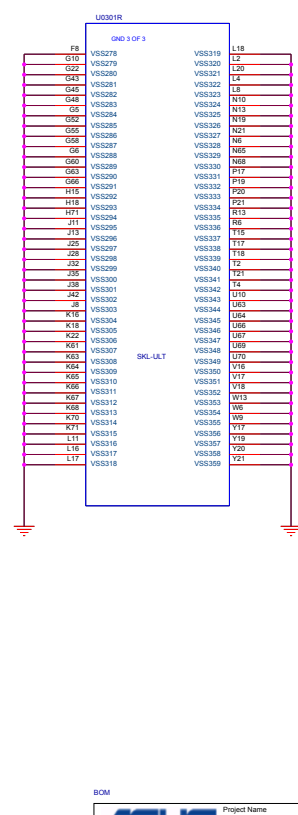
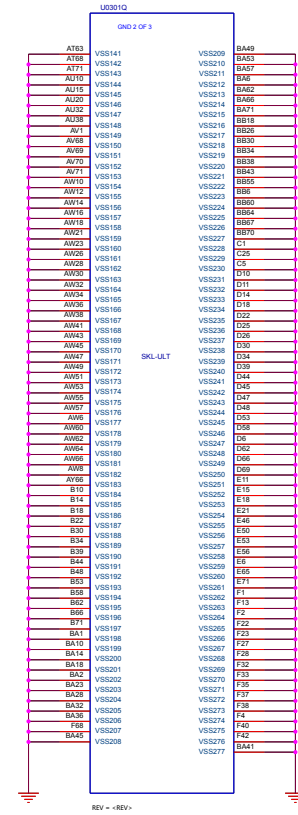
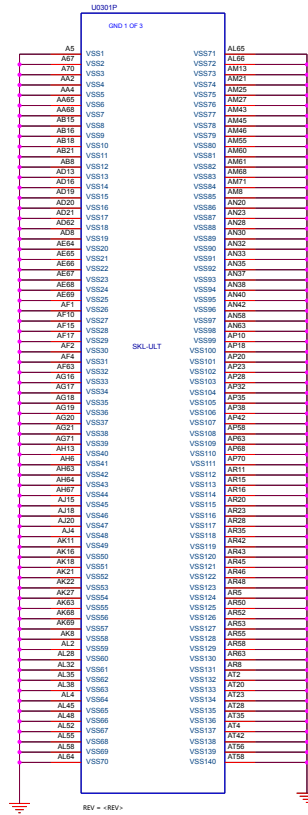
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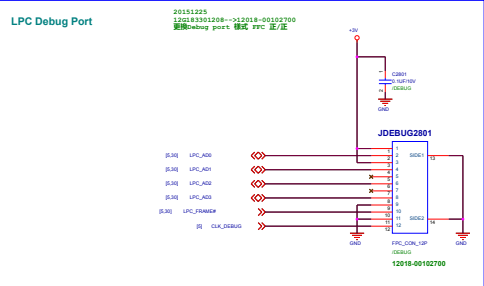
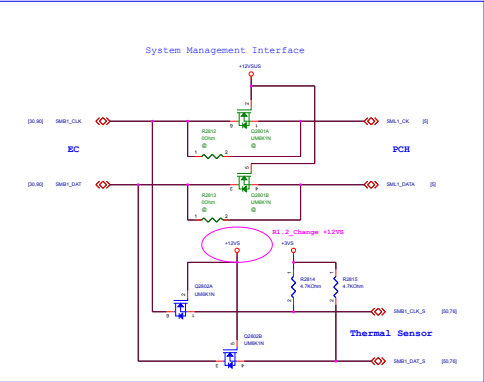
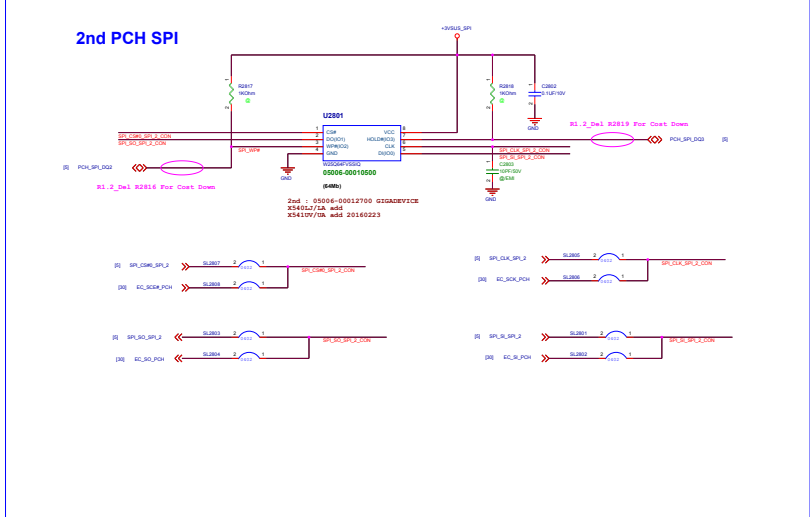
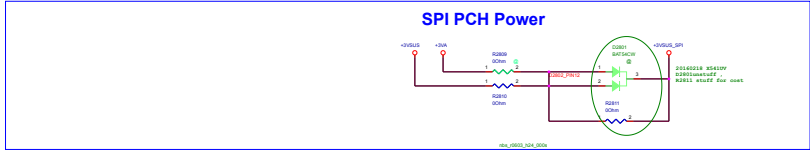
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Hide

- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen_
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTO
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- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

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- 020_CPU_PCH_POEWR,GND
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- 029_Silego_Green_CLK_Gen_
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTO
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- 043_****
- 044_
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- 050_FAN_Thermal Sensor

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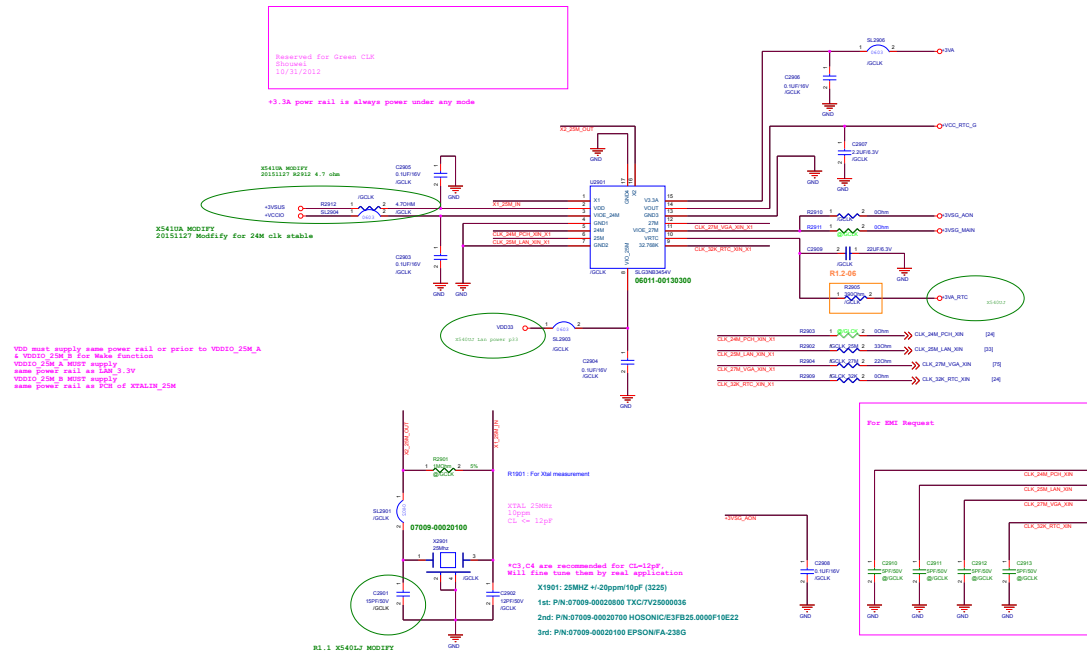
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- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen_
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
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- 041_****
- 042_CARD READER CONNECTO
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- 043_****
- 044_
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- 047_eDP to VGA & CRT D-SUB
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MoveTo

IC 8585

Only 3V Tolerance

```

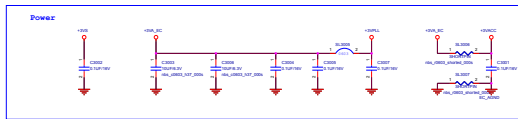
GPA[0,1,2,3,4,5,6]
GPD[0,1,2,3,4,5,6]
GPE[0,1,2,3,4,5,6]
GPF[0,1,2,3,4,5,6]
GPG[0,1,2,3,4,5,6]
GPH[0,1,2,3,4,5,6]
GPI[0,1,2,3,4,5,6]
GPO[0,1,2,3,4,5,6]
    
```

Can be replaced by Open-Drain for part:

```

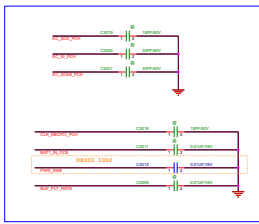
GPA0-GPA3
GPD0-GPD7
GPE0-GPE7
GPF0-GPF7
GPG0-GPG6
GPH0-GPH5
GPI0-GPI5
GPO0-GPO5
    
```

IC Require



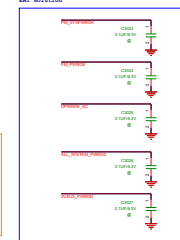
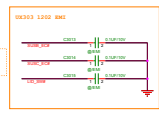
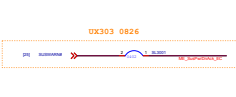
228 Version	ASUS P/N
178995E-128/CX	04037-00050500
178995E-128/CX	04037-00050500

20151123 AS410A MODIFY



目前係使用下規格，此規格係舊物料大小，功能相同：

00037-00050500	EMBEDDED CONTR IT8995E-128/CX	ITE LQFP-128
00037-00050600	EMBEDDED CONTR IT8995VG-128/CX	ITE VFBGA-128



For 8585
External battery always 0V

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- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen_
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTO
R
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

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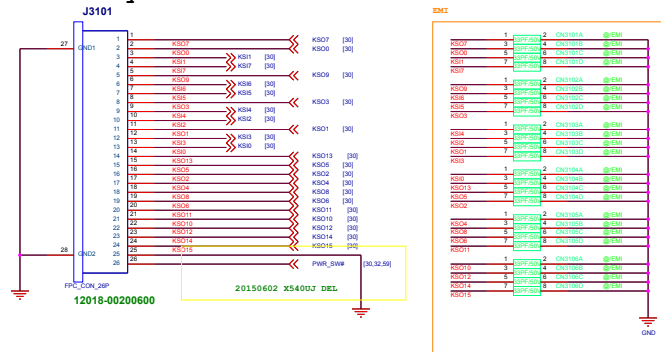
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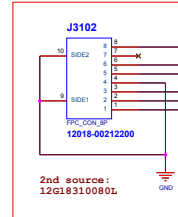
MoveTo

Internal Keyboard

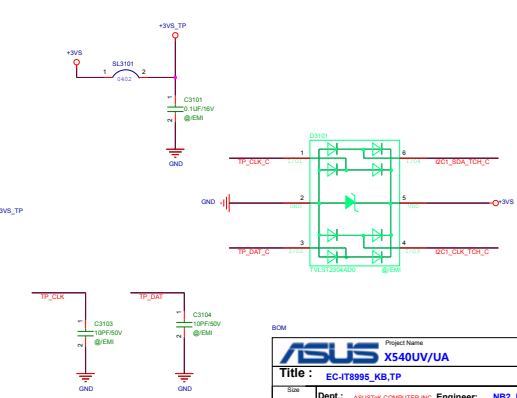
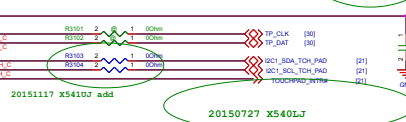


Touch PAD X540LJ 2015/06/22

20160216 X5410V TP Reversal for ME



請將測點至於TOP面
R2.0 新增_Tim_20150820



ASUS		Project Name	Rev
Title : EC-IT8995_KB,TP		EC-IT8995_KB,TP	R1.0
Size	Dept. : ASUS FW COMPUTER INC	Engineer : NBZ_EE2	
Drawn : Thursday, September 01, 2016	Sheet	31	of 99

Schematic Page List

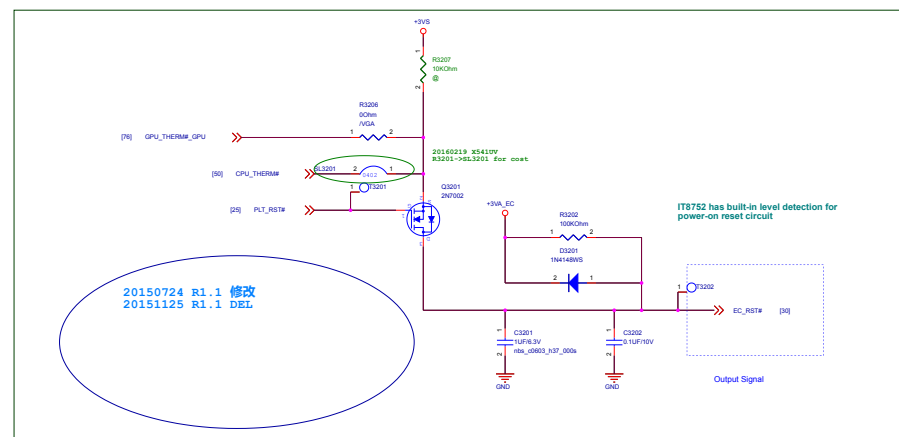
Hide

- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen_
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTO
R
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

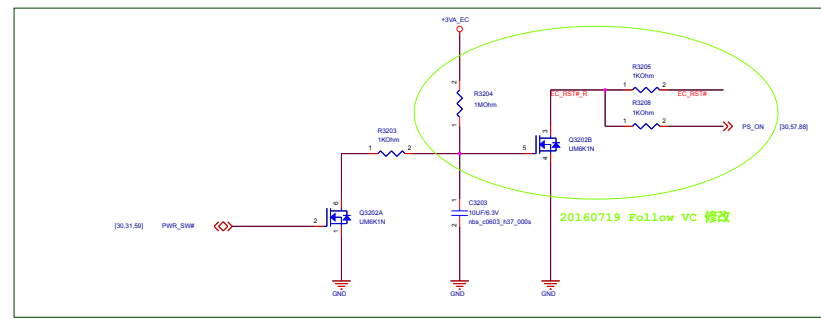
Global Search 028 **029** 030 031 032 033 034 036 037 038 042

Toggle FullScreen Pre Page Next Page MoveTo

Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)



Variant Name:

ASUS		Title :	32_RST_Reset Circuit
ASUSTEK COMPUTER INC. NHA		Engineer:	NB2_EE2
Size	Project Name	Rev	
B	X540UV/UA	R1.0	
File	Thursday, September 01, 2016	Sheet	02 of 07

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- 027_CPU_PCH_POEWR,GND
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- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
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- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTO
- R
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

5.1. Power Management/Isolation

Symbol	Type	Pin No.	Description
LANWAKEB	IO/D	31	Power Management Event Open drain, active low. Used as wake-up signal for LAN8402 and reference clock for LAN8402.
ISOLATEB	I	32	Isolate Pch Active low. Used as wake-up signal for LAN8402. The RTL8402 will not drive its PCI Express outputs (including LAN8402EN) and will not sample its PCI Express input signals as long as the Isolate pin is asserted.

5.2. PCI Express Interface

Symbol	Type	Pin No.	Description
REFCLK_P	I	23	PCI Express Differential Reference Clock Source 1000MHz +100ps.
REFCLK_N	I	22	PCI Express Differential Reference Clock Source 1000MHz +100ps.
TRST#	O	24	PCI Express Tri-state Differential Pair.
IRSTP	I	19	PCI Express Reset Differential Pair.
IRSTN	I	20	PCI Express Reset Differential Pair.
PERSTB	I	30	PCI Express Reset Signal. Active low. When the PERSTB is asserted, power-on state, the RTL8402 returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	IO/D	29	Reference Clock Request Signal. This signal is used by the RTL8402 to request timing of the PCI Express reference clock.

5.3. EEPROM (TW5)

Symbol	Type	Pin No.	Description
SCLLED_CR	O	5	I ² C1 Clock interface for TW5 EEPROM.
SDA	IO	38	SDA. Data interface for TW5 EEPROM. Refer to the reference schematics for the missing pin information. All missing pins are power-on latch pins.

5.4. Transceiver Interface

Symbol	Type	Pin No.	Description
MDI0P	IO	2	In MDI mode, this pin acts as the BL_DA ⁺ pin, and as the transmit pair in 10Base-T and 10Base-TX.
MDI0N	IO	3	In MDI mode, this pin acts as the BL_DB ⁻ pin, and as the receive pair in 10Base-T and 10Base-TX.
MDI1P	IO	4	In MDI mode, this pin acts as the BL_DA ⁺ pin, and as the transmit pair in 10Base-T and 10Base-TX.
MDI1N	IO	5	In MDI mode, this pin acts as the BL_DB ⁻ pin, and as the receive pair in 10Base-T and 10Base-TX.

5.5. Clock

Symbol	Type	Pin No.	Description
CX2TALL	I	45	Input of 25MHz Clock Reference.
CX2TAL2	IO	46	Output of 25MHz Clock Reference.

5.6. Reference

Symbol	Type	Pin No.	Description
REF	I	41	Reference. External reference.

5.7. LEDs

Symbol	Type	Pin No.	Description
SCLLED_CR	O	5	Input of 25MHz Clock Reference.
LEDO	O	39	Output of 25MHz Clock Reference.
LEDS	O	37	Output of 25MHz Clock Reference.

5.8. Card Reader

Symbol	Type	Pin No.	Description
SD_D0MS_D7AD_D0	IO	11	SD Data 0 (SD_D0), MS_Data 7 (D7), and AD Data 0 (AD_D0).
SD_D1MS_CLKAD_D0	IO	12	SD Data 1 (SD_D1), MS_Data 6 (D6), CLK, and AD Data 1 (AD_D1).
SD_D2AD_D7	IO	17	SD Data 2 (SD_D2), MS_Data 5 (D5), and AD Data 7 (AD_D7).
SD_D3MS_D1AD_D1	IO	20	SD Data 3 (SD_D3), MS_Data 4 (D4), CLK, and AD Data 3 (AD_D3).
SD_D4AD_WFA	IO	11	SD Data 4 (SD_D4) and AD Write Enable (AD_WE).
SD_D5MS_CPA	IO	10	SD Data 5 (SD_D5) and AD Chip Select (AD_CS).
SD_D6MS_D5AD_REF	IO	8	SD Data 6 (SD_D6), MS_Data 3 (D3), and AD Read Enable (AD_RE).
SD_D7AD_RDY	IO	4	SD Data 7 (SD_D7) and AD Ready Signal (AD_RDY).
SD_CLKMS_D3AD_D4	IO	18	SD Clock (SD_CLK), MS_Data 1 (D1), D3, and AD Data 4 (AD_D4).
SD_CMDMS_DEAD_D0	IO	15	SD Command Protocol Command and Response Signal, MS_Data 8 (D8), D0, and AD Data 5 (AD_D5).
SD_WPMMS_D1AD_WPM	IO	28	SD Write Protect (SD_WP), MS_Data 1 (MS_D1), and AD Write Protect (AD_WP).
SD_CMDMS_D0AD_ALE	IO	41	SD Command Protocol Address Enable (AD_ALE).
MS_ADMS_CLE	IO	23	MS Address Strobe Command Latch Enable (AD_CLE).
MS_D0AD_D0	IO	42	MS_Data 0 (MS_D0) and AD Data 0 (AD_D0).
MS_D0AD_D1	IO	43	MS_Data 0 (MS_D0) and AD Data 1 (AD_D1).
AD_CS	I	44	AD Chip Select (MS_CS).

5.9. GPO Pin

Symbol	Type	Pin No.	Description
GPO	IO	38	General Purpose IO Pin (Used for Power Saving Feature).

5.10. Power and Ground

Symbol	Type	Pin No.	Description
DVDSD3	P	6, 31	Digital 3.3V Power Supply.
DDSD30	P	34	Digital 1.05V Power Supply.
EVDDSD10	P	18	LDO Regulator 1.05V Output.
Core_VTT	P	7	3.3V Power for All Cores.
VDDSD14	P	24, 40	SD I/Os Standby Power Supply.
CTRL10	P	47	LDO Regulator 1.05V Output.
AVDDSD3	P	1	Analog 3.3V Power Supply.
GND	P	23	Ground.
GND	P	49	Ground (Exposed Pad).

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND, unless otherwise specified.

Symbol	Description	Minimum	Maximum	Unit
AVDDSD3, CARD_VTT, DVDSD3	Supply Voltage 3.3V	-0.3	3.6	V
DVDSD3, EVDDSD10, CTRL10	Supply Voltage 1.05V	-0.3	1.32	V
1.05V DC Input	Input Voltage	-0.3	3.6	V
1.05V DC Output	Output Voltage	-0.3	1.32	V
1.05V DC Input	Input Voltage	-0.3	1.32	V
1.05V DC Output	Output Voltage	-0.3	1.32	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configurations.

8.2. Recommended Operating Conditions

Description	Pin	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	AVDDSD3, CARD_VTT, DVDSD3	3.14	3.3	3.46	V
	DVDSD3, EVDDSD10, CTRL10	1.00	1.05	1.10	V
Ambient Operating Temperature T _a	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configurations.

8.6. DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
AVDDSD3, CARD_VTT, DVDSD3	I _V Supply Idios Voltage	-	3.14	3.3	3.46	V
DVDSD3, EVDDSD10, CTRL10	I _V Supply Mean Voltage	-	1.00	1.05	1.10	V
I _{oh}	Minimum High Level Output Voltage	I _{oh} = 4mA	0.9*V _{DDSD3}	-	V _{DDSD3}	V
I _{ol}	Minimum Low Level Output Voltage	I _{ol} = 4mA	0	-	0.1*V _{DDSD3}	V
I _{ih}	Minimum High Level Input Voltage	-	2.0	-	-	V
I _{il}	Minimum Low Level Input Voltage	-	-	-	0.8	V
I _{in}	Input Current	V _{in} =V _{DDSD3} or GND	0	-	0.5	µA
I _{cc33}	Maximum Operating Supply Current from 3.3V	AVDDSD3 with heavy network traffic and high Card Reader I/O operation	-	810	-	mA
I _{cc10}	Maximum Operating Supply Current from 1.05V	DVDSD3 with heavy network traffic and high Card Reader I/O operation	-	150	-	mA

Note 1: Refer to the most updated schematic circuit for correct configurations.

Note 2: All Supply Mean Voltage power limit $\leq 5\%$ of Mean Voltage.

8.8. Auxiliary Signal Timing Parameters

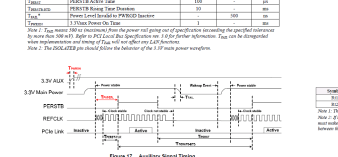
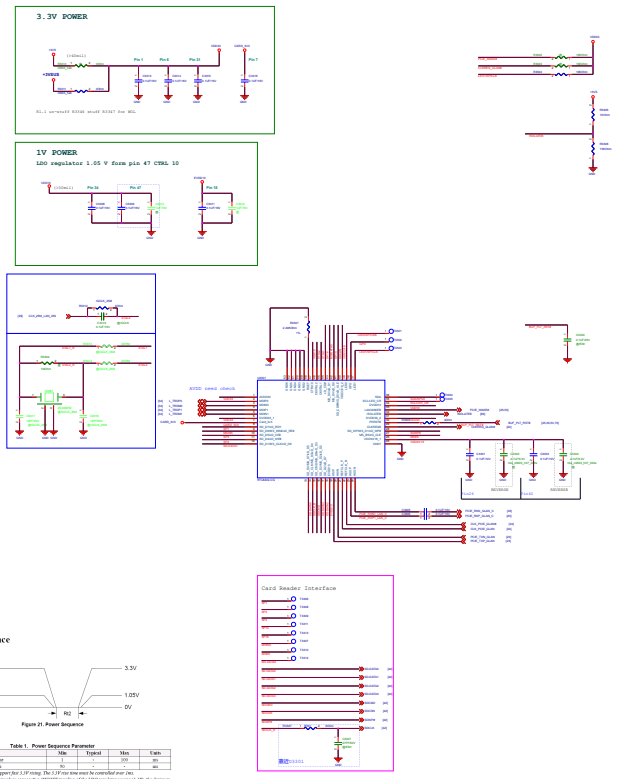


Figure 17. Auxiliary Signal Timing

www.teknisi-indonesia.com



6. Power Sequence

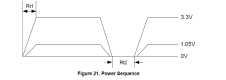


Figure 21. Power Sequence

Symbol	Description	Min	Typical	Max	Unit
t ₁	V _{DD} Rise Time	-	100	-	ns
t ₂	DV Rise Time	-	100	-	ns

Note: The DV signal must be asserted after 1.05V and before 1.05V and after 3.3V and before 3.3V. The 3.3V rise time must be controlled over 100ns.



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- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen_
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTO
R
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

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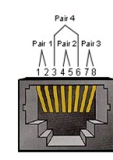
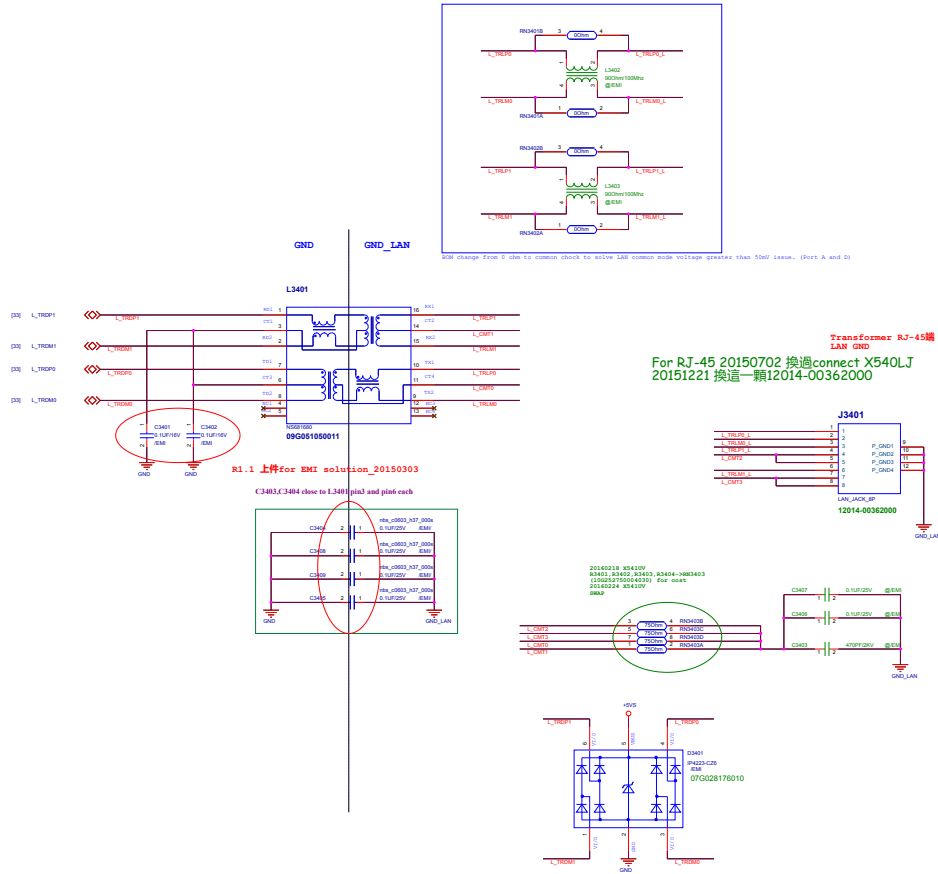
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RJ45連接腳位	傳輸訊號
1	Tx +
2	Tx -
3	Rx +
4	No Signal
5	No Signal
6	Rx -
7	No Signal
8	No Signal

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- 027_CPU_PCH_POEWR,GND
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- 029_Silego_Green_CLK_Gen_
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
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- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
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- 042_CARD READER CONNECTO
R
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

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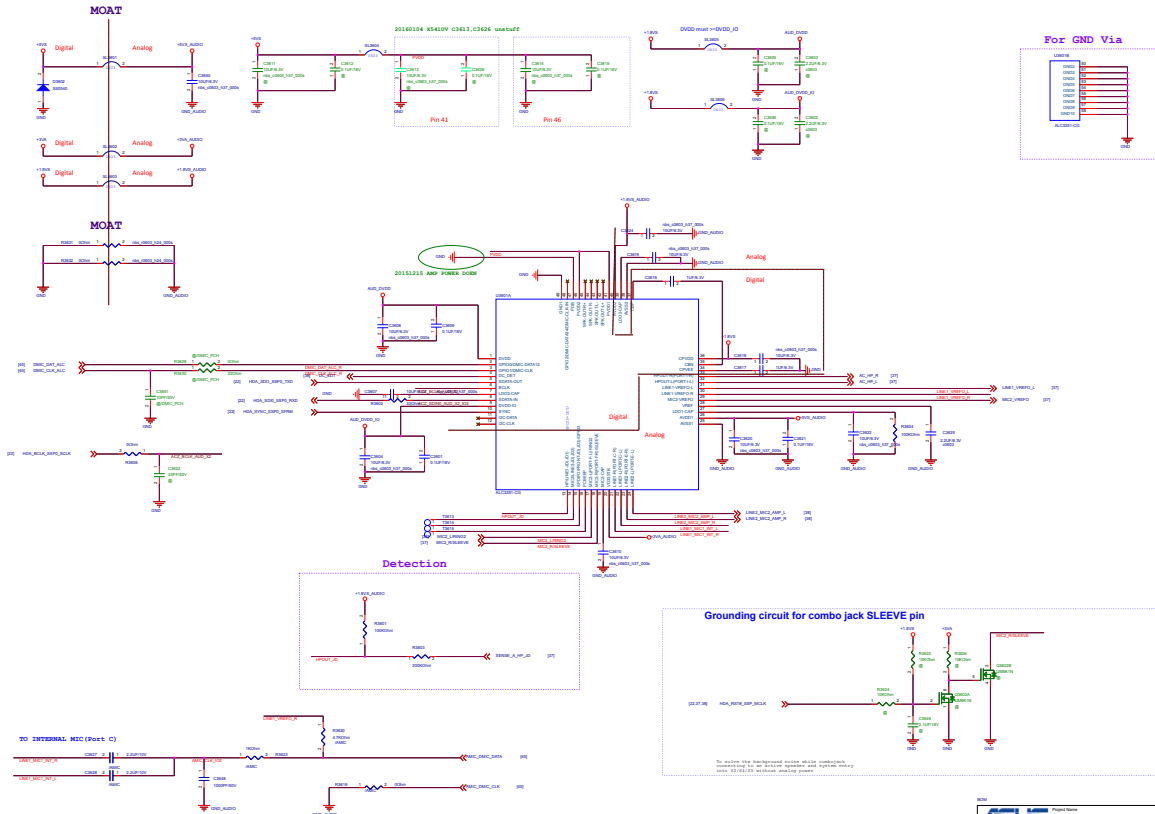
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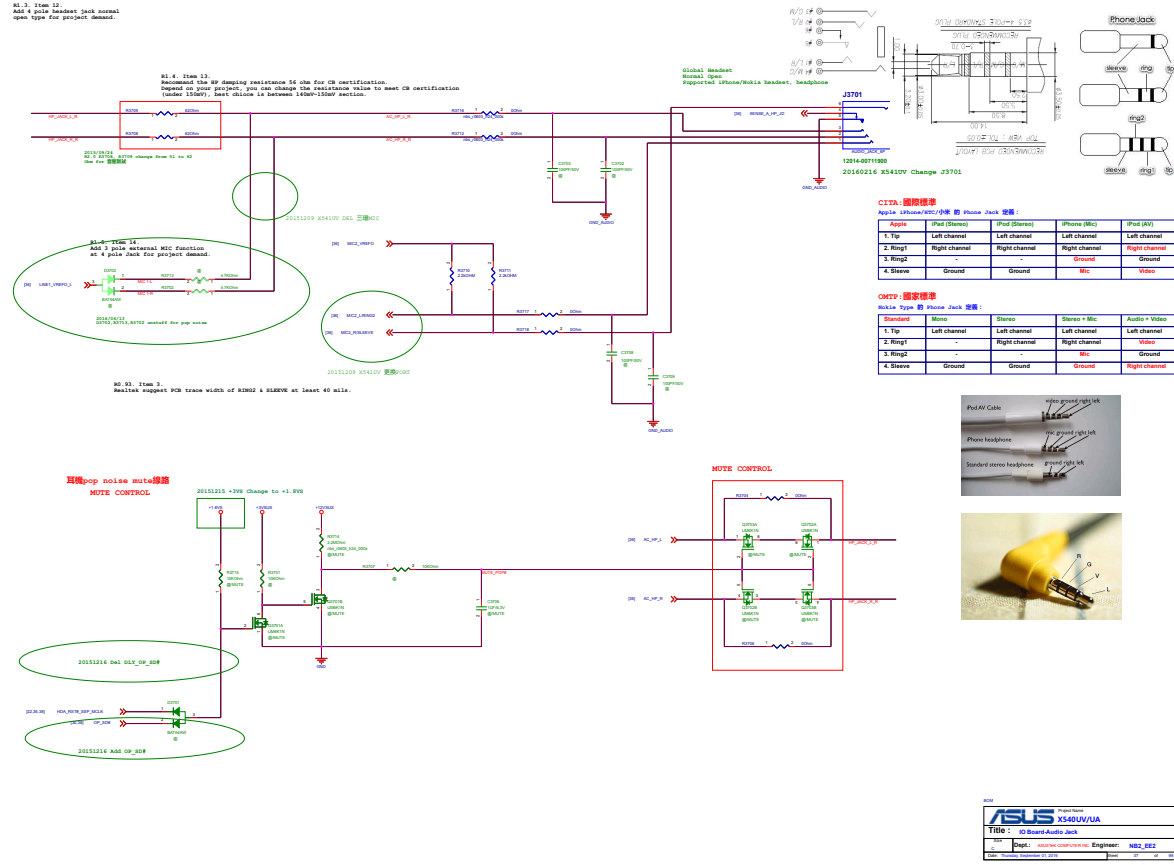
ASUS Project Name		X540UJ	
Title		HIDBIAS-AUD-ALC3251	
Doc	Rev	Equipment	EE

Schematic Page List

Hide

- 020_CPU_PCH_OTWV,CRD
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
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- 038_AMP_Speaker
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- 040_
- 041_****
- 042_CARD READER CONNECTO R
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

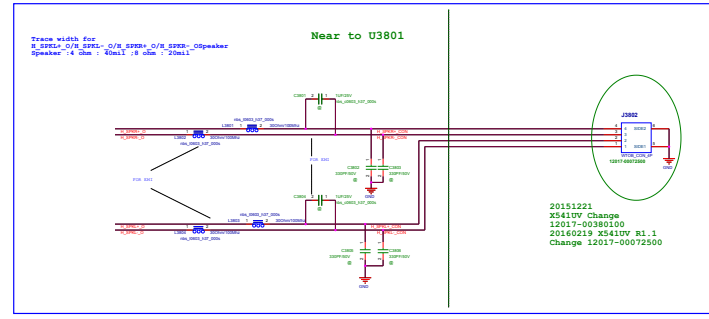
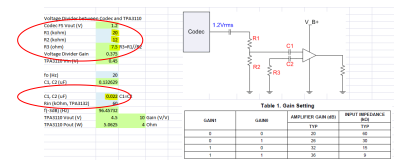
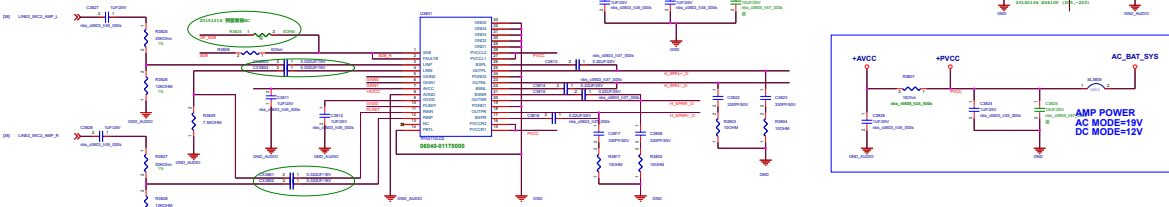
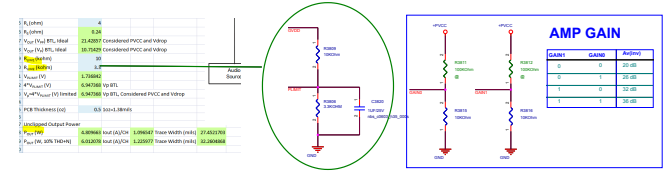
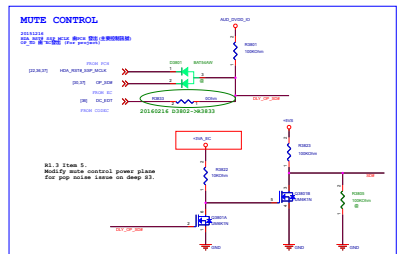
Universal Jack (Normal open type)



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- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029_Silego_Green_CLK_Gen_
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- 045_eDP_LVDS
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- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
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- 040_
- 041_****
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12023-00015500

SD CARD PIN DESIGN

Pin No.	Name	Description
1#	CD/DAT3	Card detect/Data I/O
2#	CMD	Command
3#	VSS1	Ground
4#	VDD	Power
5#	CLK	Clock
6#	VSS2	Ground
7#	DAT0	Data I/O
8#	DAT1	Data I/O
9#	DAT2	Data I/O

10-CARD DETECT PIN
11-WRITE PROTECT PIN
GROUND(SHELL)--COMMON PIN



RTL8402-C0		CARD READER CONNECTOR SIDE		
SD_WP	LOCK: H UNLOCK: L	PIN 11	WRITE PROTECT PIN	LOCK: H UNLOCK: L
SD_CD#	DETECT: L UNDETECT: FLOATING	PIN 10	CARD DETECT PIN	DETECT: L UNDETECT: FLOATING

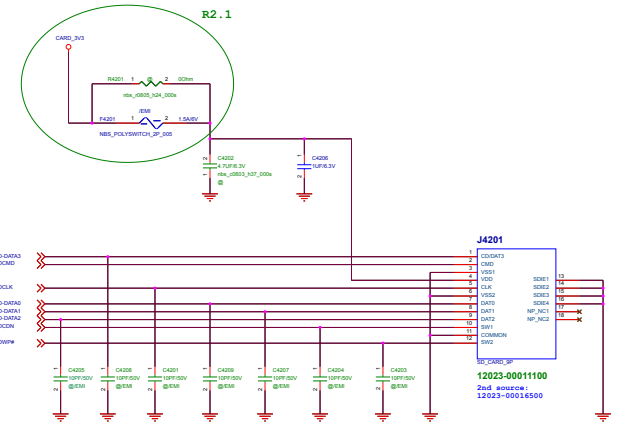
Without card: CD/GND 狀態為開路 WP/CD狀態 閉路
Insert card (unlock): CD/GND 閉路 WP/CD閉路
Insert card (lock): CD/GND 閉路 WP/CD開路

R1.1

Removed Q0501 and RN0501 for J0501 SDWP/SDCD signal reverse circuit

R2.1

移除SL0501改上R0501



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- 042_CARD READER CONNECTO
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- 043_****
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- 050_FAN_Thermal Sensor
- 051_
- 052_USB 3.0 + 2.0 CONN.
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- 055_USB 3.1 MB Type-C
- 056_***
- 057_DSG_Discharge
- 058_PRO_Protect
- 059_Power & WIFI & CAP LED&LI
D
- 060_DC_DC & BAT IN

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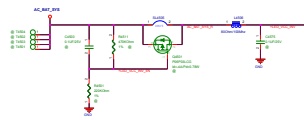
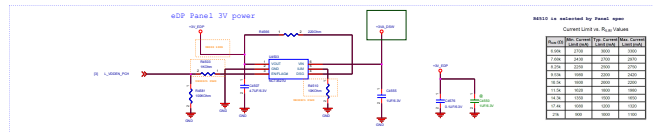
Toggle FullScreen

Pre Page

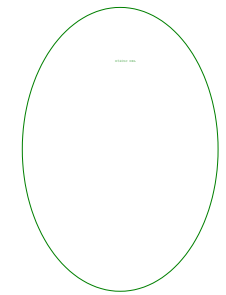
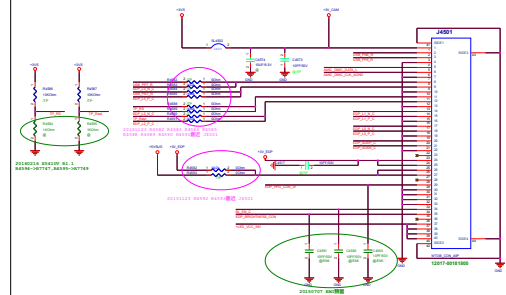
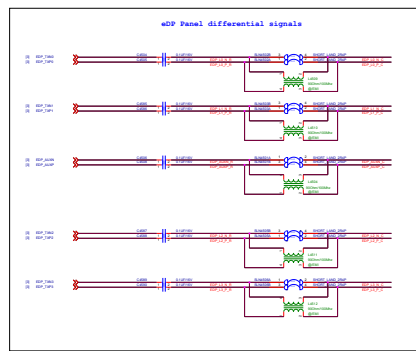
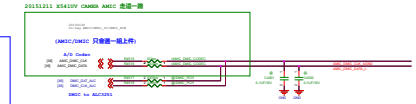
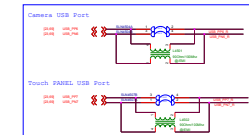
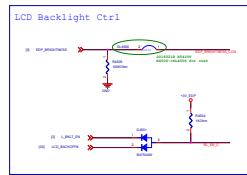
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MoveTo

eDP (LVDS) Panel



tekni-indonesia



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- 054_
- 055_USB 3.1 MB Type-C
- 056_***
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- 059_Power & WIFI & CAP LED&LI
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- 060_DC_DC & BAT IN

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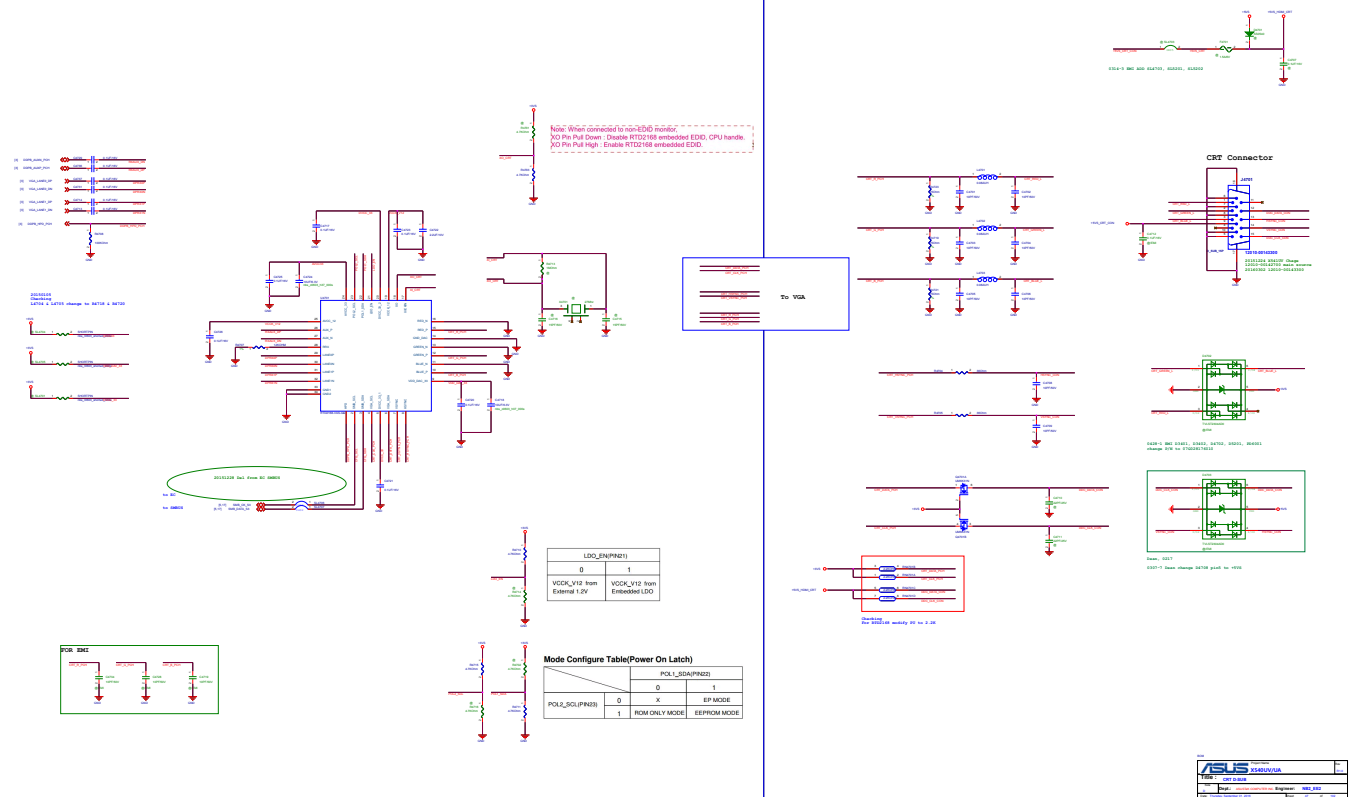
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eDP to VGA

CRT D-SUB



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- 056_***
- 057_DSG_Discharge
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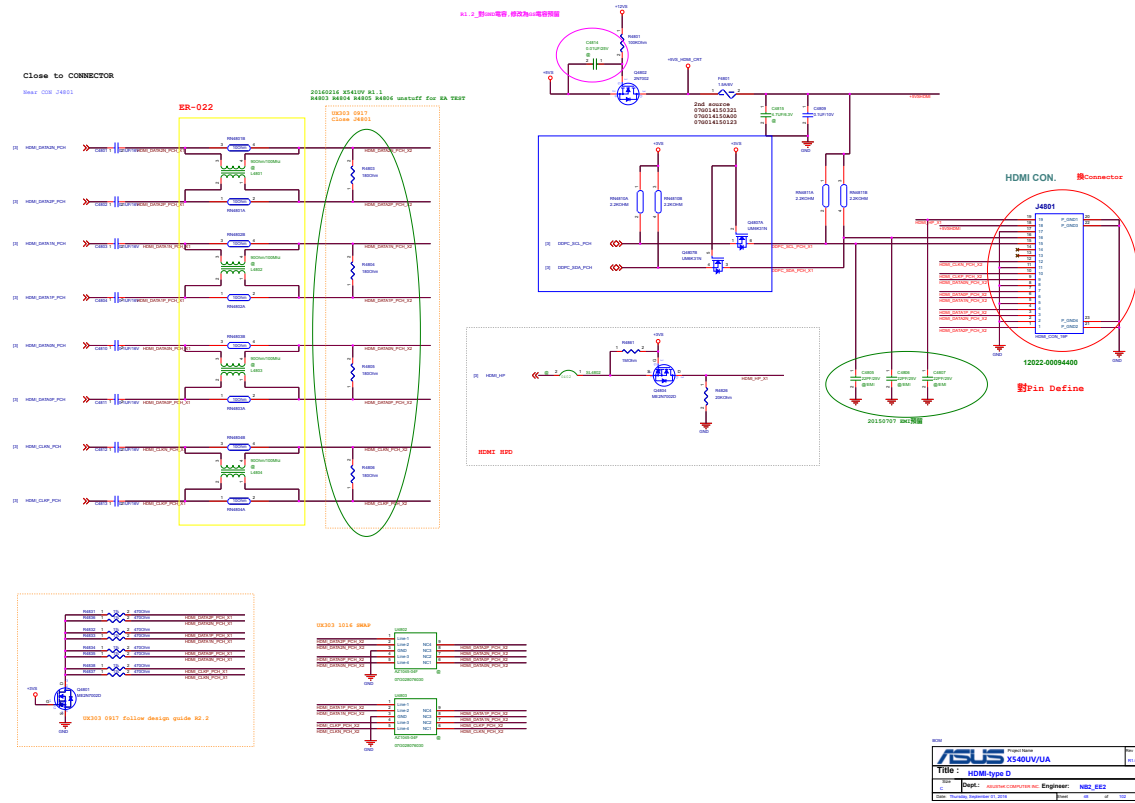
Toggle FullScreen

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HDMI type-A



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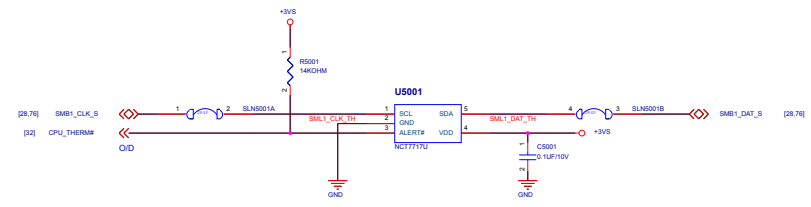
Hide

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- 050_FAN_Thermal Sensor
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CPU Thermal Sensor



5.3 Address Setting
NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

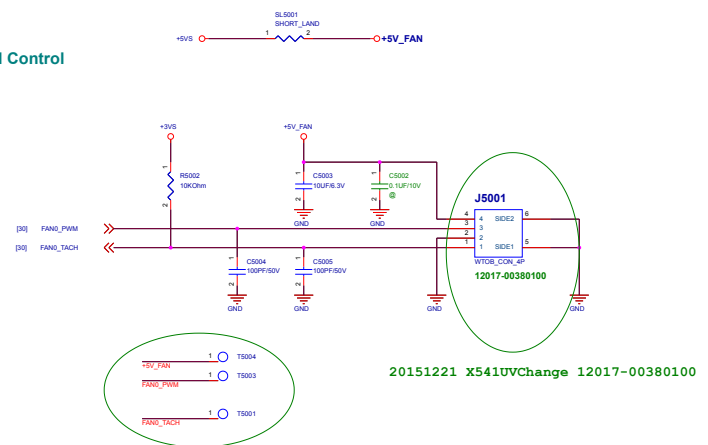
	PULL-UP RESISTOR	TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

```

-----OTHER SIGNALS
10 mils =====GND
10 mils =====H_THERMDA(10 mils)
10 mils =====H_THERMDC(10 mils)
10 mils =====GND
10 mils -----OTHER SIGNALS
Avoid FSB,Power
    
```

DC FAN Control



20151221 X541UVChange 12017-00380100

請將測點至於TOP面
R2.0 新增 Tim_20150820

ASUS Title : 05_FAN_Thermal Sensor
 ASUSAN COMPUTER INC. NBS Engineer: NB2_EE2
 Size: Project Name: X540UV/UA Rev: R1.0
 Date: Thursday, September 01, 2016 Sheet 50 of 59

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- 067_***
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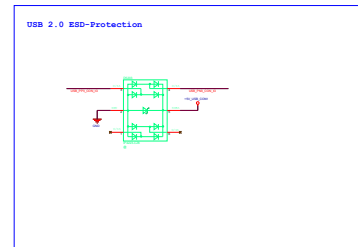
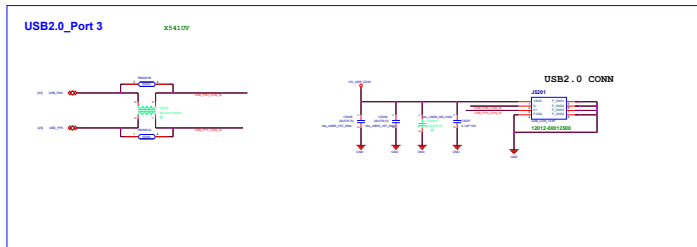
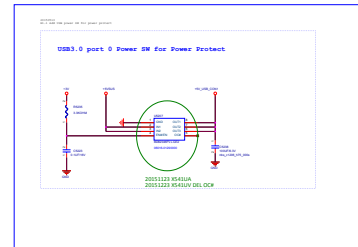
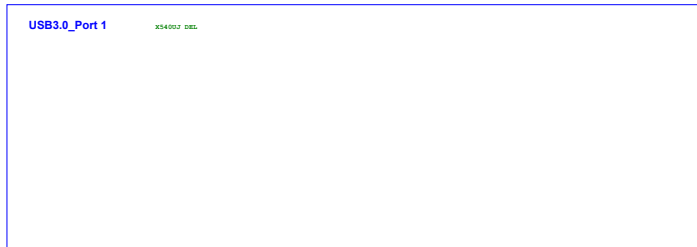
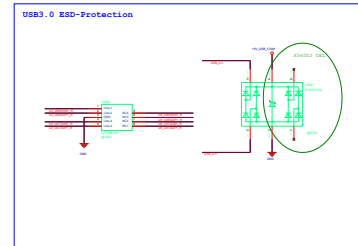
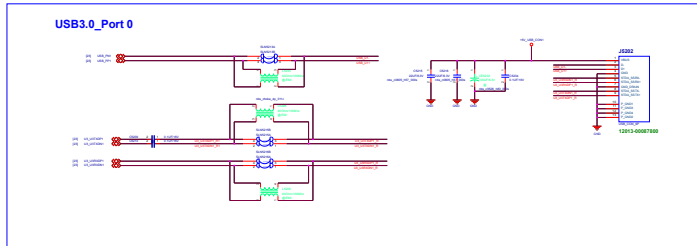
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- 067_***
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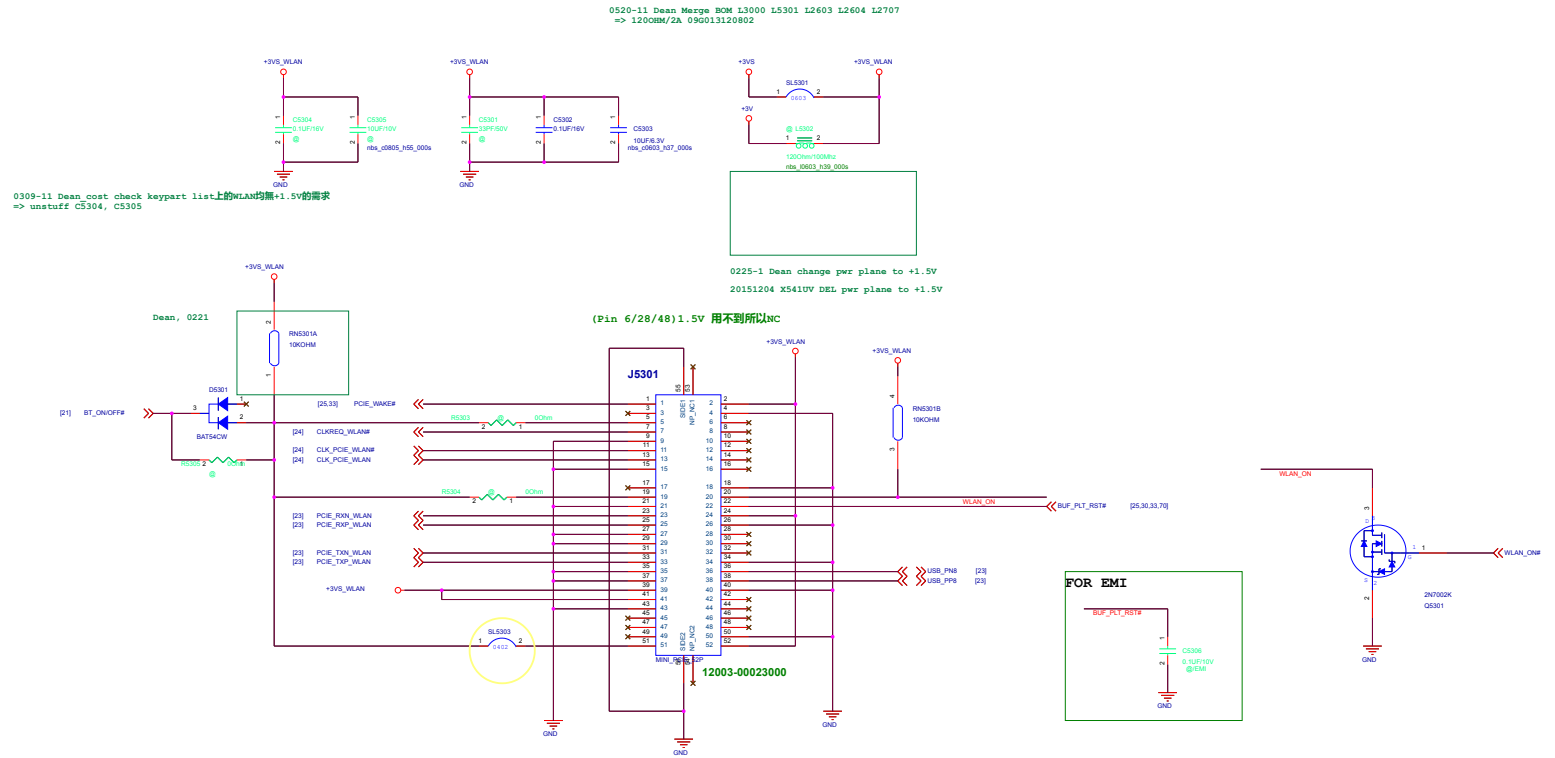
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0309-11 Dean_cost check keypart list上的WLAN均展+1.5V的需求
=> unstuff C5304, C5305

0520-11 Dean Merge BOM L3000 L5301 L2603 L2604 L2707
=> L5302RM/ZA 036013120902

0225-1 Dean change pwr plane to +1.5V
20151204 X541UV DEL pwr plane to +1.5V

(Pin 6/28/48) 1.5V 用不到所以NC

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- 067_***
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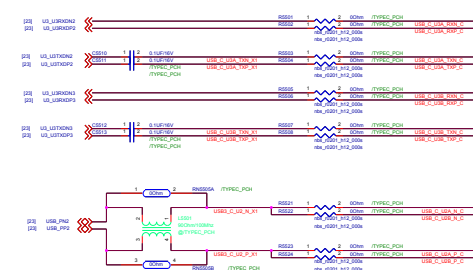
Toggle FullScreen

Pre Page

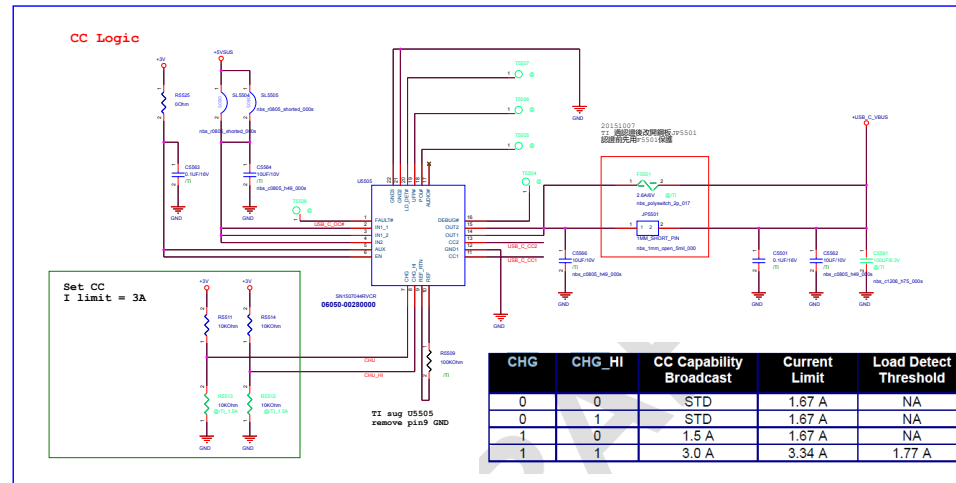
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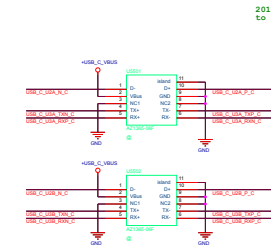
From PCH



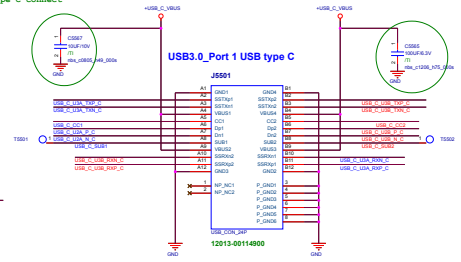
From ASM1142 US83.1



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



20151216 C5565 C5567 Near to type C connect



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- 056_***
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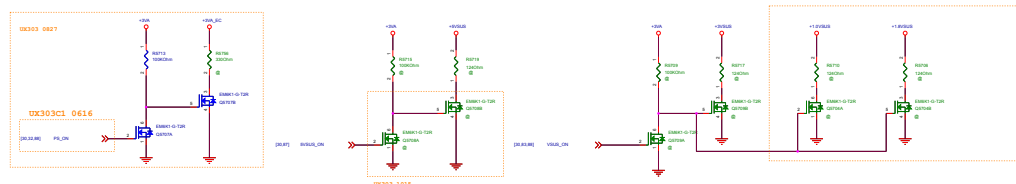
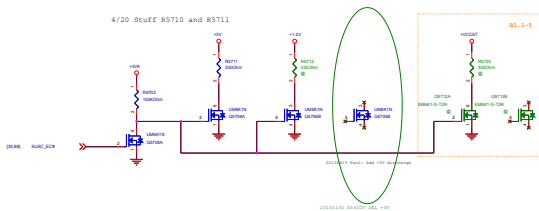
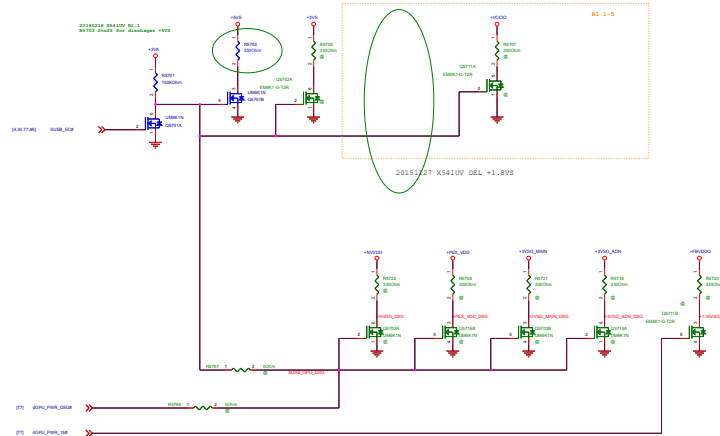
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Main Board



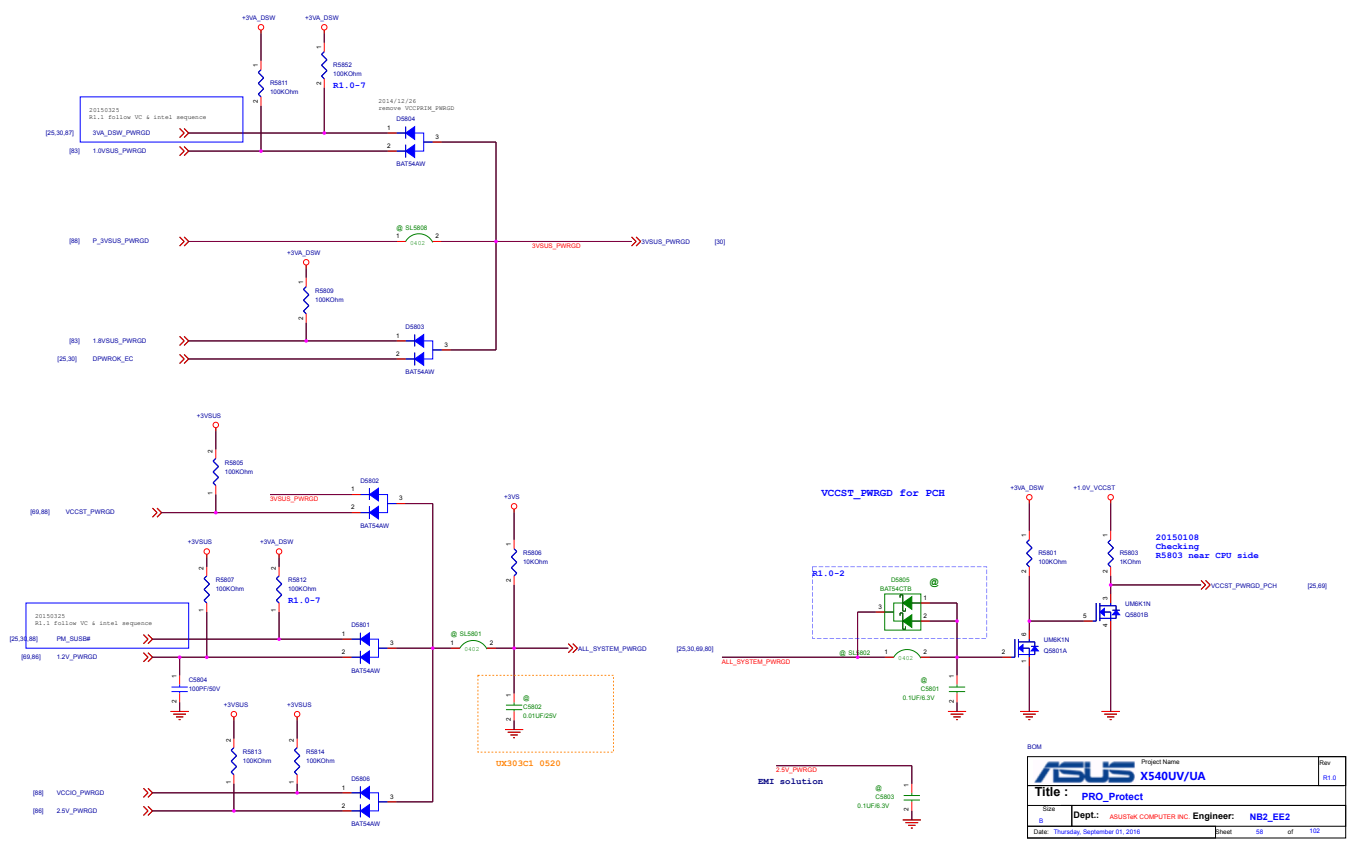
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ASUS Project Name		Rev
X540UV/UA		R1.0
Title: PRO_Protect		
Dept:	ASUSTek COMPUTER INC. Engineer:	NB2_EE2
Date: Thursday, September 01, 2016	Sheet	58 of 102

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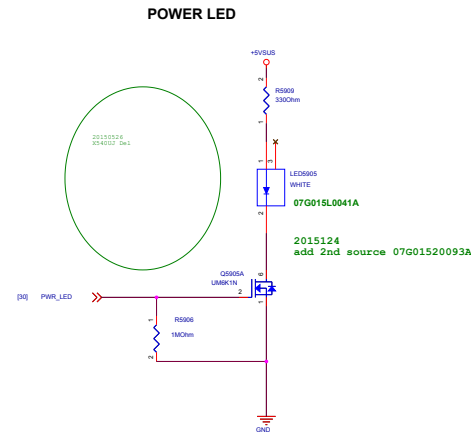
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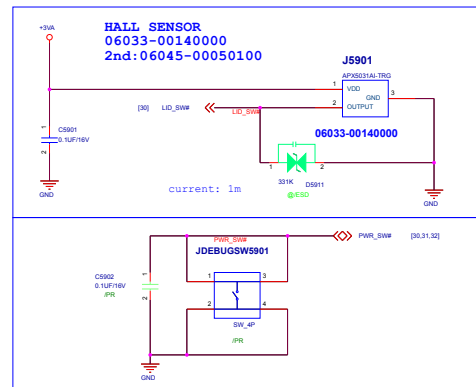
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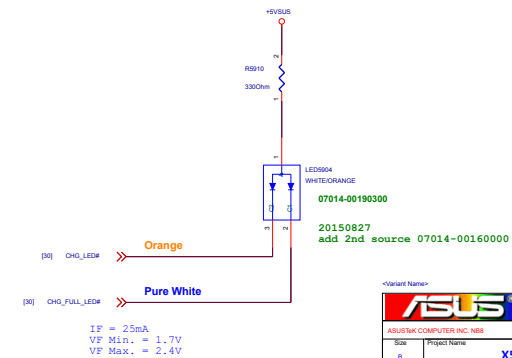


WIRELESS/ BT LED

CAP Lock LED



LED indicator
Charger LED



		Title : R1_Power & WIFI & CAP LED	
ASUSTeK COMPUTER INC. NBS		Engineer: NBS_EE2	
Size	Project Name	Rev	
6	XS40LJ&LA	R1.0	
Date: Thursday, September 01, 2016		Printed	01 of 02

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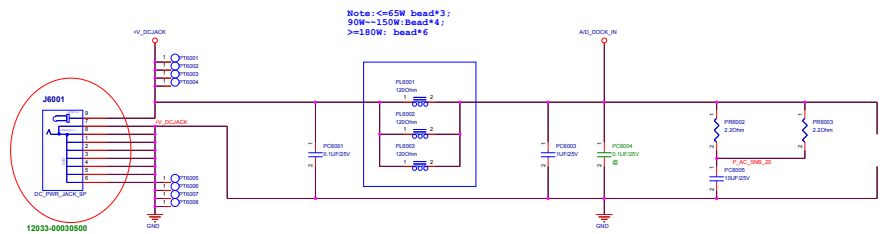
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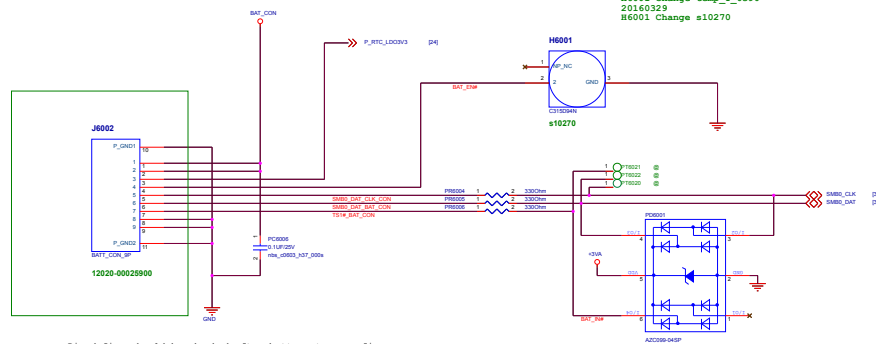
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換Connector 整個 GND shape 影響到+2A線路起承

Battery Connector



Pin define should be checked after battery team confirm

Pin Seq.	Name	Description	Remark
1	P+	Battery pack positive terminal	Output voltage
2	P+	Battery pack positive terminal	Output voltage
3	LDO 3.3V		
4	EN#	External charge & discharge Mosfet control pin.	SYSTEM Connection to GND for charge & discharge
5	SMBC	Serial clock input	SMBC
6	SMBD	Serial data input	SMBD
7	BAT_IN#	EC detect battery_in pin	PACK inside 0 Ω connect to GND
8	P-	Battery pack negative terminal.	GND
9	P-	Battery pack negative terminal.	GND

*Insert Name

ASUS		Title :	60_DC-DC & BAT IN
ASUSTeK COMPUTER INC.		Engineer :	SS
Size	Project Name	X541	Rev:
01			001
Date: Thursday, September 01, 2016			
	Print	60	of 60

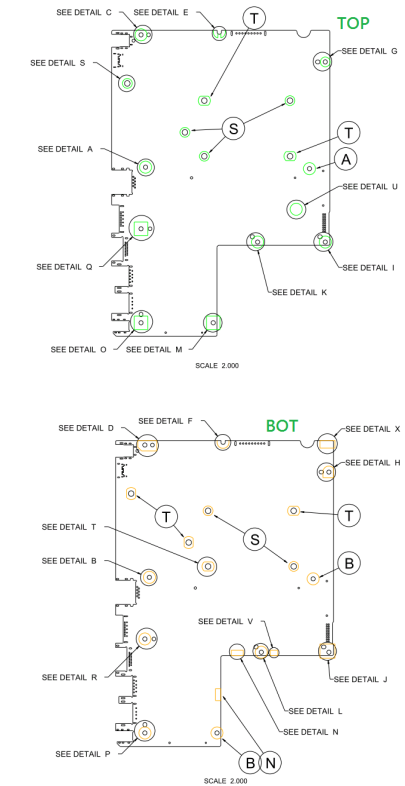
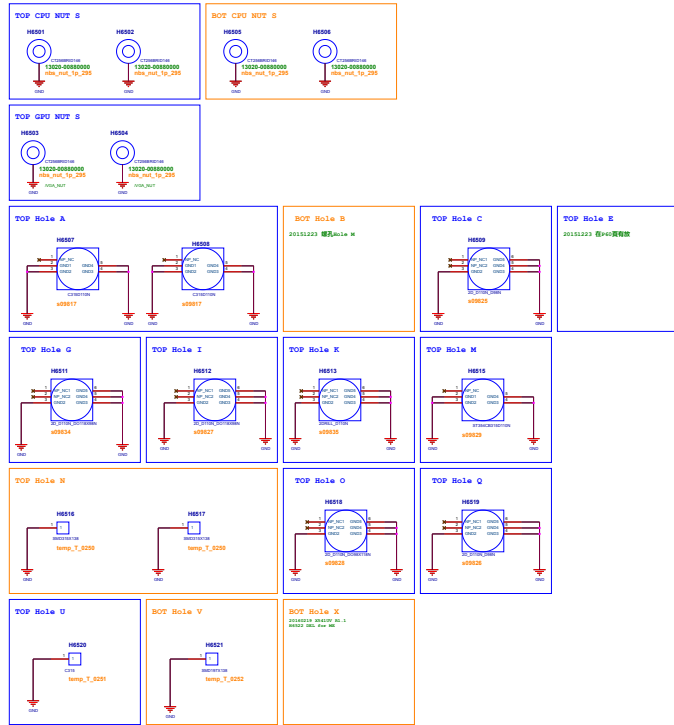
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ASUS		Title: H4_MH_Conn & Bata Hole
Project No: 00000000000000000000		Engineer: NBY_B22
Date: 2015-12-23 10:00:00		Project: XS40L1BLA
Rev: 1		Sheet: 1 of 1

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- 059_Power & WIFI & CAP LED&LI
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- 060_DC_DC & BAT IN
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- 063_
- 064_
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- 066_
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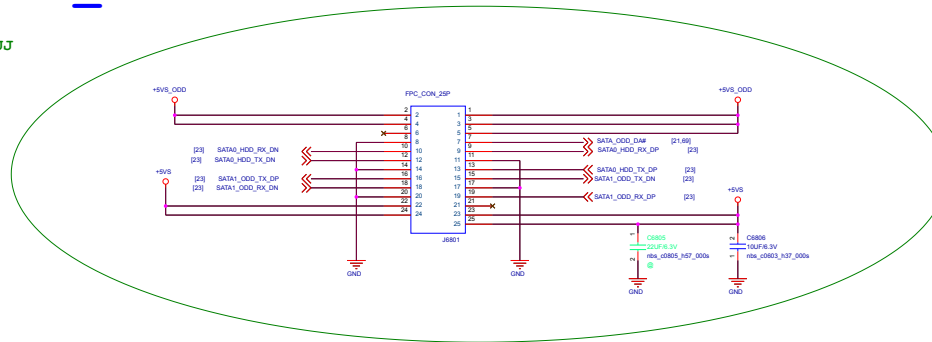
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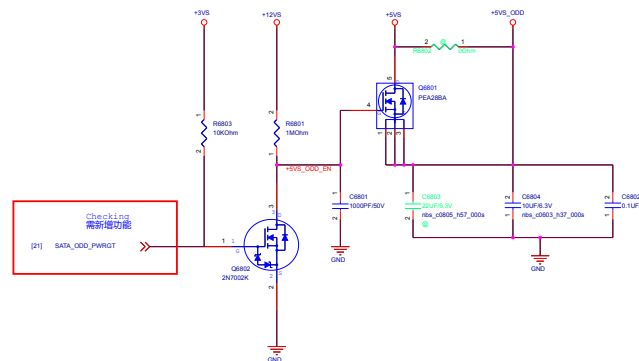
MB to HDD_B

MB端 (MB to HDD_B)

20150520 X540UJ



20160630 X541UAK/UVK follow X441 change FPC Connector



ASUS X540UV/UA		Rev: 01.0
Title: B TO B CONNECTOR		
Size: 8	Dept: ASUS/TK COMPUTER, INC.	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet: 08	of 09

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- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPL AY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWE R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

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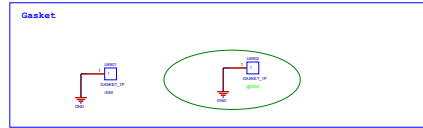
069

Toggle FullScreen

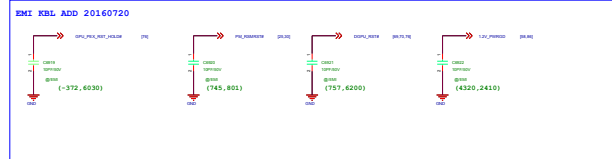
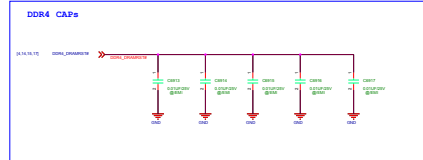
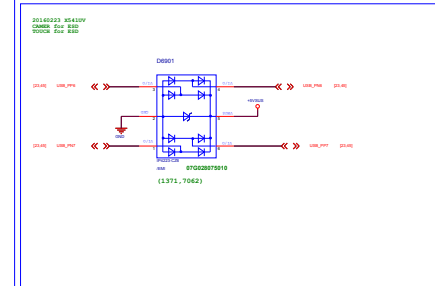
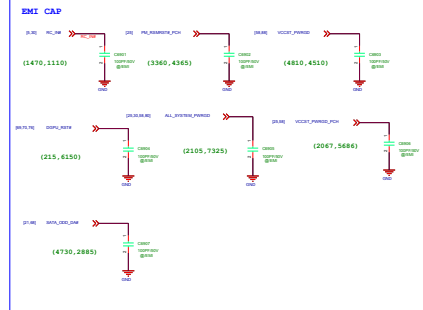
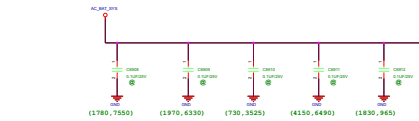
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- 080_PW_SKYLAKE-U (1)
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- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

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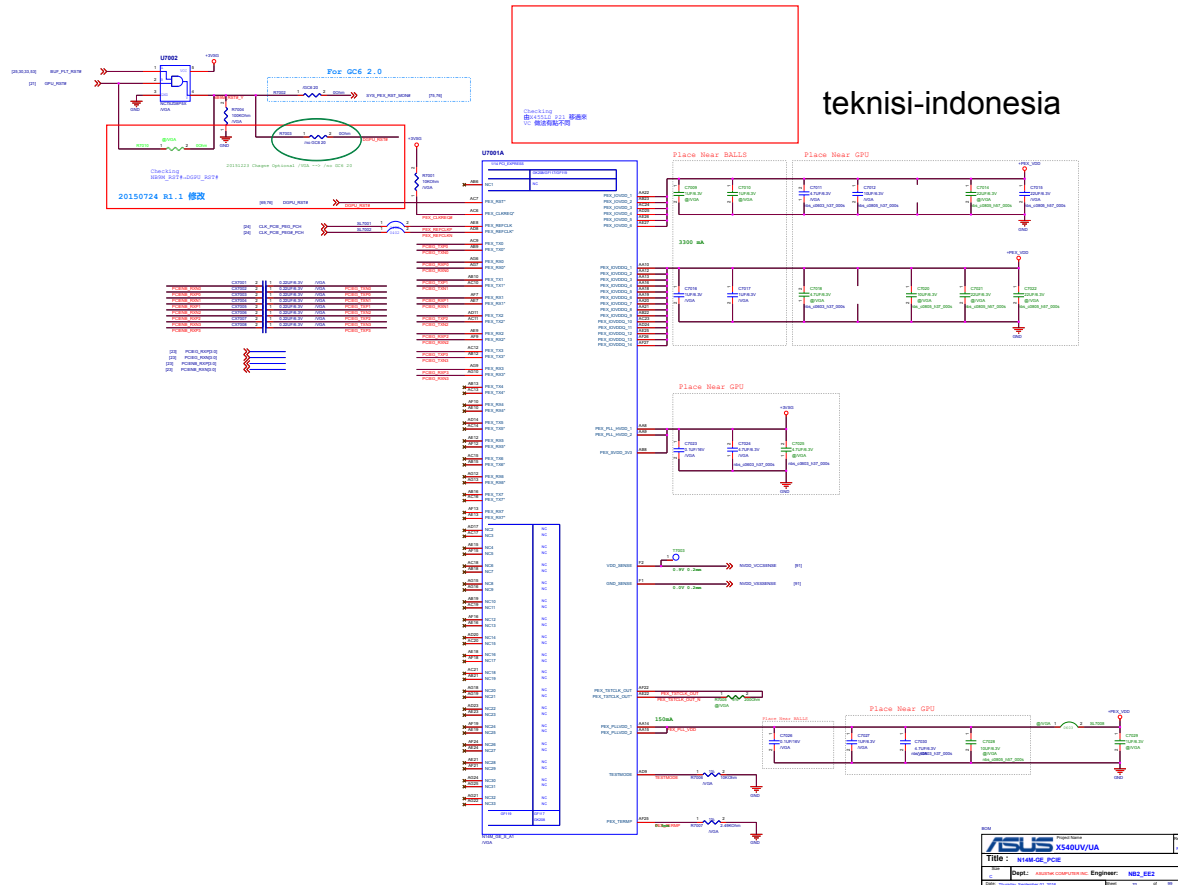
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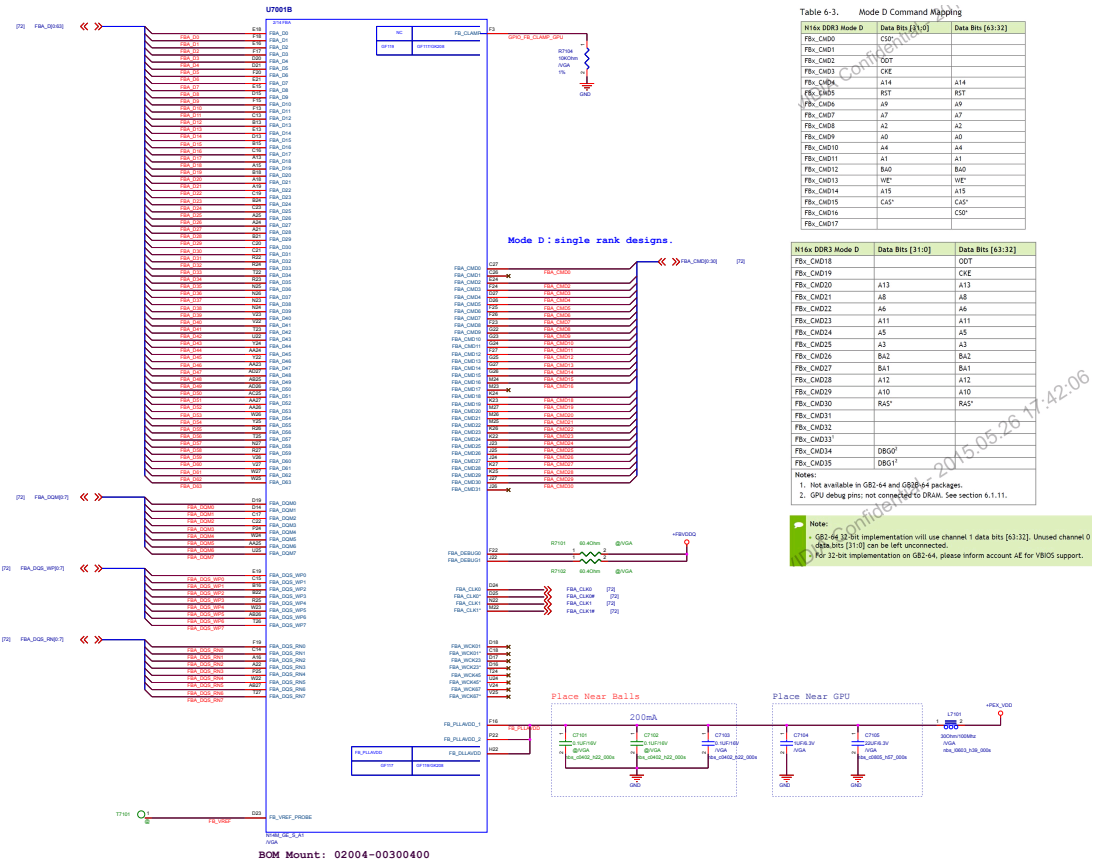


Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [3:10]	Data Bits [63:32]
FB_CSD00	C50	
FB_CSD01	C51	
FB_CSD02	CKE	
FB_CSD03	CKE	
FB_CSD04	A14	A14
FB_CSD05	A15	A15
FB_CSD06	A9	A9
FB_CSD07	A7	A7
FB_CSD08	A2	A2
FB_CSD09	A0	A0
FB_CSD10	A4	A4
FB_CSD11	A1	A1
FB_CSD12	BA0	BA0
FB_CSD13	WE*	WE*
FB_CSD14	A15	A15
FB_CSD15	CS*	CS*
FB_CSD16	CS*	CS*
FB_CSD17		

N16x DDR3 Mode D

Data Bits [3:10]	Data Bits [63:32]
FB_CSD18	ODT
FB_CSD19	CKE
FB_CSD20	A13
FB_CSD21	A8
FB_CSD22	A6
FB_CSD23	A11
FB_CSD24	A5
FB_CSD25	A3
FB_CSD26	BA2
FB_CSD27	BA1
FB_CSD28	A12
FB_CSD29	A10
FB_CSD30	RA5*
FB_CSD31	
FB_CSD32	
FB_CSD33	
FB_CSD34	DBG0*
FB_CSD35	DBG1*

Note:
 1. Not available in G82-64 and G82-64 packages.
 2. GPU debug pins: not connected to DRAM. See section 6.1.11.
 * Note: G82-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel 0 data bits [3:10] can be left unconnected.
 * For 32-bit implementation on G82-64, please inform account AE for VBIOS support.

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- 072_VGA_nVIDIA_N16V/S_FB-DD R3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

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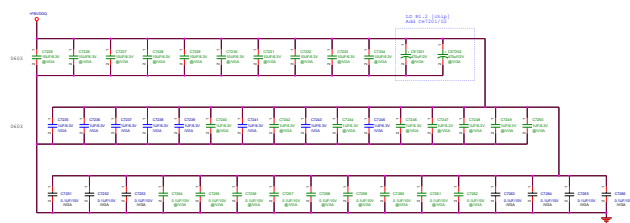
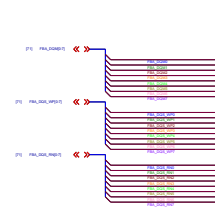
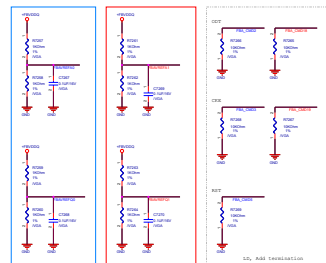
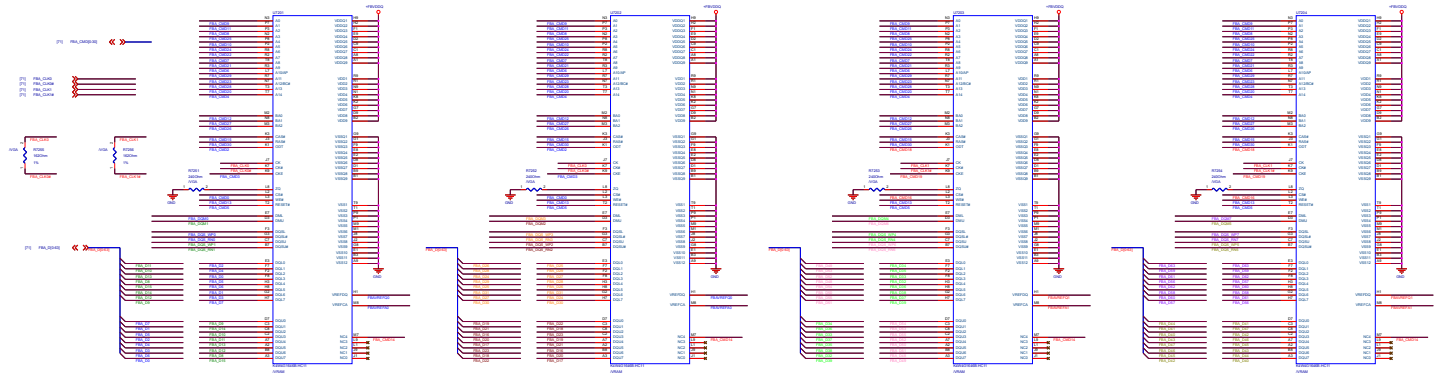
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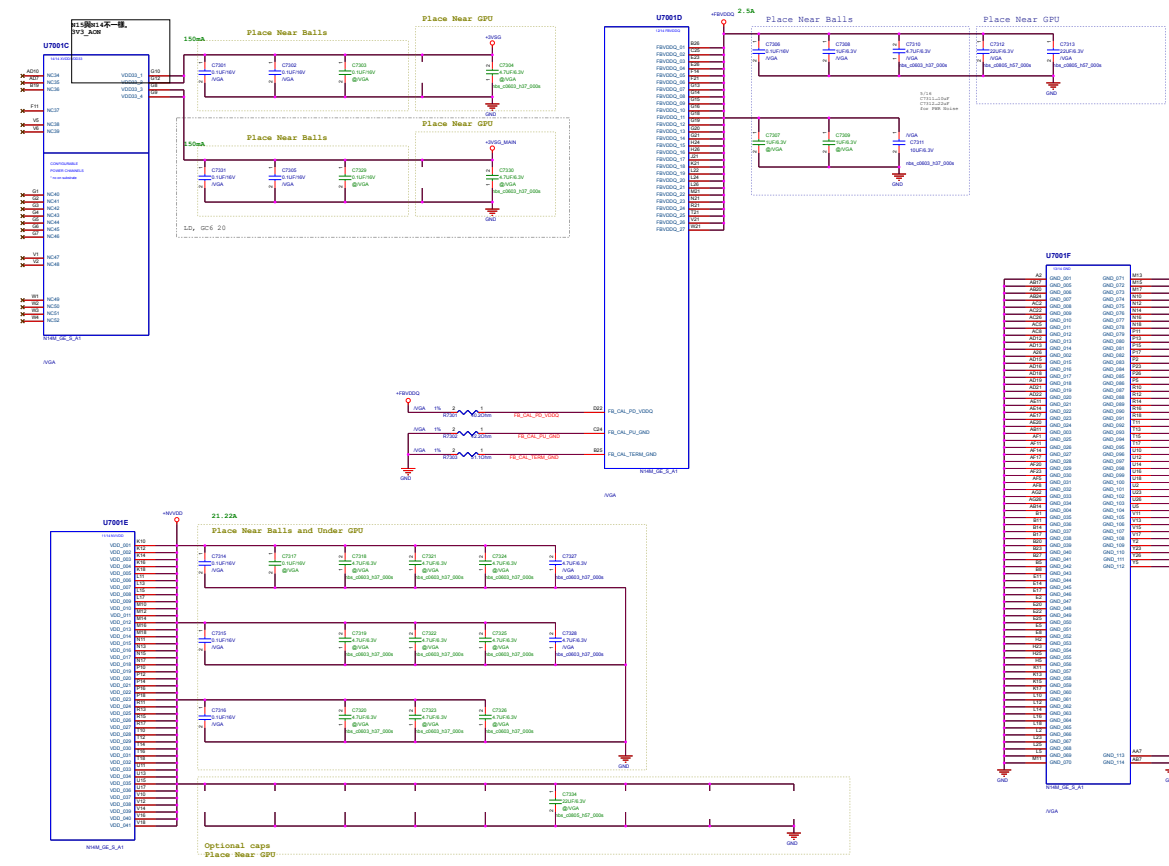
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- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

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- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
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- 079_VGA_****
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- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
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- 087_PW_+3VADSW/+5VSUS

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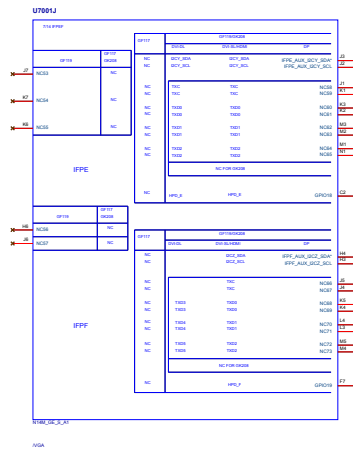
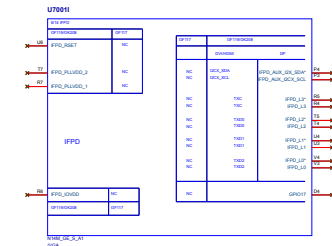
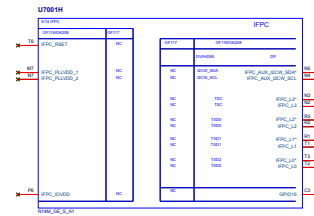
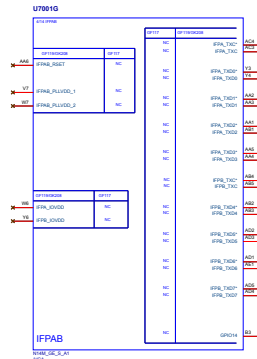
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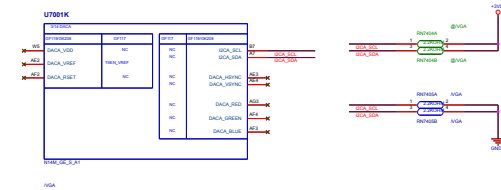
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- 072_VGA_nVIDIA_N16V/S_FB-DD R3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
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- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

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Table 15-1. HW Config and HW Config-DB Data Reconciliation

Item	Name	Type	Value	Unit	Comment
15.5.13	SRM_EXPOSED	SRM	0		SRM exposed to system
15.5.14	SRM_EXPOSED	SRM	1		SRM exposed to system

Table 15-3. GDR3-64, GDR3-128 and GDR3-256 Multi-Level Mode Mapping

Strap Pin	Logical Strapping	Physical Strapping	Logical Strapping	Physical Strapping
SRM0	SRM0	SRM0	SRM0	SRM0
SRM1	SRM1	SRM1	SRM1	SRM1

Table 15-2. Resistance Mapping to Hex Values

Resistor Value	Pull-up to VYD_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
40.3 kΩ	1111	0111

Size	Part Number	Strap	ROM Size
328x450 (2GS)	03B07-00030400	GDDR3 128M*16 1.35V FBGA-96	MIKROW/MT41128M1611-093G-K
256x450 (4GS)	03B07-00021100	GDDR3 256M*16 1.35V FBGA96	HYNIXH1T4G6G3CR-NDC
	03B07-00021300	GDDR3 256M*16 1.35V FBGA96	MIKROW/MT41256M16V1-091G-N

15.5.13 SRM_EXPOSED Strap
This strap controls the SRM exposed to the system. SRM0 and SRM1 are SRM exposed to the system. SRM0 and SRM1 are SRM exposed to the system.

15.5.14 DEV0_SEL Strap
This strap controls the device selection for the system. SRM0 and SRM1 are SRM exposed to the system.

15.5.15 PCIE_CFG Strap
This strap controls the PCIe configuration for the system. SRM0 and SRM1 are SRM exposed to the system.

15.5.6 SRM_EXPOSED Strap
This strap controls the SRM exposed to the system. SRM0 and SRM1 are SRM exposed to the system.

15.5.5 VGA_DEVICE Strap
This strap controls the VGA device selection for the system. SRM0 and SRM1 are SRM exposed to the system.

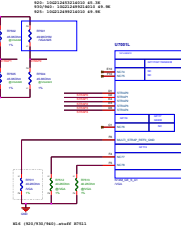
15.5.13 SRM_EXPOSED Strap
This strap controls the SRM exposed to the system. SRM0 and SRM1 are SRM exposed to the system.

15.5.14 DEV0_SEL Strap
This strap controls the device selection for the system. SRM0 and SRM1 are SRM exposed to the system.

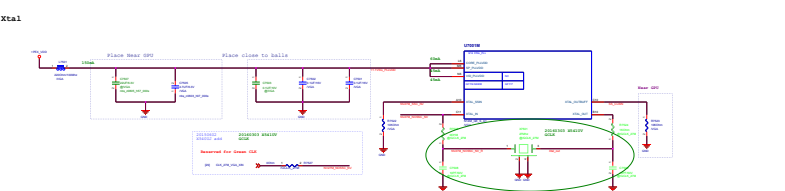
15.5.15 PCIE_CFG Strap
This strap controls the PCIe configuration for the system. SRM0 and SRM1 are SRM exposed to the system.

15.5.6 SRM_EXPOSED Strap
This strap controls the SRM exposed to the system. SRM0 and SRM1 are SRM exposed to the system.

15.5.5 VGA_DEVICE Strap
This strap controls the VGA device selection for the system. SRM0 and SRM1 are SRM exposed to the system.



VG_B04 輸入主料規格號碼End Source
4.99k = 10221249114010
10.0k = 10221250144010
15.0k = 10221251174010
20.0k = 10221252204010
24.9k = 10221253234010
30.1k = 10221254264010
34.8k = 10221255294010
40.3k = 10221256324010



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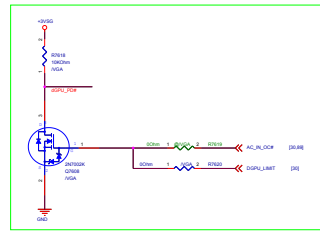
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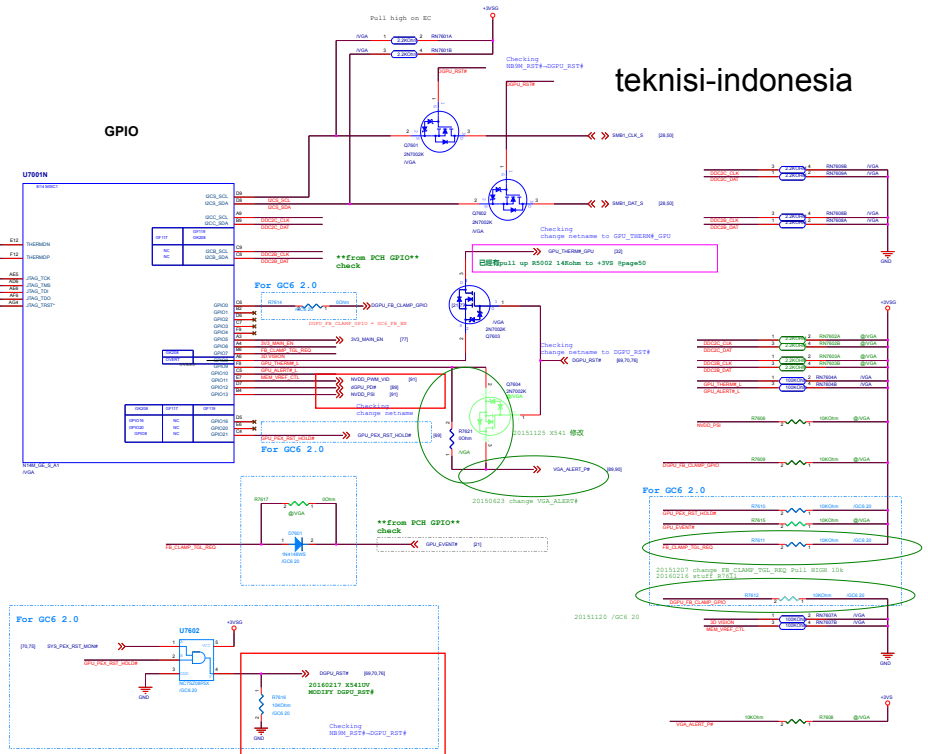
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Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	ID	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_ADRH	I	FB Clamp monitor for GC6 1.0	10K pull-down to GND
GPIO1	GC6_FB_EH	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VDD	MEM_VDD: pull-up to 3V3_ADRH or pull-down to GND for self boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100K pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_IAMN_EH	O	GPU power hobbling	10K pull-up to 3V3_ADRH
GPIO6	FB_CLAMP_VGL_REQ	O	Clamp/Enable request for GC6 1.0	10K pull-up to system 3.3V
GPIO6	GPU_EVENTH	I	GPU vlink signal for GC6 2.0	10K pull-up to 3V3_ADRH
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	3V3_PCH_RST_ADRH	I	System side PCH reset monitor	100K pull-down
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_ADRH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWAL_VDD	O	GPU Core VDD PWM control signal	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_ADRH
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_ADRH to enable line share
GPIO14	HPO_A	I	Hot Plug Detect for HPA used as DisplayPort or for HPA when used as Dual Link DVI	See Figure 12-1
GPIO15	HPO_C	I	Hot Plug Detect for HPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPO_D	I	Hot Plug Detect for HPD	See Figure 12-1
GPIO18	HPO_E	I	Hot Plug Detect for HPE	See Figure 12-1
GPIO19	HPO_F or HPO_B	I	Hot Plug Detect for HFF or for HFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PCH_RST_NHLDW	O	GPU PCH soft reset control	10K pull-up to 3V3_ADRH
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_ADRH



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- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DD R3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

Global Search

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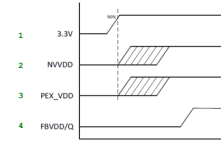
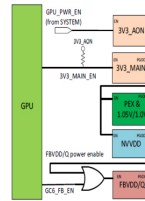
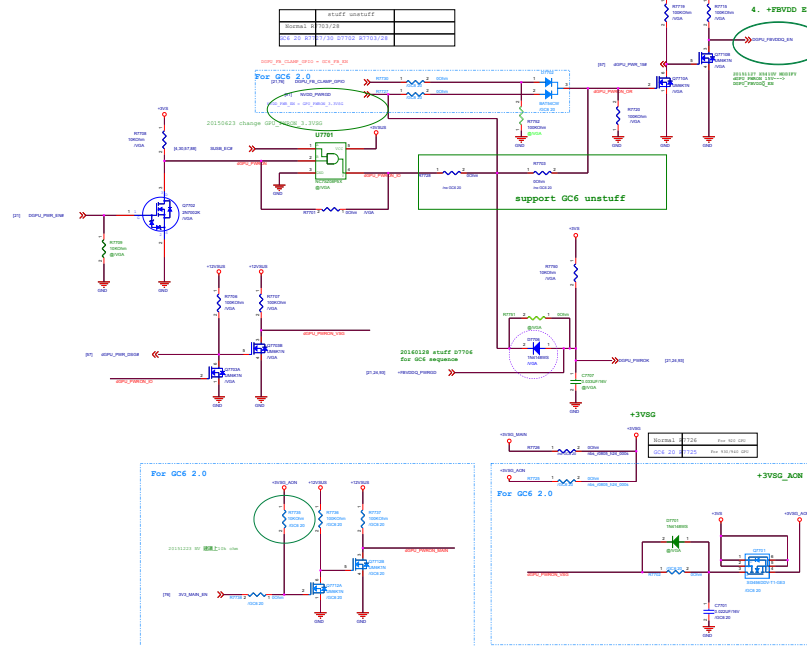
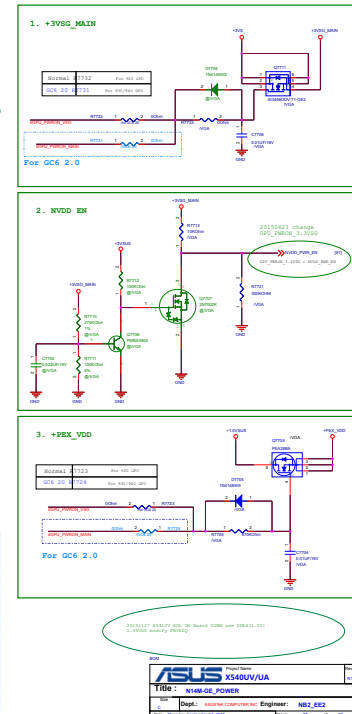


Figure 3-7. Example of Power-Up Sequencing Order

dGPU IO Power Sequence



dGPU Core Power Sequence



Schematic Page List

Hide

- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DD R3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

Global Search

081

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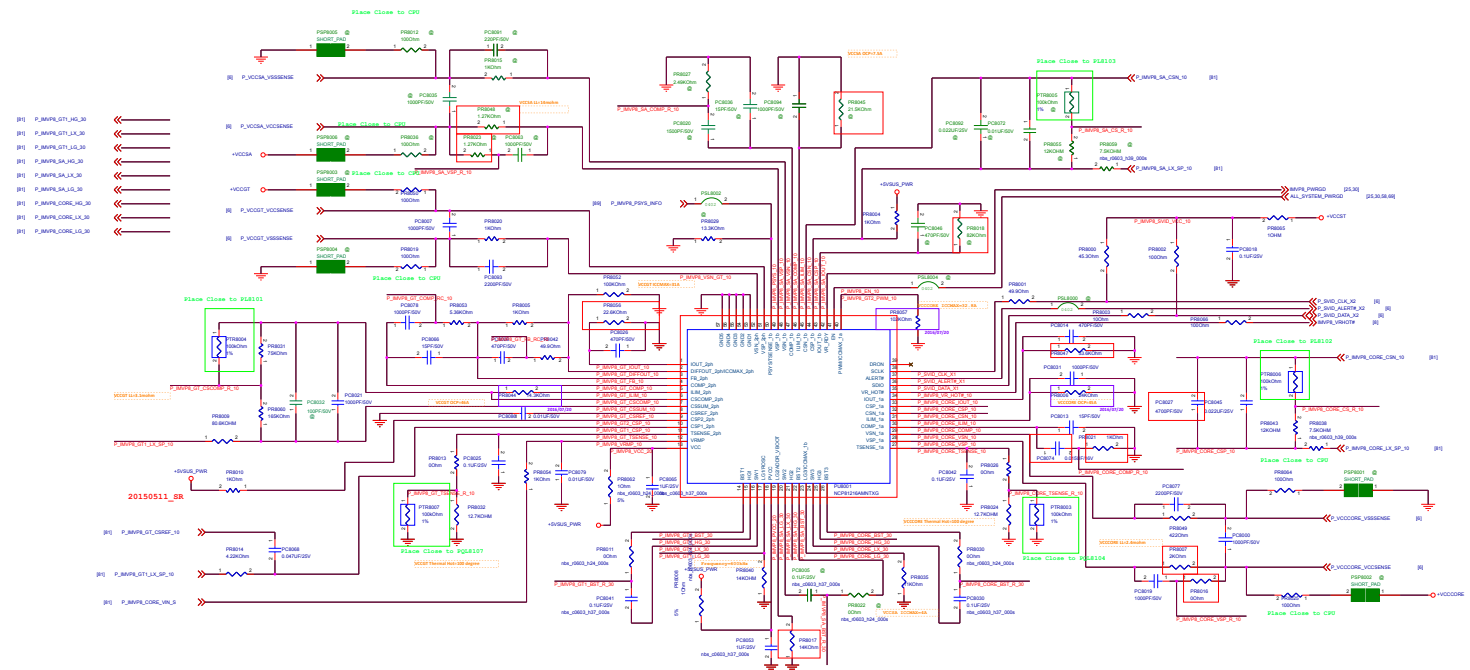
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Skylake IMVP8 (1) Power [For CPU]



Schematic Page List

Hide

- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DD R3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

Global Search

081

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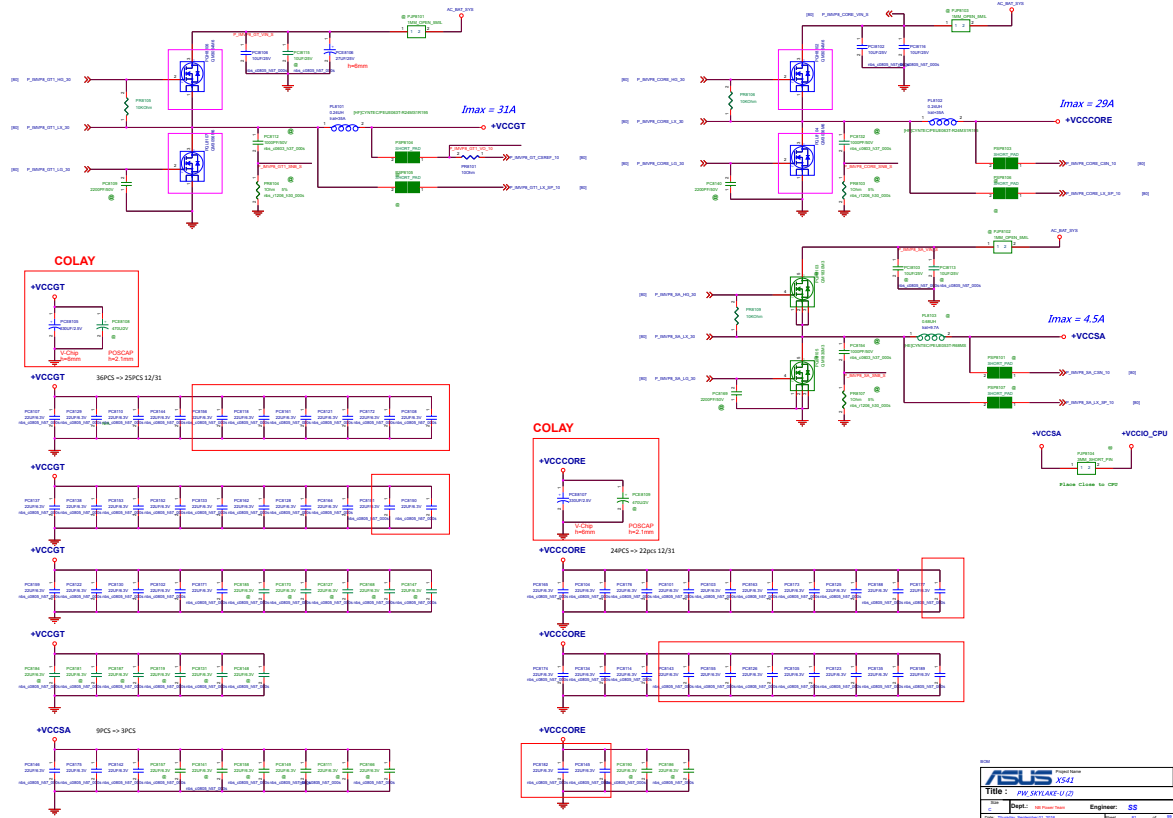
Toggle FullScreen

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MoveTo

Skylake IMVP8 Power (2) [For CPU]



ASUS	Product Name	X541
TITLE: PW_SKYLAKE-U (2)		
Rev	Author	Engineer: SS
1.0	1.0	1.0

Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

Global Search

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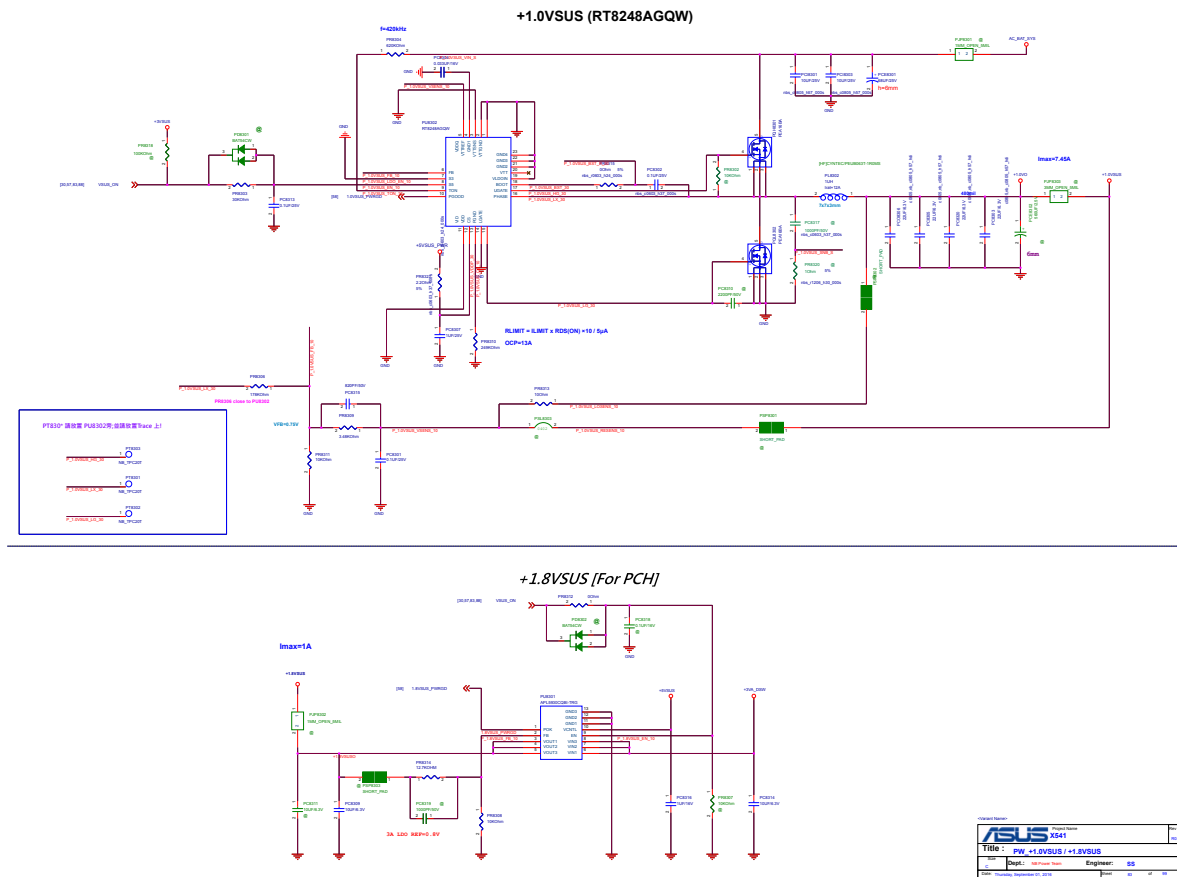
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Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

Global Search

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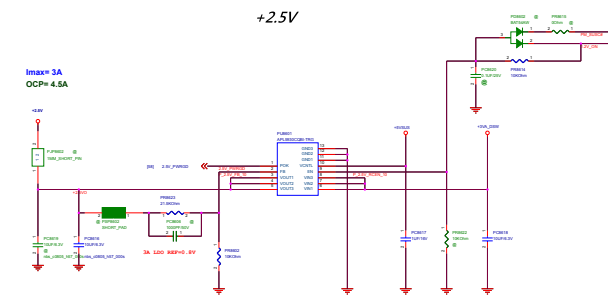
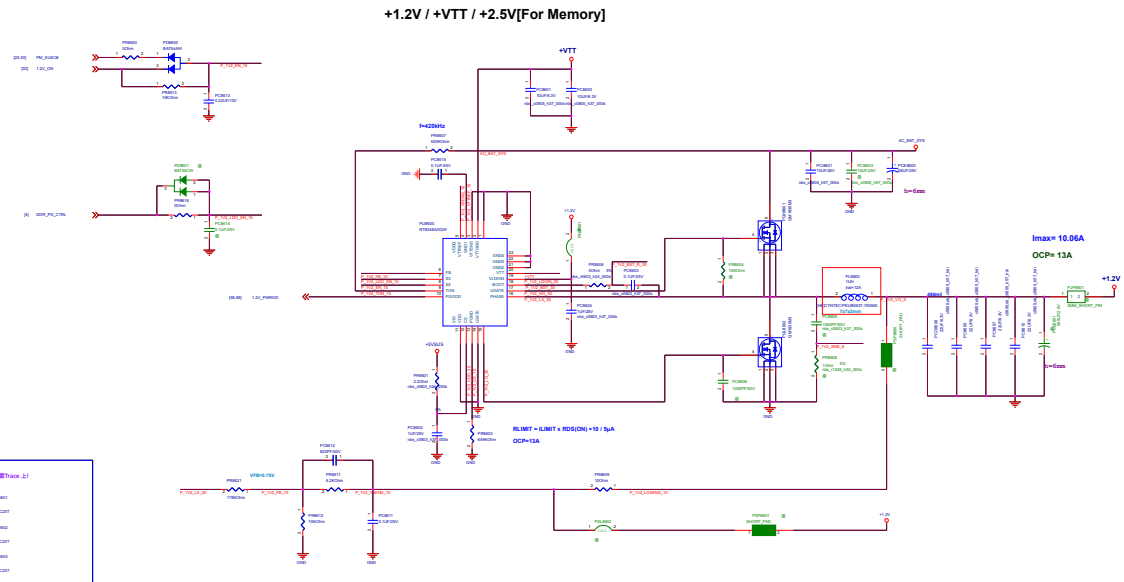
083

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Client Design	Project Name	Rev
ASUS	X541	01
Title	PW_+1.2V/+VTT/+2.5V	
Dep't	Hardware	Engineer: SS

Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

Global Search

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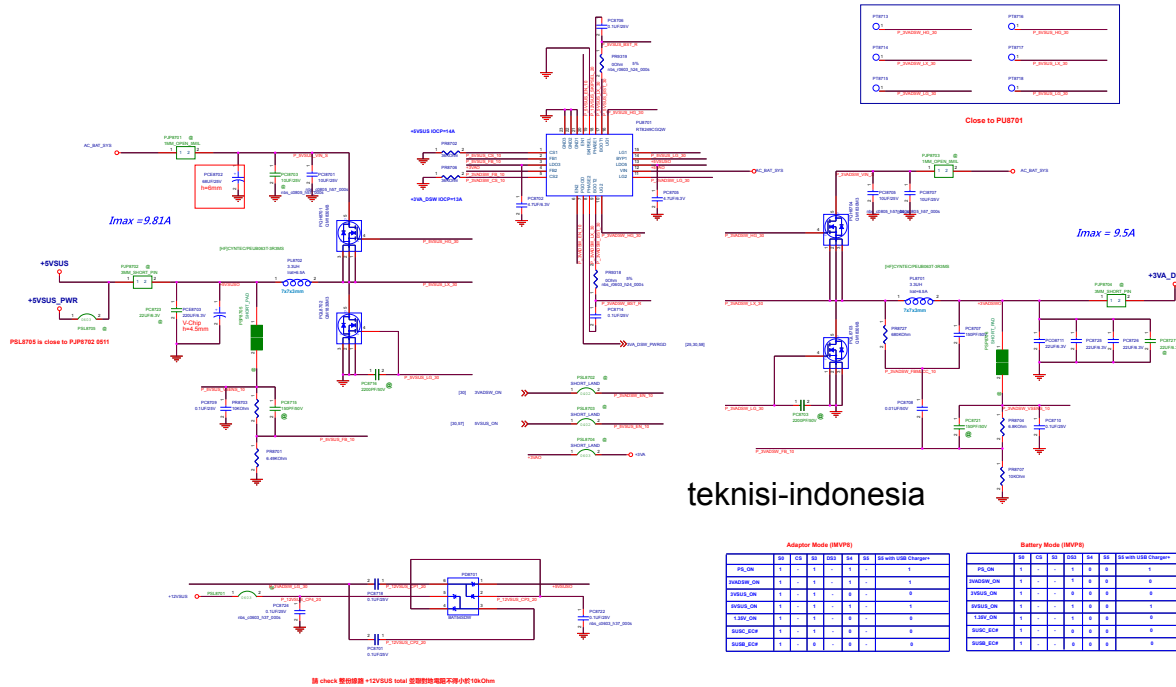
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+3VA_DSW / +5VSUS [System Power]



Close to PMP8701

teknisi-indonesia

Adaptor Mode (MVP5)

	B1	B2	B3	B4	B5	B6 with USB Charger
PLDN_ON	1	1	1	1	1	1
PLDNW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1

Battery Mode (MVP5)

	B1	B2	B3	B4	B5	B6 with USB Charger
PLDN_ON	1	1	1	1	1	1
PLDNW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1
PSUSW_ON	1	1	1	1	1	1

請 check 輸出總電 +12VSUS total 變壓器輸出電不準小於10A0m



ASUS Logo and Project Information:

Project Name: PMP8701

File: PMP_088_DSW/+5VSUS

Design: SS

Version: 1.0

Date: 2018/07/12

Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

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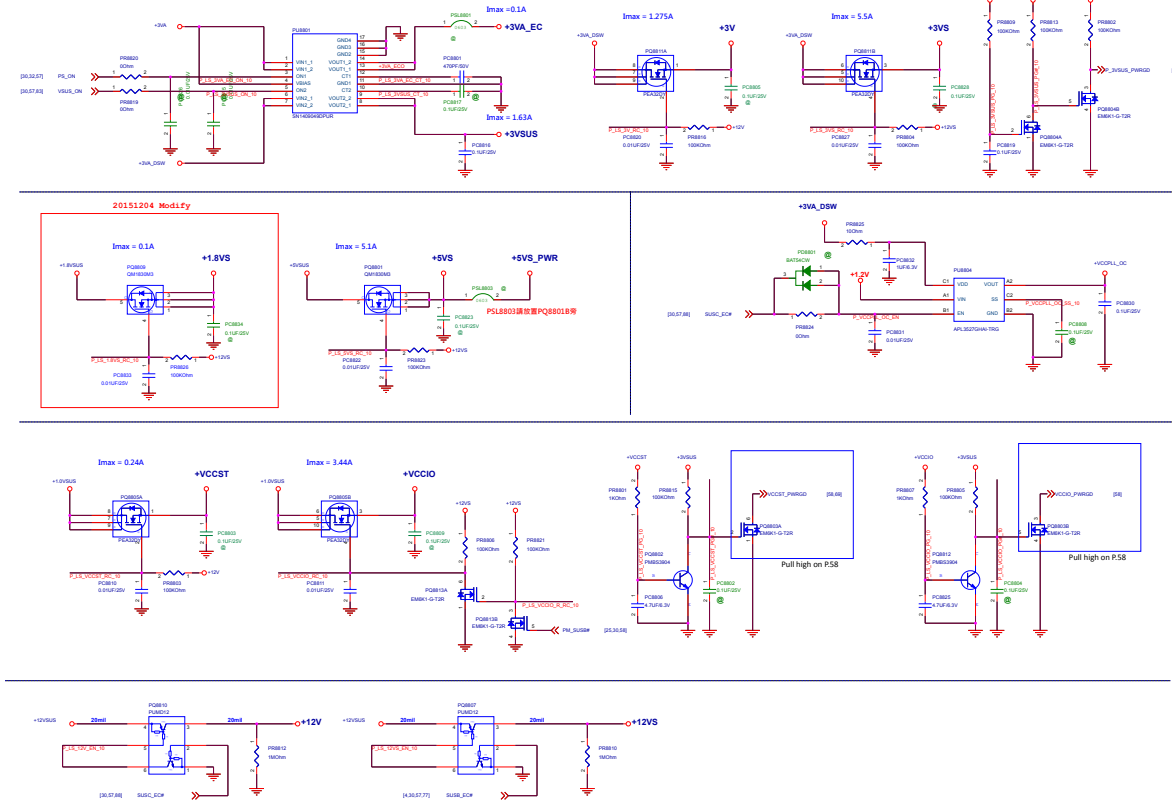
Toggle FullScreen

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Load Switch



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Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

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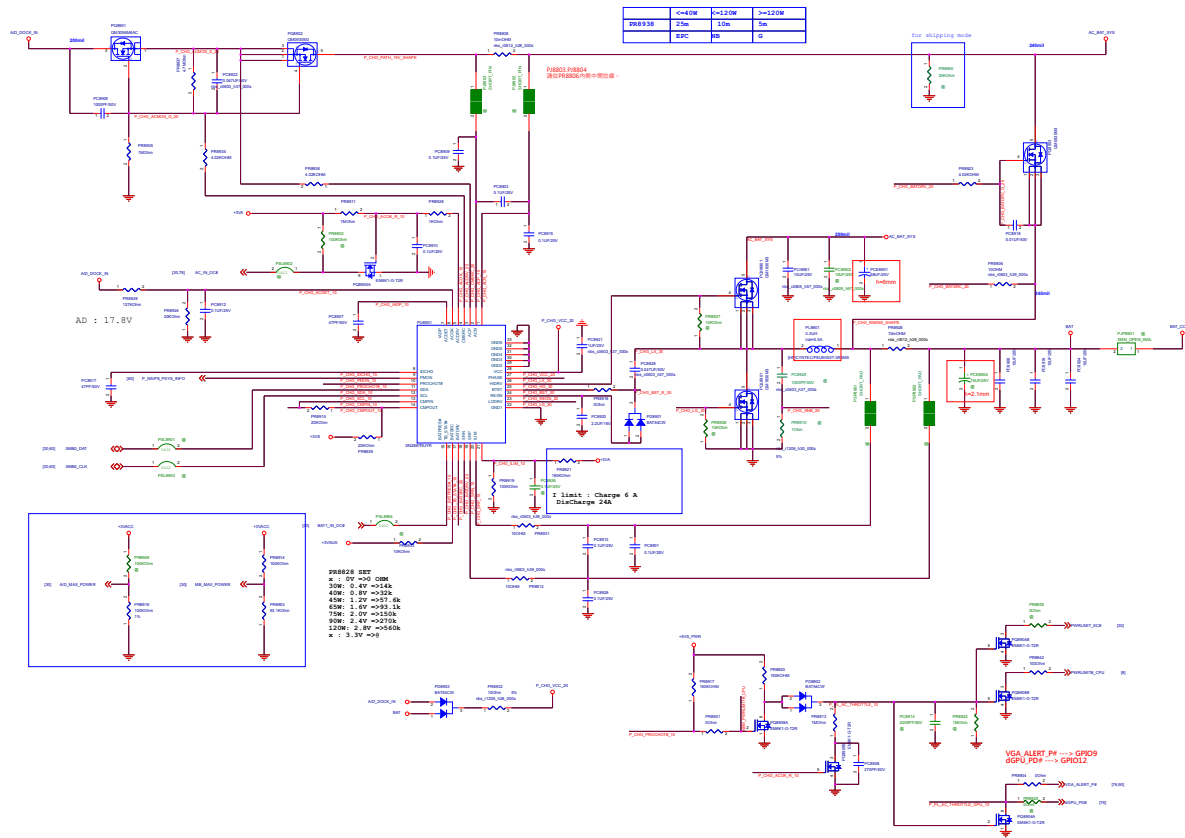
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Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

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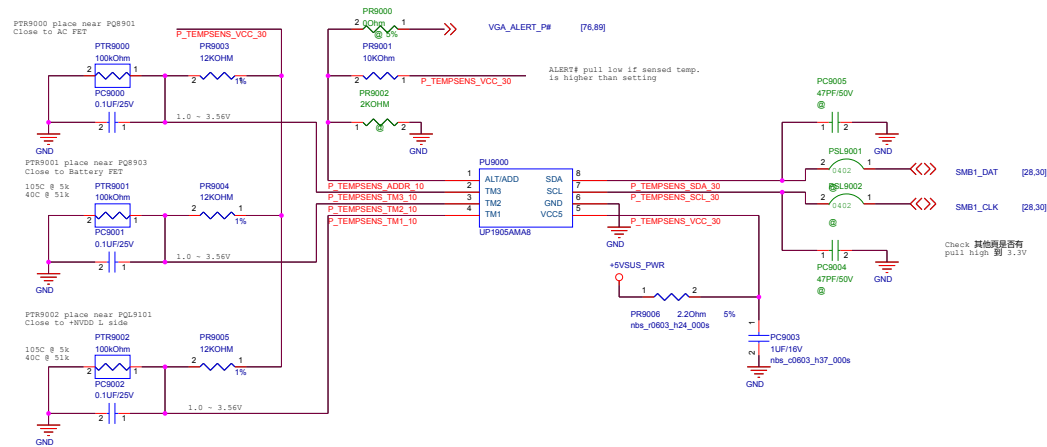
MoveTo

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	0.2k	0.2k	0.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



<Variant Name>

Project Name		Rev
ASUS X541		R0.1
Title : PW_PROTECTION		
Size	Dept.: NB Power Team	Engineer: SS
Date: Thursday, September 01, 2016	Sheet	90 of 102

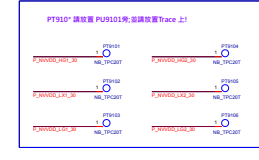
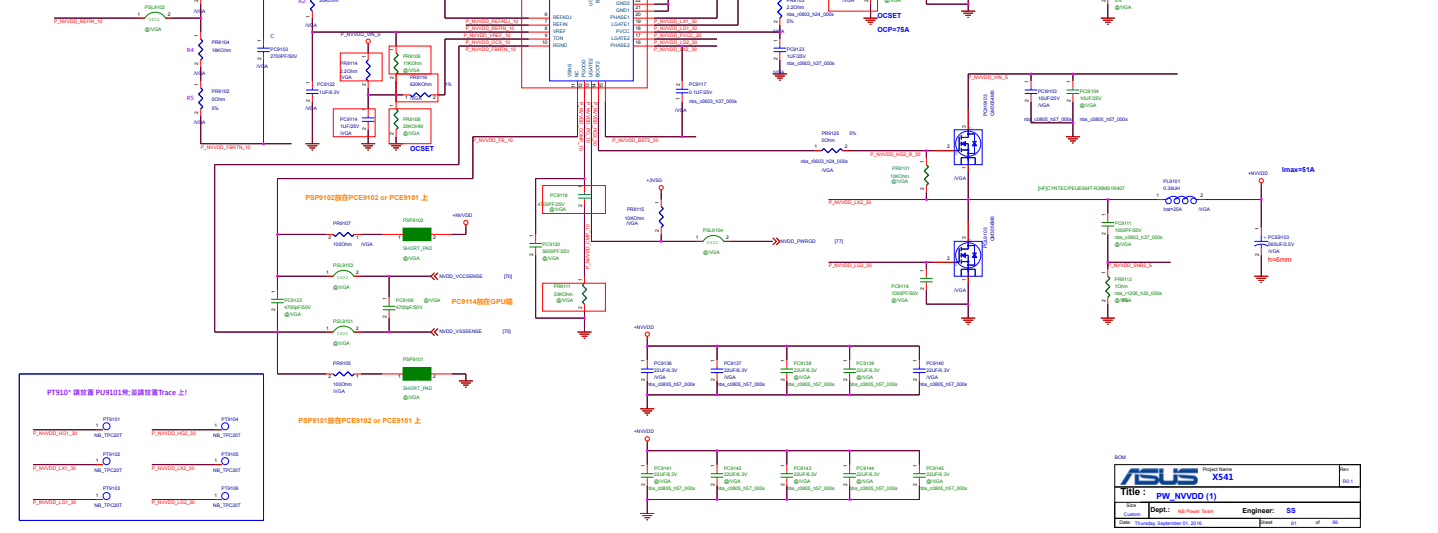
Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

PRM-VDD_Spec

	MODE A	MODE B	MODE C	MODE D
P1 (V)	1.0	1.0	1.0	1.0
P2 (V)	1.0	1.0	1.0	1.0
P3 (V)	1.0	1.0	1.0	1.0
P4 (V)	1.0	1.0	1.0	1.0
P5 (V)	1.0	1.0	1.0	1.0
P6 (V)	1.0	1.0	1.0	1.0
P7 (V)	1.0	1.0	1.0	1.0
P8 (V)	1.0	1.0	1.0	1.0
P9 (V)	1.0	1.0	1.0	1.0
P10 (V)	1.0	1.0	1.0	1.0
P11 (V)	1.0	1.0	1.0	1.0
P12 (V)	1.0	1.0	1.0	1.0
P13 (V)	1.0	1.0	1.0	1.0
P14 (V)	1.0	1.0	1.0	1.0
P15 (V)	1.0	1.0	1.0	1.0
P16 (V)	1.0	1.0	1.0	1.0
P17 (V)	1.0	1.0	1.0	1.0
P18 (V)	1.0	1.0	1.0	1.0
P19 (V)	1.0	1.0	1.0	1.0
P20 (V)	1.0	1.0	1.0	1.0
P21 (V)	1.0	1.0	1.0	1.0
P22 (V)	1.0	1.0	1.0	1.0
P23 (V)	1.0	1.0	1.0	1.0
P24 (V)	1.0	1.0	1.0	1.0
P25 (V)	1.0	1.0	1.0	1.0
P26 (V)	1.0	1.0	1.0	1.0
P27 (V)	1.0	1.0	1.0	1.0
P28 (V)	1.0	1.0	1.0	1.0
P29 (V)	1.0	1.0	1.0	1.0
P30 (V)	1.0	1.0	1.0	1.0
P31 (V)	1.0	1.0	1.0	1.0
P32 (V)	1.0	1.0	1.0	1.0
P33 (V)	1.0	1.0	1.0	1.0
P34 (V)	1.0	1.0	1.0	1.0
P35 (V)	1.0	1.0	1.0	1.0
P36 (V)	1.0	1.0	1.0	1.0
P37 (V)	1.0	1.0	1.0	1.0
P38 (V)	1.0	1.0	1.0	1.0
P39 (V)	1.0	1.0	1.0	1.0
P40 (V)	1.0	1.0	1.0	1.0
P41 (V)	1.0	1.0	1.0	1.0
P42 (V)	1.0	1.0	1.0	1.0
P43 (V)	1.0	1.0	1.0	1.0
P44 (V)	1.0	1.0	1.0	1.0
P45 (V)	1.0	1.0	1.0	1.0
P46 (V)	1.0	1.0	1.0	1.0
P47 (V)	1.0	1.0	1.0	1.0
P48 (V)	1.0	1.0	1.0	1.0
P49 (V)	1.0	1.0	1.0	1.0
P50 (V)	1.0	1.0	1.0	1.0
P51 (V)	1.0	1.0	1.0	1.0
P52 (V)	1.0	1.0	1.0	1.0
P53 (V)	1.0	1.0	1.0	1.0
P54 (V)	1.0	1.0	1.0	1.0
P55 (V)	1.0	1.0	1.0	1.0
P56 (V)	1.0	1.0	1.0	1.0
P57 (V)	1.0	1.0	1.0	1.0
P58 (V)	1.0	1.0	1.0	1.0
P59 (V)	1.0	1.0	1.0	1.0
P60 (V)	1.0	1.0	1.0	1.0
P61 (V)	1.0	1.0	1.0	1.0
P62 (V)	1.0	1.0	1.0	1.0
P63 (V)	1.0	1.0	1.0	1.0
P64 (V)	1.0	1.0	1.0	1.0
P65 (V)	1.0	1.0	1.0	1.0
P66 (V)	1.0	1.0	1.0	1.0
P67 (V)	1.0	1.0	1.0	1.0
P68 (V)	1.0	1.0	1.0	1.0
P69 (V)	1.0	1.0	1.0	1.0
P70 (V)	1.0	1.0	1.0	1.0
P71 (V)	1.0	1.0	1.0	1.0
P72 (V)	1.0	1.0	1.0	1.0
P73 (V)	1.0	1.0	1.0	1.0
P74 (V)	1.0	1.0	1.0	1.0
P75 (V)	1.0	1.0	1.0	1.0
P76 (V)	1.0	1.0	1.0	1.0
P77 (V)	1.0	1.0	1.0	1.0
P78 (V)	1.0	1.0	1.0	1.0
P79 (V)	1.0	1.0	1.0	1.0
P80 (V)	1.0	1.0	1.0	1.0
P81 (V)	1.0	1.0	1.0	1.0
P82 (V)	1.0	1.0	1.0	1.0
P83 (V)	1.0	1.0	1.0	1.0
P84 (V)	1.0	1.0	1.0	1.0
P85 (V)	1.0	1.0	1.0	1.0
P86 (V)	1.0	1.0	1.0	1.0
P87 (V)	1.0	1.0	1.0	1.0
P88 (V)	1.0	1.0	1.0	1.0
P89 (V)	1.0	1.0	1.0	1.0
P90 (V)	1.0	1.0	1.0	1.0
P91 (V)	1.0	1.0	1.0	1.0
P92 (V)	1.0	1.0	1.0	1.0
P93 (V)	1.0	1.0	1.0	1.0
P94 (V)	1.0	1.0	1.0	1.0
P95 (V)	1.0	1.0	1.0	1.0
P96 (V)	1.0	1.0	1.0	1.0
P97 (V)	1.0	1.0	1.0	1.0
P98 (V)	1.0	1.0	1.0	1.0
P99 (V)	1.0	1.0	1.0	1.0
P100 (V)	1.0	1.0	1.0	1.0



Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

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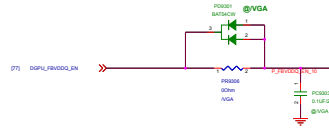
Pre Page

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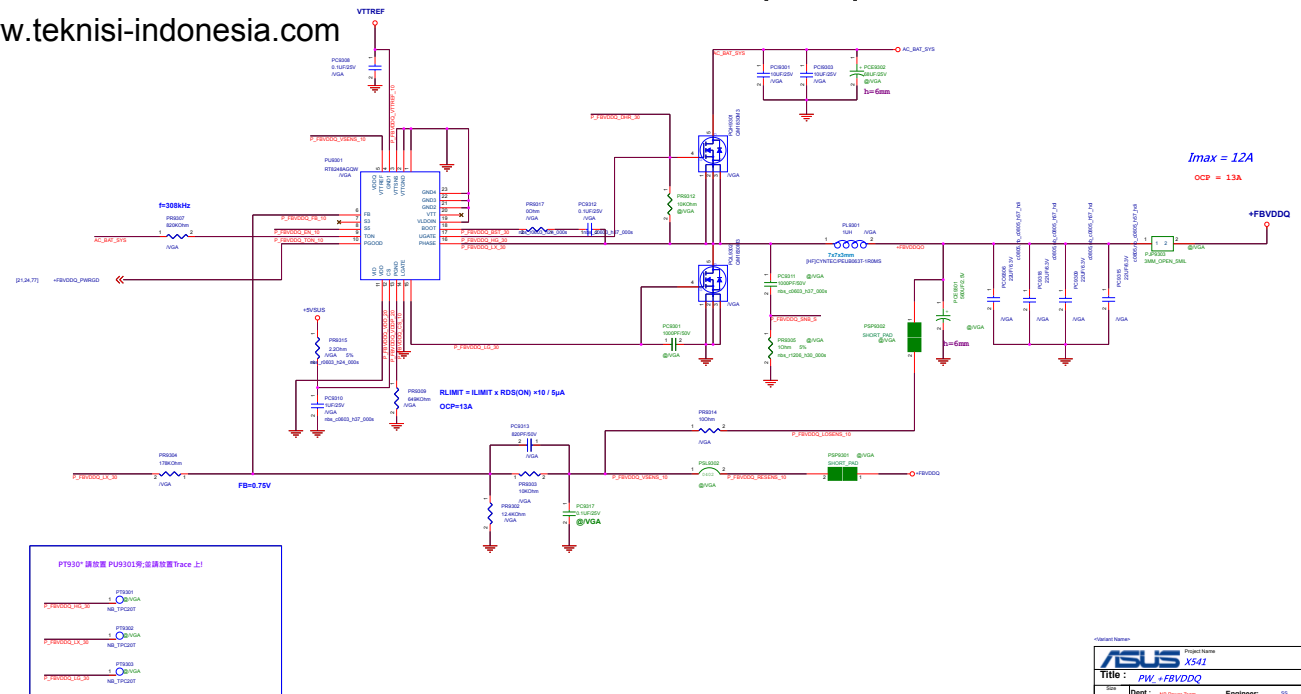
MoveTo

S3 And S6 Truth Table

State	Pin7(S3)	Pin8(S6)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)



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+FBVDDQ
[For FRAM]

I_{max} = 12A
OCP = 13A

Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
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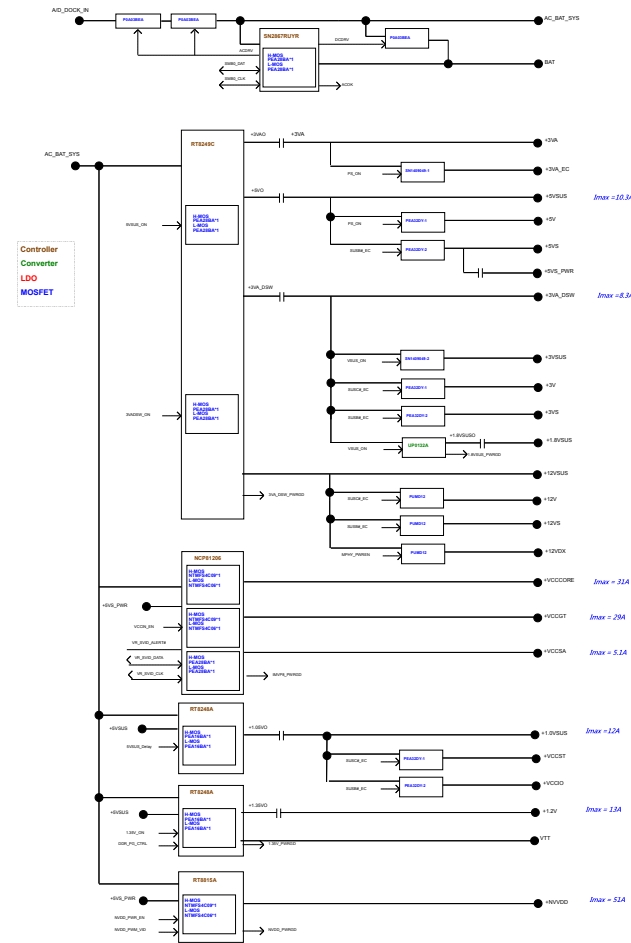
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Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
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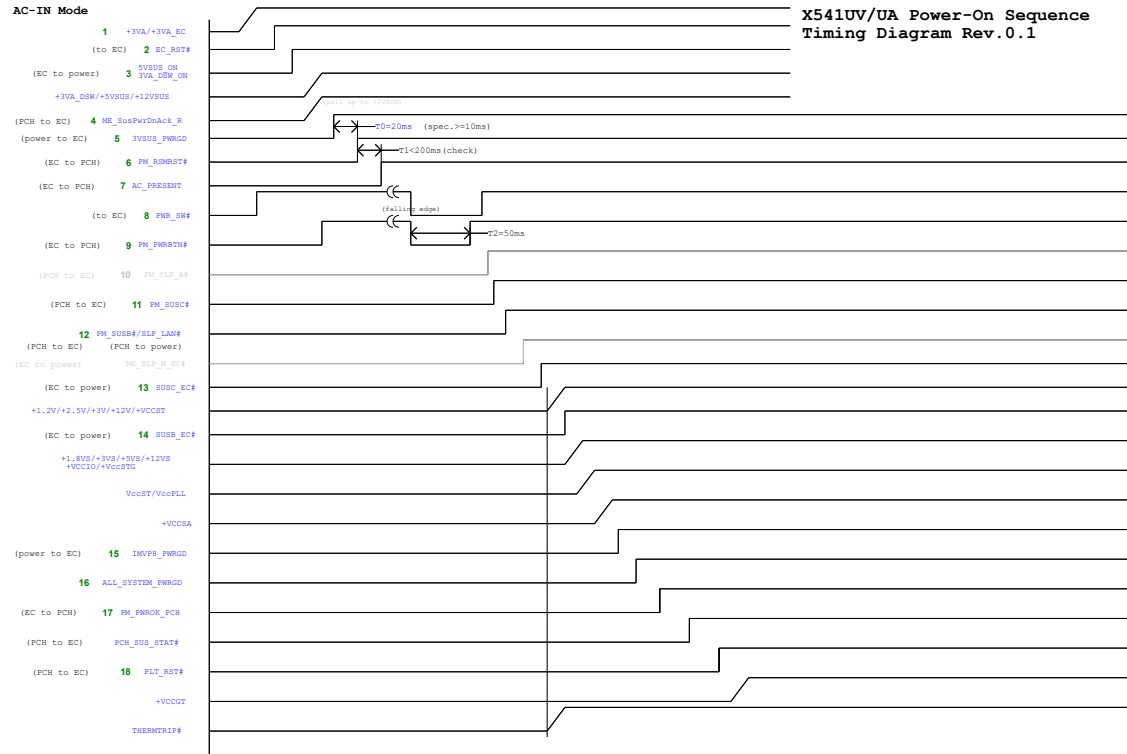
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AC-IN Mode X541UV/UA Power-On Sequence Timing Diagram Rev.0.1



Schematic Page List

Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

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Toggle FullScreen

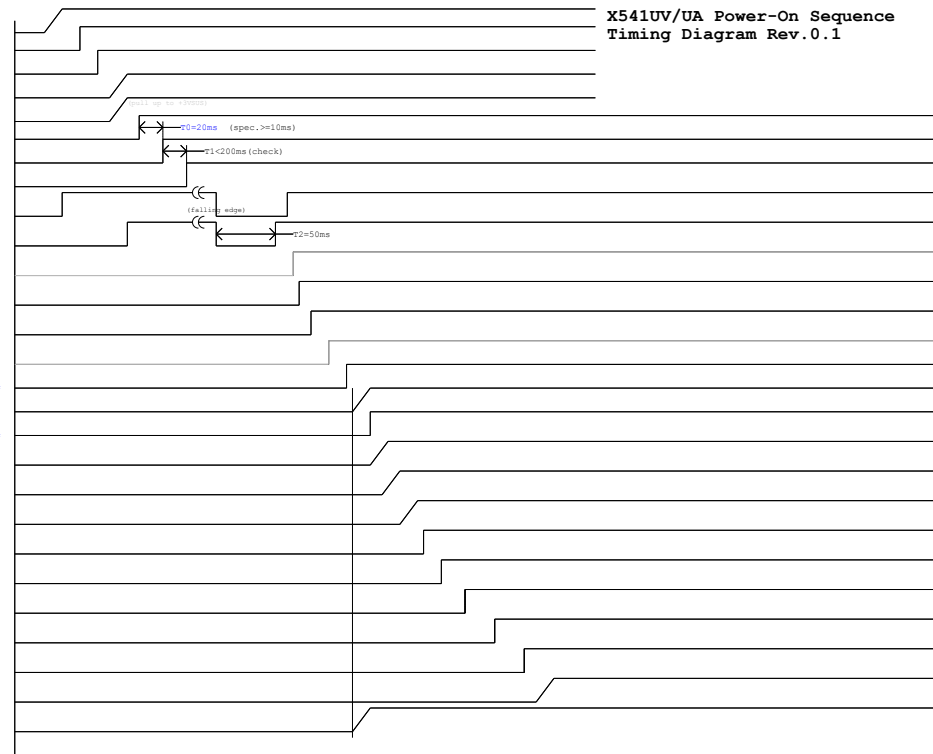
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DC-IN Mode

- 1 +3VA/+3VA_EC
- (to EC) 2 EC_RST#
- (EC to power) 3 5VSUS_ON
- +3VA_DSW/+5VSUS/+12VSUS
- (PCH to EC) 4 MR_BusPwrOnAck_R
- (power to EC) 5 3VSUS_PWRGD
- (EC to PCH) 6 PM_RMRST#
- (EC to PCH) 7 AC_PRESENT
- (to EC) 8 PWR_DW#
- (EC to PCH) 9 PM_PRRST#
- (PCH to EC) 10 PM_SLP_M#
- (PCH to EC) 11 PM_SUSCH#
- 12 PM_SUSB#/SLP_LAN#
- (PCH to EC) (PCH to power)
- (EC to power) MR_SLP_M_EC#
- (EC to power) 13 SUSC_EC#
- +1.2V/+2.5V/+3V/+12V/+VCCST
- (EC to power) 14 SUSB_EC#
- +1.8V/+3V/+12V/+12VS
- +VCC10/+VCC50
- VccST/VccPLL
- +VCCSA
- (power to EC) 15 INVFB_PWRGD
- 16 ALL_SYSTEM_PWRGD
- (EC to PCH) 17 PM_PRRST_PCH
- (PCH to EC) PCH_SUS_STAT#
- (PCH to EC) 18 PLT_RST#
- +VCCOT
- THERMTRIP#



X541UV/UA Power-On Sequence
Timing Diagram Rev.0.1