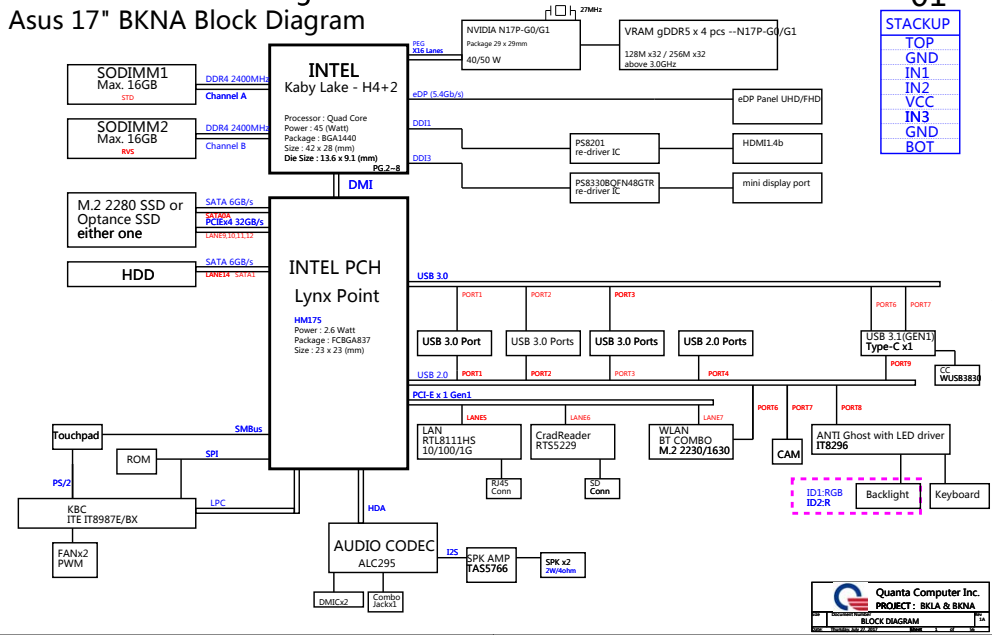
Asus 15" BKLA Block Diagram
Asus 17" BKNA Block Diagram

01

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



Quanta Computer Inc.
PROJECT : BKLA & BKNA
BLOCK DIAGRAM
1A

Model	REV	CHANGE LIST
BKLA BKNA	ER	ER-01:Add KD10,KD11,KD12 for power off Sequence ER-02:5.L6 Change CKSAG1710ID2 to CKSBB271109 ER-03:Page 50:4/EDEL KQ7 and KR99/KR108,KR106, ADD U24 for support keyboard backlight use S3. ER-04:Page 50:4/EDEL change KBLED_R1_R_LED_G1_R_LED_B1 net name for support keyboard backlight issue ER-05:Page 11~13/11Change R1224,R1225,R1226 from 47K to 10K and R1197 from 10K to 0 ohm mount ER-06:Page 10~3/31 Change R937 and R939 from 10K to no-mount, BIOS internal PU ok ER-07:Page 14~3/31 Chande R935 and R936 form 10K to no-mount, BIOS internal PU ok ER-08:Page 36~3/31 Add SPK IDD and SPK_ID1 for AMP PW ER-09:Page 36~3/31 3/31 Change KR72 from 200K to 100K for ER stage ER-10:Page 53~4/5 Change JZRE1 from 3.9K to 4.99K for VD15 and VD17 EA pass ER-11:Page 53~4/5 Change C1038,C1039 from mount 68P to no-mount for EA pass ER-12:Page 50:4/5Del net name LEDD_R1_R_LED_G1_R_LED_B1 and KR105,KR102,KR103 ER-13:Page 50:4/5,Change net name:KBLEDB1,KBLED_R1,KBLED_G1. ER-14:Page 11~4/5:DEL ACZ_RST#AUDIO net name and ADD TP183 on R90 side,R90 chnage to no-mount ER-15:Page 35~4/5 1.Change AU2 pin 13 define to EAPD# 2.Change ACZ_RST#AUDIO to TAS5766_XSMT# ER-16:Page 50~4/6:Add KR129 0ohm no-mount and KR130 0ohm on KCN1#11 ER-17:Page 17~4/6 H26 to GND ER-18:Page 10~4/7 Change U7 CPU to 51225, LDO5 form battery LED source. ER-19:Page 10~4/7+13 ZDD 0ohm x2 to GND for ESD verify. ER-20:Page 22~4/11:VQ5 change from 2N7002 to PJA138K. ER-21:Page 22~4/11:VQ6 change from 2N7002 to Dual PJA138K. ER-22:Page 23~4/11:Add VR165, VR166, VQ13 for VRAM Power IC VIH. ER-23:Page 23~4/11:Reserved VR167 and no mount for sequence. ER-24:Page 36~4/11:Reserved 1V8_AON_EN IN/OUT on EC. ER-25:Page 48~4/11:Reserved PR342 and no mount for GPU sequence. ER-26:Page 48~4/11:Add PC408 0.047uF for GPU sequence. ER-27:Page 46~4/11:PR283 change from 100ohm to 10ohm. ER-28:Page 46~4/11:PR288, PR294 change from 100ohm to 10ohm by FAE suggestion. ER-29:Page 30~4/11mount SL1,SL6,SL7,SL4 for EMI request ER-31:Page 30~4/11mount C1033~1037 for EMI request ER-32:Page 34~4/11Change TR6 10K to no-mount ER-33:Page 34~4/11Change power soure to +3V_S5
	PR	PR-01:COU29 Enable pin change to SUS_ON from +5V_S5 PR-02:Add FAN 12V PR-03:Co-lay TI Smart Amp & RTK CODEC internal Amp
	MP	MP-01:Change net SIO_EXT_SMI# connection to GPP_C22 MP-02 Add KR134,KR135,KR137,KR138 150ohm , add KC93 for noise issue MP-03 Add KR131 and KR132 for SHDN# debug MP-04 Change KR72 from 200K to no-mount for MP MP-05 Add EMI GND PAD , SPAD5 , SPAD6 ,SPAD7 , SPAD8 MP-06 Add LED_PWRFB net for separate LED for KB , LED board MP-07 Add MP1 for Card reader power MP-08 Change VC to VC_CORE for schematic MP-09 Change AC65,AC69,AC71,AC74 1000P to 2200P MP-10 Change AC4,AC5,AC6,AC7 1000P to mount MP-11 Change R940,R947 R948,R949,R950 to 390ohm from 200ohm MP-12 Change PD10 to RB500-40 from 1SS355 for GC6 timing MP-13 change PC295 to 220p from 2200u for GC6 timing MP-14 change PR274 to 1K from 20K for GC6 timing MP-15 change VR166 to 10K from 47K for GC6 timing MP-16 Add D3 for PCIE_SSD_LED# circuit

DOC NO.	PROJECT MODEL :	BKLA/BKNA	APPROVED BY:		DATE:	2017/03/31
	PART NUMBER:		DRAWING BY:		REVISON:	1A

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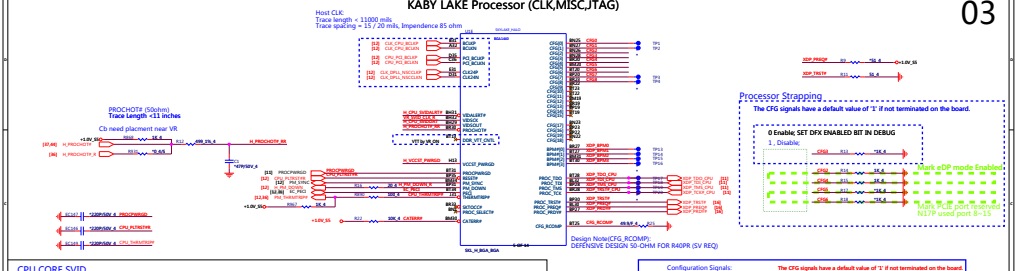
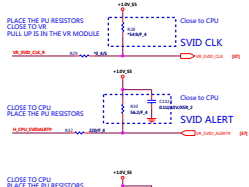
PROJECT : BKLA & BKNA
POWER UP SEQUENCE

KABY LAKE Processor (CLK,MISC,JTAG)



CPU CORE SVID

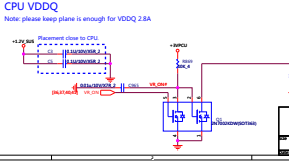
Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.
CFG[0]	Flash boot sequence after PCU PLL lock until be asserted	Note that some of the SVID reference design might connect CFG[0] to HDCI#[2]. This route is not needed on a CNM board.
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 &2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express
CFG[7]	PEG defer training	x1 = PEG train follow RESET# de-assert x0 = PEG wait for BIOS fro training

CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



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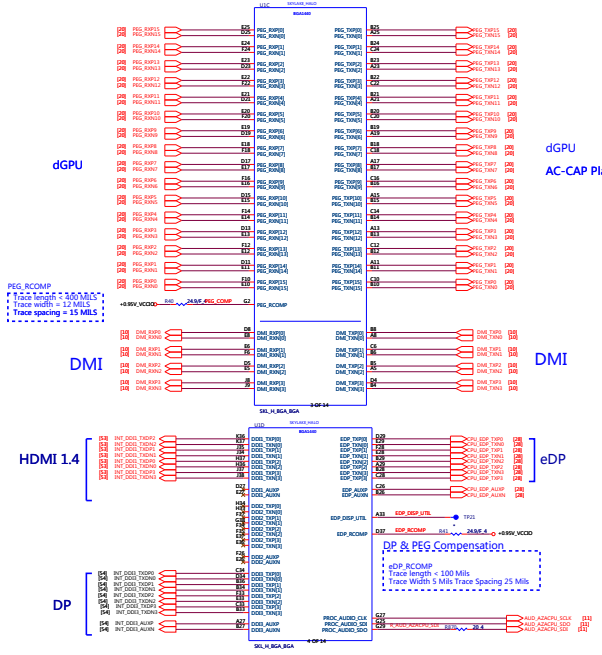
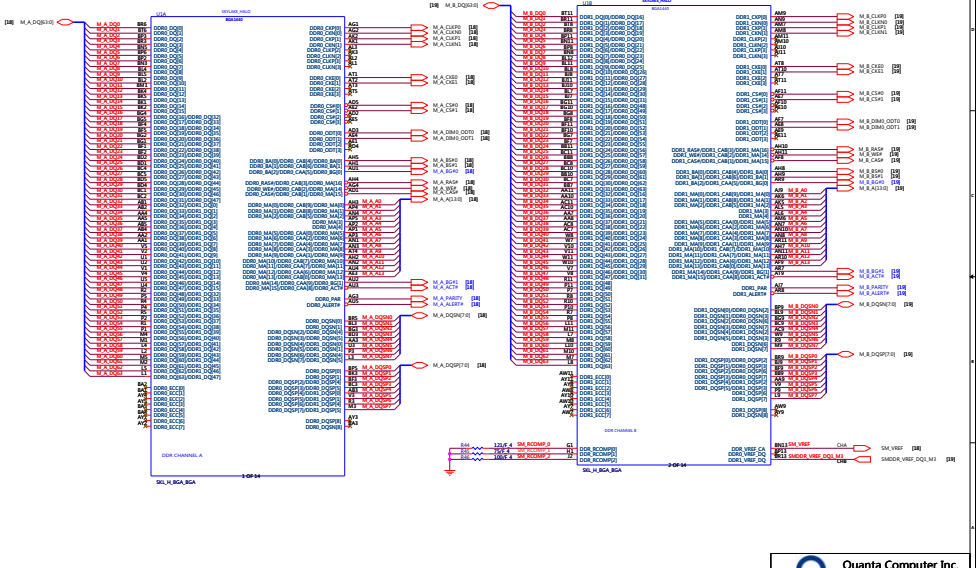
PROJECT : BKLA & BKNA			
Size	Document Number		Rev
	KBL 1/7 (JTAG/MISC)		1A
Date:	Sheet	of	

KABY LAKE Processor (DMI,PEG,FDI)



KABY LAKE Processor (DDR4)



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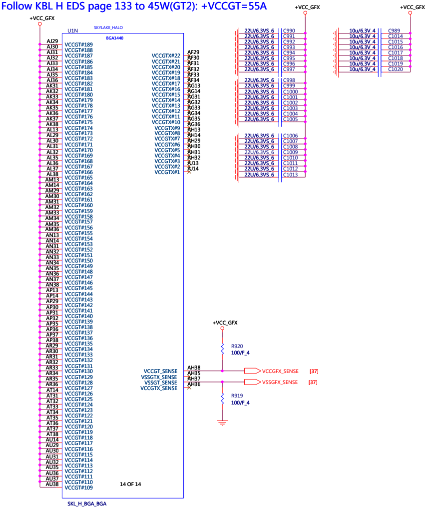
PROJECT : BKLA & BKNA	
Size:	Document Number: KBL 3/7 (DDR4 I/F) Rev: 1A
Date: Thursday, July 27, 2017	Sheet 5 of 56

KABY LAKE Processor (POWER)

Follow KBL H EDS page 133 to 45W(GT2): +VCCGT=55A



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Size	Document Number	Rev
	KBL 4/7 (POWER)	1A
Date: Thursday, July 27, 2017	Sheet 6 of 56	

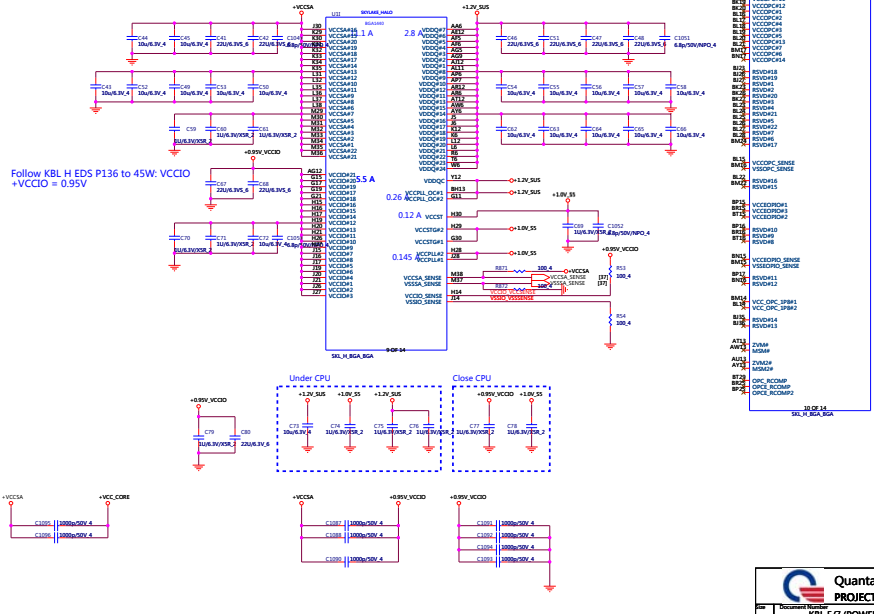
Follow KBL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow KBL H EDS page 135 45W: VDDQ=2.8A

Follow KBL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V

Under CPU

Close CPU



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KBL 5/7 (POWER&GND)

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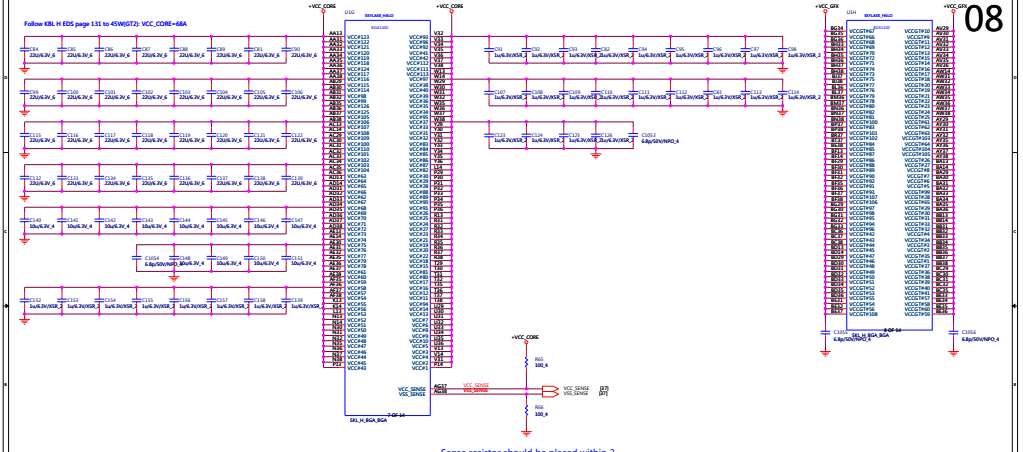
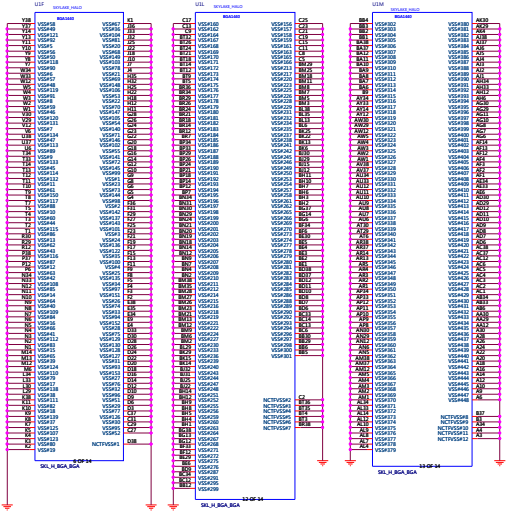
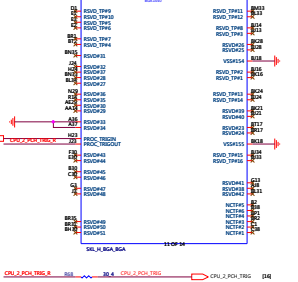

08
Follow KBL H EDS page 131 to 45W(GT2): VCC_CORE=68A
+VCC_CORE
+VCC_GFX
U11G
U11H
SKYLAKE_HALO
SKL_H_BGA_BGA
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impendence 50 ohm
Quanta Computer Inc.
PROJECT : BKLA & BKNA
KBL 6/7 (POWER&GND)
1A

KBL-HProcessor (GND)



KBL-H Processor (RESERVED, CFG)



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	KBL 7/7 (GND)		1A
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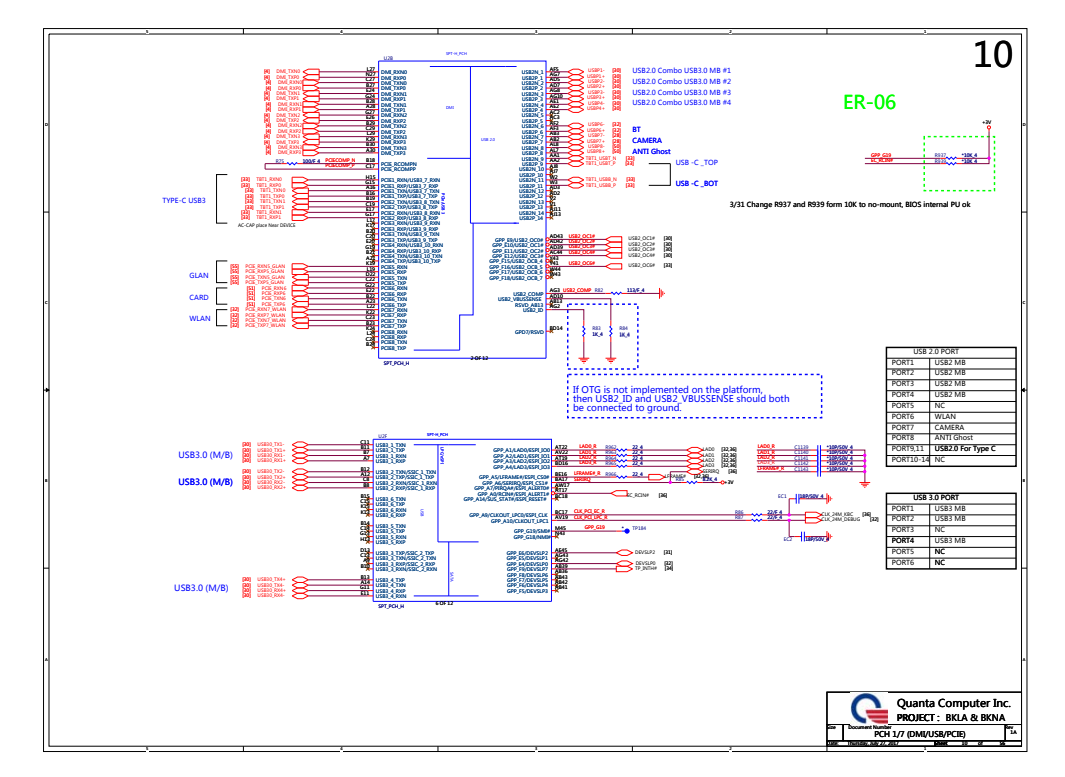

USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 MB
PORT3	USB2 MB
PORT4	USB2 MB
PORT5	NC
PORT6	WLAN
PORT7	CAMERA
PORT8	ANTI Ghost
PORT9,11	**USB2.0 For Type C**
PORT10~14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 MB
PORT3	NC
PORT4	**USB3 MB**
PORT5	**NC**
PORT6	**NC**

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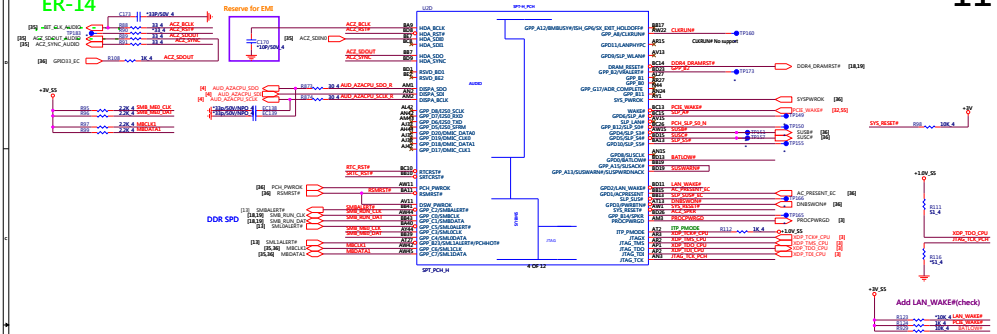
PROJECT : BKLA & BKNA			
Size	Document Number		Rev
	PCH 1/7 (DMI/USB/PCIE)		1A
Date: Thursday, May 21, 2015		Sheet 10 of 56	

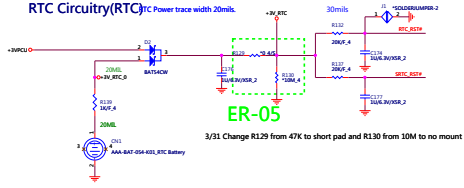
4/5:DEL ACZ_RST#AUDIO net name and ADD TP183 on R90 side,R90 chnage to no-mount

HDA Bus(CLG)

ER-14



RTC Circuitry(RTC)



ER-05

3/31 Change R129 from 47K to short pad and R130 from 10M to no mount

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PROJECT : BKLA & BKNA			
Size	Document Number		Rev
	PCH 2/7 (HDA/SMBUS)		1A
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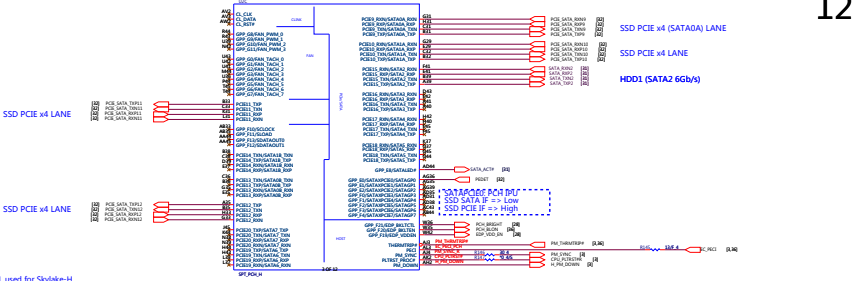
HSIO MUX PORT	
PCIE1~2	USB3.0
PCIE3	NC
PCIE4	NC
PCIE5	LAN
PCIE6	CARD
PCIE7	WLAN
PCIE8	NC
PCIE9	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	NC
PCIE17	NC
PCIE18-20	NC



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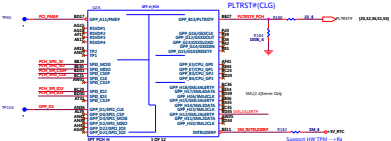
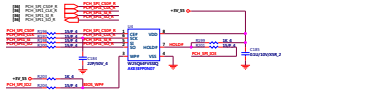
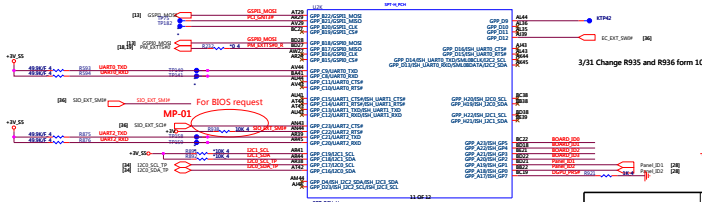
PROJECT : BKLA & BKNA			
Size	Document Number		Rev
	PCH 3/7 (SATA/LPC/CLK)		1A
Date: Wednesday, May 27, 2015	Sheet 3 of 47		





Skylake-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	**PCH_PWROK**	**0 = *Disable Top Swap (iPD 20K) Default** 1 = Enable Top Swap Mode	
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) Default **1 = Enable No Reboot Mode**	+3V_S0 → 10K → GSPI0_MOSI [14]
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	**0 = *Disable Intel ME Crypto TLS(iPD 20K) Default** **1 = Enable Intel ME Crypto TLS** Pch support SMT TLS	+3V_S0 → 10K → 33_4 → SUSACLKBTP [32]
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	**0 = *SPI (iPD 20K) Default** **1 = LPC**	3.3V → 10K → GSPI1_MOSI [14]
GPP_C5 (SMI1ALERT#)	eSPI or LPC	RSMRST#	**0 = *LPC is selected for EC (iPD 20K) Default** **1 = eSPI selected for EC**	3.3V → 10K → SMI1ALERTP [32]
SPI0_MOSI	Reserved	RSMRST#	(PU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_MISO	Reserved	RSMRST#	(PU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(PD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	3.3V → 10K → SML1ALERTP [32]
SPI0_IO2	Reserved	RSMRST#	(PU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device **driving it to opposite direction during strap sampling.**	
SPI0_IO3	Reserved	RSMRST#	(PU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	**0 = *Enable security in the Flash Description (iPD 20K) Default** **1 = Disable Flash Descriptor Security (Override)**	
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	**0 = *Port B is not detected (iPD 20K) (Default)** **1 =Port B is detected**	
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	**0 = *Port C is not detected (iPD 20K) (Defaulte)** **1 =Port C is detected**	
GPP_J10 (DDPD_CTRLDATA)	Display Port D Detected	**PCH_PWROK**	**0 = *Port D is not detected (iPD 20K) Default** **1 =Port D is detected**	
GPP_H12 (SML2ALERT#)	Reserved	**RSMRST#**	(PD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device **driving it to opposite direction during strap sampling.**	TP183 → SML2ALERTP



ER-07

3/31 Change R935 and R936 form 10K to no-mount, BIOS internal PU ok

GPIO Pull-up/Pull-down(CLG)

R need place to BOT

R need place to BOT

	Panel ID1	Panel ID2
FHD	1	1
4K2K	1	0
HD	0	1

	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
VM15 1060 ID1 ROG	0	1	0	0
VM15 1060 ID2	0	1	0	1
VD15 1050 ID1 ROG	1	0	0	0
VD15 1050Ti ID1 ROG	1	1	0	0
VD15 1050Ti ID2	1	1	0	1
VD15 1050 ID2	1	0	0	1
VM17 1060 ID1 ROG	0	1	1	**0**
VM17 1060 ID2	0	1	1	1
VD17 1050 ID1 ROG	1	0	1	0
VD17 1050 ID2	1	0	1	1
VD17 1050Ti ID1 ROG	1	1	1	0
VD17 1050Ti ID2	1	1	1	1

HPD0 --> HDMI1.4
HPD2 --> DP++

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

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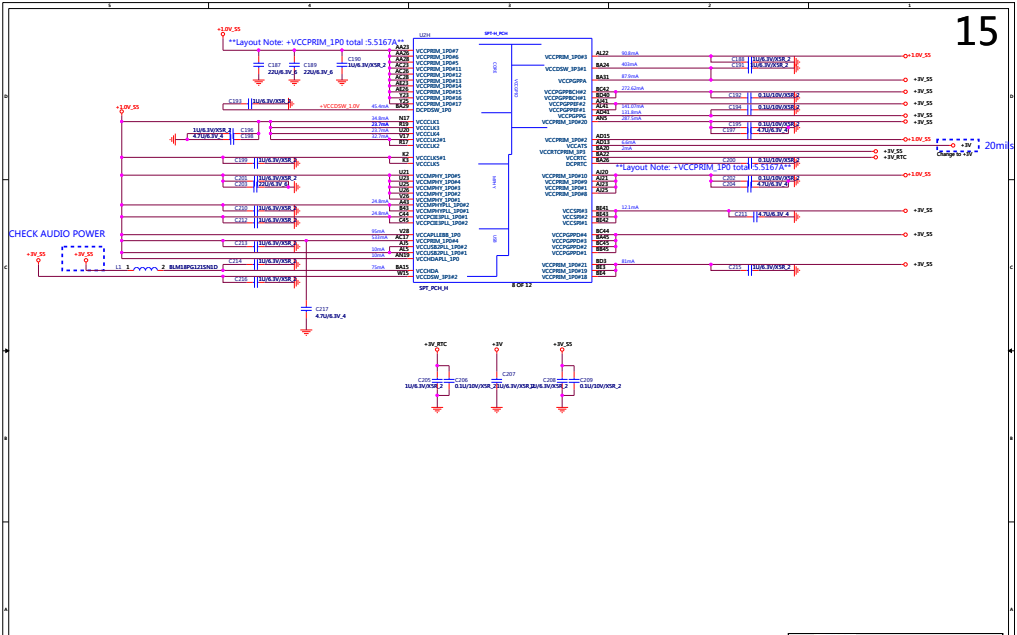
Layout Note: +VCCPRIM_1P0 total :5.5167A
Layout Note: +VCCPRIM_1P0 total:5.5167A
CHECK AUDIO POWER
20mils
Change to 1.0V
SPT_PCH_H
8 OF 12
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PROJECT : BKLA & BKNA
PCH 6/7 (POWER)
Thursday, July 27, 2017

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PROJECT: BKLA & BKNA

Size	Document Number	Rev
	PCH 7/7 (GND)	1A
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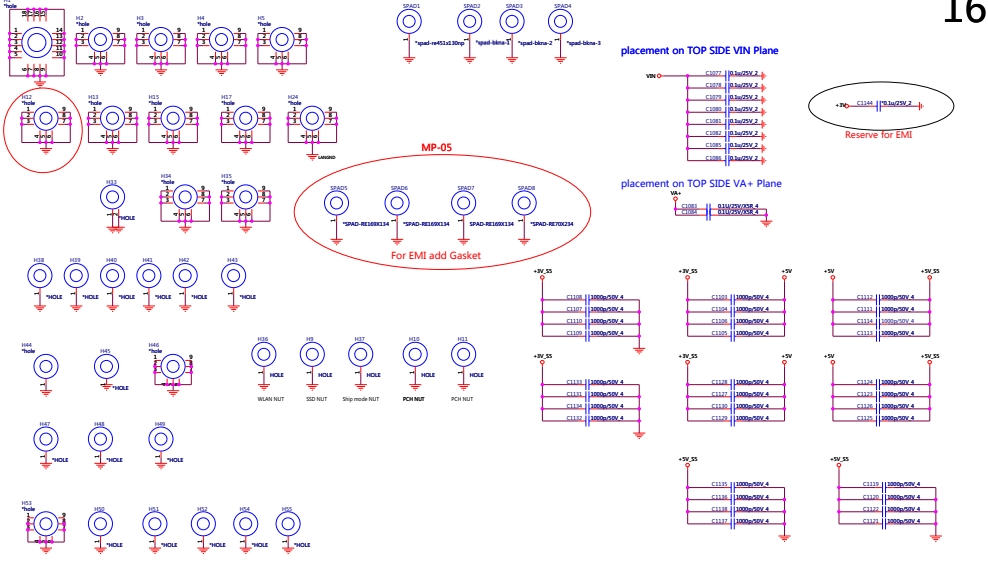
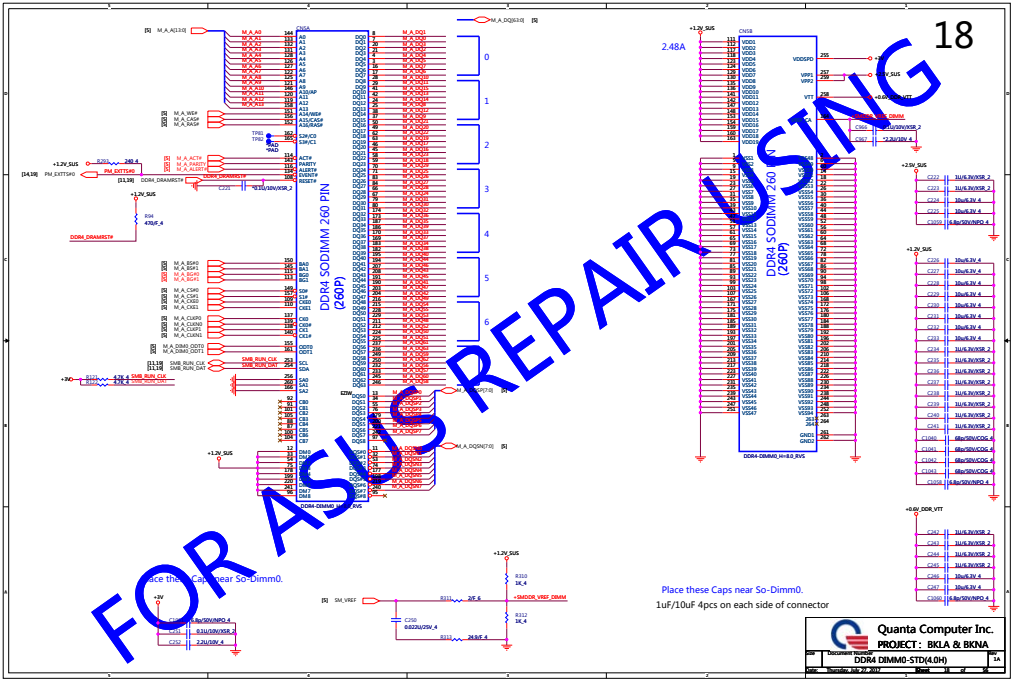
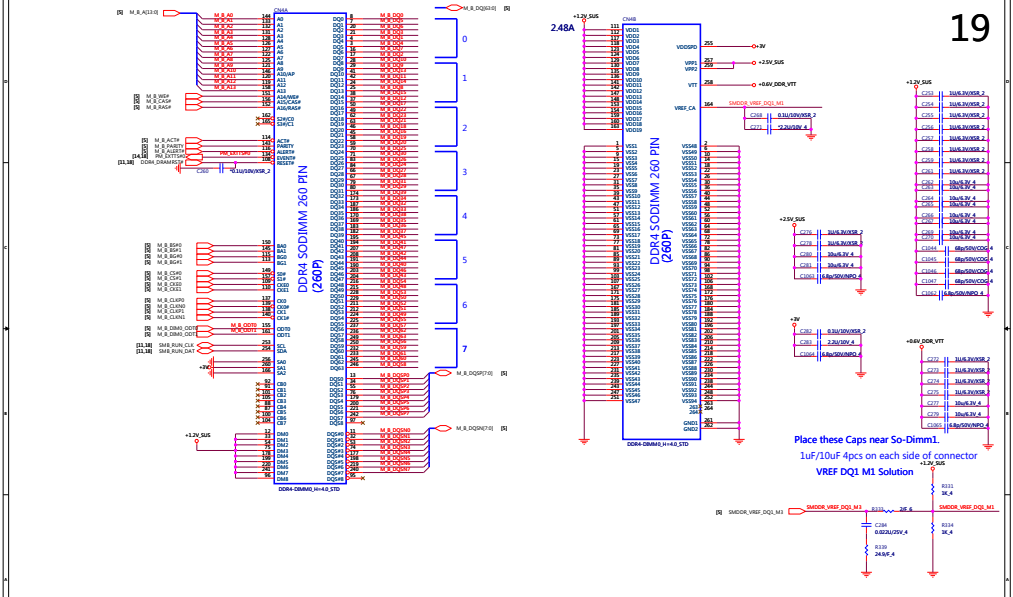

placement on TOP SIDE VIN Plane
placement on TOP SIDE VA+ Plane
Reserve for EMI
MP-05
For EMI add Gasket
WLAN NUT
SSD NUT
Ship mode NUT
PCH NUT
PCH NUT




DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=4.0_STD
2.48A
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
VREF DQ1 M1 Solution
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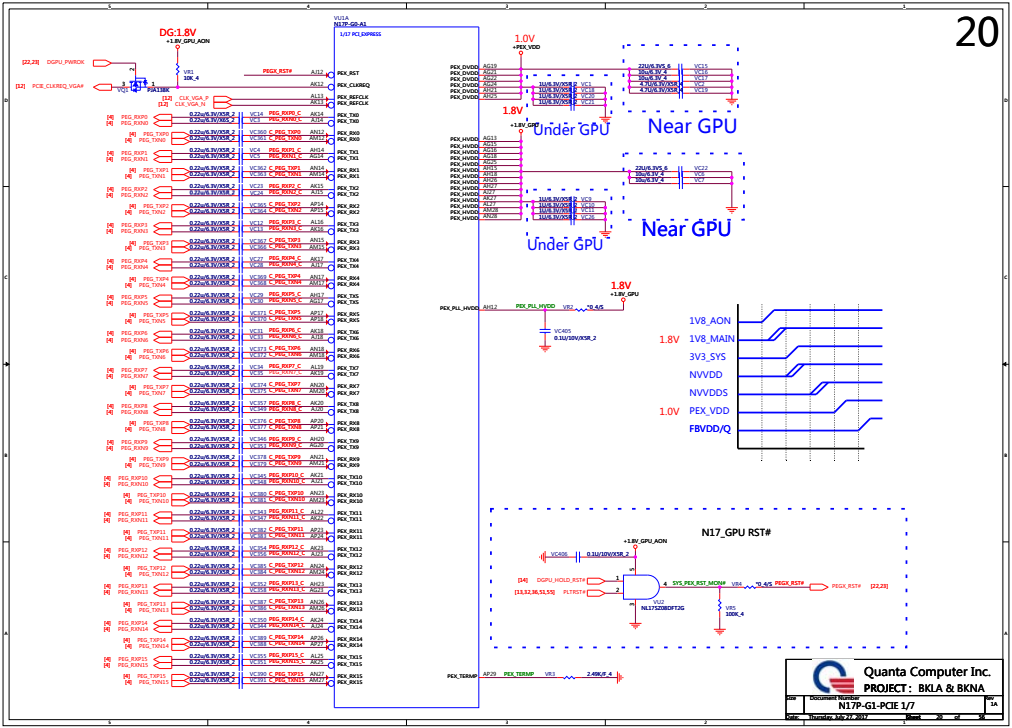
PROJECT: BKLA & BKNA
DDR4 DIMM1-RVS(4.0H)
Thursday, July 27, 2017



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PROJECT : BKLA & BKNA			
Size	Document Number		1A
	N17P-G1-PCIE 1/7		
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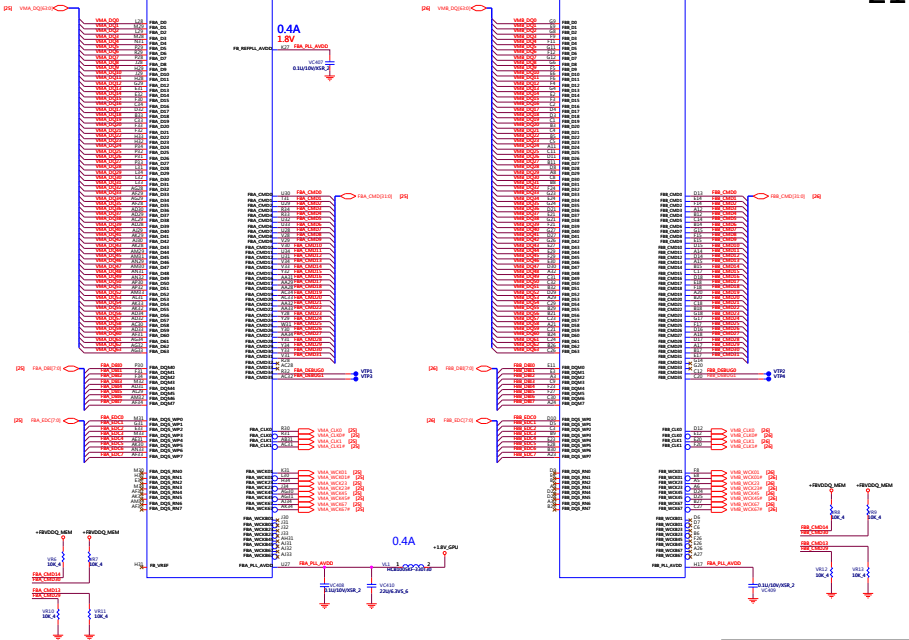
0.4A
1.8V
0.4A
+1.8V_GPU
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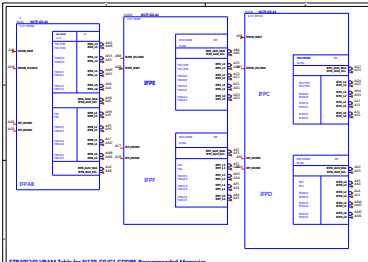
PROJECT : BKLA & BKNA
N17P-G1-MEMORY 1/7
Thursday, July 22, 2010
21



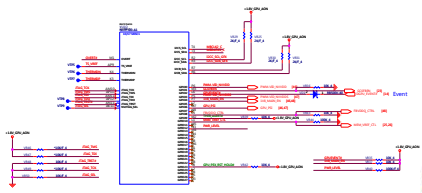


Table 14.2 GPIO Descriptions for G84-750 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVID_EN_HD	B	PWM Output to control NVVID	2 to10 PWM output
GPIO1	GPIO_GC6_FB_EN	I	FB Enable for GC6 2.1	Open Source 10 kΩ pull-down
GPIO2	GPU_PWR_READY	O	GPU wake signal for GC6 2.1	10kΩ pull-up to +1V8_ALW, active driven actively
GPIO3	NVVID_SMB_PWR	B	PWM output to control the Main power supply	0 to 1V8 resistor
GPIO4	LCD_BLK_PWM	O	LCD panel dimming for GC6 2.1	Open Drain 10kΩ pull-up to +1V8_ALW
GPIO5	PWR_LED	O	active src frame Light	Open Drain 10 pull-up to +1V8_ALW

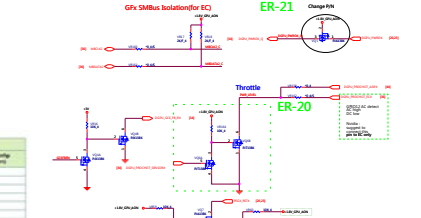
Table 14.2 GPIO Descriptions for G84C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVVID_PN	O	Photo Sensitive Dim function (0.5 V)	10 kΩ pull-up to +1V8_ALW, active driven actively
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	10kΩ pull-down
GPIO8	MEM_VID_CTL	O	Memory voltage control	10kΩ pull-up to +1V8_ALW, active driven actively
GPIO9	THERM_ALERT	I/O	active Low Thermal Alert	10kΩ pull-up to +3V_ALW, active driven actively
GPIO10	MEM_VREF_CTL	O	Memory Control	10 kΩ pull-down
GPIO11	LCD_VDD Quadro Power_Enable	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LCOS	O	LCD Panel power control Driver supply shutdown signal	10kΩ pull-up to +1V8_ALW
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	MFG_STRA	I	Hardware Strap Select for XTAL	Inverted Input, See Figure 11.5
GPIO15	MFG_STRA	I	Hardware Strap Select for XTAL	Inverted Input, See Figure 11.5
GPIO16	MFG_STRA	I	System side PCIe mode	10 kΩ pull-up to +1V8_ALW, active pulldown
GPIO17	MFG_STRA	I	Hardware Strap Select for XTAL	Inverted Input, See Figure 11.5
GPIO18	MFG_STRA	I	Hardware Strap Select for XTAL	Inverted Input, See Figure 11.5
GPIO19	SCANEN	O	SE Chain-in IB Signal	100 kΩ pull-down
GPIO20	GPU_MODE			
GPIO21	GPU_MODE	I/O		
GPIO22	GPU_MODE	I/O		

Table 14.2 GPIO Descriptions for G84C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	VCAM-GPU_REF_MODE	O	MFG Strap used mode control	Open Drain 10 kΩ pull-up to +1V8_ALW
GPIO24	MFG_STRP	I	Not plug detect for PPP	Inverted Input, See Figure 11.5
GPIO25	GPIO25			
GPIO26	GPIO26			
GPIO27	MFG_STRP	I	Not plug detect for PPP	Inverted Input, See Figure 11.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO97	GPIO97	I/O	Clock/Data Over Temperature	100 kΩ pull-up to 3V3_ALW



STRAP[2:0] VRAM Table for N17P-GQ/G1 GDDR5 Recommended Memories

STRAP	MANUFACTURER	Part Number	Quanta P/N	MARKIQ
000	1024Mb 32Bit/x16 * 2pcs	Samsung	K4G80325FB-HC28	1.5V
001	1024Mb 32Bit/x16 * 2pcs	Hynix H5GQ1H24AFR-T2C	A5GQ0QJ0100	1.5V
010	1024Mb 32Bit/x16 * 2pcs	Samsung	K4G80325FB-HC28	1.5V
011	1024Mb 32Bit/x16 * 2pcs	Hynix H5GQ1H24AFR-T2C	A5GQ0QJ0100	1.5V
100	1024Mb 32Bit/x16 * 2pcs	SAMSUNG K4G80325FB-HC28	A5GQ0QJ0100	1.5V

Default

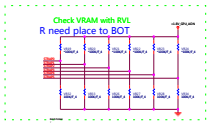


Table 5.3 RAMCFG

Strap Pins			RAMCFG Setting Number (see desktop SVL for memory config corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x000)
L	L	H	1 (0x001)
L	H	L	2 (0x002)
L	H	H	3 (0x003)
H	L	L	4 (0x004)
H	L	H	5 (0x005)
H	H	L	6 (0x006)
H	H	H	7 (0x007)
L	L	FB	8 (0x008)
L	H	FB	9 (0x009)
H	L	FB	10 (0x00a)

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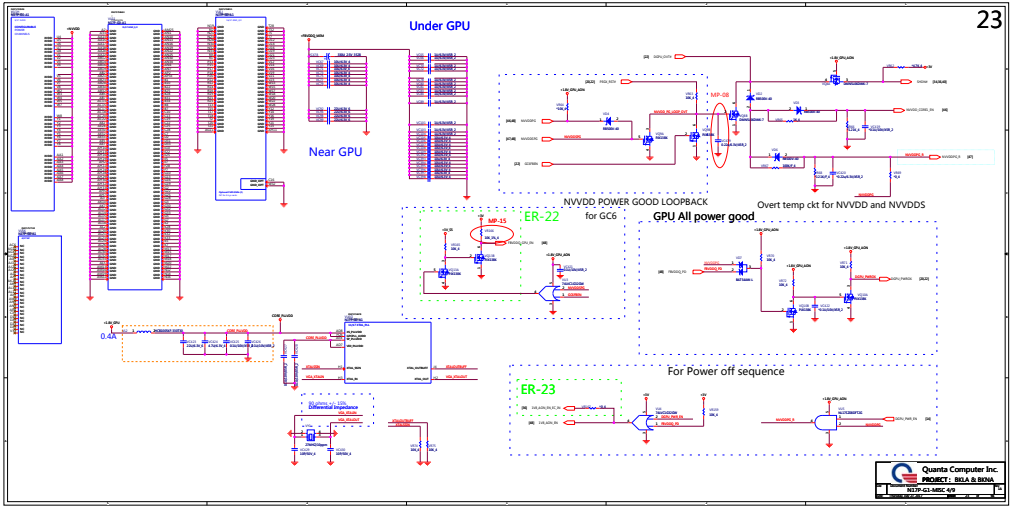
N17P-G1-DISPLAY 3/9


Under GPU
Near GPU
NVVDD POWER GOOD LOOPBACK
Overt temp ckt for NVVDD and NVVDDS
GPU All power good
for GC6
ER-22
MP-15
MP-28
ER-23
For Power off sequence
0.4A
Differential Impedance
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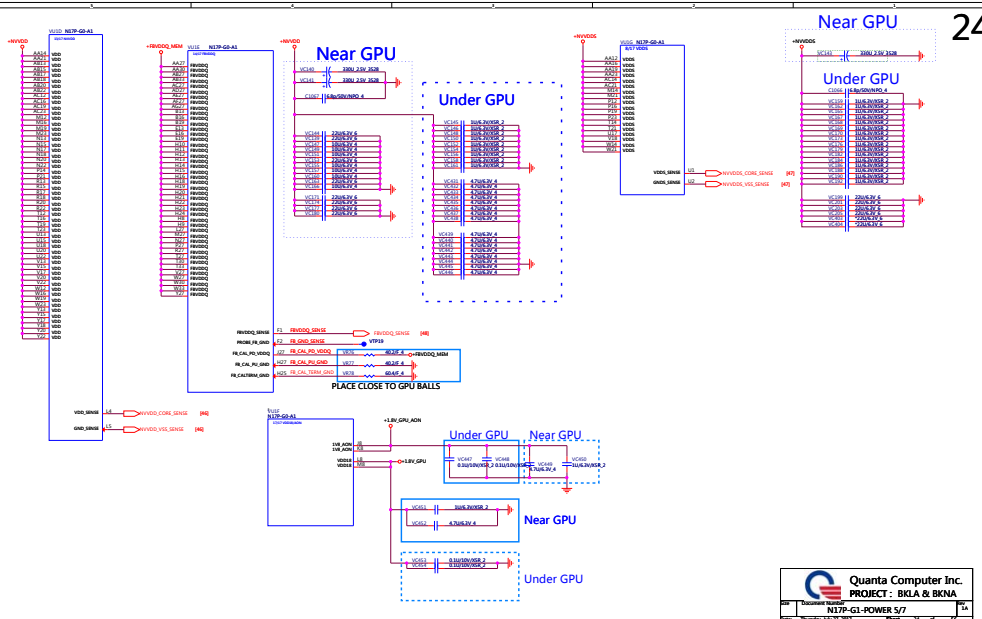
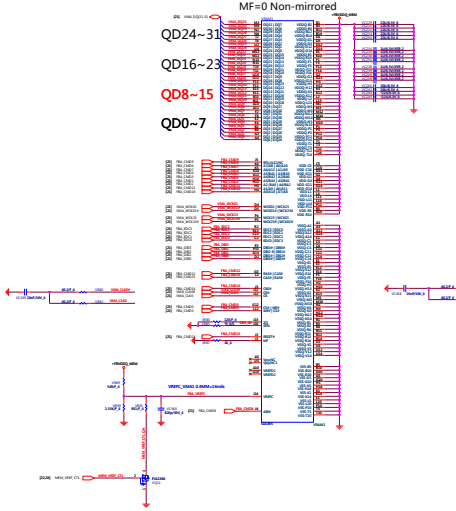
M17P-G1-MISC 4/9


Near GPU
Under GPU
Near GPU
Under GPU
PLACE CLOSE TO GPU BALLS
Under GPU
Near GPU
Near GPU
Under GPU
Quanta Computer Inc.
PROJECT : BKLA & BKNA
N17P-G1-POWER S/7
Thursday, May 07, 2015
24

CHANNEL A: 2G/4G GDDR5

Channel 0
<0-31>
MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7



Channel 1
<32-63>
MF=1 mirrored

QD32~39
QD40~47
QD48~55
QD56~63

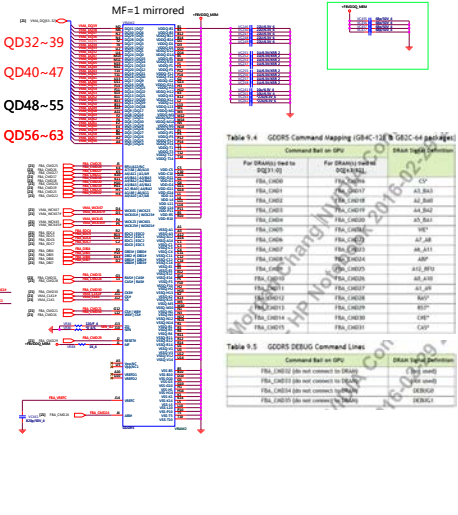


Table 9.4 GDDR5 Command Mapping (GB4C-12E to GB2C-64 package)

Command Ball on GPU	
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]
FBA_CMD0	FBA_CMD16
FBA_CMD1	FBA_CMD17
FBA_CMD2	FBA_CMD18
FBA_CMD3	FBA_CMD19
FBA_CMD4	FBA_CMD20
FBA_CMD5	FBA_CMD21
FBA_CMD6	FBA_CMD22
FBA_CMD7	FBA_CMD23
FBA_CMD8	FBA_CMD24
FBA_CMD9	FBA_CMD25
FBA_CMD10	FBA_CMD26
FBA_CMD11	FBA_CMD27
FBA_CMD12	FBA_CMD28
FBA_CMD13	FBA_CMD29
FBA_CMD14	FBA_CMD30
FBA_CMD15	FBA_CMD31

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD12 (do not connect to DRAM)	(Test used)
FBA_CMD13 (do not connect to DRAM)	(Test used)
FBA_CMD14 (do not connect to DRAM)	DEBUG0
FBA_CMD15 (do not connect to DRAM)	DEBUG1

CHANNEL B: 2G/4G GDDR5

Channel 0
<0-31 >
MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7

Channel 1
<32-63>
MF=1 mirrored

QD32~39
QD40~47
QD48~55
QD56~63

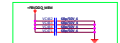


Table 9.4 GDDR5 Command Mapping (GB4C-12E & GB2C-64 package)

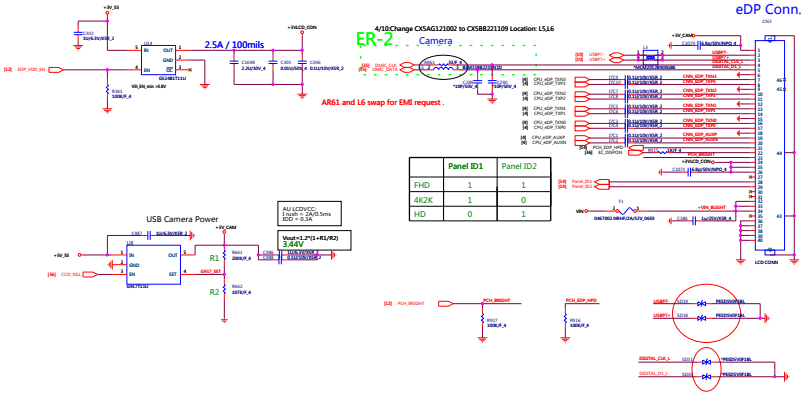
Command Bail on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS'
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA2
FBA_CMD3	FBA_CMD19	A4_BA1
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	VRS'
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI'
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS'
FBA_CMD13	FBA_CMD29	RST'
FBA_CMD14	FBA_CMD30	CKE'
FBA_CMD15	FBA_CMD31	CAS'

Table 9.5 GDDR5 DEBUG Command Lines

Command Bail on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

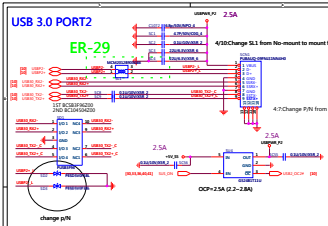
eDP & Camera

eDP Conn.

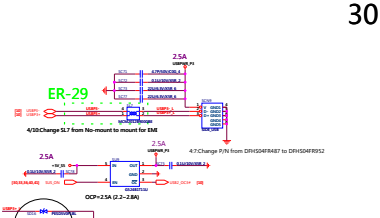


	Panel ID1	Panel ID2
FHD	1	1
4K2K	1	0
HD	0	1

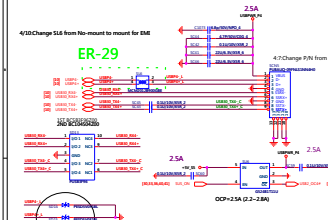
USB 3.0 PORT2



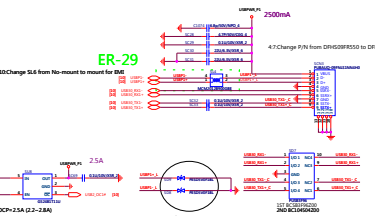
USB 2.0 PORT3



USB 3.0 PORT4



USB 3.0 PORT1



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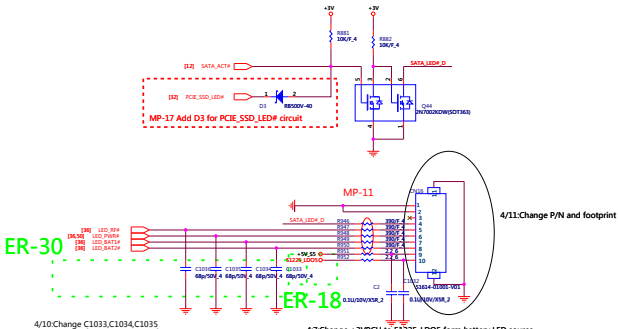
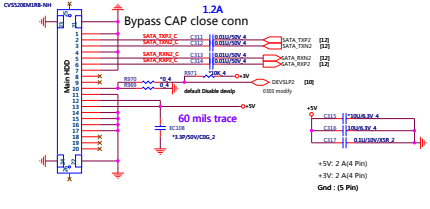
LED



SATA HDD Connector(Cable type)



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	HDD/LED	1A
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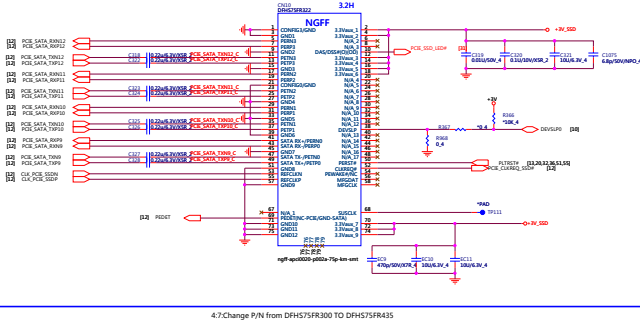
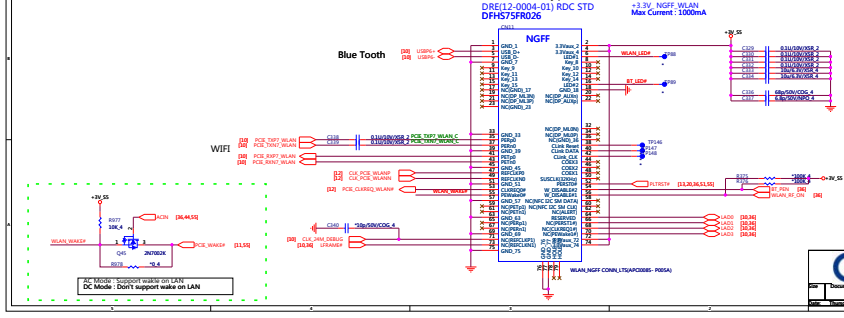
SSD



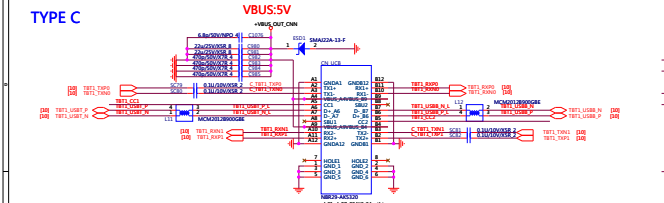
4:7:Change P/N from DFHS75FR300 TO DFHS75FR435

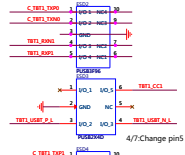
WLAN/BT



TYPE C

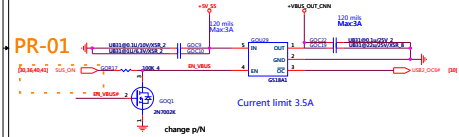
VBUS:5V

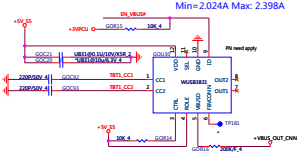




4/7:Change pin5 to +VBUS_OUT_CNN for 2nd source

PR-01





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USB-C(USB/PD/DP-OUT)

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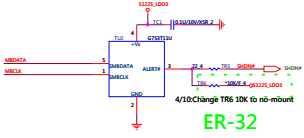
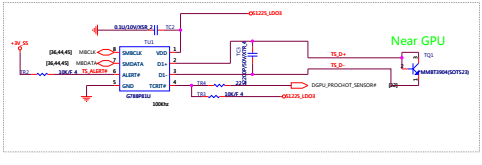
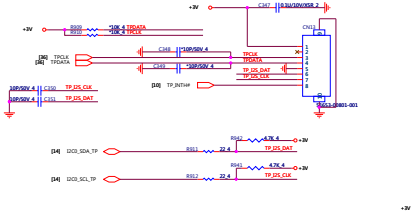
Thermal

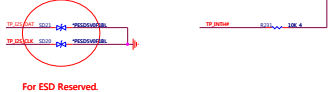
Near CPU





Touch Pad Connector AA type





For ESD Reserved.

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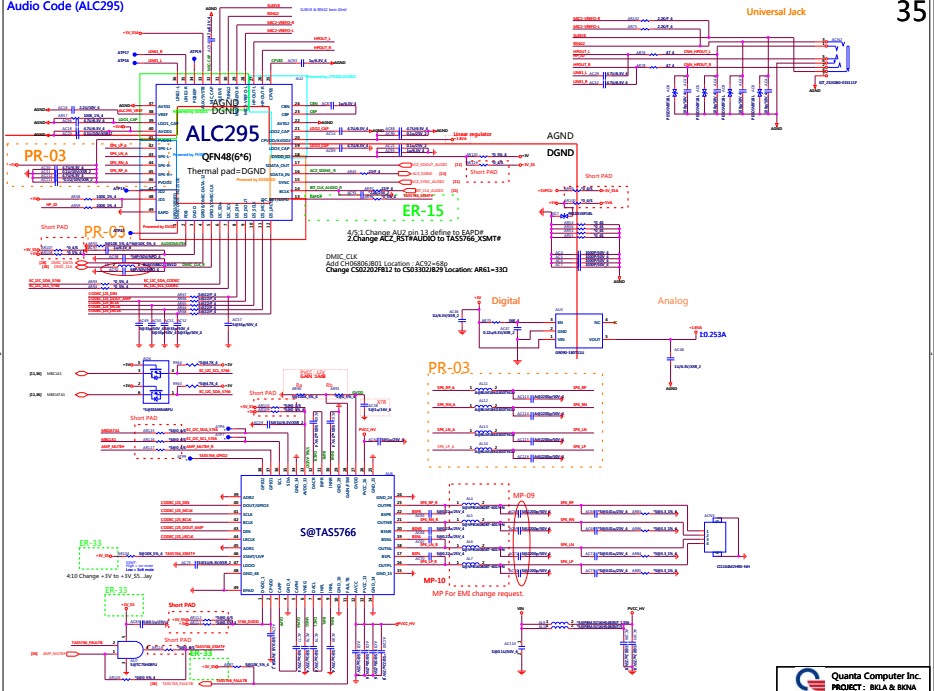
Audio Code (ALC295)



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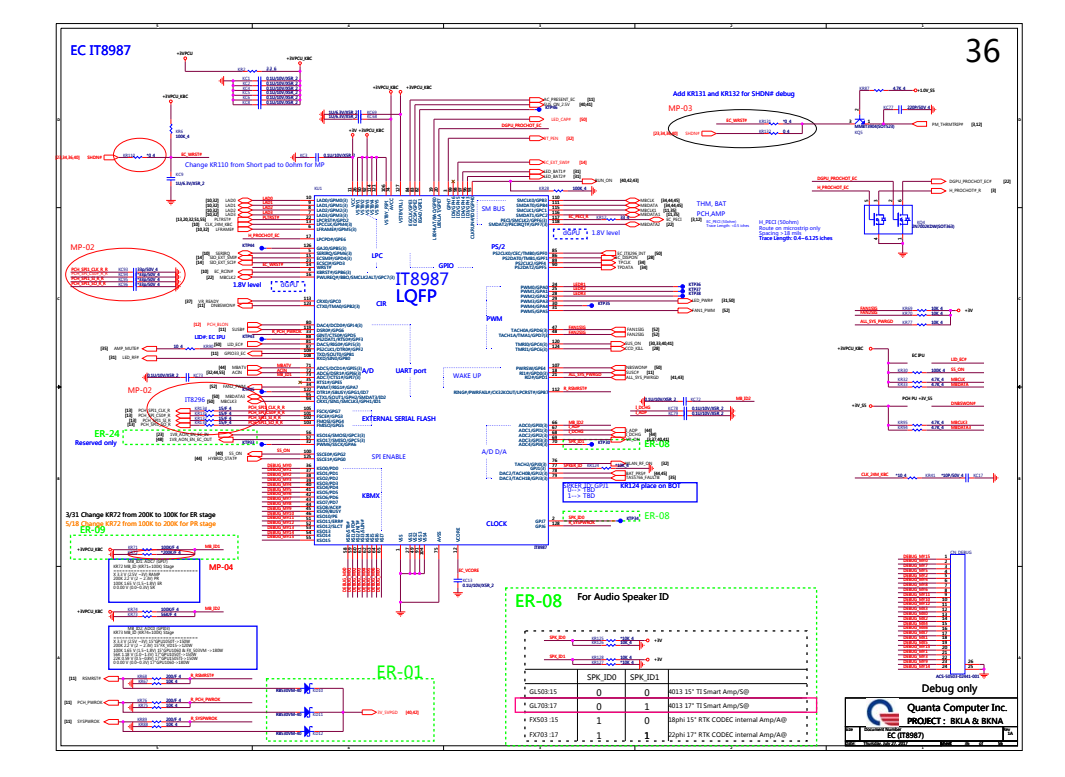
AudIo(ALC295-CG+TAS5766)

EC IT8987



	SPK_ID0	SPK_ID1
GL503:15	0	0
GL703:17	0	1
FX503 :15	1	0
FX703 :17	1	1

4013 15" TI Smart Amp/S@
4013 17" TI Smart Amp/S@
4Phi 15" RTK CODEC internal Amp/A@
2Phi 17" RTK CODEC internal Amp/A@

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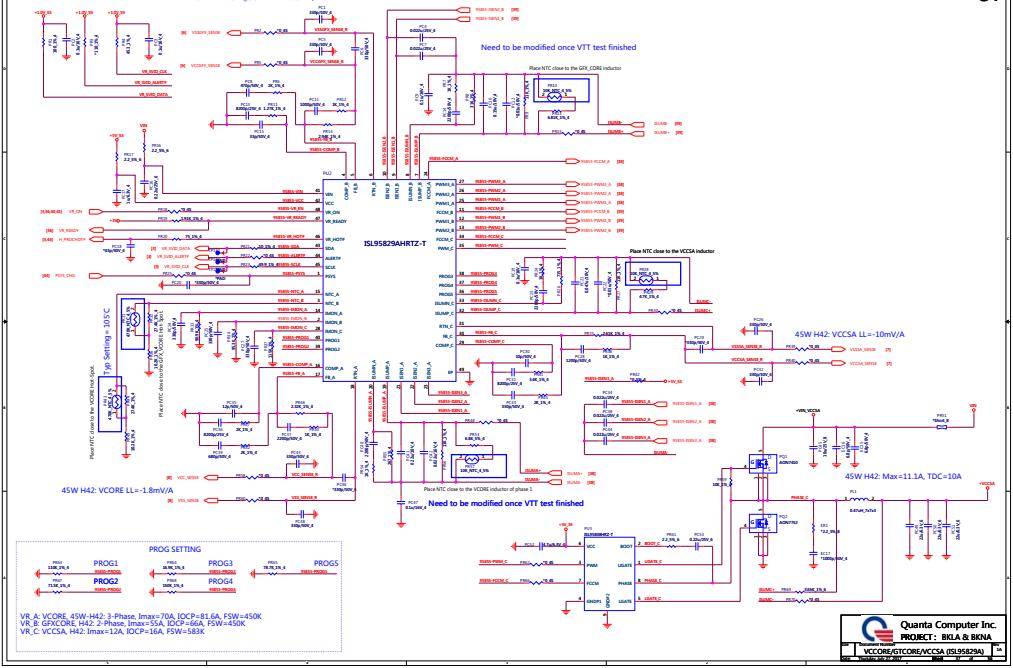
EC (IT8987)


45W H42: GFX_CORE LL=-2.65mV/A
Need to be modified once VTT test finished
Place NTC close to the GFX_CORE inductor
ISL95829AHRTZ-T
Place NTC close to the VCCSA inductor
45W H42: VCCSA LL=-10mV/A
45W H42: VCORE LL=-1.8mV/A
Need to be modified once VTT test finished
Place NTC close to the VCORE inductor of phase 1
45W H42: Max=11.1A, TDC=10A
Vin Setting = 10.5°C
Place NTC close to the VCORE hot spot.
PLACE NTC close to the VCCSA hot spot.
PROG SETTING
PROG1
PROG2
PROG3
PROG4
PROG5
VR_A: VCORE_45W-H42: 3-Phase, Imax=70A, IOCP=81.6A, FSW=450K
VR_B: GFXCORE, H42: 2-Phase, Imax=55A, IOCP=66A, FSW=450K
VR_C: VCCSA, H42: Imax=12A, IOCP=16A, FSW=583K
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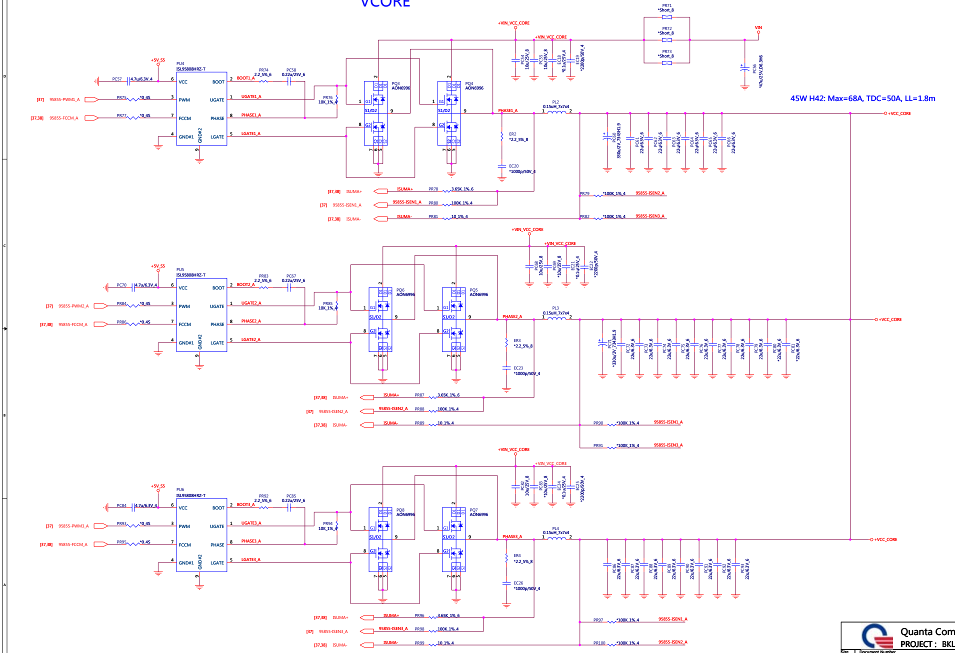
VCCORE/GTCORE/VCCSA (ISL95829A)

VCORE



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	VCCORE/GTCORE/VCCSA (ISL95829A)	1A

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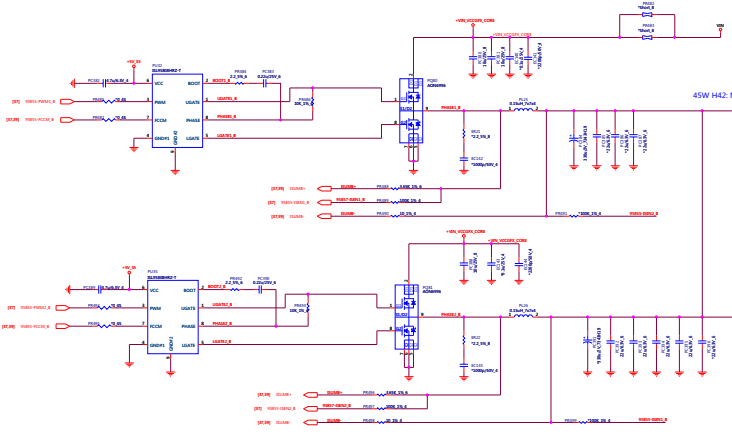
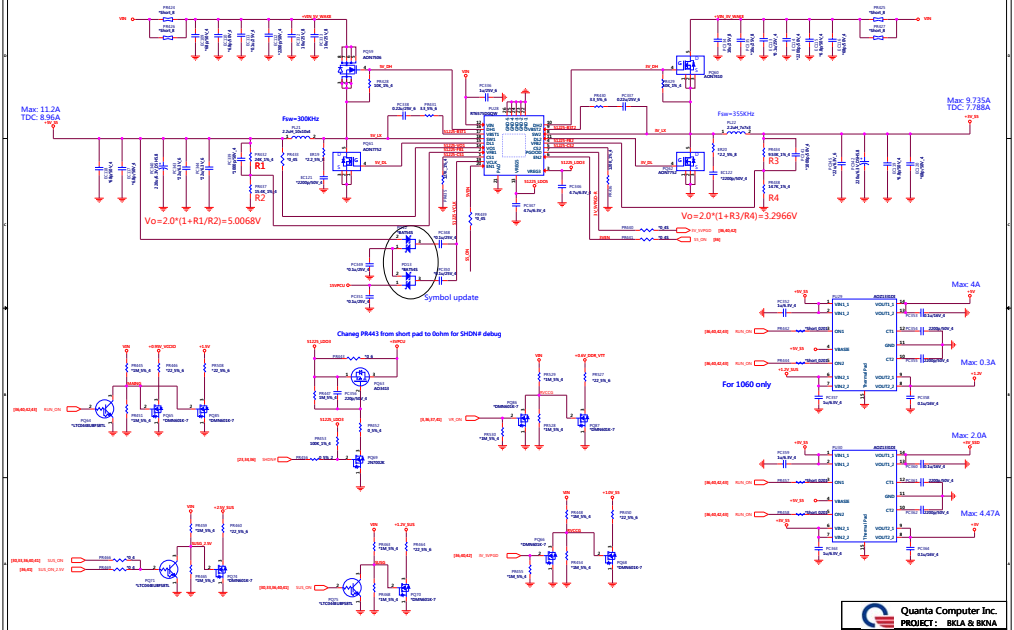
GFX_CORE





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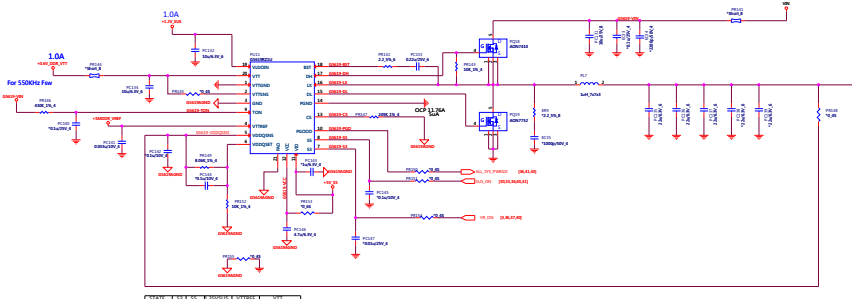
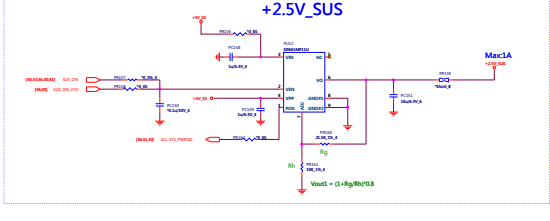
1.2VSUS/VTT_MEM

1.2VSUS & VTT_MEM



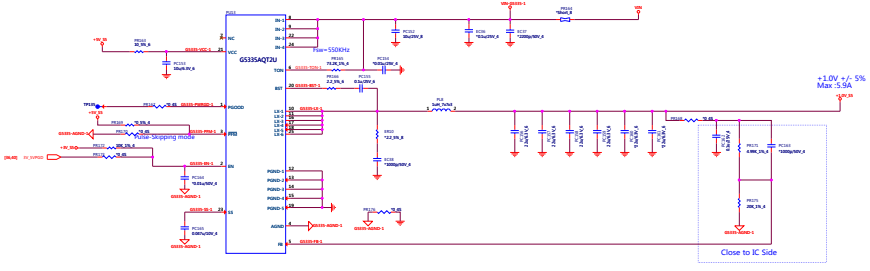
STATE	S4	S5	1.05VSUS	VTTREF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF/High-Z
S4/S5	0	0	OFF	OFF	OFF

+2.5V_SUS

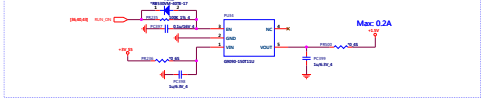


Quanta Computer Inc.	
PROJECT :	BKLA & BKNA
1.2VSUS/VTT_MEM	

+1.0V_S5

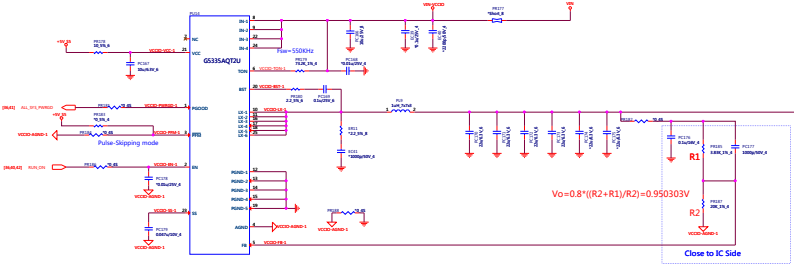


+1.5V

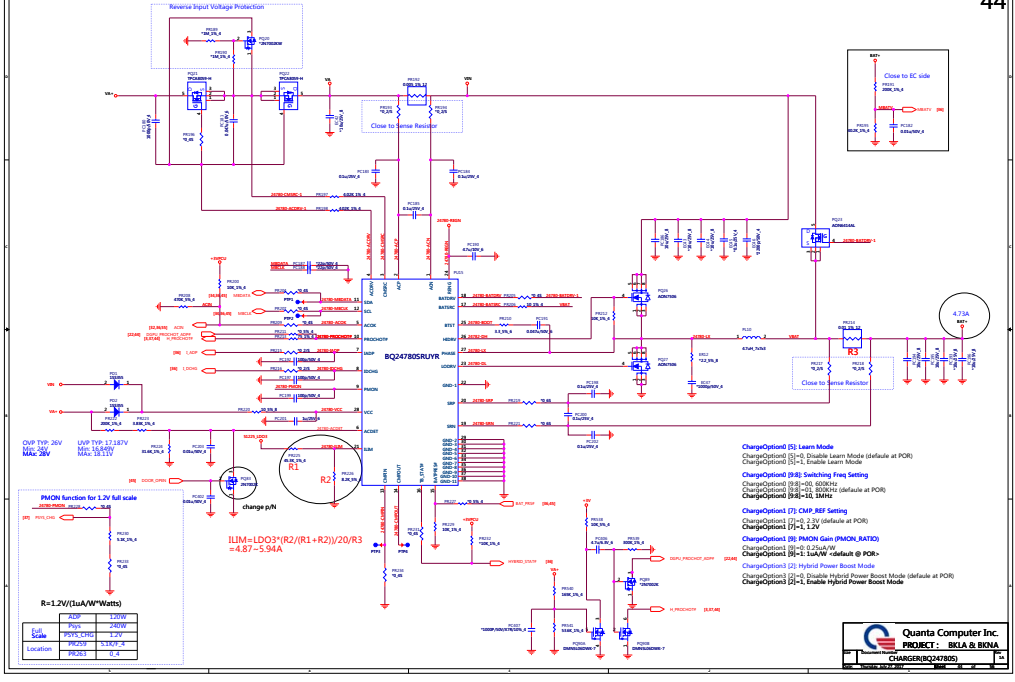


Quanta Computer Inc.			
PROJECT: BKLA & BKNA			
Size	Document Number		Rev
	+1.0V_S5 / +1.5V		1A
Date: Tuesday, May 07, 2013		Sheet 42 of 47	

+VCCIO (Fix VCCIO=0.95V)

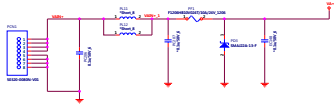


Quanta Computer Inc.
PROJECT : BKLA & BKNA
+0.95V_VCCIO
Size: 1A
Date: Thursday, July 01, 2021
Sheet 41 of 56

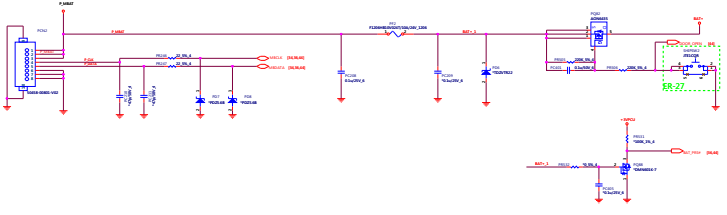

Reverse Input Voltage Protection
Close to Sense Resistor
Close to EC side
BQ24780SRUYR
OVP TYP: 26V
Min: 25V
MAX: 28V
UVP TYP: 17.187V
Min: 16.84V
MAX: 18.11V
PMON function for 1.2V full scale
change p/N
ILIM=LDO3*(R2/(R1+R2))/20/R3
=4.87~5.94A
R=1.2V/(1uA/W*Watts)
ADP 120W
Full Scale Rsys 240W
PSYS_CHG 1.2V
Location PR259 5.1K/F_4
PR263 0_4
ChargeOption0 [5]: Learn Mode
ChargeOption0 [5]=0, Disable Learn Mode (defaule at POR)
ChargeOption0 [5]=1, Enable Learn Mode
ChargeOption0 [9:8]: Switching Freq Setting
ChargeOption0 [9:8]=00, 600KHz
ChargeOption0 [9:8]=01, 800KHz (defaule at POR)
ChargeOption0 [9:8]=10, 1MHz
ChargeOption1 [7]: CMP_REF Setting
ChargeOption1 [7]=0, 2.3V (defaule at POR)
ChargeOption1 [7]=1, 1.2V
ChargeOption0 [9]: PMON Gain (PMON_RATIO)
ChargeOption0 [9]=0, 0.25uA/W
ChargeOption0 [9]=1: 1uA/W <default @ POR>
ChargeOption0 [2]: Hybrid Power Boost Mode
ChargeOption0 [2]=0, Disable Hybrid Power Boost Mode (defaule at POR)
ChargeOption0 [2]=1, Enable Hybrid Power Boost Mode
Quanta Computer Inc.
PROJECT: BKLA & BKNA
CHARGER(BQ24780S)
Size: A3 Document Number: Rev: 3A
Date: Tuesday, July 07, 2015 Sheet 58 of 60

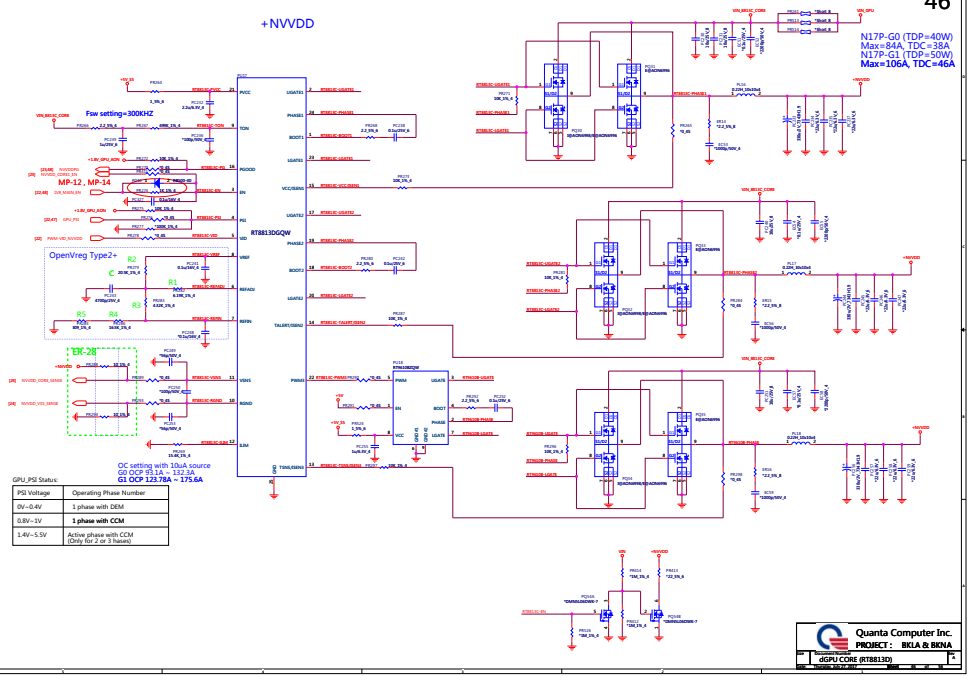
AC IN

AC ADAPTOR IN CONN

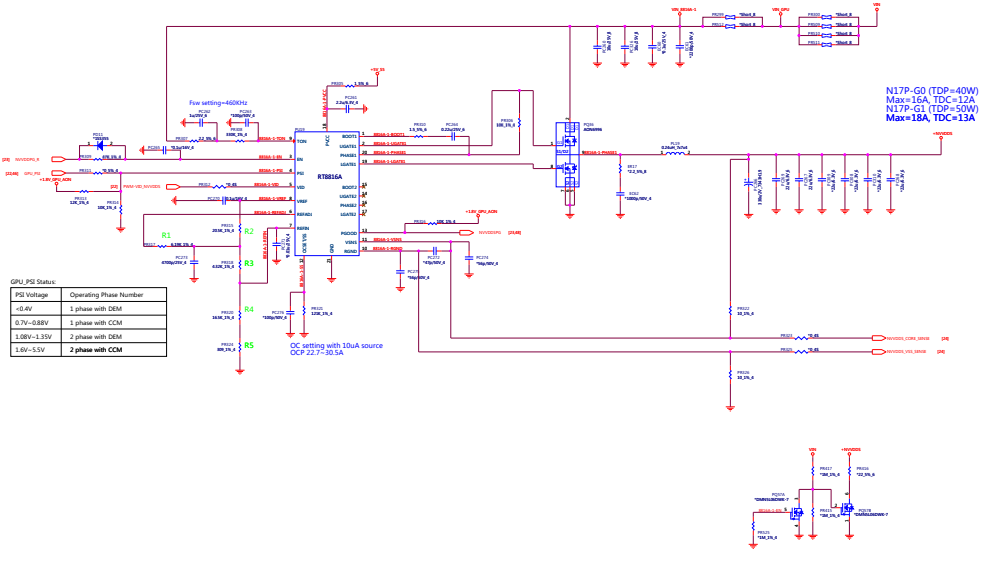


BAT IN



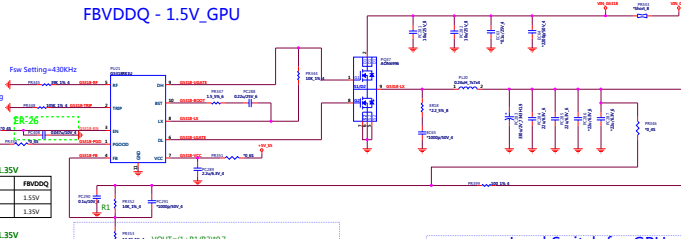

+NVVDD
N17P-G0 (TDP=40W)
Max=84A, TDC=38A
N17P-G1 (TDP=50W)
Max=106A, TDC=46A
Fsw setting=300KHZ
MP-12 , MP-14
OpenVreg Type2+
ER-28
RT8813DGQW
OC setting with 10uA source
G0 OCP 93.1A ~ 137.3A
G1 OCP 123.78A ~ 175.6A
GPU_PSI Status:
PSI Voltage
Operating Phase Number
0V~0.4V
1 phase with DEM
0.8V~1V
1 phase with CCM
1.4V~5.5V
Active phase with CCM
(Only for 2 or 3 hases)
Quanta Computer Inc.
PROJECT : BKLA & BKNA
dGPU CORE (RT8813D)

+NVVDDS



Quanta Computer Inc.
PROJECT: BKLA & BKNA
+NVVDDS (RT8816A)

FBVDDQ - 1.5V_GPU



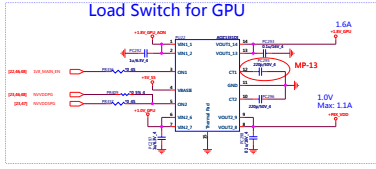
FBVDDQ Voltage Setting: 1.55V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12K	3.57K	1.55V
0	12K	3.57K	1.35V

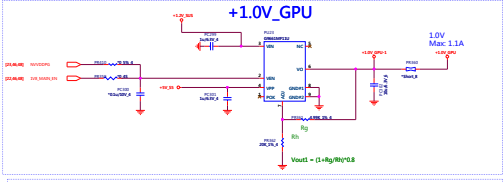
FBVDDQ Voltage Setting: 1.50V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12.4K	2.94K	1.50V
0	12.4K	**2.94K**	**1.35V**

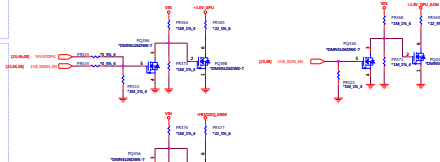
Load Switch for GPU



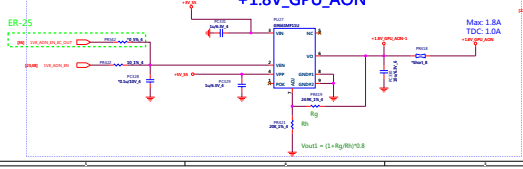
+1.0V_GPU



Discharge



+1.8V_GPU_AON



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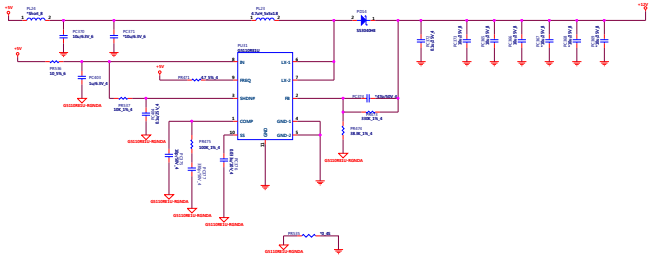
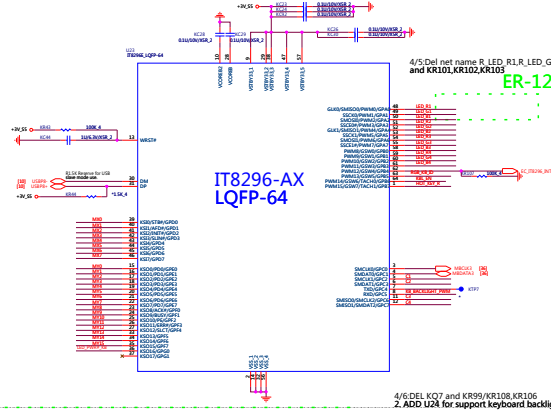
+FBVDDQ (65318)

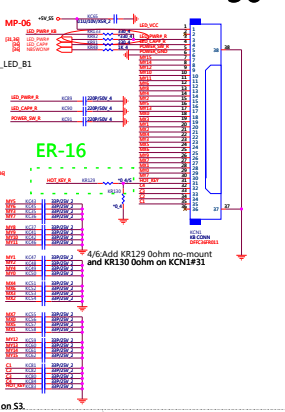
+12V for FAN



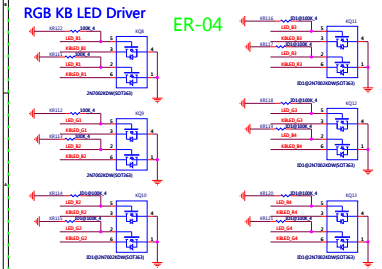
ANTI Ghost with LED driver

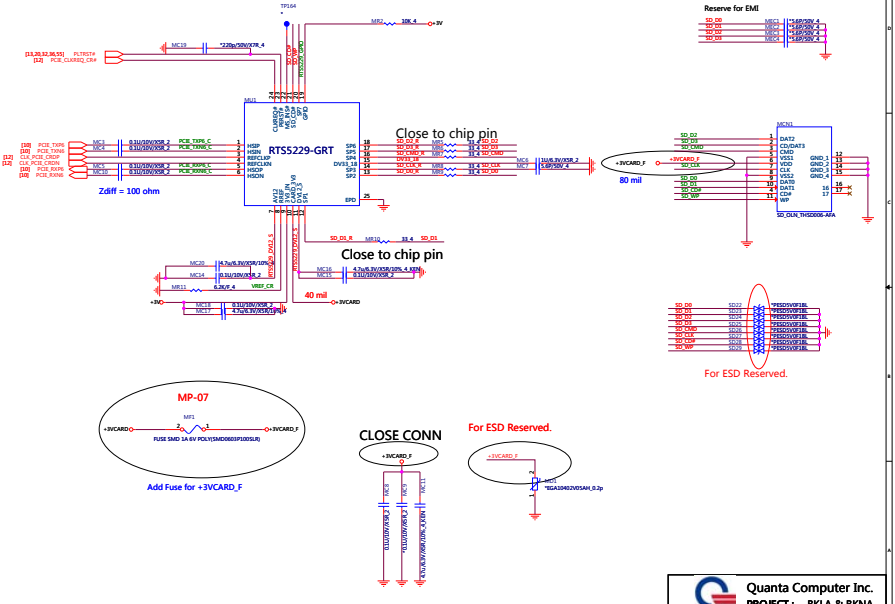


KEYBOARD Con.



RGB KB LED Driver




RTS5229-GRT
Close to chip pin
Zdiff = 100 ohm
Close to chip pin
40 mil
80 mil
Reserve for EMI
For ESD Reserved.
MP-07
Add Fuse for +3VCARD_F
CLOSE CONN
For ESD Reserved.
Quanta Computer Inc.
PROJECT : BKLA & BKNA
CR RTS5229 & CR SOCKET
Thursday, July 27, 2017
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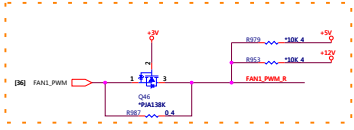
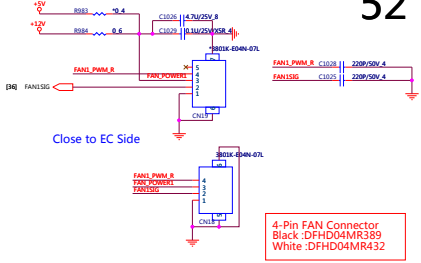
PR-02

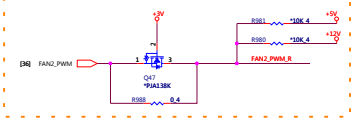


FAN1 for GPU

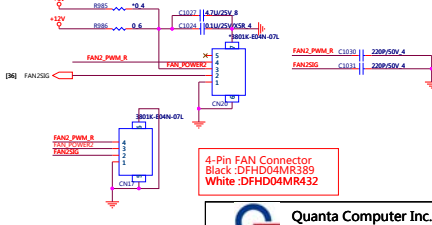


4-Pin FAN Connector
Black :DFHD04MR389
White :DFHD04MR432

PR-02



FAN2 for CPU



4-Pin FAN Connector
Black :DFHD04MR389
White :DFHD04MR432

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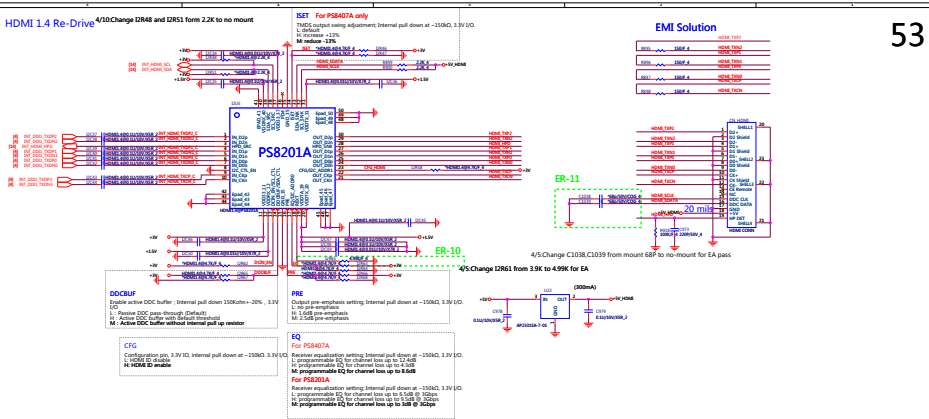
PROJECT : BKLA & BKNA

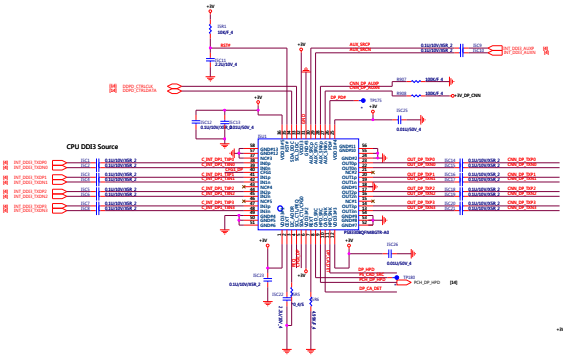
Size	Document Number	Rev
	FAN	1A
Date: Thursday, July 27, 2017	Sheet 52 of 58	

HDMI 1.4 Re-Drive

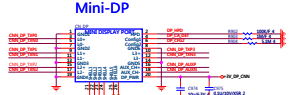
4/10:Change I2R48 and I2RS1 form 2.2K to no mount



Dual-Mode DisplayPort (DP++)

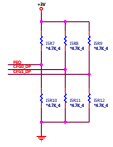


Mini-DP



4:7:Change P/N from DFHS20FR105 to DFDI20FR036

PS8330 strap pin



PEQ
Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15DB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

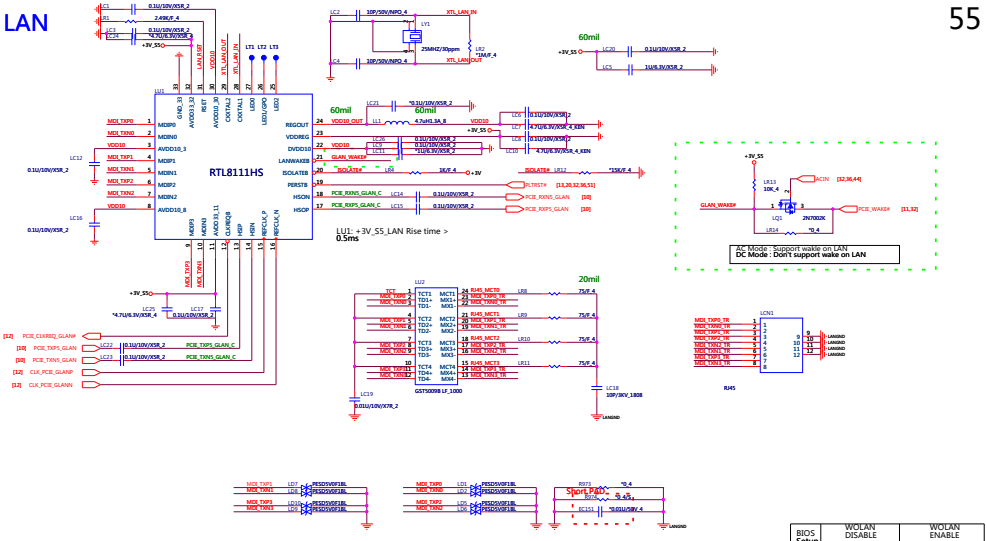
CFGD_DP
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mV/pp swing

CFGS_DP
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

Table 2-1: Source-Side Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR

LAN



BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H

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Size	Document Number	Rev
	Giga LAN RTL8111HS	1A
Date: Thursday, July 27, 2017	Sheet 55 of 58	

SkyLake ULT Power-Up Sequencing (G3-->S0-->S3-->S4-->S5)